

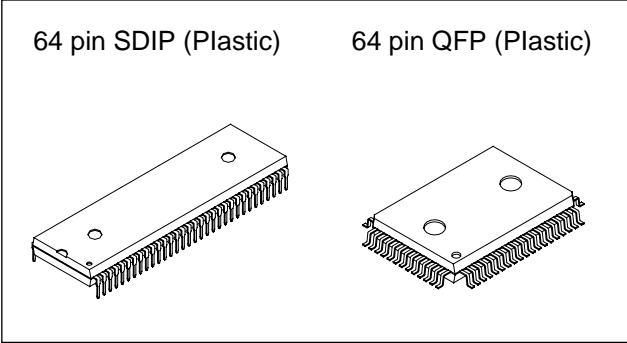
**CMOS 8-bit Single-chip Microcomputer**

**Description**

The CXP853P40A are a highly integrated micro-computers composed of a 8-bit CPU, PROM, RAM, and I/O ports. These chips feature many other high-performance circuits in a single-chip CMOS design, including an A/D converter, serial interface, timer/counter, time-base timer, vector interrupt, on-screen display function, I<sup>2</sup>C bus interface, PWM generator, remote control receiver, HSYNC counter, power supply frequency counter, and watchdog timer.

Also, this IC provides power-on reset and sleep functions. The designers have ensured low power consumption for these powerful microcomputers.

The CXP853P40A is the one-chip PROM version of the CXP85340A with on-chip mask ROM, providing the function of being able to write directly into the program. Furthermore, because of the OSD character ROM can also be written directly into, it is suitable for evaluation use during system development and for small quantity production.



**Structure**

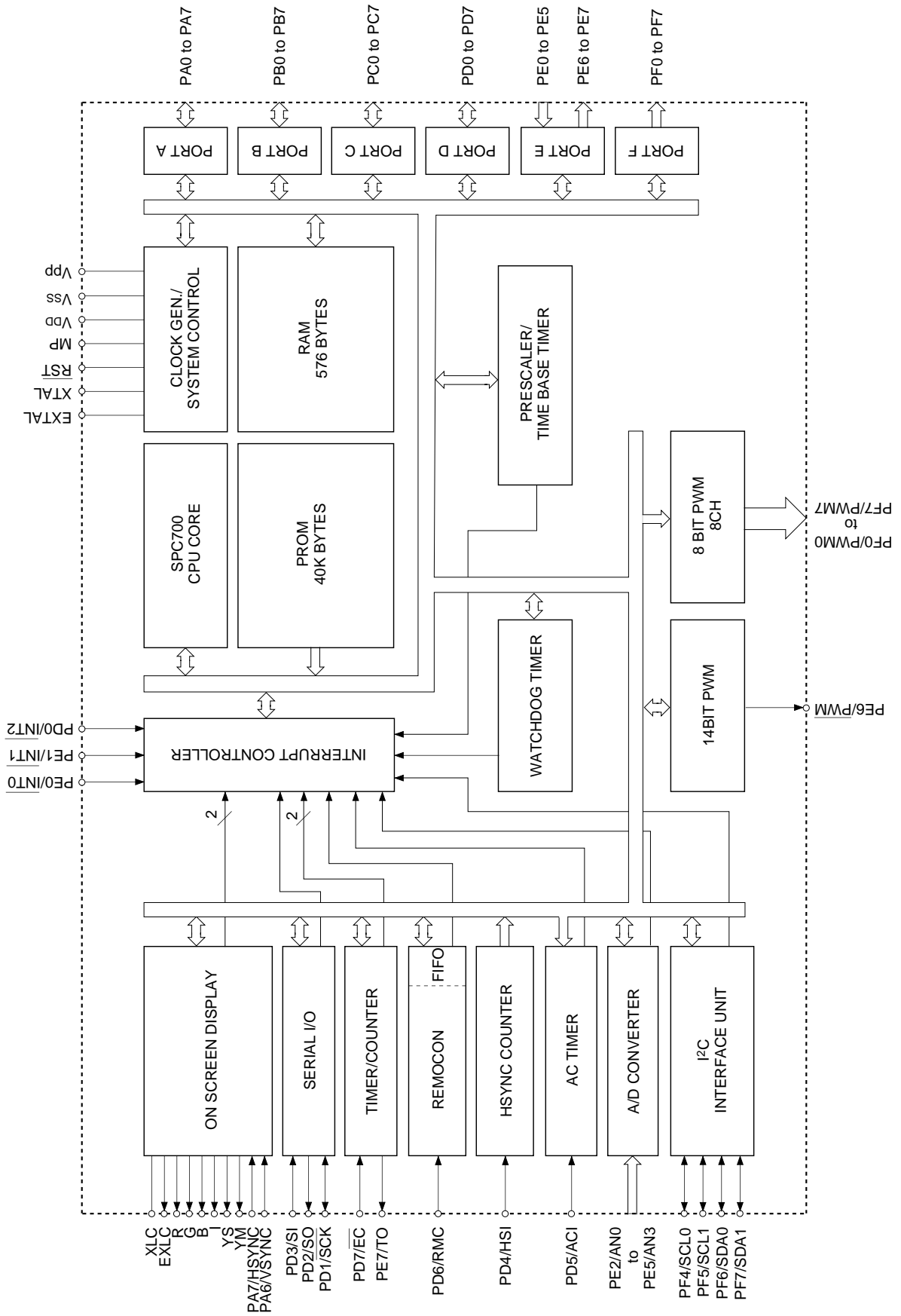
Silicon gate CMOS IC

**Features**

- A wide instruction set (213 instructions) which covers various of data
  - 16-bit arithmetic instruction/multiplication and division instructions/boolean bit operation instruction
- Minimum instruction cycle
  - 1μs/4MHz (4MHz version)
  - 0.5μs/8MHz (8MHz version)
- Incorporated PROM capacity
  - 40K bytes (For program)
  - 6.75K bytes (For OSD)
- Incorporated RAM capacity
  - 576 bytes
- Peripheral functions
  - On-screen display function
    - 12 × 18 dots, 256 types, 15 colors, 12 lines of 21 characters
    - Black frame output half blanking, shadow, background color on full screen/half blanking
    - Double scanning mode supported, jitter elimination circuit
  - I<sup>2</sup>C bus interface
  - PWM output
    - 14 bits, 1 channel
    - 8 bits, 8 channels
  - Remote control receiver circuit
    - 8-bit pulse measuring counter, 6-stage FIFO
  - A/D converter
    - 8-bit, 4 channels, successive approximation system
    - (conversion time of 40μs/4MHz, 8MHz)
  - HSYNC counter
  - Power supply frequency counter
  - Watchdog timer
  - Serial I/O
    - 8-bit synchronized
  - Timer
    - 8-bit timer, 8-bit timer/counter, 19-bit time-base timer
- Interruption
  - 14 factors, 14 vectors, multiple interrupt possible
- Standby mode
  - Sleep
- Package
  - 64-pin plastic SDIP/QFP

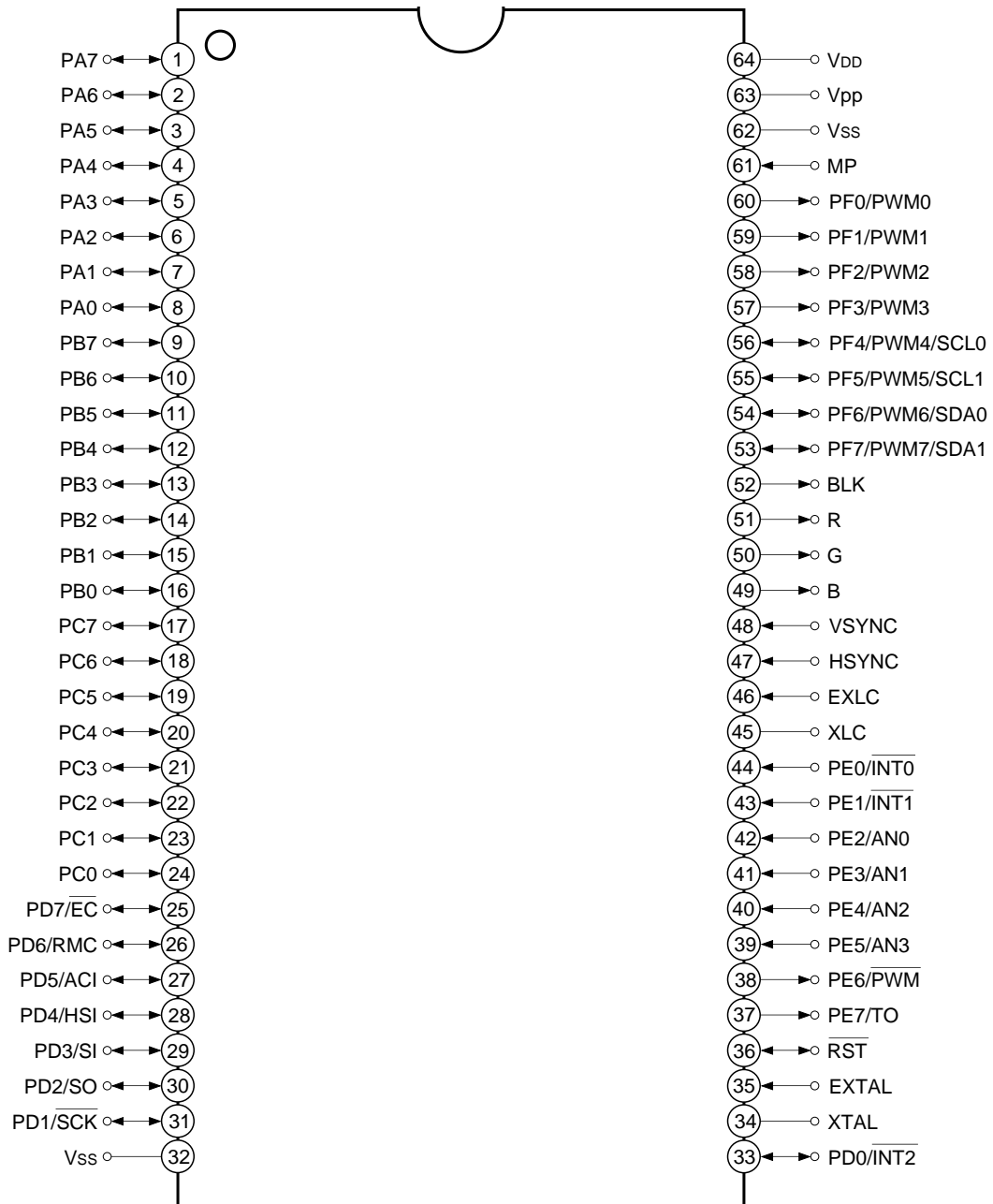
Purchase of Sony's I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system, provided that the system conforms to the I<sup>2</sup>C Standard Specifications as defined by Philips.

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.



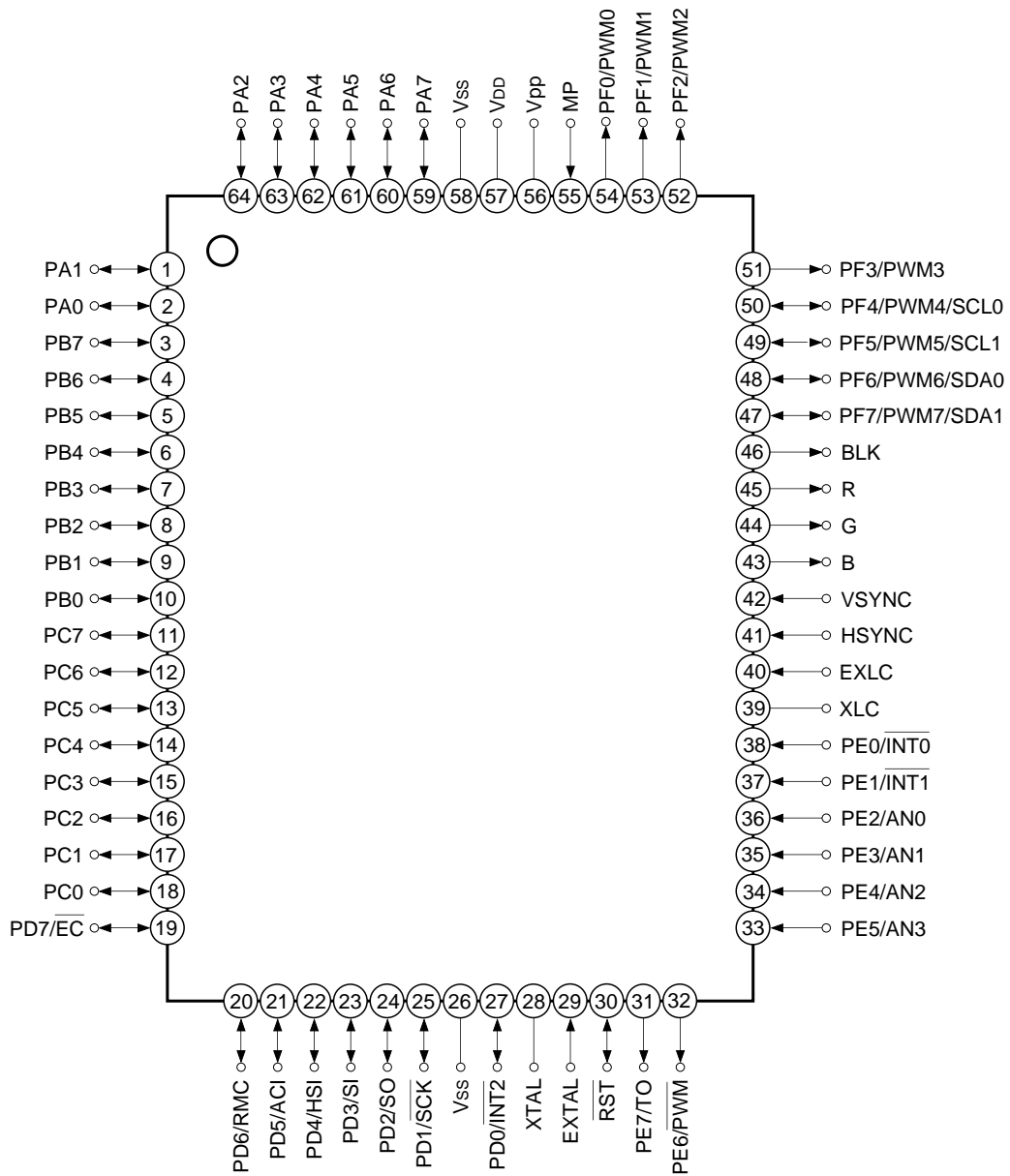
Block Diagram

Pin Assignment 1 (Top View) 64 pin SDIP Package



- Note)**
1. Vpp (Pin 63) is always connected to VDD.
  2. Vss (Pins 32 and 62) are both connected to GND.
  3. MP (Pin 61) is always connected to GND.

Pin Assignment 2 (Top View) 64 pin QFP Package



- Note)**
1. Vpp (Pin 56) is always connected to Vdd.
  2. Vss (Pins 26 and 58) are both connected to GND.
  3. MP (Pin 55) is always connected to GND.

Pin Description

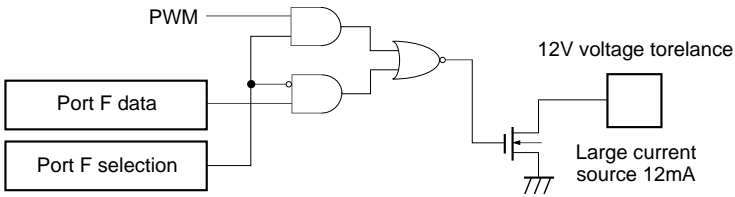
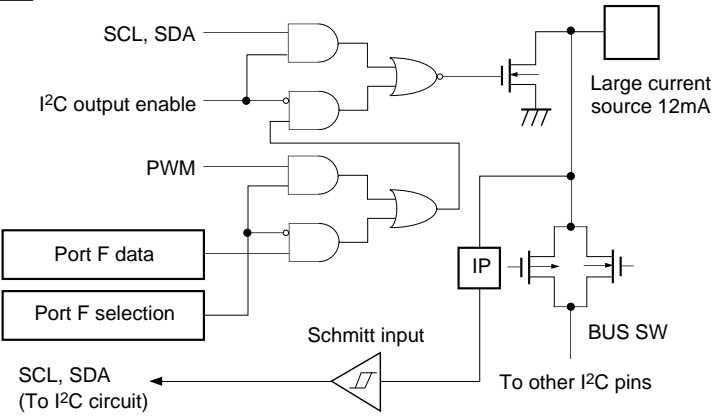
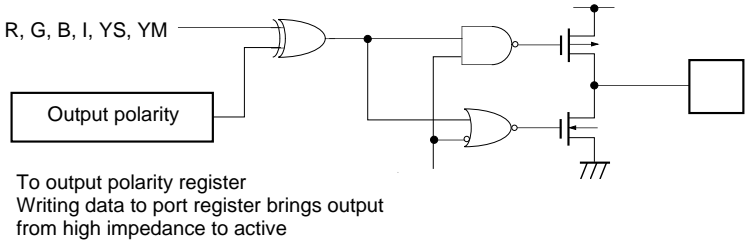
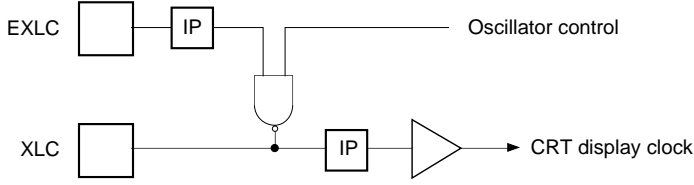
Symbol	I/O	Description	
PA0 to PA5	I/O	(Port A) Single bit selectable 8-bit I/O port.	
PA6/VSYNC	I/O/Input	(8 pins)	CRT display vertical synchronization signal input pin.
PA7/HSYNC	I/O/Input		CRT display horizontal synchronization signal input pin.
PB0 to PB7	I/O	(Port B) Single bit selectable 8-bit I/O port. (8 pins)	
PC0 to PC7	I/O	(Port C) Single bit selectable 8-bit I/O port. (8 pins)	
PD0/ $\overline{\text{INT2}}$	I/O/Input	(Port D) Single bit selectable 8-bit I/O port. 12mA sink current drive possible. (8 pins)	Input pin for external interrupt request. Active on falling edge.
PD1/ $\overline{\text{SCK}}$	I/O/I/O		Serial clock I/O pin.
PD2/SO	I/O/Output		Serial data output pin.
PD3/SI	I/O/Input		Serial data input pin.
PD4/HSI	I/O/Input		HSYNC counter input pin.
PD5/ACI	I/O/Input		Power supply frequency counter input pin.
PD6/RMC	I/O/Input		Remote control receiver circuit input pin.
PD7/ $\overline{\text{EC}}$	I/O/Input		External event timer/counter input pin.
PE0/ $\overline{\text{INT0}}$ PE1/ $\overline{\text{INT1}}$	Input/Input	(Port E) 8-bit port, lower 6 bits for input, upper 2 bits for output. (8 pins)	Input pin for external interrupt request. Active on falling edge. (2 pins)
PE2/AN0 to PE5/AN3	Input/Input		Analog input pin for A/D converter. (4 pins)
PE6/ $\overline{\text{PWM}}$	Output/Output		14-bit PWM output pin. (CMOS output)
PE7/TO	Output/Output		Square wave output for timer 1. (50% duty cycle)
PF0/PWM0 to PF3/PWM3	Output/Output	(Port F) 8-bit output port with large current (12mA) N-ch open drain output. Lower 4 bits middle voltage tolerance (12V), upper 4 bits 5V suppression. (8 pins)	8-bit PWM output pin. (8 pins)
PF4/PWM4/ SCL0 PF5/PWM5/ SCL1	Output/Output/ I/O		I <sup>2</sup> C bus interface transfer clock I/O pin.
PF6/PWM6/ SDA0 PF7/PWM7/ SDA1	Output/Output/ I/O		I <sup>2</sup> C bus interface transfer data I/O pin.
R, G, B, I, YS, YM	Output	CRT display 6-bit output pin.	

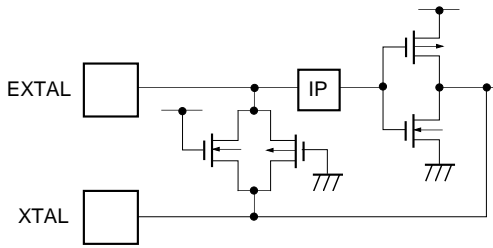
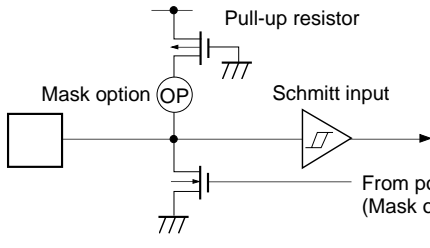
Symbol	I/O	Description
EXLC	Input	CRT display clock oscillator I/O pin. Oscillator frequency is determined by external L, C circuit.
XLC	Output	
EXTAL	Input	System clock oscillator crystal connection pin. When using an external clock, input to EXTAL pin and leave XTAL pin open.
XTAL	Output	
$\overline{\text{RST}}$	I/O	"L" level active system reset. This pin also acts as an I/O pin during power up. While internal power-on reset function is taking place a "L" level is output. (Mask option)
MP	Input	Test mode input pin. Must be connected to GND.
V <sub>DD</sub>		Positive supply voltage pin.
V <sub>pp</sub>		Positive power supply pin for incorporated PROM writing. Connect to V <sub>DD</sub> for normal operation.
V <sub>ss</sub>		GND. Both V <sub>ss</sub> pins should be connected to common GND.

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
PA0 to PA5 PB0 to PB7 PC0 to PC7  22 pins		Hi-Z
PA6/VSYNC PA7/HSYNC  2 pins		Hi-Z
PD0/ $\overline{\text{INT2}}$ PD3/SI PD4/HSI PD5/ACI PD6/RMC PD7/EC  6 pins		Hi-Z

Pin	Circuit format	When reset
<p>PD1/<math>\overline{\text{SCK}}</math> PD2/<math>\overline{\text{SO}}</math></p> <p>2 pins</p>	<p>Port D</p>	<p>Hi-Z</p>
<p>PE0/<math>\overline{\text{INT0}}</math> PE1/<math>\overline{\text{INT1}}</math></p> <p>2 pins</p>	<p>Port E</p>	<p>Hi-Z</p>
<p>PE2/<math>\overline{\text{AN0}}</math> to PE5/<math>\overline{\text{AN3}}</math></p> <p>4 pins</p>	<p>Port E</p>	<p>Hi-Z</p>
<p>PE6/<math>\overline{\text{PWM}}</math> PE7/<math>\overline{\text{TO}}</math></p> <p>2 pins</p>	<p>Port E</p>	<p>High level</p>

Pin	Circuit format	When reset
<p>PF0/PWM0 to PF3/PWM3</p> <p>4 pins</p>	<p>Port F</p> 	<p>Hi-Z</p>
<p>PF4/PWM4/ SCL0 PF5/PWM5/ SCL1 PF6/PWM6/ SDA0 PF7/PWM7/ SDA1</p> <p>4 pins</p>	<p>Port F</p> 	<p>Hi-Z</p>
<p>R G B I YS YM</p> <p>6 pins</p>	 <p>To output polarity register Writing data to port register brings output from high impedance to active</p>	<p>Hi-Z</p>
<p>EXLC XLC</p> <p>2 pins</p>		<p>Oscillation halted</p>

Pin	Circuit format	When reset
<p>EXTAL XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> <li>• Diagram indicates circuit composition during oscillation</li> <li>• Feedback resistor is disconnected during stop</li> </ul>	<p>Oscillation</p>
<p><math>\overline{\text{RST}}</math></p> <p>1 pin</p>	 <p>Pull-up resistor</p> <p>Mask option (OP)</p> <p>Schmitt input</p> <p>From power-on reset circuit (Mask option)</p>	<p>Low level</p>

## Absolute Maximum Ratings

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V <sub>DD</sub>	-0.3 to +7.0	V	
	V <sub>pp</sub>	-0.3 to +13.0	V	Incorporated PROM
Input voltage	V <sub>IN</sub>	-0.3 to +7.0* <sup>1</sup>	V	
Output voltage	V <sub>OUT</sub>	-0.3 to +7.0* <sup>1</sup>	V	
Medium voltage tolerance output voltage	V <sub>OUTP</sub>	-0.3 to +15.0	V	Pins PF0 to PF3
High level output current	I <sub>OH</sub>	-5	mA	
High level total output current	∑I <sub>OH</sub>	-50	mA	Total of all output pins
Low level output current	I <sub>OL</sub>	15	mA	Excludes large current output
	I <sub>OLC</sub>	20	mA	Large current output* <sup>2</sup>
Low level total output current	∑I <sub>OL</sub>	130	mA	Total of all output pins
Operating temperature	T <sub>opr</sub>	-10 to +75	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	
Allowable power dissipation	P <sub>D</sub>	1000	mW	SDIP
		600	mW	QFP

\*<sup>1</sup> V<sub>IN</sub> and V<sub>OUT</sub> should not exceed V<sub>DD</sub> + 0.3V.

\*<sup>2</sup> The large current drivetransistor for the PD and PF ports is a N-ch transistor.

**Note)** Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

## Recommended Operating Conditions

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V <sub>DD</sub>	4.5	5.5	V	Guaranteed range during operation
		3.5	5.5	V	Guaranteed range for low speed data*1
		2.5	5.5	V	Guaranteed data hold operation range during stop
	V <sub>pp</sub>	V <sub>pp</sub> = V <sub>DD</sub>		V	*5
High level input voltage	V <sub>IH</sub>	0.7V <sub>DD</sub>	V <sub>DD</sub>	V	I <sup>2</sup> C Schmitt input included*2
	V <sub>IHS</sub>	0.8V <sub>DD</sub>	V <sub>DD</sub>	V	CMOS Schmitt input*3
	V <sub>IHEX</sub>	V <sub>DD</sub> - 0.4	V <sub>DD</sub> + 0.3	V	EXTAL pin*4
Low level input voltage	V <sub>IL</sub>	0	0.3V <sub>DD</sub>	V	I <sup>2</sup> C Schmitt input included*2
	V <sub>ILS</sub>	0	0.2V <sub>DD</sub>	V	CMOS Schmitt input*3
	V <sub>ILEX</sub>	-0.3	0.4	V	EXTAL pin*4
Operating temperature	Topr	-10	+75	°C	

\*1 Rating for 1/16 frequency mode and sleep mode.

\*2 Normal input port (All pins of PA, PB, PC, PE2 to PE5), PF4 to PF7 pins.

\*3 Includes PD0/ $\overline{\text{INT2}}$ , PD1/ $\overline{\text{SCK}}$ , PD2, PD3/SI, PD4/HSI, PD5/ACI, PD6/RMC, PD7/ $\overline{\text{EC}}$ , PE0/ $\overline{\text{INT0}}$ , PE1/ $\overline{\text{INT1}}$ , HSYNC, VSYNC,  $\overline{\text{RST}}$  pins.

\*4 It specifies only when the external clock is input.

\*5 V<sub>pp</sub> and V<sub>DD</sub> should be set to the same voltage.

Electrical Characteristics

DC Characteristics

(Ta = -10 to +75°C, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit	
High level output voltage	VOH	PA to PD, PE6, PE7, R, G, B, I, YS, YM	VDD = 4.5V, IOH = -0.5mA	4.0			V	
			VDD = 4.5V, IOH = -1.2mA	3.5			V	
Low level output voltage	VOL	PA to PD, PE6, PE7, R, G, B, I, YS, YM, PF0 to PF3, RST	VDD = 4.5V, IOL = 1.8mA			0.4	V	
			VDD = 4.5V, IOL = 3.6mA			0.6	V	
		PD, PF	VDD = 4.5V, IOL = 12.0mA			1.5	V	
		PF4 to PF7 (SCL0, SCL1, SDA0, SDA1)	VDD = 4.5V, IOL = 3.0mA			0.4	V	
			VDD = 4.5V, IOL = 4.0mA			0.6	V	
Input current	IiHE	EXTAL	VDD = 5.5V, VIH = 5.5V	0.5		40	μA	
	IiHL		VDD = 5.5V, VIL = 0.4V	-0.5		-40	μA	
	IiLR	RST	VDD = 5.5V, VIL = 0.4V	-1.5		-400	μA	
I/O leakage current	IIZ	PA to PE, HSYNC, VSYNC, R, G, B, I, YS, YM	VDD = 5.5V, VI = 0, 5.5V			±10	μA	
Open drain output leakage current (N-ch Tr off case)	ILOH	PF0 to PF3	VDD = 5.5V, VOH = 12.0V			50	μA	
		PF4 to PF7	VDD = 5.5V, VOH = 5.5V			10	μA	
I <sup>2</sup> C bus switch connection impedance (output Tr off case)	RBS	SCL0: SCL1 SDA0: SDA1	VDD = 4.5V VSCL0 = VSCL1 = 2.25V VSDA0 = VSDA1 = 2.25V			120	Ω	
Supply current	IDD	VDD*1	Operating mode (1/2, 1/4 clock rate) 4MHz, 8MHz crystal oscillator (C1 = C2 = 22pF) All output pins open		11*2	30*2	mA	
					17*3	40*3		
	IDDSL			Sleep mode		0.6*2	3*2	mA
						0.8*3	3*3	
IDDST	Stop mode*4		—	—	—	μA		
Input capacitance	CIN	Pins other than VDD and Vss	1MHz clock 0V other than the measure pins		10	20	pF	

\*1 Rating applies only if OSD oscillator is halted.

\*2 Oscillator clock 4MHz version

\*3 Oscillator clock 8MHz version

\*4 This device does not enter the stop mode.

AC Characteristics

(1) Clock timing

(Ta = -10 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	3.5*2	4.5	MHz
				7*3	9	
System clock input pulse width	tXL, tXH	EXTAL	Fig. 1, Fig. 2 External clock drive	100*2		ns
				50*3		
System clock rise and fall times	tCR, tCF	EXTAL	Fig 1, Fig 2 External clock drive		200	ns
Event counter input clock pulse width	tEH, tEL	$\overline{EC}$	Fig. 3	tsys + 50*1		ns
Event counter input clock rise and fall times	tER, tEF	$\overline{EC}$	Fig. 3		20	ms

\*1 tsys indicates one of three values according to the contents of the clock control register (address : 00FEH) upper 2 bits (CPU clock selection)

tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

\*2 Oscillator clock 4MHz version

\*3 Oscillator clock 8MHz version

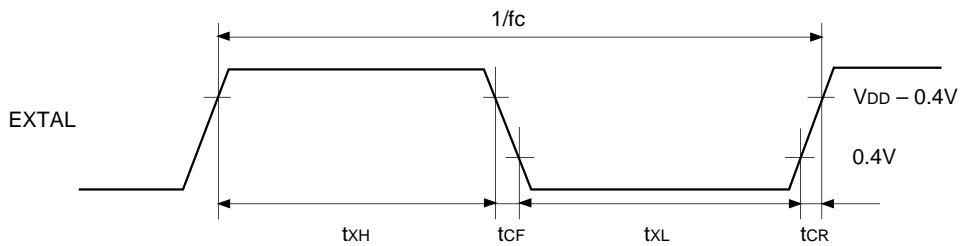


Fig. 1. Clock timing

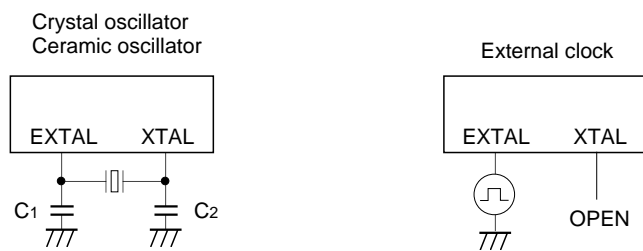


Fig. 2. Clock applied condition

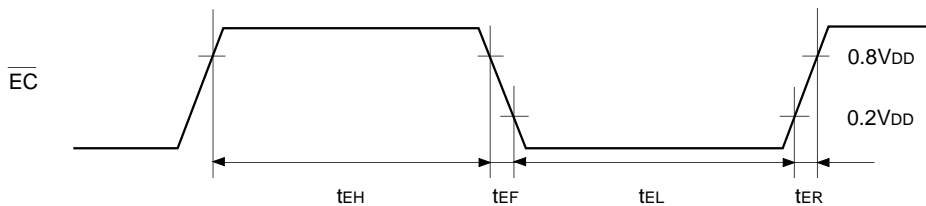


Fig. 3. Event count clock timing

(2) Serial transfer

(Ta = -10 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK}}$ cycle time	$t_{\text{KCY}}$	$\overline{\text{SCK}}$	Input mode	1000		ns
			Output mode	$8000/\text{fc}'^{*1}$		ns
$\overline{\text{SCK}}$ High and Low level widths	$t_{\text{KH}}$	$\overline{\text{SCK}}$	$\overline{\text{SCK}}$ input mode			ns
	$t_{\text{KL}}$		$\overline{\text{SCK}}$ output mode	400		ns
SI input setup time (referenced to $\overline{\text{SCK}} \uparrow$ )	$t_{\text{SIK}}$	SI	$\overline{\text{SCK}}$ input mode	$4000/\text{fc}' - 50^{*1}$		ns
			$\overline{\text{SCK}}$ output mode	100		ns
SI input hold time (referenced to $\overline{\text{SCK}} \uparrow$ )	$t_{\text{KSI}}$	SI	$\overline{\text{SCK}}$ input mode	200		ns
			$\overline{\text{SCK}}$ output mode	200		ns
$\overline{\text{SCK}} \downarrow \rightarrow \text{SO}$ delay time	$t_{\text{KSO}}$	SO	$\overline{\text{SCK}}$ input mode	100	200	ns
			$\overline{\text{SCK}}$ output mode		100	ns

**Note)** The load of  $\overline{\text{SCK}}$  output mode and SO output delay time is 50pF + 1TTL.

\*1 The value of  $\text{fc}'$  varies as shown below depending on the specification of oscillation clock option.

4MHz version ...  $\text{fc}' = \text{fc}$

8MHz version ...  $\text{fc}' = \text{fc}/2$

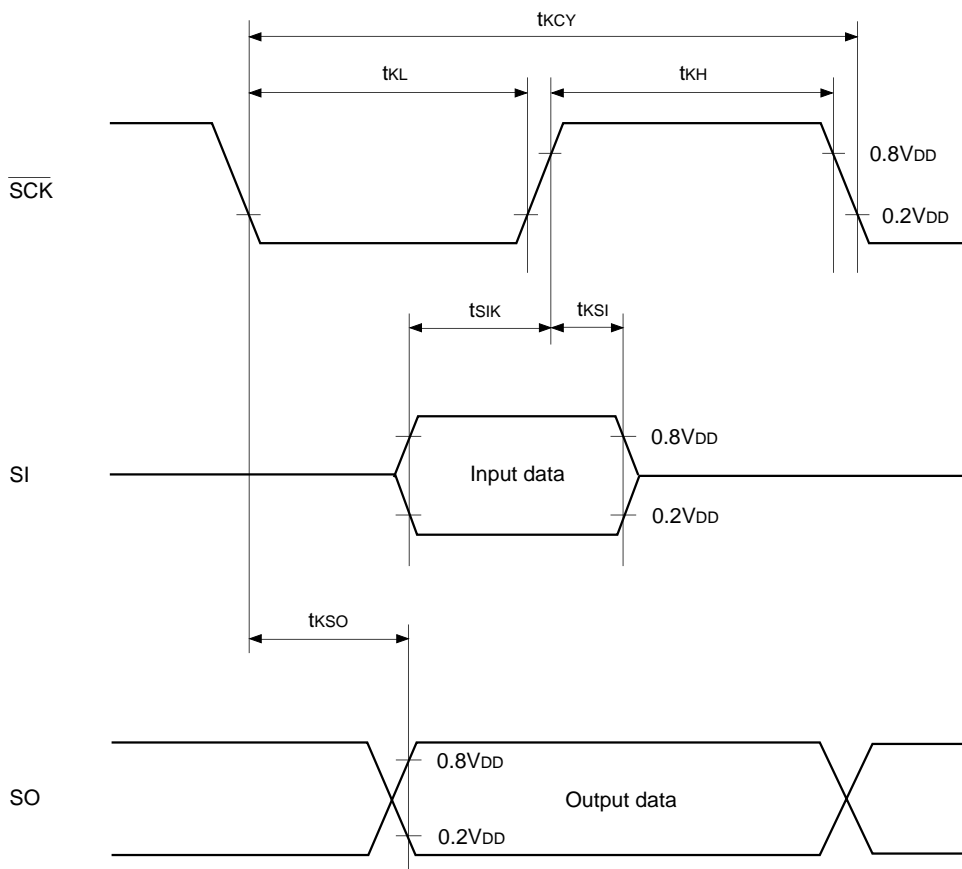


Fig. 4. Serial transfer timing

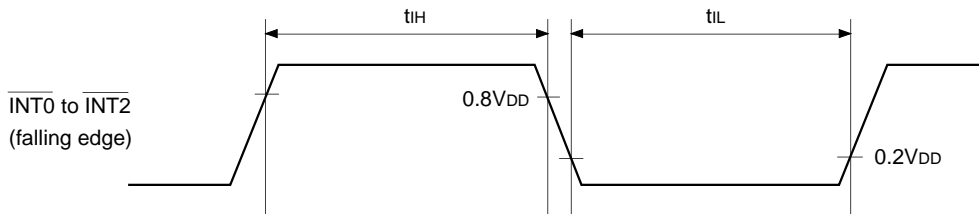
**(3) Interrupt, Reset input** (Ta = -10 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interrupt High and Low level widths	t <sub>IH</sub> t <sub>IL</sub>	$\overline{\text{INT0}}$ to $\overline{\text{INT2}}$		1		μs
Reset input low level width	t <sub>RSL</sub>	$\overline{\text{RST}}$		8/fc' *1		μs

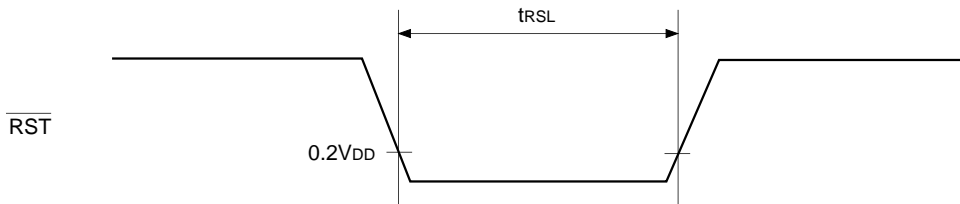
\*1 The value of fc' varies as shown below depending on the specification of oscillation clock option.

4MHz version ... fc' = fc

8MHz version ... fc' = fc/2



**Fig. 5. Interrupt input timing**

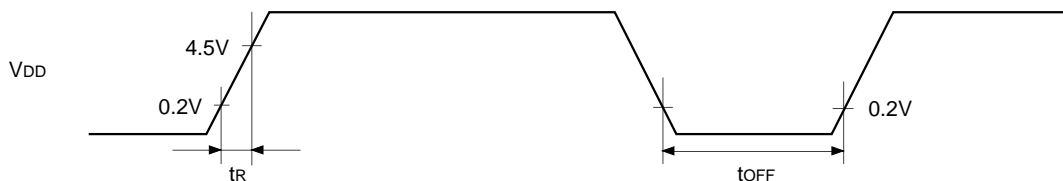


**Fig. 6.  $\overline{\text{RST}}$  input timing**

**(4) Power-on reset**

Power-on reset (Ta = -10 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rise time	t <sub>R</sub>	V <sub>DD</sub>	Power-on reset	0.05	50	ms
Power supply cutt-off time	t <sub>OFF</sub>		Repeated power-on reset	1		ms



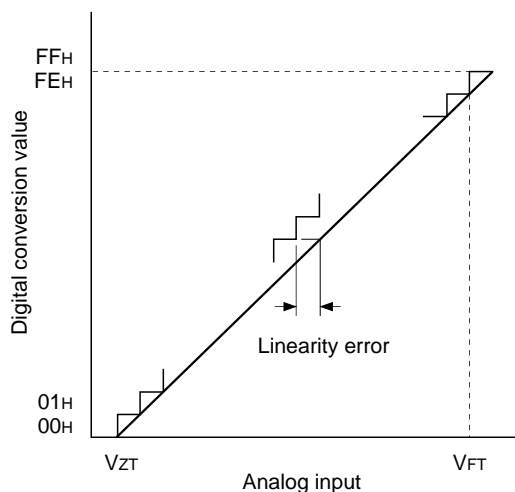
The power supply should rise smoothly.

**Fig. 7. Power-on reset**

(5) A/D converter characteristics

( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			$T_a = 25^\circ\text{C}$ $V_{DD} = 5.0\text{V}$ $V_{SS} = 0\text{V}$			$\pm 3$	LSB
Zero transition voltage	$V_{ZT}^{*1}$			-10	70	150	mV
Full-scale transition voltage	$V_{FT}^{*2}$			4930	5050	5120	mV
Conversion time	$t_{CONV}$			$160/fc' \text{ }^{*3}$			$\mu\text{s}$
Sampling time	$t_{SAMP}$			$12/fc' \text{ }^{*3}$			$\mu\text{s}$
Analog input voltage	$V_{IAN}$	AN0 to AN3		0		$V_{DD}$	V



- \*1  $V_{ZT}$ : Digital conversion values change between  $00\text{H} \leftrightarrow 01\text{H}$ .
- \*2  $V_{FT}$ : Digital conversion values change between  $\text{FEH} \leftrightarrow \text{FFH}$ .
- \*3 The value of  $fc'$  varies as shown below depending on the specification of oscillation clock option.  
 4MHz version ...  $fc' = fc$   
 8MHz version ...  $fc' = fc/2$

Fig. 8. Definitions for A/D converter terms

(6) I<sup>2</sup>C bus timing

(Ta = -10 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
SCL clock frequency	f <sub>SCL</sub>	SCL		0	100	kHz
Bus free time before starting transfer	t <sub>BUF</sub>	SDA, SCL		4.7		μs
Hold time for starting transfer	t <sub>HD; STA</sub>	SDA, SCL		4.0		μs
Clock Low level width	t <sub>LOW</sub>	SCL		4.7		μs
Clock High level width	t <sub>HIGH</sub>	SCL		4.0		μs
Setup time for repetitive transfers	t <sub>SU; STA</sub>	SDA, SCL		4.7		μs
Data hold time	t <sub>HD; DAT</sub>	SDA, SCL		0*1		μs
Data setup time	t <sub>SU; DAT</sub>	SDA, SCL		250		ns
SDA, SCL rise time	t <sub>R</sub>	SDA, SCL			1	μs
SDA, SCL fall time	t <sub>F</sub>	SDA, SCL			300	ns
Setup time for transfer completion	t <sub>SU; STO</sub>	SDA, SCL		4.7		μs

\*1 Since for part of data hold time SCL rise time (max: 300ns) is not considered, allow at least 300ns.

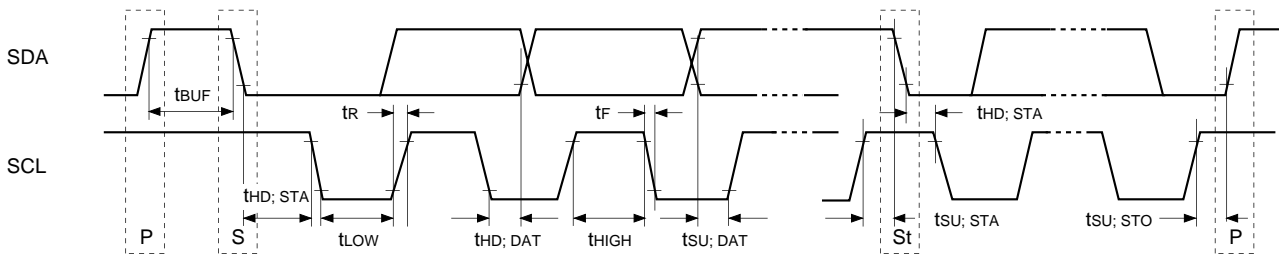


Fig. 9. I<sup>2</sup>C bus transfer data timing

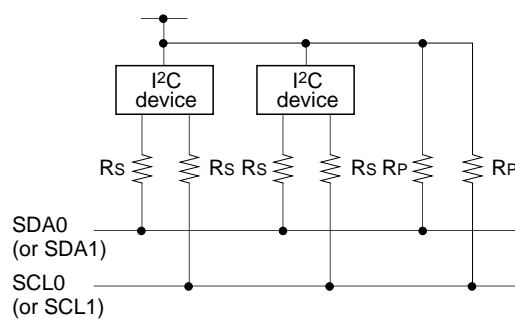


Fig. 10. I<sup>2</sup>C device recommended circuit

- A pull-up resistor (R<sub>P</sub>) must be connected to SDA0 (or SDA1), and SCL0 (or SCL1).
- The SDA0 (or SDA1) and SCL0 (or SCL1) series resistance (R<sub>s</sub> = 300Ω or less) can be used to reduce spike noise caused by CRT flashover.

(7) OSD (On Screen Display) timing

(Ta = -10 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pin	Condition	Shadow Existent		Shadow Non-existent		Unit
				Min.	Max.	Min.	Max.	
OSD clock frequency	fosc	EXLC XLC	Fig. 12	4	7*1	4	11*1	MHz
					14*2		16*2	
HSYNC pulse width	tHWD	HSYNC	Fig. 11	1.2		1.2		µs
HSYNC afterwrite rise and fall times	tHCG	HSYNC	Fig. 11		200		200	ns
VSYNC afterwrite rise and fall times	tVCG	VSYNC	Fig. 11		1.0		1.0	µs

\*1 Oscillator clock 4MHz version

\*2 Oscillator clock 8MHz version

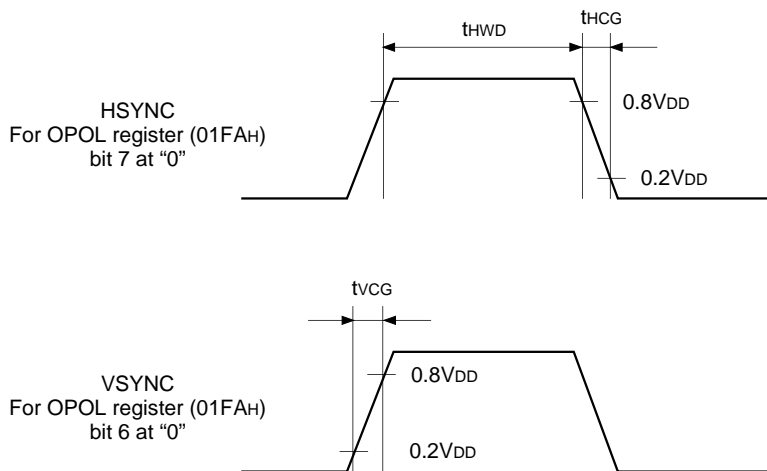


Fig. 11. OSD timing

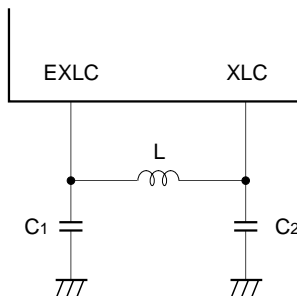


Fig. 12. LC oscillator circuit connection

Supplement



Fig. 13. Recommended oscillation circuit

Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit Example
MURATA MFG CO., LTD.	CSA4.00MG	4.00	30	30	0	(i)
	CSA4.19MG	4.19				
	CSA8.00MTZ	8.00				
	CST4.00MGW*	4.00				(ii)
	CST4.19MGW*	4.19				
	CST8.00MTW*	8.00				
RIVER ELETEC CORPORATION	HC-49/U03	4.00	12	12	0	(i)
		4.19				
		8.00				
KINSEKI LTD.	HC-49/U(-S)	4.00	27	27	0	(i)
		4.19				
		8.00				

\* Indicates types with on-chip grounding capacitors (C1 and C2).

Product List

Option item	Mask	CXP853P40AS-2- □□□ CXP853P40AQ-2- □□□	CXP853P40AS-3- □□□ CXP853P40AQ-3- □□□
Package	64-pin plastic SDIP/QFP	64-pin plastic SDIP/QFP	64-pin plastic SDIP/QFP
PROM capacitance	24K/32K/40K bytes	PROM 40K bytes	PROM 40K bytes
Reset pin pull-up resistor	Existent/Non-existent	Existent	Existent
Power-on reset circuit	Existent/Non-existent	Existent	Existent
Font data	User specified	User specified (PROM)*1	User specified (PROM)*1
Oscillator clock	4MHz/8MHz	4MHz	8MHz

\*1 The font data for the one-time PROM version is operated in the same way as the program writing.

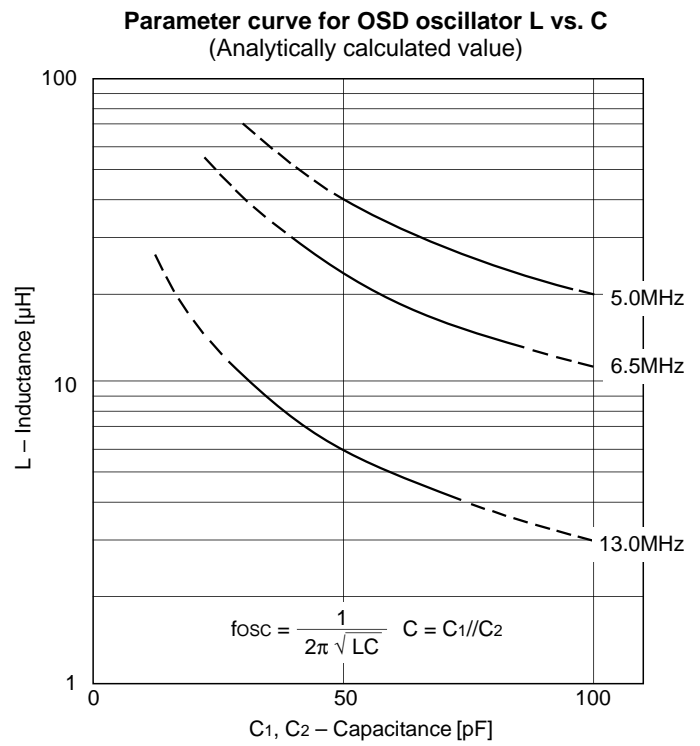
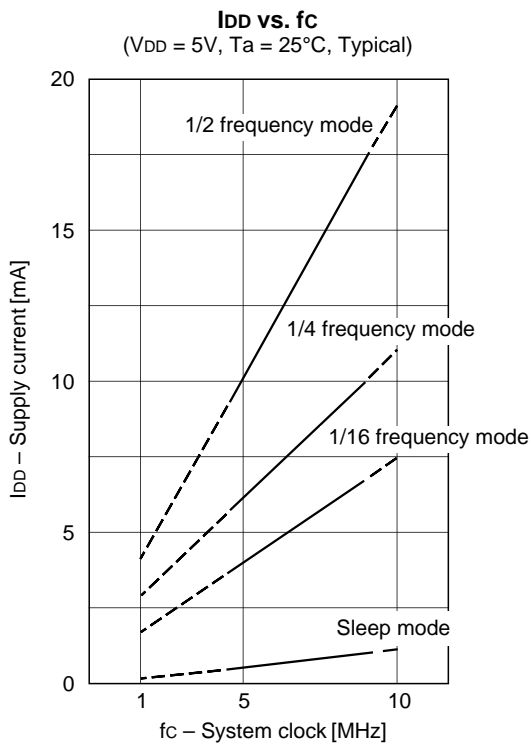
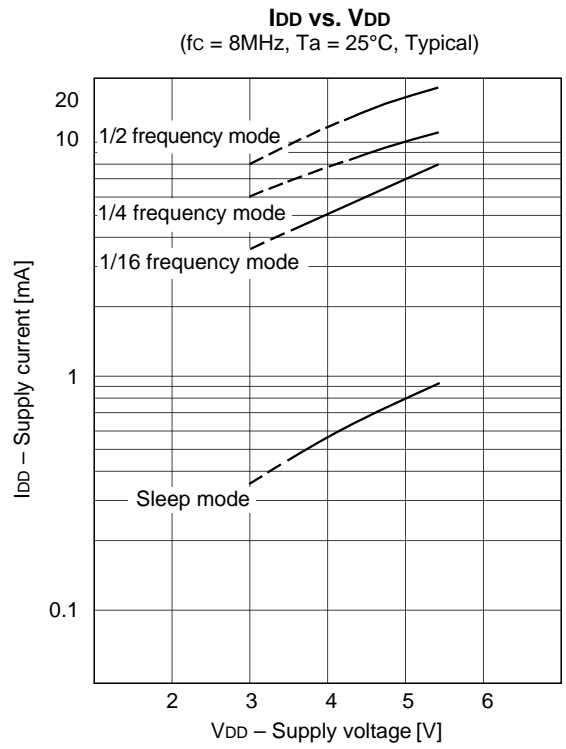
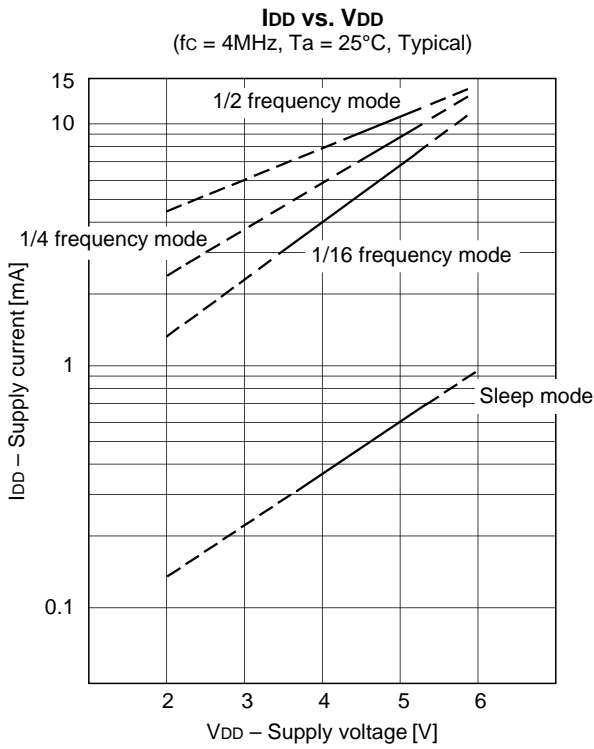
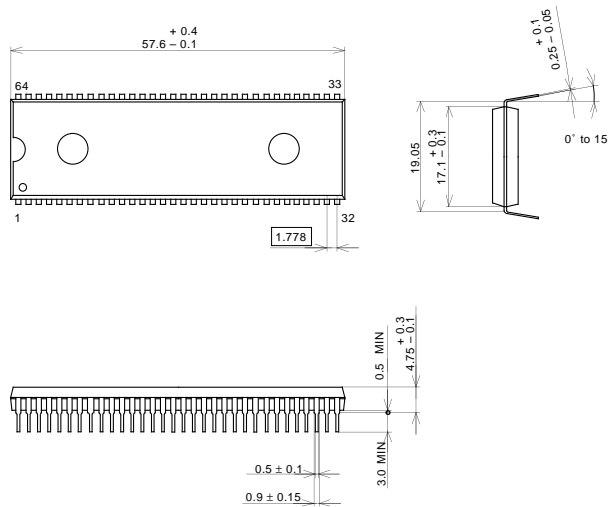


Fig. 14. Characteristic curves

Package Outline

Unit: mm

64PIN SDIP (PLASTIC)

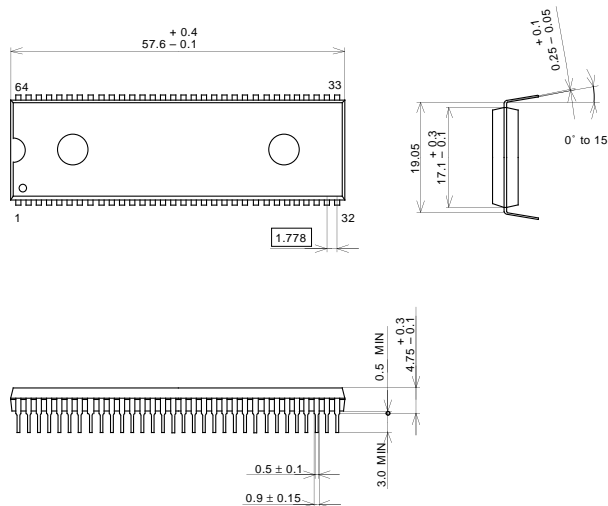


PACKAGE STRUCTURE

SONY CODE	SDIP-64P-01
EIAJ CODE	P-SDIP64-17.1x57.6-1.778
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	8.6g

64PIN SDIP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SDIP-64P-01
EIAJ CODE	P-SDIP64-17.1x57.6-1.778
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	8.6g

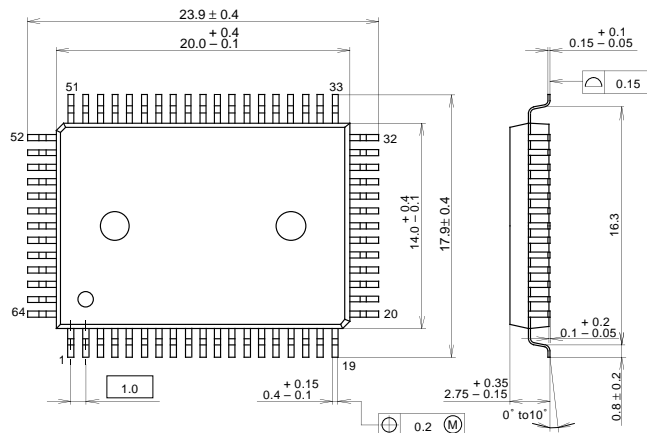
LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18 $\mu$ m

Package Outline

Unit: mm

64PIN QFP (PLASTIC)

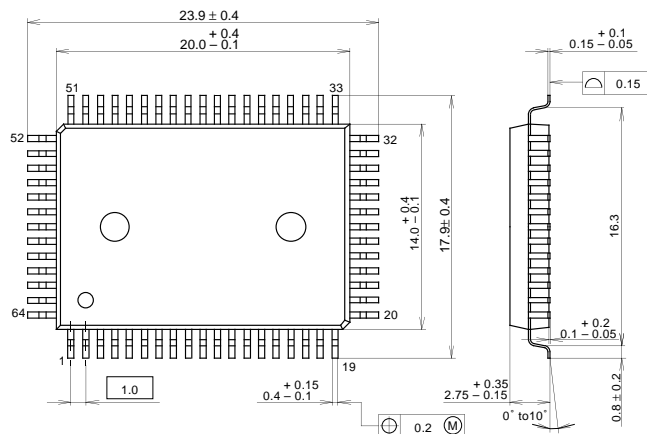


PACKAGE STRUCTURE

SONY CODE	QFP-64P-L01
EIAJ CODE	P-QFP64-14x20-1.0
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g

64PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-64P-L01
EIAJ CODE	P-QFP64-14x20-1.0
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18 $\mu$ m



LittleDiode supplies new, hard to find or obsolete electronic components and semiconductors all over the world.

With over two million different components listed you are sure to find the part you need.

Feel free to visit us today at our online store:

[LittleDiode.com](http://LittleDiode.com)

Looking forward to providing you with the best possible service.