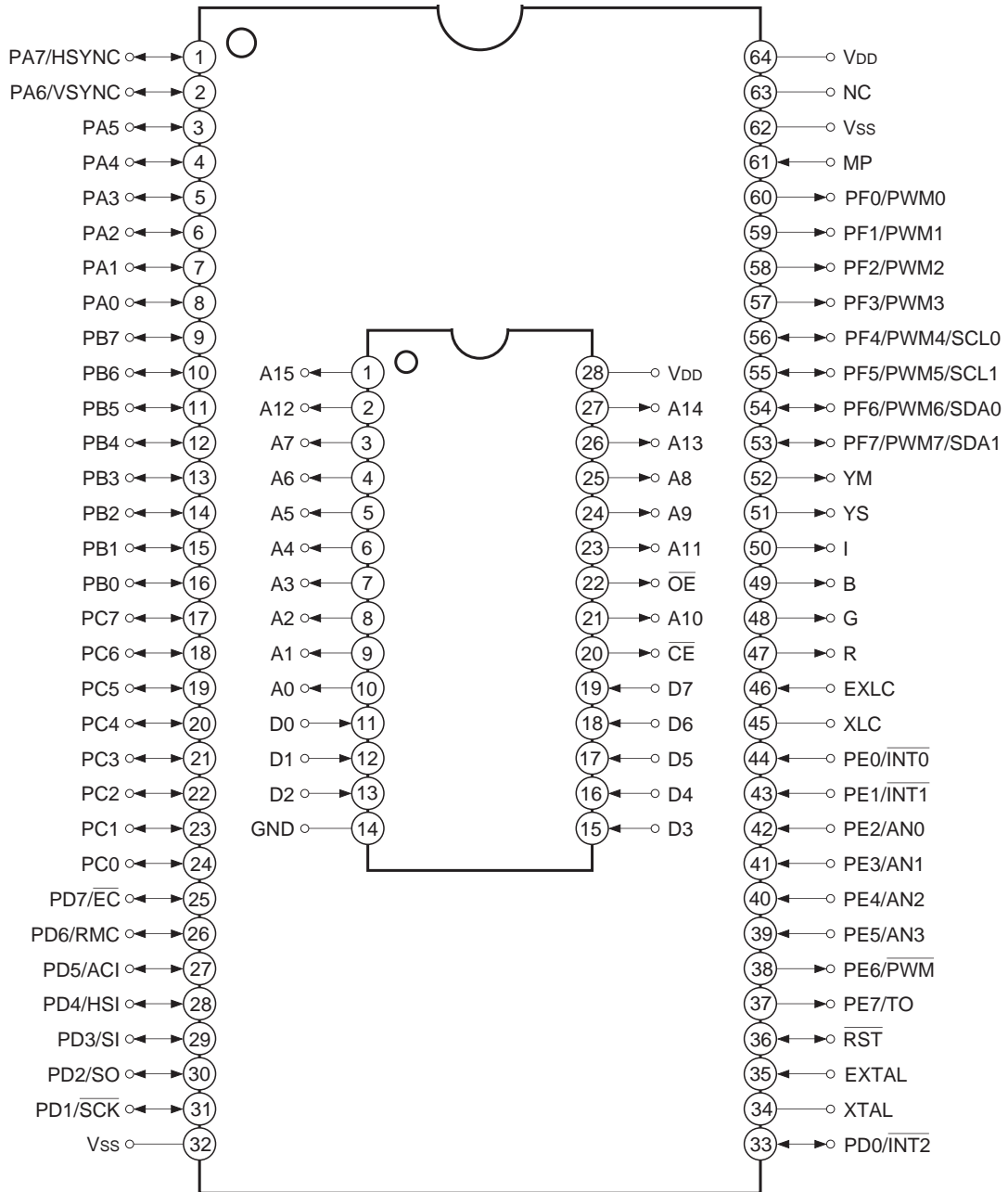


CXP85300A

Pin Assignment: Piggyback mode 1

(Top View) 64 pin PSDIP Package

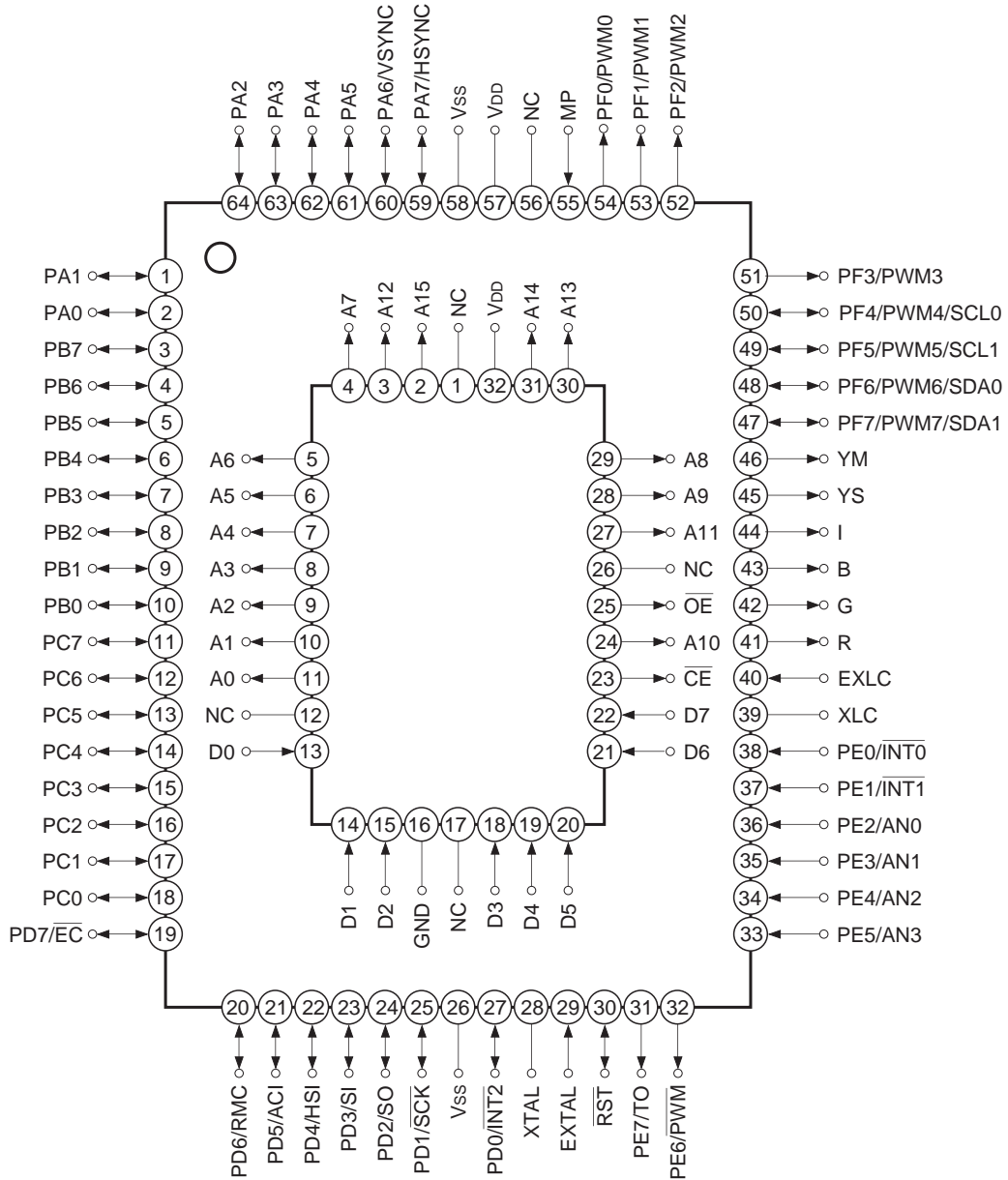


- Note)**
1. NC (Pin 63) is always connected to VDD.
 2. Vss (Pins 32 and 62) are always connected to GND.
 3. MP (Pin 61) is always connected to GND.

CXP85300A

Pin Assignment: Piggyback mode 2

(Top View) 64 pin PQFP Package

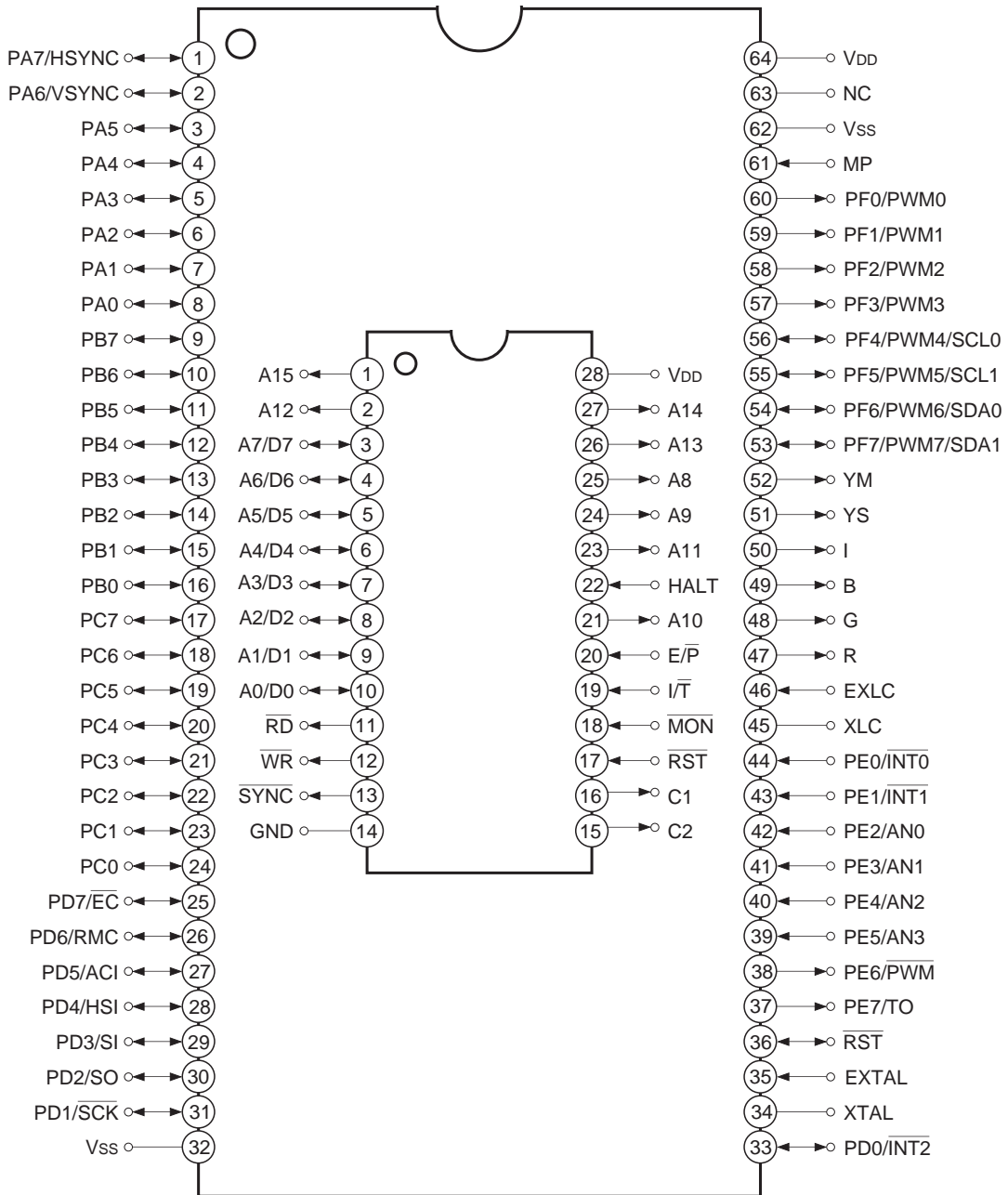


- Note)**
1. NC (Pin 56) is always connected to VDD.
 2. Vss (Pins 26 and 58) are always connected to GND.
 3. MP (Pin 55) is always connected to GND.

CXP85300A

Pin Assignment: Evaluator Mode 1

(Top View) 64 pin PSDIP Package

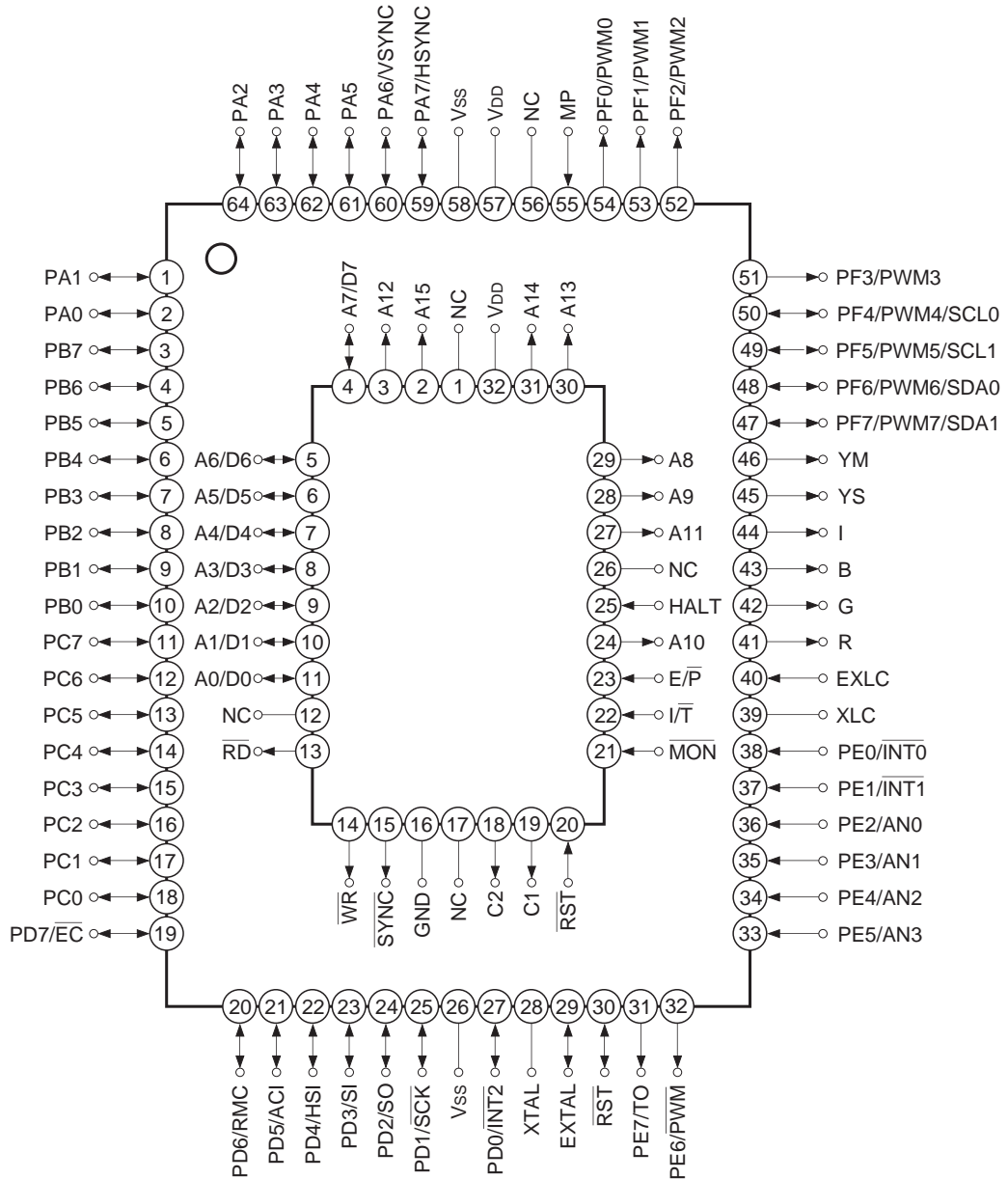


- Note)**
1. NC (Pin 63) is always connected to VDD.
 2. Vss (Pins 32 and 62) are always connected to GND.
 3. MP (Pin 61) is always connected to GND.

CXP85300A

Pin Assignment: Evaluator Mode 2

(Top View) 64 pin PQFP Package

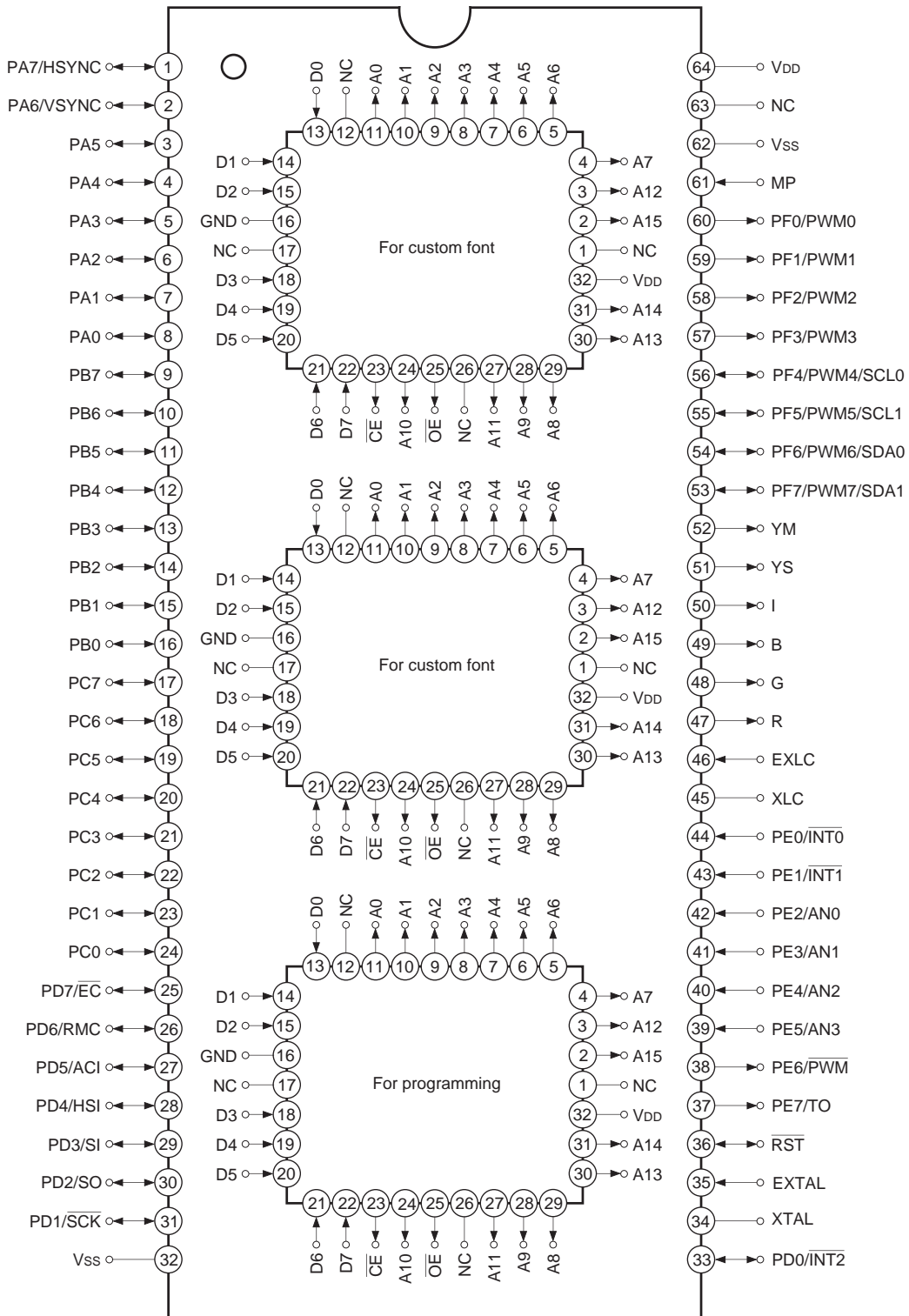


- Note)**
1. NC (Pin 56) is always connected to VDD.
 2. Vss (Pins 26 and 58) are always connected to GND.
 3. MP (Pin 55) is always connected to GND.

CXP85390A

Pin Assignment: Piggyback Mode

(Top View) 64 pin PSDIP Package

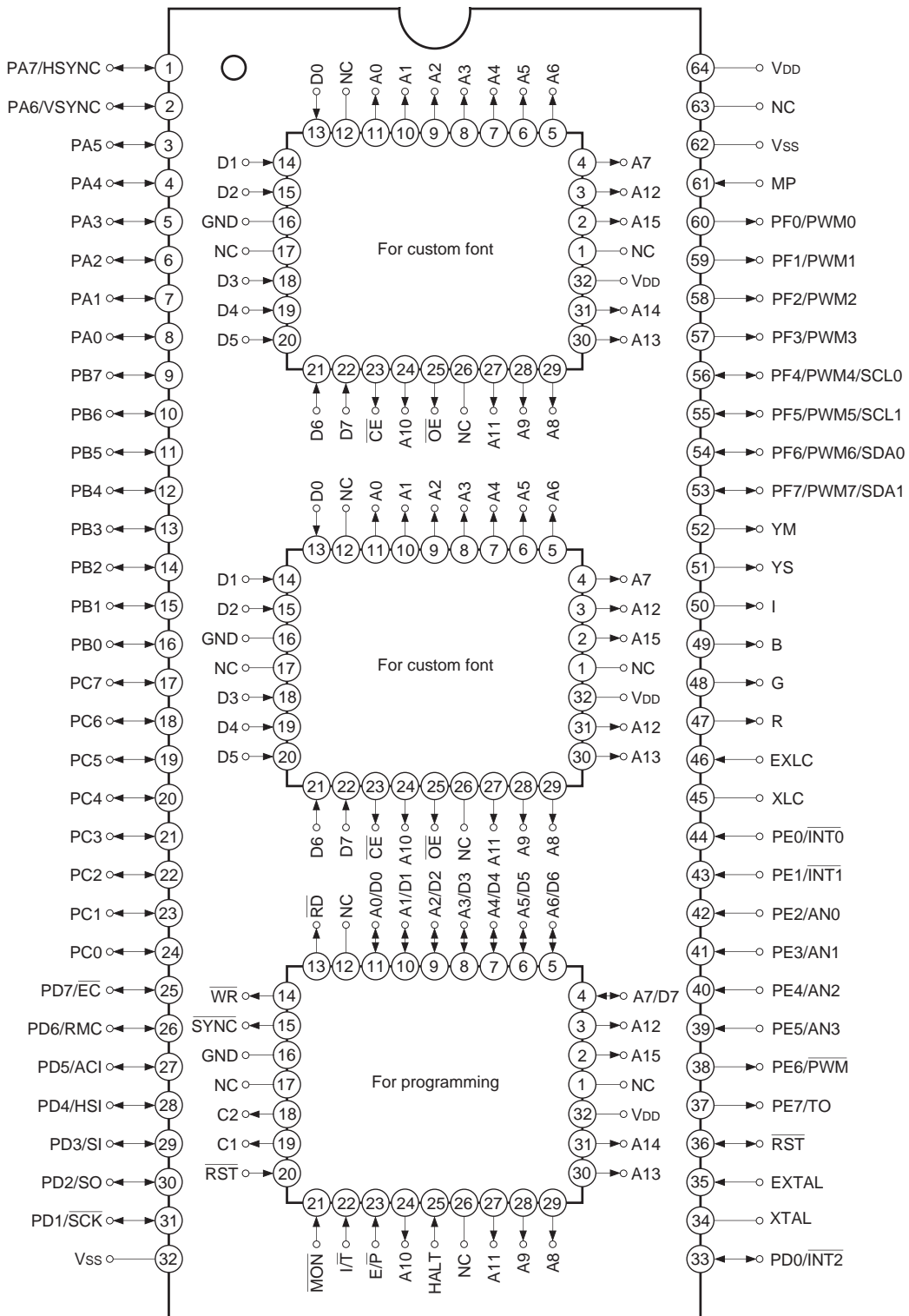


- Note)**
1. NC (Pin 63) is always connected to V_{DD}.
 2. V_{ss} (Pins 32 and 62) are always connected to GND.
 3. MP (Pin 61) is always connected to GND.

CXP85390A

Pin Assignment: Evaluator Mode

(Top View) 64 pin PSDIP Package



- Note)**
1. NC (Pin 63) is always connected to V_{DD}.
 2. V_{SS} (Pins 32 and 62) are always connected to GND.
 3. MP (Pin 61) is always connected to GND.

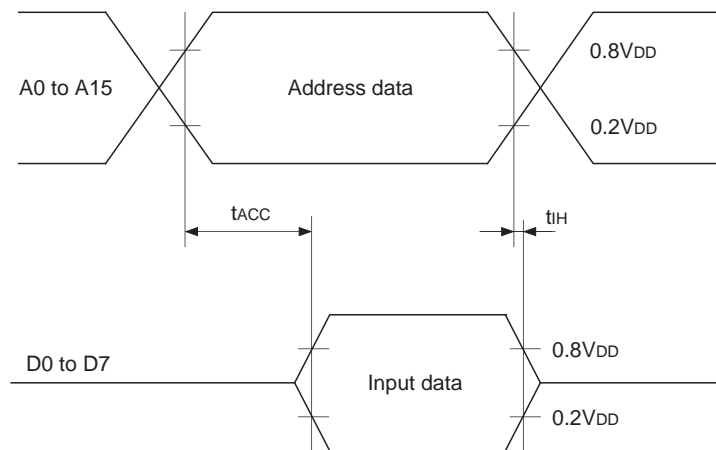
EPROM Read Timing

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$)

| Item | Symbol | Pin | Min. | Max. | Unit |
|---------------------------------|-----------|-----------------------|------|-------|------|
| Address → data input delay time | t_{ACC} | A0 to A15 D0 to D7 | | 150*1 | ns |
| | | | | 250*2 | |
| Address → data hold time | t_{IH} | A0 to A15 D0 to D7 | 0 | | ns |

*1 Oscillator clock 8MHz version

*2 Oscillator clock 4MHz version

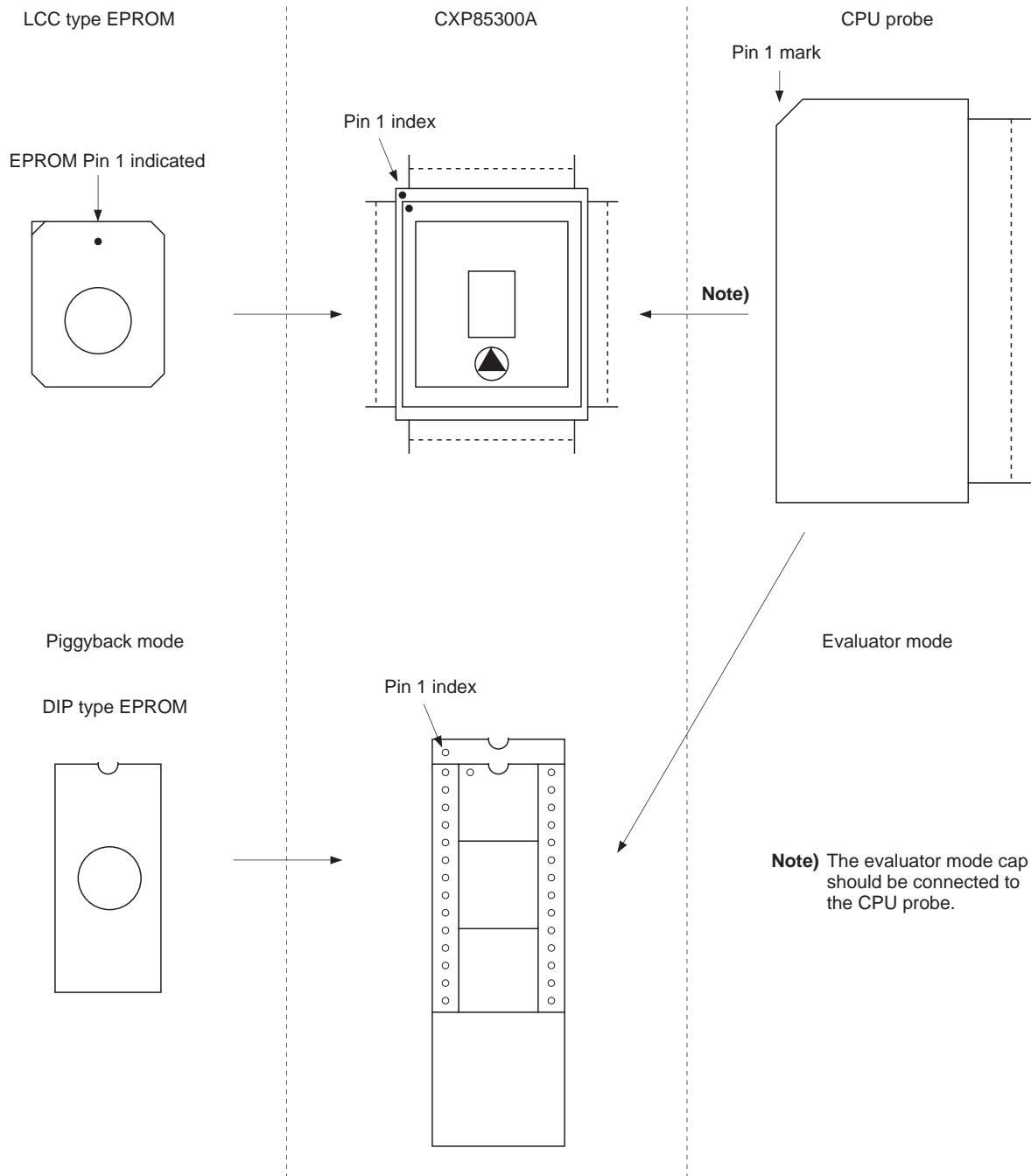


Product List

| Optional item | Product | | | | | | |
|----------------------------|-------------------------|-----------|-----------|----------------------------------|----------------------------------|----------------------|----------------|
| | Mask | | | Piggyback/evaluator | | | |
| | CXP85324A | CXP85332A | CXP85340A | CXP85300A-U02S CXP85300A-U02Q | CXP85300A-U03S CXP85300A-U03Q | CXP85390A-U02S | CXP85390A-U03S |
| Package | 64 pin plastic SDIP/QFP | | | 64 pin ceramic PSDIP/PQFP | | 64 pin ceramic PSDIP | |
| Oscillator clock | 4MHz/8MHz | | | 4MHz | 8MHz | 4MHz | 8MHz |
| ROM capacity | 24K bytes | 32K bytes | 40K bytes | EPROM 40K bytes | | | |
| Reset pin pull-up resistor | Existent/Non existent | | | Existent | | | |
| Power-on reset circuit | Existent/Non existent | | | Existent | | | |
| Font data | User data | | | Fixed | | EPROM 16K bytes | |

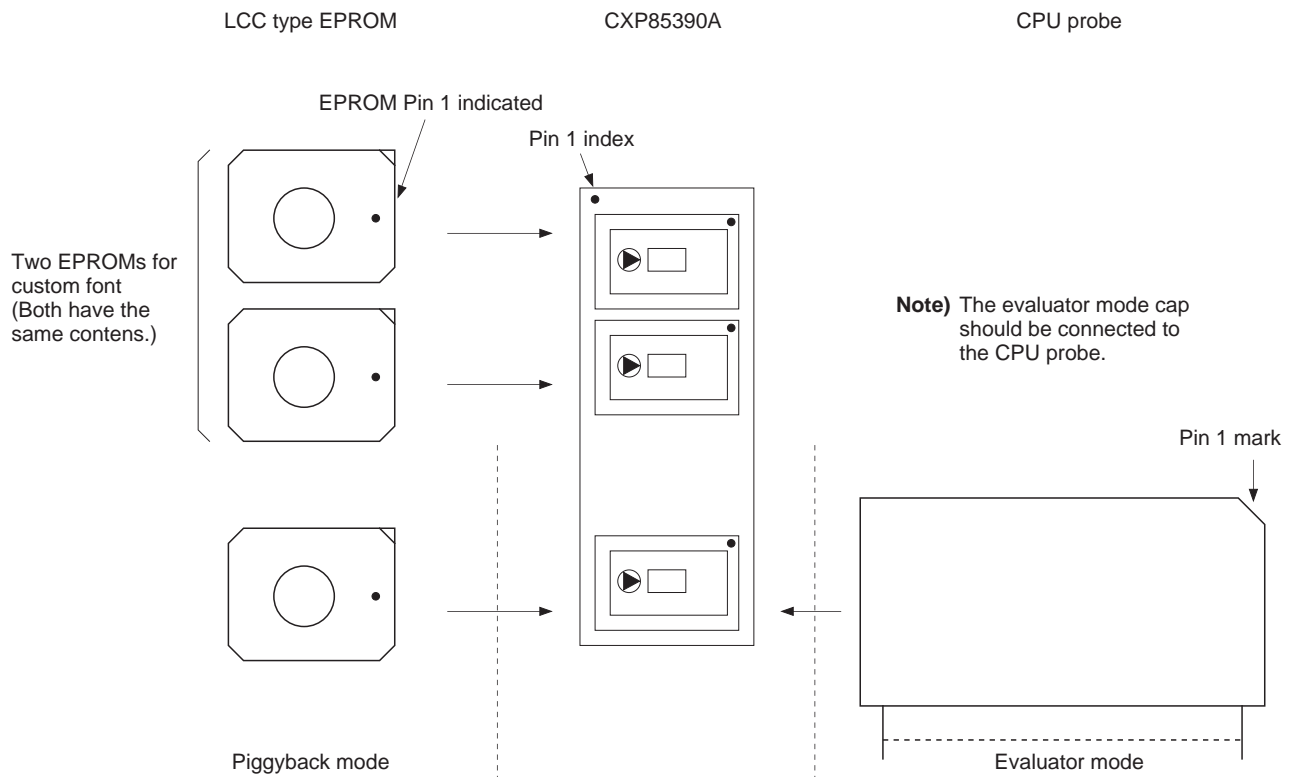
CXP85300A

Piggyback mode/evaluator mode switching process is as follows.



CXP85390A

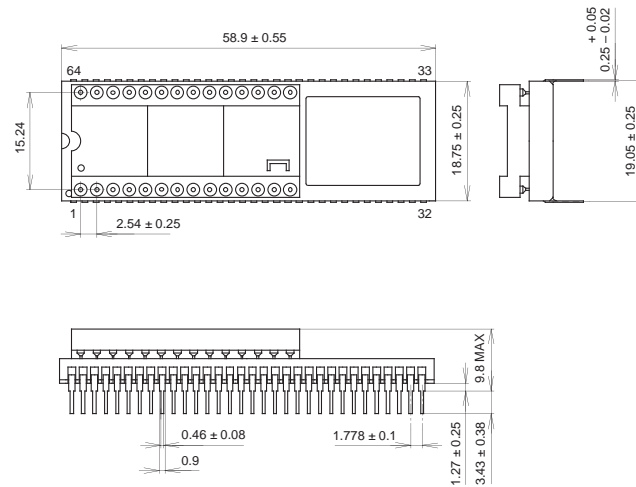
Piggyback mode/evaluator mode switching process is as follows.



Package Outline

Unit: mm

64PIN PSDIP (CERAMIC) 750mil

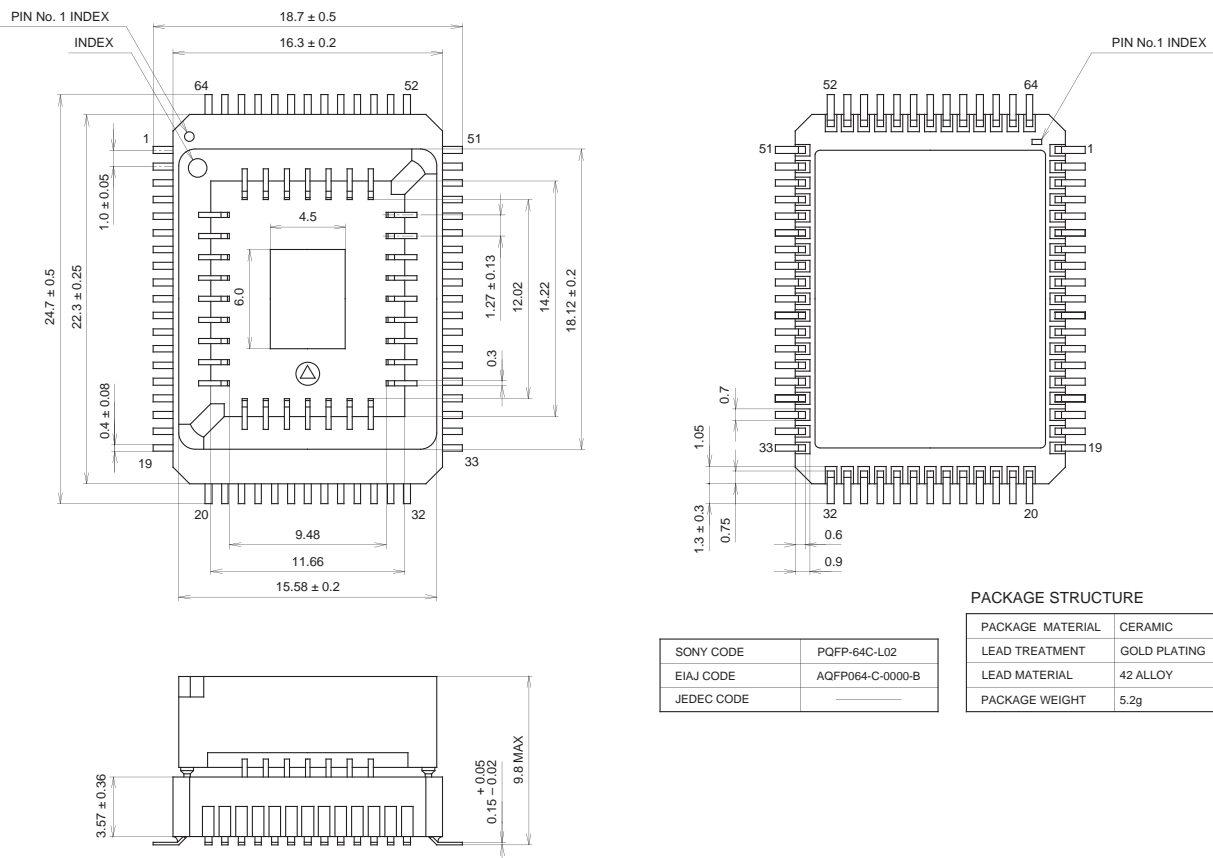


PACKAGE STRUCTURE

| | |
|------------|------------------|
| SONY CODE | PSDIP-64C-01 |
| EIAJ CODE | ADIP064-C-0750-A |
| JEDEC CODE | |

| | |
|------------------|--------------|
| PACKAGE MATERIAL | CERAMIC |
| LEAD TREATMENT | GOLD PLATING |
| LEAD MATERIAL | 42 ALLOY |
| PACKAGE WEIGHT | 16.0g |

64PIN PQFP (CERAMIC)



PACKAGE STRUCTURE

| | |
|------------|------------------|
| SONY CODE | PQFP-64C-L02 |
| EIAJ CODE | AQFP064-C-0000-B |
| JEDEC CODE | |

| | |
|------------------|--------------|
| PACKAGE MATERIAL | CERAMIC |
| LEAD TREATMENT | GOLD PLATING |
| LEAD MATERIAL | 42 ALLOY |
| PACKAGE WEIGHT | 5.2g |



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