SONY

CXP851P16

CMOS 8-bit Single Chip Microcomputer

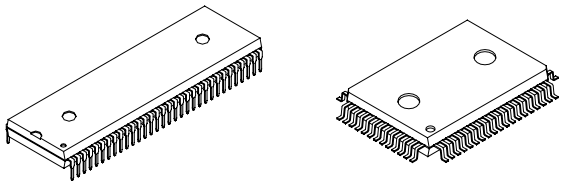
Description

The CXP851P16 are highly integrated microcomputers composed of a 8-bit CPU, PROM, RAM, and I/O ports. These chips feature many other high-performance circuits in a single-chip CMOS design, including an A/D converter, serial interface, timer/counter, time-base timer, vector interrupt, on-screen display function, I²C bus interface, PWM generator, remote control receiver, HSYNC counter, power supply frequency counter, and watchdog timer.

Also this IC provides power-on reset and sleep functions. The designers have ensured low power consumption for these powerful microcomputers.

The CXP851P16 is the on-chip PROM version of the CXP85116 with on-chip mask ROM, providing the function of being able to write directly into the program. Furthermore, because of the OSD character ROM can also be written directly into, it is suitable for evaluation use during system development and for small quantity production.

64 pin SDIP (Plastic) 64 pin QFP (Plastic)



Structure

Silicon gate CMOS IC

Features

- A wide instruction set (213 instructions) which cover various types of data.
  — 16-bit arithmetic instruction/multiplication and division instructions/boolean bit operation instruction
- Minimum instruction cycle — During operation 1µs/4MHz
- Incorporated PROM capacity — 16K bytes (For program)
  3K bytes (For OSD)
- Incorporated RAM capacity — 352 bytes
- Peripheral functions
  — On-screen display function — 12 × 16 dots, 128 types
  4 lines of 21 characters (5 or more lines possible)
  double scanning mode supported includes jitter elimination circuit
  — I²C bus interface
  — PWM output — 14-bits, 1 channel
  6-bits, 8 channels
  — Remote control receiving circuit — 8-bit pulse measuring counter, 6-stage FIFO
  — A/D converter — 4-bit, 4-channel, successive approximation method
  (conversion time of 40µs/4MHz)
  — HSYNC counter
  — Power supply frequency counter
  — Watchdog timer
  — 8-bit synchronized serial I/O
  — 8-bit timer, 8-bit timer/counter, 19-bit time-base timer
- Interruption — 14 factors, 14 vectors, multiple interrupt possible
- Standby mode — SLEEP/STOP
- Package — 64-pin plastic SDIP/QFP

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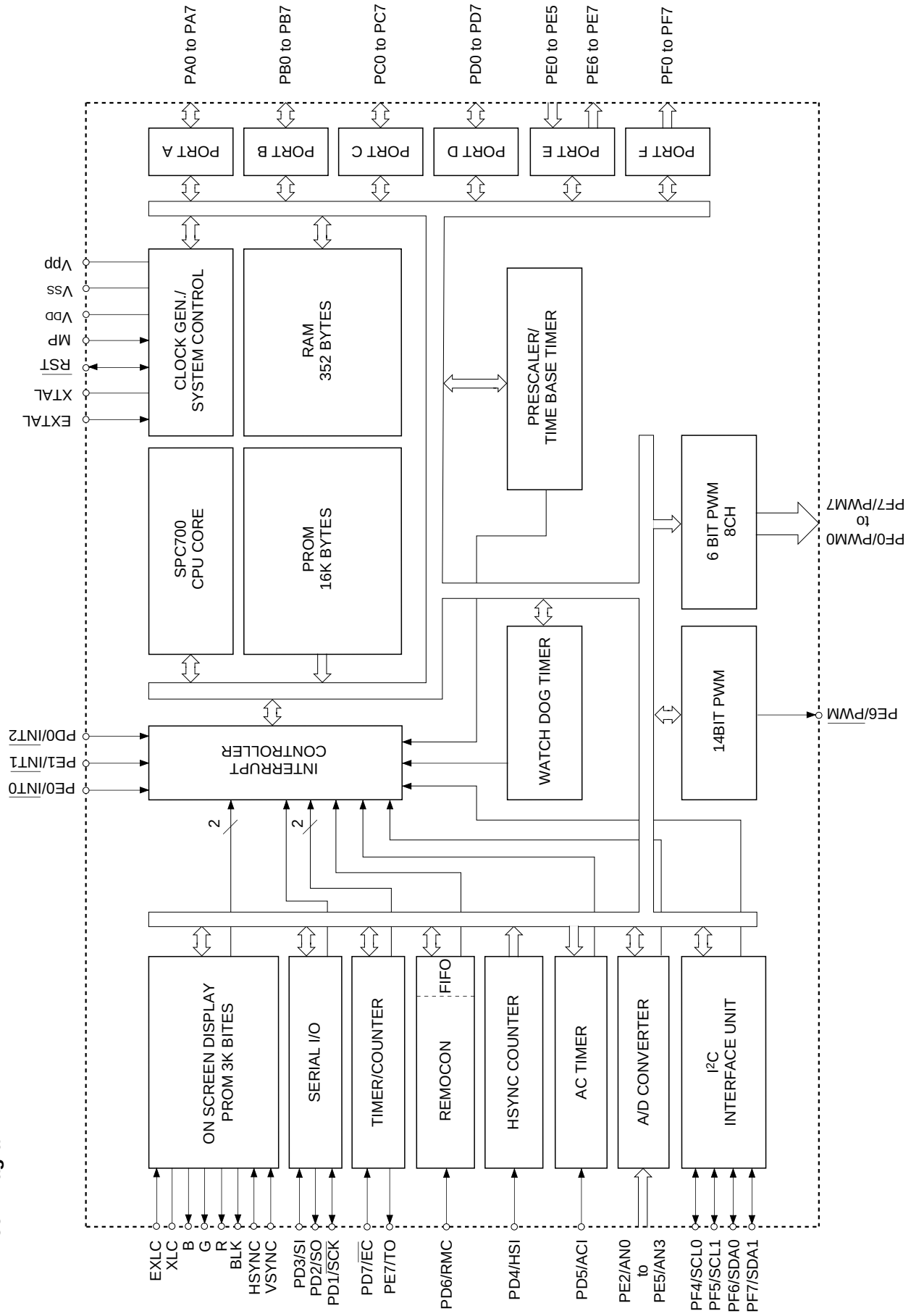
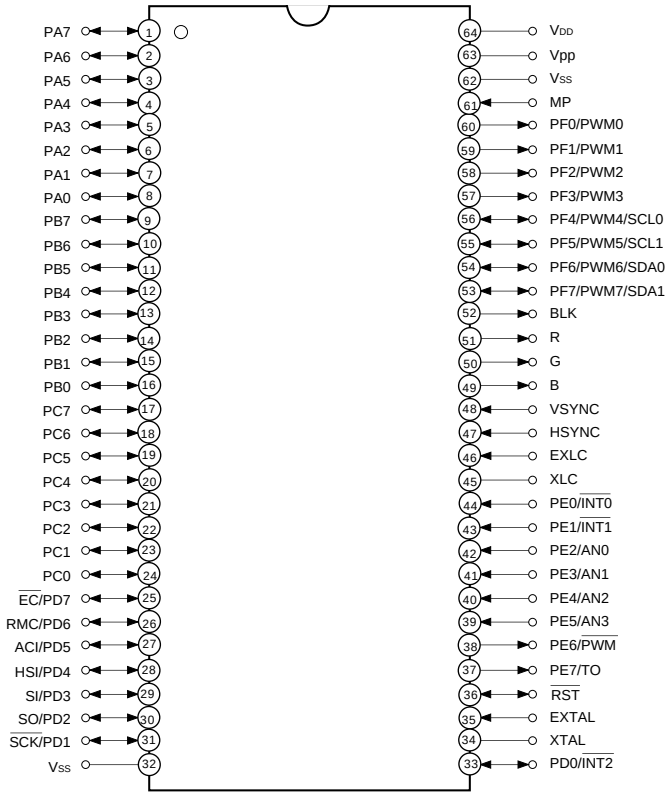
E94332A18-PS

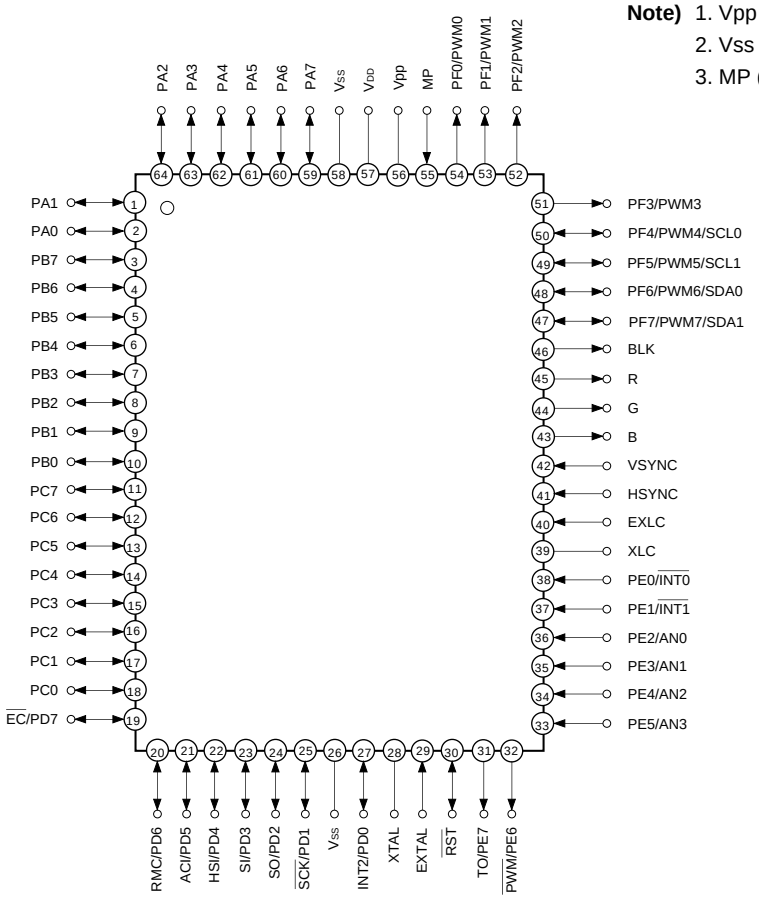
Block Diagram



Pin Configuration (Top View)



Note) 1. Vpp (Pin 63) is always connected to VDD.
2. Vss (Pins 32 and 62) are both connected to GND.
3. MP (Pin 61) is always connected to GND.



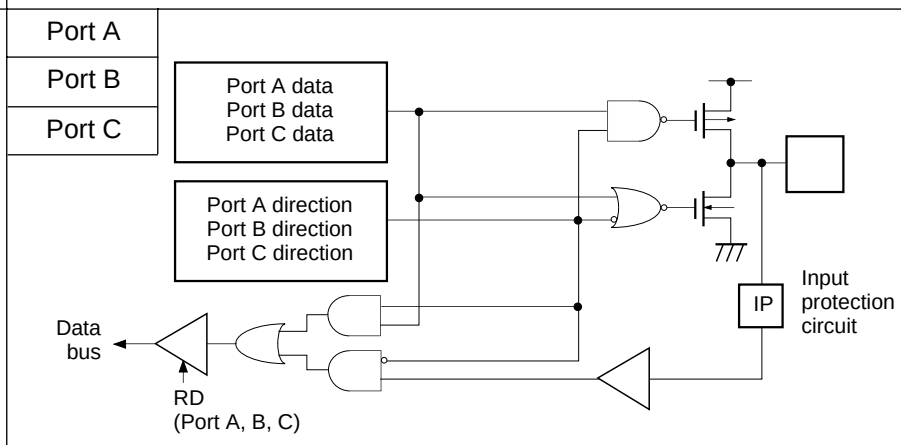
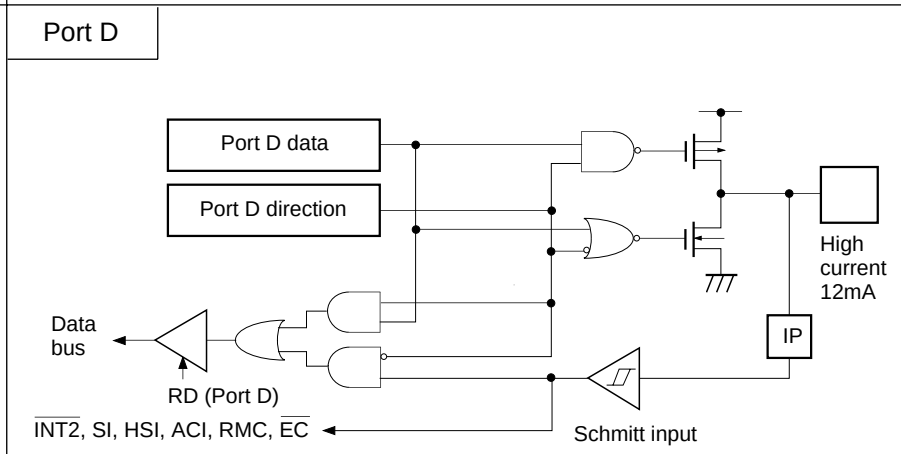
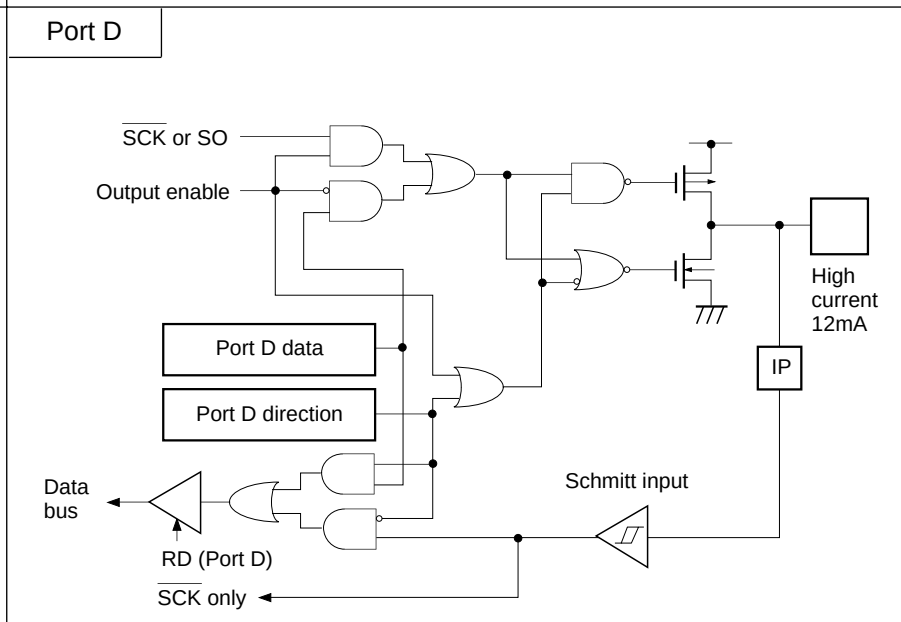
Note) 1. Vpp (Pin 56) is always connected to VDD.
2. Vss (Pins 26 and 58) are both connected to GND.
3. MP (Pin 55) is always connected to GND.

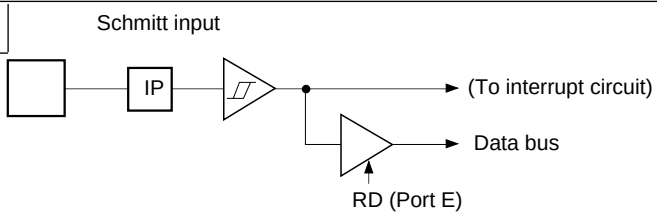
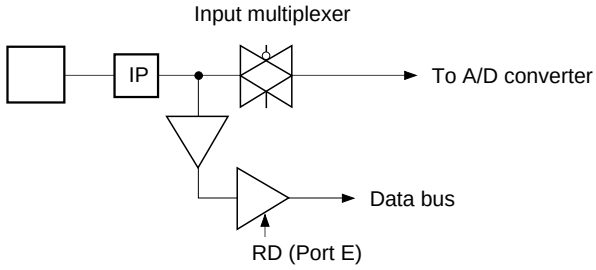
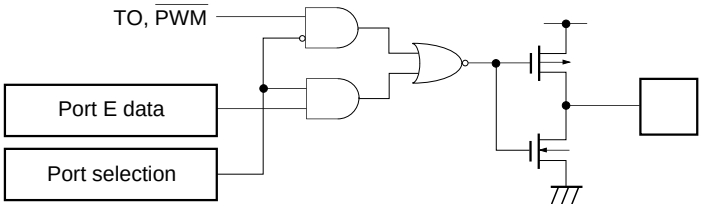
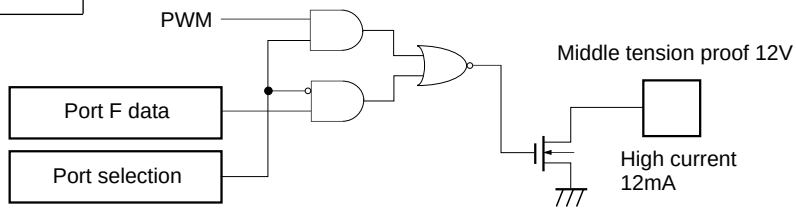
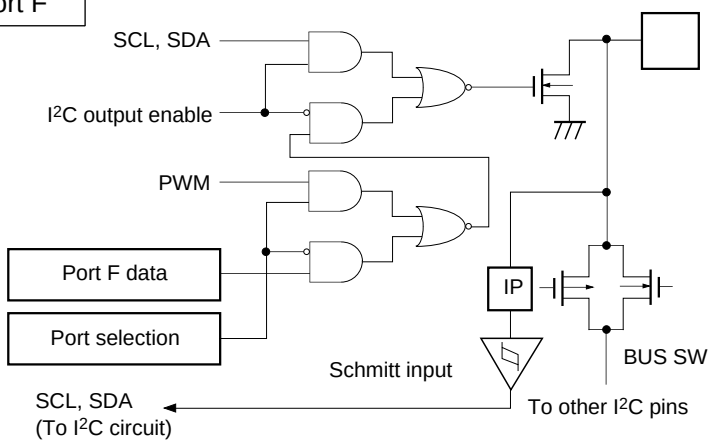
Pin Description

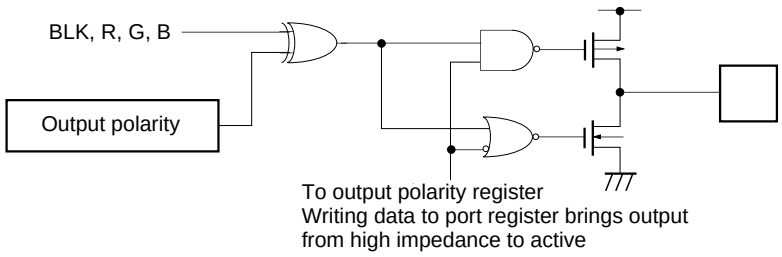
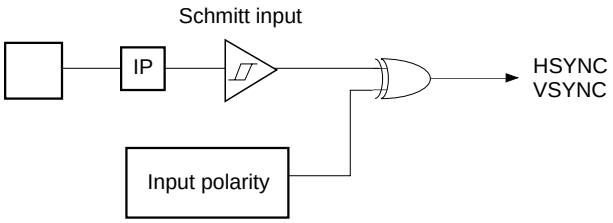
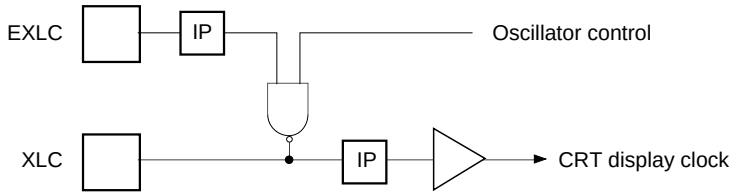
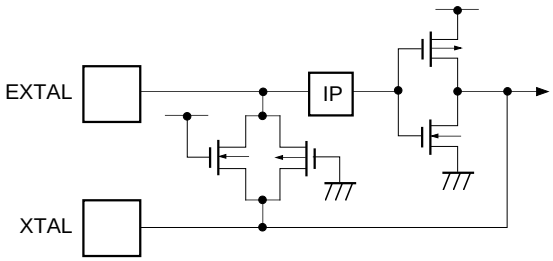
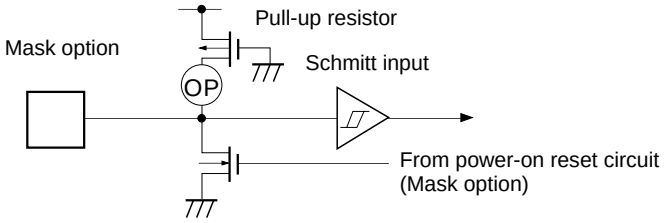
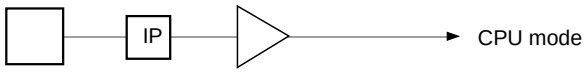
Symbol	I/O	Description		
PA0 to PA7	I/O	(Port A) Single bit selectable 8-bit port. (8 lines)		
PB0 to PB7	I/O	(Port B) Single bit selectable 8-bit port. (8 lines)		
PC0 to PC7	I/O	(Port C) Single bit selectable 8-bit port. (8 lines)		
PD0/$\overline{INT2}$	I/O/Input	(Port D) Single bit selectable 8-bit port. 12mA sink current drive possible. (8 lines)	Input pin for external interrupt request. Active on falling edge.	
PD1/$\overline{SCK}$	I/O/I/O		Serial clock pin.	
PD2/SO	I/O/Output		Serial data output pin.	
PD3/SI	I/O/Input		Serial data input pin.	
PD4/HSI	I/O/Input		HSYNC counter input pin.	
PD5/ACI	I/O/Input		Power supply frequency counter input pin.	
PD6/RMC	I/O/Input		Remote control receiver circuit input pin.	
PD7/$\overline{EC}$	I/O/Input		External event timer/counter input pin.	
PE0/$\overline{INT0}$ PE1/$\overline{INT1}$	Input/Input	(Port E) 8-bit port, lower 6 bits for input, upper 2 bits for output. (8 lines)	Input pin for external interrupt request. Active on falling edge. (2 lines)	
PE2/AN0 to PE5/AN3	Input/Input		Analog input pin for A/D converter. (4 lines)	
PE6/$\overline{PWM}$	Output/Output		14-bit PWM output pin. (CMOS output)	
PE7/TO	Output/Output		Square wave output for timer 1. (50% duty cycle)	
PF0/PWM0 to PF3/PWM3	Output/Output	(Port F) 8-bit output port with large current (12mA) N-ch open drain output. Lower 4 bits middle voltage tolerance (12V), upper 4 bits 5V suppression. (8 lines)	6-bit PWM output pin. (8 lines)	
PF4/PWM4/ SCL0 PF5/PWM5/ SCL1	Output/Output/ I/O			I^2C bus interface transfer clock input/output pin.
PF6/PWM6/ SDA0 PF7/PWM7/ SDA1	Output/Output/ I/O			I^2C bus interface transfer data input/output pin.
R, G, B, BLK	Output	CRT display 4-bit output pin.		
HSYNC	Input	CRT display horizontal synchronization signal input pin.		
VSYNC	Input	CRT display vertical synchronization signal input pin.		

Symbol	I/O	Description
EXLC	Input	CRT display clock oscillator input/output pin. Oscillator frequency is determined by external L, C circuit.
XLC	Output	
EXTAL	Input	System clock oscillator crystal connection pin. When using an external clock, input to EXTAL pin and leave XTAL pin open.
XTAL	Output	
$\overline{RST}$	I/O	"L" level active system reset. This pin also acts as an input/output pin during power up. While internal power-on reset function is taking place a "L" level is output. (Mask option)
MP	Input	Microprocessor mode input pin. Must be connected to GND.
V_{DD}		Positive power supply pin.
Vpp		Positive power supply pin for on-chip PROM writing. Please connect to V_{DD} for normal operation.
Vss		GND. Both Vss pins should be connected to common GND.

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
PA0 to PA7 PB0 to PB7 PC0 to PC7 24 pins		Hi-Z
PD0/$\overline{INT2}$ PD3/SI PD4/HSI PD5/ACI PD6/RMC PD7/$\overline{EC}$ 6 pins		Hi-Z
PD1/$\overline{SCK}$ PD2/SO 2 pins		Hi-Z

Pin	Circuit format	When reset
PE0/$\overline{INT0}$ PE1/$\overline{INT1}$ 2 pins	Port E 	Hi-Z
PE2/AN0 to PE5/AN3 4 pins	Port E 	Hi-Z
PE6/$\overline{PWM}$ PE7/TO 2 pins	Port E 	H level
PF0/PWM0 to PF3/PWM3 4 pins	Port F 	Hi-Z
PF4/PWM4/ SCL0 PF5/PWM5/ SCL1 PF6/PWM6/ SDA0 PF7/PWM7/ SDA1 4 pins	Port F 	Hi-Z

Pin	Circuit format	When reset
BLK R G B 4 pins		Hi-Z
HSYNC VSYNC 2 pins		Hi-Z
EXLC XLC 2 pins		Oscillation halted
EXTAL XTAL 2 pins		Oscillation
$\overline{\text{RST}}$ 1 pin		L level
MP 1 pin		HI-Z

Absolute Maximum Ratings (Vss = 0V)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
	Vpp	–0.3 to +13.0	V	Incorporated PROM
Input voltage	V_{IN}	–0.3 to +7.0*1	V	
Output voltage	V_{OUT}	–0.3 to +7.0*1	V	
Medium voltage tolerance output voltage	V_{OUTP}	–0.3 to +15.0	V	Pins PF0 to PF3
High level output current	I_{OH}	–5	mA	
High level total output current	$\sum I_{OH}$	–50	mA	Total of all output pins
Low level output current	I_{OL}	15	mA	Excludes large current output
	I_{OLC}	20	mA	Large current output*2
Low level total output current	$\sum I_{OL}$	130	mA	Total of all output pins
Operating temperature	Topr	–10 to +75	°C	
Strage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	1000	mW	SDIP
		600	mW	QFP

*1) V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*2) The high current operation transistors are the N-ch transistors of the PD and PF0 to PF3 ports.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operation Conditions (Vss = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	Guaranteed range during operation
		3.5	5.5	V	Guaranteed range for low speed data *1
		2.5	5.5	V	Guaranteed data hold operation range during stop
	Vpp	Vpp = V_{DD}		V	*5
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	I²C Schmitt input included *2
	V_{IHS}	0.8V_{DD}	V_{DD}	V	CMOS Schmitt input *3
	V_{IHEX}	V_{DD} – 0.4	V_{DD} + 0.3	V	EXTAL pin *4
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	I²C Schmitt input included *2
	V_{ILS}	0	0.2V_{DD}	V	CMOS Schmitt input *3
	V_{ILEX}	–0.3	0.4	V	EXTAL pin *4
Operating temperature	Topr	–10	+75	°C	

*1) Rating for 1/16 frequency mode and sleep mode.

*2) Normal input port (All pins of PA, PB, PC, PE2 to PE5), PF4 tp PF7, and MP pins.

*3) Includes PD0/$\overline{INT2}$, PD1/$\overline{SCK}$, PD2, PD3/SI, PD4/HSI, PD5/ACI, PD6/RMC, PD7/$\overline{EC}$, PE0/$\overline{INT0}$, PE1/$\overline{INT1}$, HSYNC, VSYNC, $\overline{RST}$ pins.

*4) It specifies only when the external clock is input.

*5) Vpp and V_{DD} should be set to a same voltage.

DC Characteristics (Ta = –10 to +75°C, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE6, PE7, R, G, B, BLK	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output voltage	V_{OL}	PA to PD, PE6, PE7, R, G, B, BLK, PF0 to PF3, $\overline{RST}$	V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PD, PF0 to PF3	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
		PF4 to PF7 (SCL0, SCL1, SDA0, SDA1)	V_{DD} = 4.5V, I_{OL} = 3.0mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 4.0mA			0.6	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{IHL}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{ILR}	$\overline{RST}$	V_{DD} = 5.5V, V_{IL} = 0.4V	–1.5		–400	µA
Input/output leak current	I_{IZ}	PA to PE, HSYNC, VSYNC, R, G, B, BLK, MP	V_{DD} = 5.5V V_I = 0, 5.5V			±10	µA
Open drain output leak current (N-ch Tr off case)	I_{LOH}	PF0 to PF3	V_{DD} = 5.5V, V_{OH} = 12.0V			50	µA
		PF4 to PF7	V_{DD} = 5.5V, V_{OH} = 5.5V			10	µA
I^2C bus switch connection impedance (output Tr off case)	R_{BS}	SCL0: SCL1 SDA0: SDA1	V_{DD} = 4.5V V_{SCL0} = V_{SCL1} = 2.25V V_{SDA0} = V_{SDA1} = 2.25V			120	Ω
Supply current	I_{DD}	V_{DD}*	Operating mode* (1/2 clock rate) 4MHz crystal oscillator (C_1 = C_2 = 22pF) All output pins open		10	25	mA
	I_{DDSL}		SLEEP mode		0.7	3	mA
	I_{DDST}		STOP mode			30	µA
Input capacitance	C_{IN}	Pins other than V_{DD} and Vss	1MHz clock 0V other than the measure pins		10	20	pF

* Rating applies only if OSD oscillator is haited.

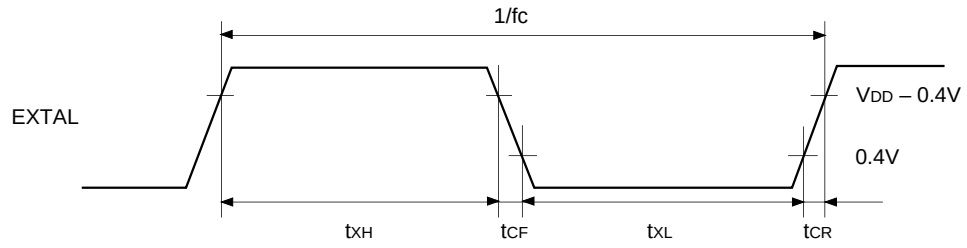
AC Characteristics

(1) Clock timing (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	3.5	4.5	MHz
System clock input pulse width	t_{XL}, t_{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	100		ns
System clock rise and fall times	t_{CR}, t_{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive		200	ns
Event counter input clock pulse width	t_{EH}, t_{EL}	$\overline{EC}$	Fig. 3	tsys + 50*		ns
Event counter input clock rise and fall times	t_{ER}, t_{EF}	$\overline{EC}$	Fig. 3		20	ms

* tsys indicates three values according to the contents of the clock control register (address: 00FE$_H$) upper 2 bits (CPU clock selection).
tsys (ns) = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Fig. 1. Clock timing



Fig, 2. Clock applied condition

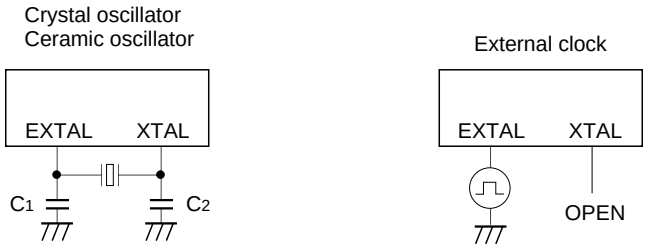
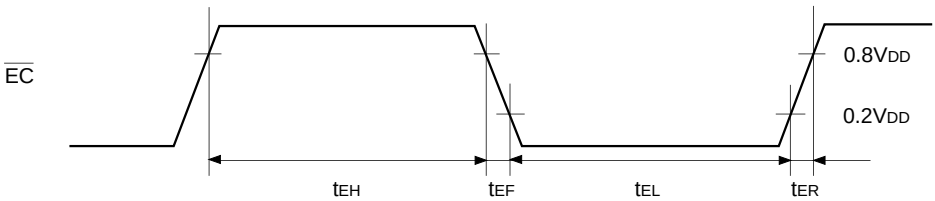


Fig. 3. Event count clock timing

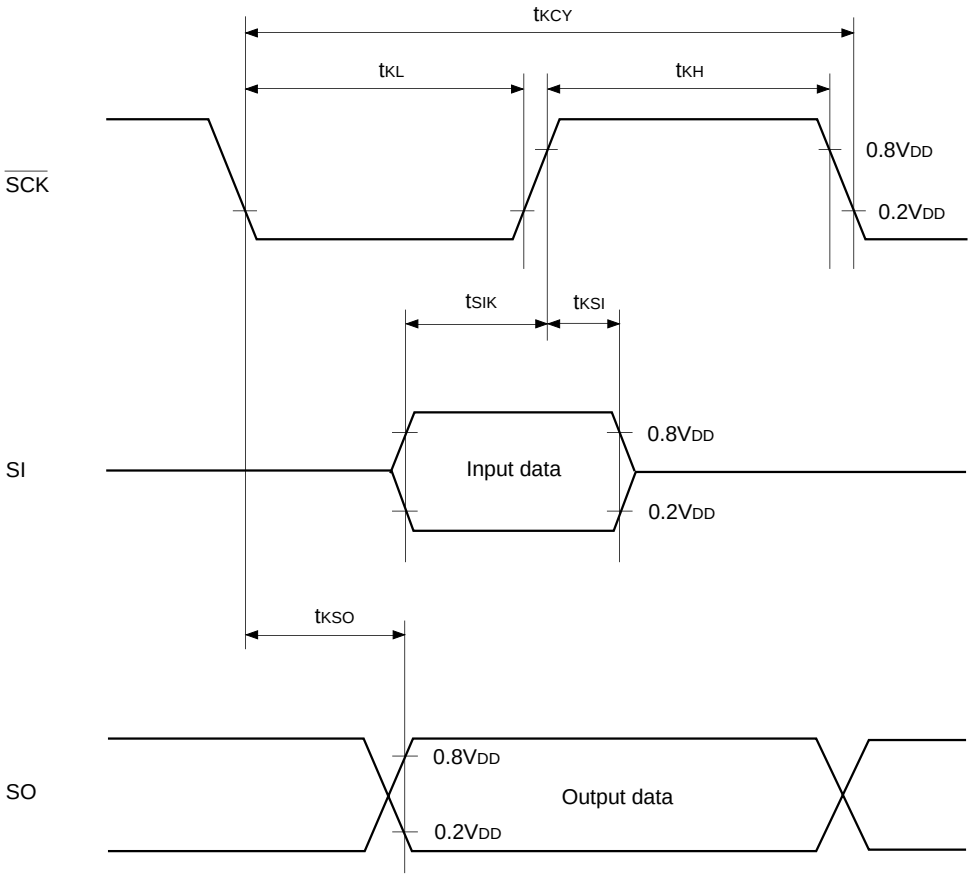


(2) Serial transfer (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK}$	Input mode	1000		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK}$	$\overline{SCK}$ input mode	400		ns
			$\overline{SCK}$ output mode	4000/fc – 50		ns
SI input set up time (against $\overline{SCK}$ ↑)	t_{SIK}	SI	$\overline{SCK}$ input mode	100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (against $\overline{SCK}$ ↑)	t_{KSI}	SI	$\overline{SCK}$ input mode	200		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK}$ ↓ → SO delay time	t_{KSO}	SO	$\overline{SCK}$ input mode		200	ns
			$\overline{SCK}$ output mode		100	ns

Note) The load of $\overline{SCK}$ output mode and SO output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer timing



(3) Interrupt, Reset input (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interrupt high and low level widths	t_{IH} t_{IL}	$\overline{INT0}$ to $\overline{INT2}$		1		µs
Reset input low level width	t_{RSL}	$\overline{RST}$		8/fc		µs

Fig. 5. Interrupt input timing

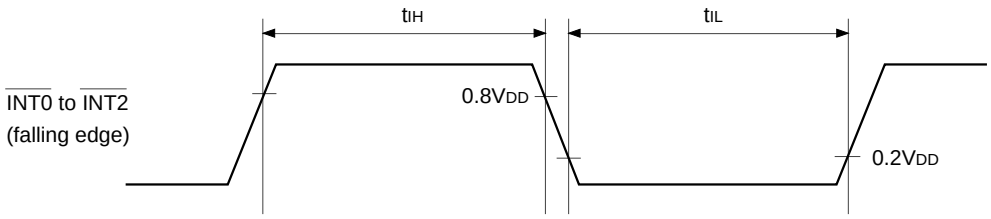
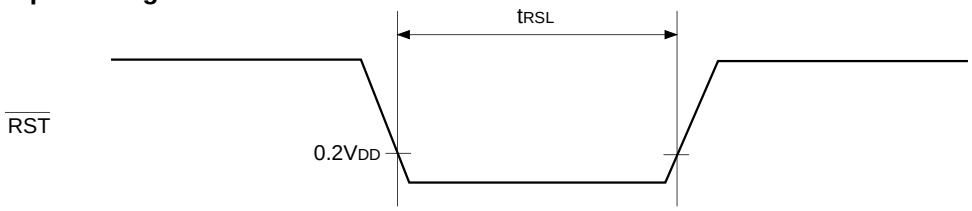


Fig. 6. $\overline{RST}$ input timing



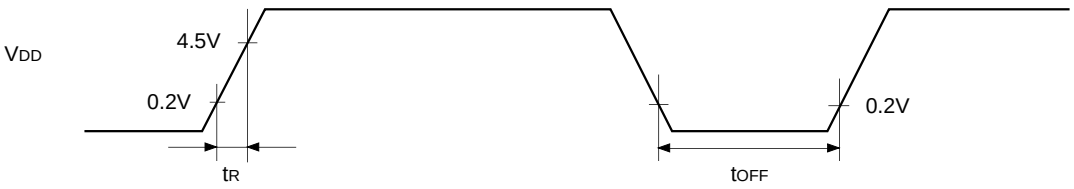
(4) Power-on reset

Power-on reset* (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rise time	t_R	V_{DD}	Power-on reset	0.05	50	ms
Power supply cut-off time	t_{OFF}		Repetitive power-on	1		ms

* Specifies only when power-on reset function is selected.

Fig. 7. Power-on reset

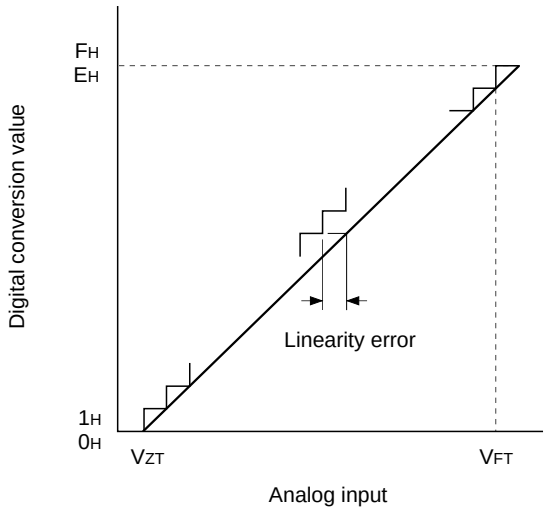


The power supply should rise smoothly.

(5) A/D converter characteristics (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						4	Bits
Linearity error			Ta = 25°C V_{DD} = 5.0V Vss = 0V			±1	LSB
Zero transition voltage	V_{ZT}*1			–10	160	320	mV
Full-scale transition voltage	V_{FT}*2			4370	4530	4690	mV
Conversion time	t_{CONV}			160/fc			µs
Sampling time	t_{SAMP}			12/fc			µs
Analog Input voltage	V_{IAN}	AN0 to AN3		0		V_{DD}	V

Fig. 8. Definitions for A/D converter terms



*1) V_{ZT}: Indicates the value that digital conversion value changes from 00_H to 01_H and vice versa.

*2) V_{FT}: Indicates the value that digital conversion value changes from E_H to F_H and vice versa.

Note) For 4-bit conversion, correction of the upper 5 bits A/D data register (ADD: address $00F5_H$) into 4 bit data is defined according to the following program example.

(A/D converter program example)

```
        MOV     A, ADD      ; ACC ← conversion data
        LSR     A           ; logical shift right (4 times)
        LSR     A           ;
        LSR     A           ;
        LSR     A           ;
        ADC     A, #00H     ; carry addition (if AD3 is 1, data is incremented)
        CMP     A, #10H     ;
        BNE     ADC_SKIP    ;
        MOV     A, #0FH     ;
ADC_SKIP:
```

(6) I²C bus timing (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
SCL clock frequency	f_{SLC}	SCL		0	100	kHz
Bus free time before starting transfer	t_{BUF}	SDA, SCL		4.7		µs
Hold time for starting transfer	$t_{HD;\,STA}$	SDA, SCL		4.0		µs
Clock low level width	t_{LOW}	SCL		4.7		µs
Clock high level width	t_{HIGH}	SCL		4.0		µs
Set-up time for repetitive transfers	$t_{SU;\,STA}$	SDA, SCL		4.7		µs
Data hold time	$t_{HD;\,DAT}$	SDA, SCL		0*		µs
Data set-up time	$t_{SU;\,DAT}$	SDA, SCL		250		ns
SDA, SCL rise time	t_R	SDA, SCL			1	µs
SDA, SCL fall time	t_F	SDA, SCL			300	ns
Set-up time for transfer completion	$t_{SU;\,STO}$	SDA, SCL		4.7		µs

* Since SCL rise time (max: 300ns) is not considered part of data hold time, allow at least 300ns.

Fig. 9. I²C Bus transfer data timing

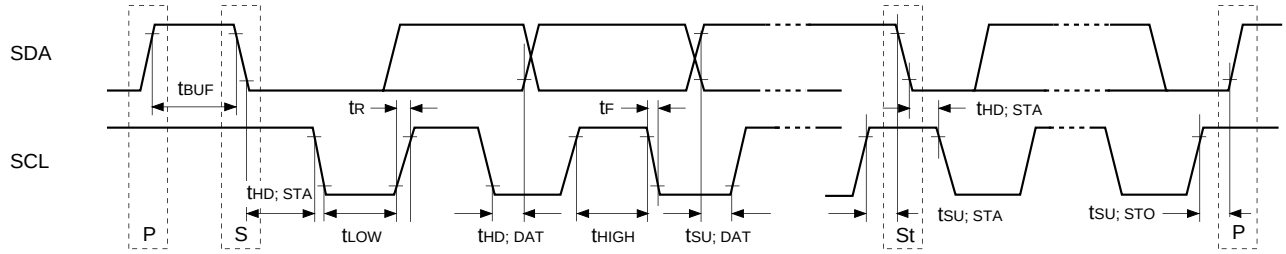
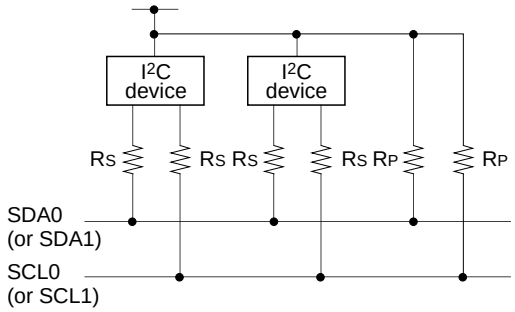


Fig. 10. I²C device recommended circuit



- A pull-up resistor must be connected to SDA0 (or SDA1), and SCL0 (or SCL1).
- The SDA0 (or SDA1) and SCL0 (or SCL1) series resistance (RS = 300Ω or less) can be used to reduce spike noise caused by CRT flashover.

(7) OSD (On Screen Display) timing (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
OSD clock frequency	f_{OSC}	EXLC XLC	Fig. 12	4	13	MHz
HSYNC pulse width	t_{HWD}	HSYNC	Fig. 11	1.2		µs
HSYNC afterwrite rise and fall times	t_{HCG}	HSYNC	Fig. 11		200	ns
VSYNC afterwrite rise and fall times	t_{VCG}	VSYNC	Fig. 11		1.0	µs

Fig. 11. OSD timing

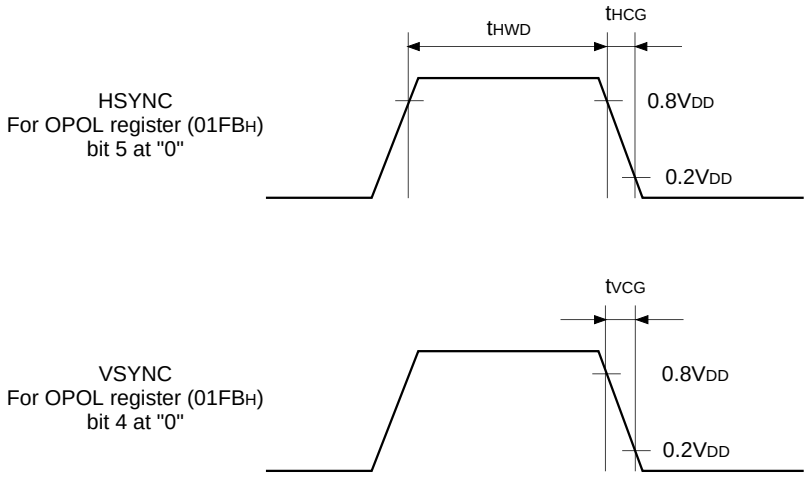
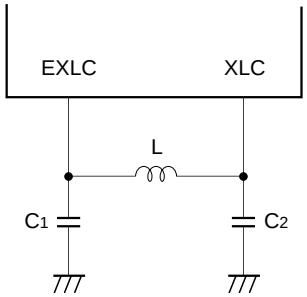


Fig. 12. LC oscillator circuit connection



Supplement

Fig. 13. Recommended Oscillation Circuit

Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit Example
MURATA MFG CO., LTD.	CSA4.00MG	4.00	30	30	0	(i)
	CSA4.19MG	4.19				
	CST4.00MGW*	4.00				(ii)
	CST4.19MGW*	4.19				
RIVER ELETEC CO., LTD.	HC-49/U03	4.00	15	15	0	(i)
		4.19				
KINSEKI LTD.	HC49/U (-S)	4.00	22	22	0	
		4.19	18	18		

* Indicates types with on-chip grounding capacitors (C_1 and C_2).

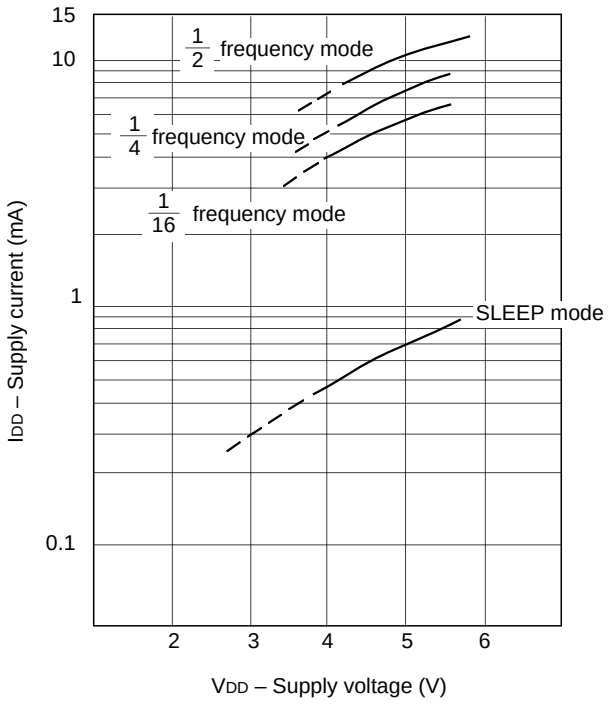
Selection Guide

Option item	Mask version	CXP851P16AS-1-□□□	CXP851P16AQ-1-□□□
Package	64-pin plastic SDIP/QFP	64-pin plastic SDIP	64-pin plastic QFP
PROM capacitance	12K/16K bytes	PROM 16K bytes	PROM 16K bytes
Reset pin pull-up resistor	Existent/non-existent	Existent	Existent
Power-on reset circuit	Existent/non-existent	Existent	Existent
Font data	User specified	User specified (PROM) *	User specified (PROM)*

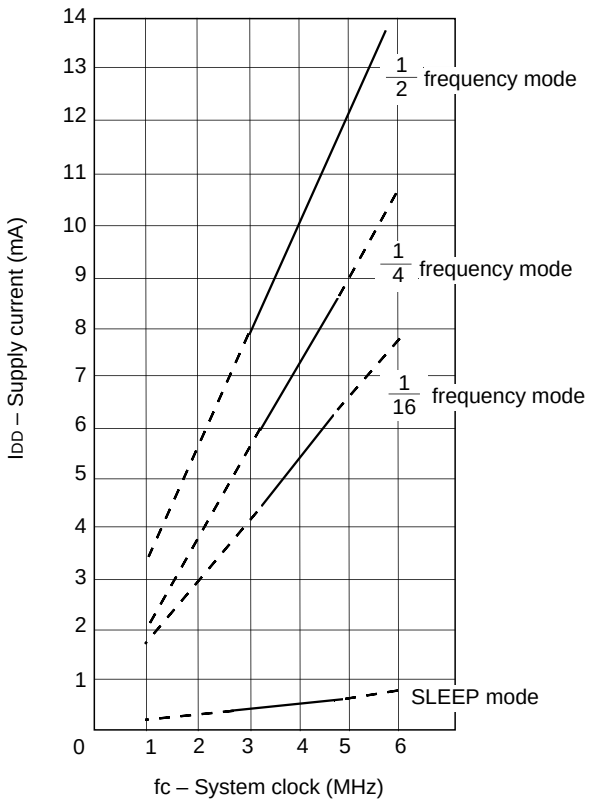
* The font data for the one-time PROM version is operated in the same way as the program writing.

Fig. 14. Characteristic curves

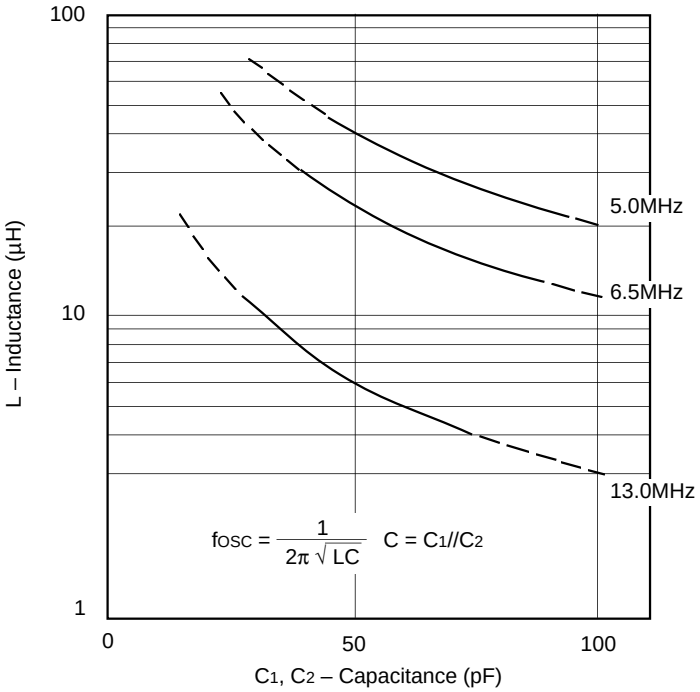
IDD vs. VDD (fc = 4MHz, Ta = 25°C, Typical)



IDD vs. fc (VDD = 5V, Ta = 25°C, Typical)

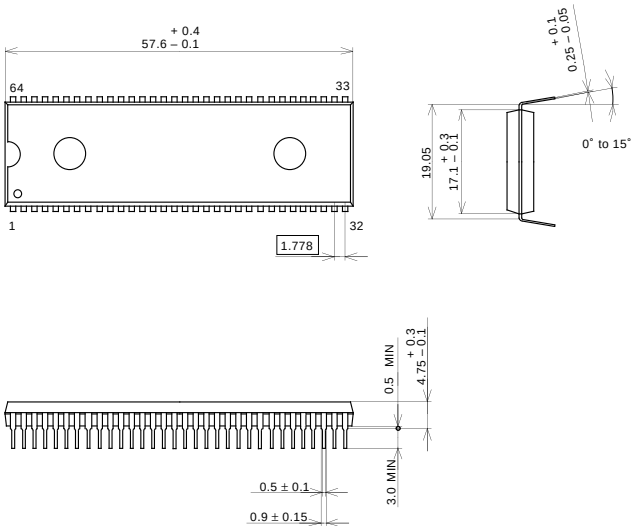


Parameter Curve for OSD Oscillator L vs. C (Analytically calculated value)



Package Outline Unit: mm

64PIN SDIP (PLASTIC)

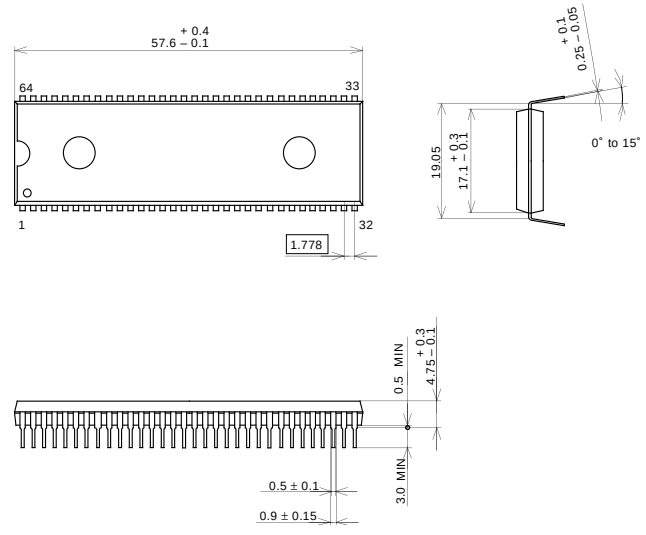


PACKAGE STRUCTURE

SONY CODE	SDIP-64P-01
EIAJ CODE	P-SDIP64-17.1x57.6-1.778
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	8.6g

64PIN SDIP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SDIP-64P-01
EIAJ CODE	P-SDIP64-17.1x57.6-1.778
JEDEC CODE	————

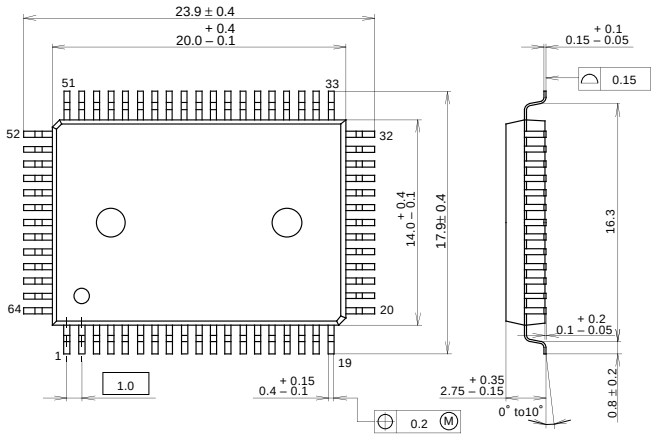
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	8.6g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18µm

Package Outline Unit: mm

64PIN QFP (PLASTIC)

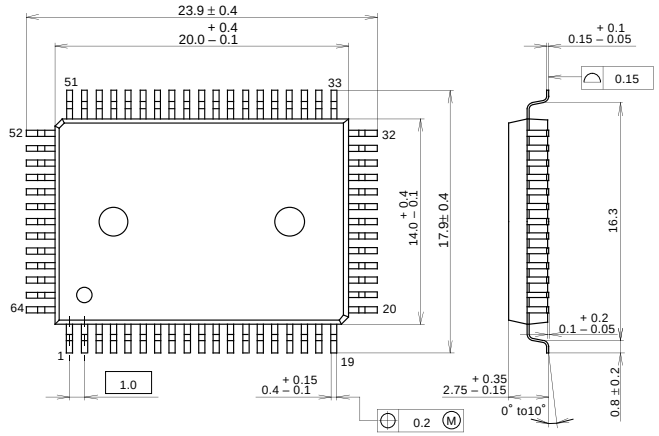


PACKAGE STRUCTURE

SONY CODE	QFP-64P-L01
EIAJ CODE	P-QFP64-14x20-1.0
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g

64PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-64P-L01
EIAJ CODE	P-QFP64-14x20-1.0
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18µm

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