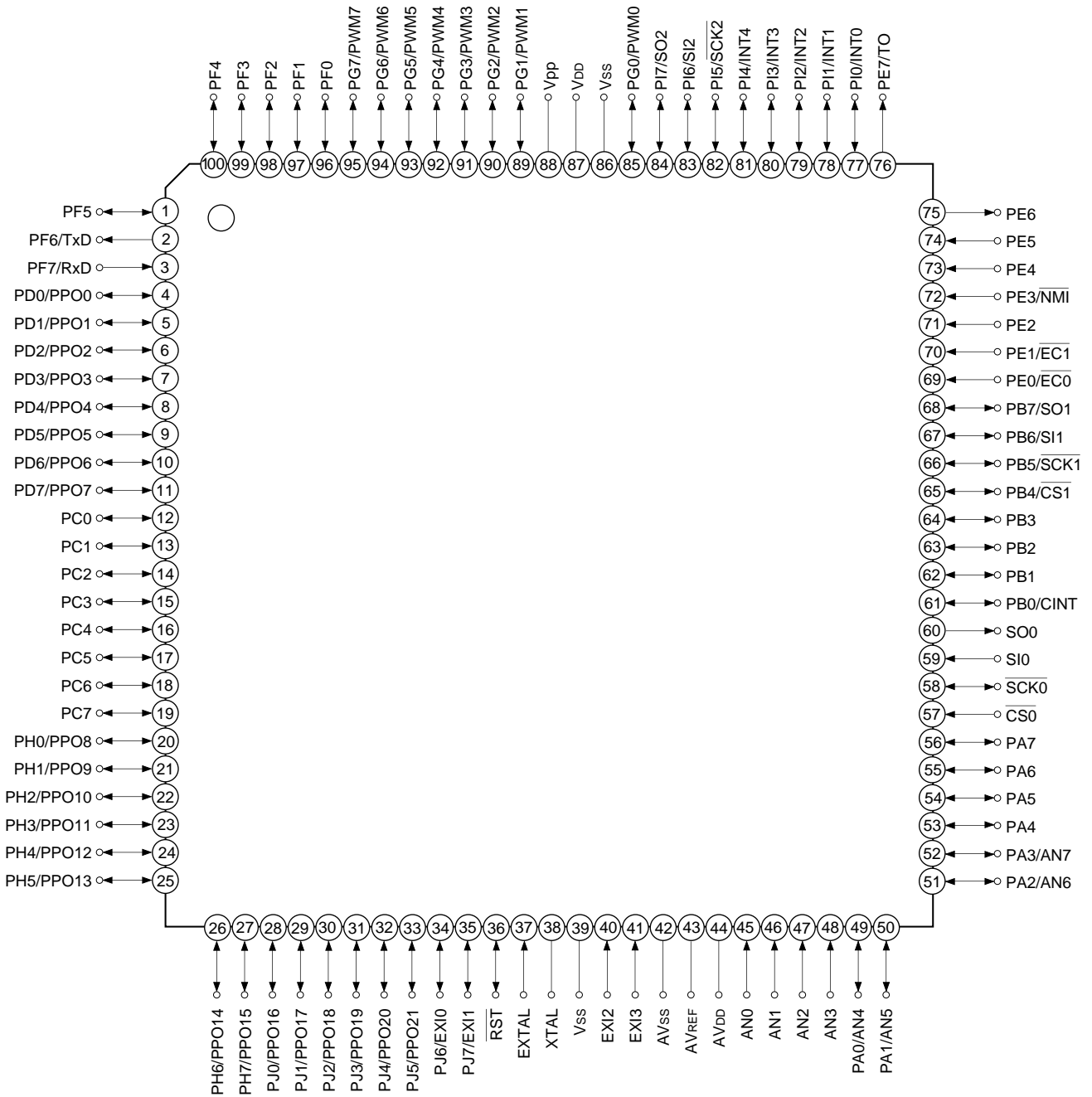


Block Diagram

Pin Assignment (Top View) 100-pin LQFP package



- Note)** 1. Vpp (Pin 88) is left open.
 2. Vss (Pins 39 and 86) are both connected to GND.

Pin Description

Symbol	I/O	Description	
AN0 to AN3	Input	Analog inputs to A/D converter. (4 pins)	
PA0/AN4 to PA3/AN7	I/O/Input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (4 pins)
PA4 to PA7	I/O		
PB0/CINT	I/O/Input		External capture input to 16-bit timer/counter.
PB1 to PB3	I/O	(Port B) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PB4/ $\overline{CS1}$	I/O/Input		Chip select input for serial interface (CH1).
PB5/ $\overline{SCK1}$	I/O/I/O		Serial clock I/O (CH1).
PB6/SI1	I/O/Input		Serial data input (CH1).
PB7/SO1	I/O/Output		Serial data output (CH1).
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Can drive 12mA sink current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PD0/PPO0 to PD7/PPO7	I/O/Real-time output	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	PPO0 to PPO7 outputs for programmable pattern generator (PPG0). Functions as high-precision real-time pulse output port. (PPG0: 11 pins; PPG1: 11 pins)
PE0/ $\overline{EC0}$	Input/Input		External event inputs for timer/counter. (2 pins)
PE1/ $\overline{EC1}$	Input/Input		
PE2	Input	(Port E) 8-bit port. Lower 6 bits are for input; upper 2 bits are for output. (8 pins)	
PE3/ \overline{NMI}	Input/Input		Non-maskable interruption request.
PE4 to PE5	Input		
PE6	Output		
PE7/TO	Output/Output		Rectangular wave output for 16-bit timer/counter.

Symbol	I/O	Description	
PF0 to PF5	I/O	(Port F) Lower 6 bits are for I/O. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits (PF0 to PF3) or 2 bits (PF4, PF5). PF6 is for output; PF7 is for input. (8 pins)	
PF6/TXD	Output/Output		UART transmission data output.
PF7/RXD	Input/Input		UART reception data input.
PG0/PWM0 to PG7/PWM7	I/O/Output	(Port G) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	PWM outputs. (8 pins)
PH0/PPO8 to PH7/PPO15	I/O/Real-time output	(Port H) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	PPO8 to PPO11 (PPG0) outputs and PPO12 to PPO15 (PPG1) outputs for programmable pattern generator (PPG0, PPG1). Functions as high-precision real-time pulse output port.
PI0/INT0 to PI4/INT4	I/O/Input	(Port I) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	External interruption request inputs. (5 pins)
PI5/SCK2	I/O/I/O		Serial clock I/O (CH2).
PI6/SI2	I/O/Input		Serial data input (CH2).
PI7/SO2	I/O/Output		Serial data output (CH2).
PJ0/PPO16 to PJ5/PPO21	I/O/Real-time output	(Port J) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	PPO16 to PPO21 outputs for programmable pattern generator (PPG1). Functions as high-precision real-time pulse output port.
PJ6/EXI0	I/O/Input		External inputs to FRC capture unit. (2 pins)
PJ7/EXI1	I/O/Input		
EXI2 to EXI3	Input	External inputs to FRC capture unit. (2 pins)	
$\overline{CS0}$	Input	Chip select input for serial interface (CH0).	
$\overline{SCK0}$	I/O	Serial clock I/O (CH0).	
SI0	Input	Serial data input (CH0).	
SO1	Output	Serial data output (CH0).	

Symbol	I/O	Description
EXTAL	Input	Connects a crystal for system clock oscillation. When a clock is supplied externally, input it to EXTAL pin and input a reversed phase clock to XTAL pin.
XTAL	Output	
$\overline{\text{RST}}$	I/O	System reset; active at Low level. This pin is I/O pin, and outputs Low level at the power on with the power-on reset function executed. (Mask option)
V _{pp}		Positive power supply for incorporated PROM writing. Leave this pin open for normal operation. (Internally connected to V _{DD} .)
AV _{DD}		Positive power supply of A/D converter.
AV _{REF}	Input	Reference voltage input of A/D converter.
AV _{SS}		GND of A/D converter.
V _{DD}		Positive power supply.
V _{SS}		GND.

I/O Circuit Format for Pins

Pin	Circuit format	When reset
PA0/AN4 to PA3/AN7 4 pins	<p> Pull-up resistor "0" when reset Port A data Port A direction "0" when reset Data bus RD (Port A) Port A function selection "0" when reset Input multiplexer A/D converter IP Input protection circuit </p> <p>* Pull-up transistors approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 300kΩ (V_{DD} = 3.0 to 3.6V)</p>	Hi-Z
PA4 to PA7 PB1 to PB3 PF0 to PF5 13 pins	<p> Pull-up resistor "0" when reset Ports A, B, F data Ports A, B, F direction "0" when reset Data bus RD (Ports A, B, F) </p> <p>* Pull-up transistors approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 300kΩ (V_{DD} = 3.0 to 3.6V)</p>	Hi-Z
PB0/CINT PB4/CS1 PB6/SI1 PI6/SI2 PJ6/EXI0 PJ7/EXI1 6 pins	<p> Pull-up resistor "0" when reset Ports B, I, J data Ports B, I, J direction "0" when reset Data bus RD (Ports B, I, J) Schmitt input CINT CS1 SI1 SI2 EXI0 EXI1 </p> <p>* Pull-up transistors approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 300kΩ (V_{DD} = 3.0 to 3.6V)</p>	Hi-Z

Pin	Circuit format	When reset
<p>PB5/SCK1 PI5/SCK2</p> <p>2 pins</p>	<p>Pull-up resistor "0" when reset</p> <p>SCK OUT</p> <p>Serial clock output enable</p> <p>Ports B, I function selection "0" when reset</p> <p>Ports B, I data</p> <p>Ports B, I direction "0" when reset</p> <p>Data bus</p> <p>RD (Ports B, I)</p> <p>SCK in</p> <p>Schmitt input</p> <p>* Pull-up transistors approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 300kΩ (V_{DD} = 3.0 to 3.6V)</p>	<p>Hi-Z</p>
<p>PB7/SO1 PI7/SO2</p> <p>2 pins</p>	<p>Pull-up resistor "0" when reset</p> <p>SO</p> <p>Serial data output enable</p> <p>Ports B, I function selection "0" when reset</p> <p>Ports B, I data</p> <p>Ports B, I direction "0" when reset</p> <p>Data bus</p> <p>RD (Ports B, I)</p> <p>* Pull-up transistors approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 300kΩ (V_{DD} = 3.0 to 3.6V)</p>	<p>Hi-Z</p>
<p>PC0 to PC7</p> <p>8 pins</p>	<p>Pull-up resistor "0" when reset</p> <p>Port C data</p> <p>Port C direction "0" when reset</p> <p>Data bus</p> <p>RD (Port C)</p> <p>*1 Large current 12mA</p> <p>*2 Pull-up transistors approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 300kΩ (V_{DD} = 3.0 to 3.6V)</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
PD0/PPO0 to PD7/PPO7 PH0/PPO8 to PH7/PPO15 PJ0/PPO16 to PJ5/PPO21 22 pins	<p>Pull-up resistor "0" when reset</p> <p>Ports D, H, J data</p> <p>Ports D, H, J direction "0" when reset</p> <p>Data bus</p> <p>RD (Ports D, H, J)</p> <p>* Pull-up transistors approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 300kΩ (V_{DD} = 3.0 to 3.6V)</p>	Hi-Z
PE0/ $\overline{EC0}$ PE1/ $\overline{EC1}$ PE2 PE3/ \overline{NMI} PE4 PE5 PF7/RxD 7 pins	<p>Schmitt input (Inverter input for PE2, PE4, PE5)</p> <p>IP</p> <p>$\overline{EC0}$, $\overline{EC1}$, \overline{NMI}, RxD</p> <p>Data bus</p> <p>RD (Ports E, F)</p>	Hi-Z
PE6 1 pin	<p>Port E data "1" when reset</p> <p>Data bus</p> <p>RD (Port E)</p>	High level
PE7/TO 1 pin	<p>Internal reset signal</p> <p>Port E data "1" when reset</p> <p>MPX</p> <p>TO</p> <p>Port E function selection (upper)</p> <p>Port E function selection (lower)</p> <p>"00" when reset</p> <p>TO output enable</p> <p>* Pull-up transistors approx. 150kΩ (V_{DD} = 4.5 to 5.5V) approx. 400kΩ (V_{DD} = 3.0 to 3.6V)</p>	High level (with the resistor of pull-up transistor ON for reset)

Pin	Circuit format	When reset
<p>PF6/TxD</p> <p>1 pin</p>	<p>Port F</p> <p>UART transmission circuit</p> <p>Control for transmission and ports</p> <p>"0" when reset</p> <p>Port F data</p> <p>"1" when reset</p> <p>Data bus</p> <p>RD (Port F)</p>	<p>High level</p>
<p>PG0/PWM0 to PG7/PWM7</p> <p>8 pins</p>	<p>Port G</p> <p>Pull-up resistor</p> <p>"0" when reset</p> <p>PWM</p> <p>Port G function selection</p> <p>"0" when reset</p> <p>Port G data</p> <p>Port G direction</p> <p>"0" when reset</p> <p>Data bus</p> <p>RD (Port G)</p> <p>* Pull-up transistors approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 300kΩ (V_{DD} = 3.0 to 3.6V)</p>	<p>Hi-Z</p>
<p>PI0/INT0 to PI4/INT4</p> <p>5 pins</p>	<p>Port I</p> <p>Pull-up resistor</p> <p>"0" when reset</p> <p>Port I data</p> <p>Port I direction</p> <p>"0" when reset</p> <p>Data bus</p> <p>RD (Port I)</p> <p>INT0</p> <p>INT1</p> <p>INT2</p> <p>INT3</p> <p>INT4</p> <p>Schmitt input</p> <p>* Pull-up transistors approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 300kΩ (V_{DD} = 3.0 to 3.6V)</p>	<p>Hi-Z</p>
<p>AN0 to AN3</p> <p>4 pins</p>	<p>Input multiplexer</p> <p>IP</p> <p>A/D converter</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
EXI2 EXI3 2 pins	<p>Schmitt input</p>	Hi-Z
$\overline{\text{CS0}}$ SIO 2 pins	<p>Schmitt input</p>	Hi-Z
SO0 1 pin		Hi-Z
$\overline{\text{SCK0}}$ 1 pin		High level
EXTAL XTAL 2 pins	<ul style="list-style-type: none"> • Diagram shows the circuit composition during oscillation. • Feedback resistor is removed during stop mode and XTAL becomes High level. 	Oscillation
$\overline{\text{RST}}$ 1 pin	<p>See the Selection Guide for the Mask option.</p>	Low level (During a reset)

Absolute Maximum Ratings

(V_{SS} = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	-0.3 to +7.0	V	
	V _{pp}	-0.3 to +13.0	V	Incorporated PROM
	AV _{DD}	AV _{SS} to +7.0* ¹	V	
	AV _{SS}	-0.3 to +0.3	V	
	AV _{REF}	AV _{SS} to +7.0	V	
Input voltage	V _{IN}	-0.3 to +7.0* ²	V	
Output voltage	V _{OUT}	-0.3 to +7.0* ²	V	
High level output current	I _{OH}	-5	mA	Output (value per pin)
High level total output current	∑I _{OH}	-50	mA	Total for all output pins
Low level output current	I _{OL}	15	mA	All pins excluding large current outputs (value per pin)
	I _{OLC}	20	mA	Large current outputs (value per pin) * ³
Low level total output current	∑I _{OL}	100	mA	Total for all output pins
Operating temperature	T _{opr}	-10 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	600	mW	QFP package
		380		LQFP package

*¹ AV_{DD} and V_{DD} must be set to the same voltage.

*² V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*³ The large current output pins are Port C (PC).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	4.5	5.5	V	fc = 16MHz or less Guaranteed operation range for 1/2 and 1/4 frequency dividing clock.
		3.0	5.5	V	
		2.7	5.5	V	Guaranteed operation range for 1/16 frequency dividing clock or sleep mode
		2.5	5.5	V	Guaranteed data hold range during stop mode
Analog voltage	AV _{DD}	3.0	5.5	V	*1
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*2, *5
		0.8V _{DD}	V _{DD}	V	*2, *6
	V _{IHS}	0.8V _{DD}	V _{DD}	V	Hysteresis input*3
	V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL pin*4, *5
		V _{DD} - 0.2	V _{DD} + 0.2	V	EXTAL pin*4, *6
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	*2, *5
		0	0.2V _{DD}	V	*2, *6
	V _{ILS}	0	0.2V _{DD}	V	Hysteresis input*3
	V _{ILEX}	-0.3	0.4	V	EXTAL pin*4, *5
		-0.3	0.2	V	EXTAL pin*4, *6
Operating temperature	T _{opr}	-10	+75	°C	

*1 AV_{DD} and V_{DD} must be set to the same voltage.

*2 Normal input port (PA, PB1 to PB3, PB7, PC, PD, PE2, PE4, PE5, PF0 to PF5, PG, PH, PI7, PJ0 to PJ5)

*3 \overline{RST} , \overline{CINT} , $\overline{CS0}$, $\overline{CS1}$, $\overline{SCK0}$, $\overline{SCK1}$, $\overline{SCK2}$, SI0, SI1, SI2, $\overline{EC0}$, $\overline{EC1}$, \overline{NMI} , RxD, INT0, INT1, INT2, INT3, INT4, EXI0, EXI1, EXI2 and EXI3

*4 Specifies only when the external clock is input.

*5 This case applies to the range of 4.5 to 5.5V supply voltage (V_{DD}).

*6 This case applies to the range of 3.0 to 5.5V supply voltage (V_{DD}).

Electrical Characteristics

DC Characteristics ($V_{DD} = 4.5$ to $5.5V$)($T_a = -10$ to $+75^\circ C$, $V_{SS} = 0V$ reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE6, PE7, PF0 to PF6, PG to PJ, SCK0, SO0	$V_{DD} = 4.5V$, $I_{OH} = -0.5mA$	4.0			V
			$V_{DD} = 4.5V$, $I_{OH} = -1.2mA$	3.5			V
Low level output voltage	V_{OL}	PA to PD, PE6, PE7, PF0 to PF6, PG to PJ, SCK0, SO0, RST*1	$V_{DD} = 4.5V$, $I_{OL} = 1.8mA$			0.4	V
			$V_{DD} = 4.5V$, $I_{OL} = 3.6mA$			0.6	V
		PC	$V_{DD} = 4.5V$, $I_{OL} = 12.0mA$			1.5	V
Input current	I_{IHE}	EXTAL	$V_{DD} = 5.5V$, $V_{IH} = 5.5V$	0.5		40	μA
	I_{ILE}		$V_{DD} = 5.5V$, $V_{IL} = 0.4V$	-0.5		-40	μA
	I_{IHT}	TEX	$V_{DD} = 5.5V$, $V_{IH} = 5.5V$	0.1		10	μA
	I_{ILT}		$V_{DD} = 5.5V$, $V_{IL} = 0.4V$	-0.1		-10	μA
	I_{ILR}	RST*2	$V_{DD} = 5.5V$, $V_{IL} = 0.4V$	-1.5		-400	μA
	I_{IL}	PA to PD*3, PF0 to PF5*3, PG to PJ*3	$V_{DD} = 4.5V$, $V_{IL} = 4.0V$	-2.78		-45	μA
I/O leakage current	I_{IZ}	PA to PD*3, PE0 to PE5, PF0 to PF5*3, PF7, PG to PJ*3, CS0, SCK0, SI0, EXI2, EXI3, AN0 to AN3 RST*2	$V_{DD} = 5.5V$ $V_i = 0, 5.5V$			± 10	μA

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Supply current*4	I _{DD}	V _{DD}	1/2 frequency dividing clock operation V _{DD} = 5.5V, 16MHz crystal oscillation (C ₁ = C ₂ = 15pF)		24	50	mA
	I _{DDS1}		Sleep mode V _{DD} = 5.5V, 16MHz crystal oscillation (C ₁ = C ₂ = 15pF)		1.5	10	mA
	I _{DDS2}		Stop mode V _{DD} = 5.5V, termination of 16MHz crystal oscillation			10	μA
Input capacity	C _{IN}	PA to PD, PE0 to PE5, PF0 to PF5, PF7, PG to PJ, CS ₀ , SCK ₀ , SI0, EXI2, EXI3, AN0 to AN3, EXTAL, RST	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1 $\overline{\text{RST}}$ pin specifies the output voltage only when the power-on reset circuit is selected with mask option.

*2 $\overline{\text{RST}}$ pin specifies the input current when the pull-up resistance is selected, and specifies the leakage current when no resistance is selected.

*3 PA to PD, PF0 to PF5 and PG to PJ pins specify the input current when the pull-up resistance is selected, and specify the leakage current when no resistance is selected.

*4 When all pins are open.

Note) See the Selection Guide for the mask option.

Electrical Characteristics

DC Characteristics ($V_{DD} = 3.0$ to $3.6V$)

($T_a = -10$ to $+75^\circ C$, $V_{SS} = 0V$ reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE6, PE7, PF0 to PF6, PG to PJ, SCK0, SO0	$V_{DD} = 3.0V$, $I_{OH} = -0.15mA$	2.7			V
			$V_{DD} = 3.0V$, $I_{OH} = -0.5mA$	2.3			V
Low level output voltage	V_{OL}	PA to PD, PE6, PE7, PF0 to PF6, PG to PJ, SCK0, SO0, RST*1	$V_{DD} = 3.0V$, $I_{OL} = 1.2mA$			0.3	V
			$V_{DD} = 3.0V$, $I_{OL} = 1.6mA$			0.5	V
		PC	$V_{DD} = 3.0V$, $I_{OL} = 5.0mA$			1	V
Input current	I_{IHE}	EXTAL	$V_{DD} = 3.6V$, $V_{IH} = 3.6V$	0.3		20	μA
	I_{ILE}		$V_{DD} = 3.6V$, $V_{IL} = 0.3V$	-0.3		-20	μA
	I_{IHT}	TEX	$V_{DD} = 3.6V$, $V_{IL} = 3.6V$	0.1		10	μA
	I_{ILT}		$V_{DD} = 3.6V$, $V_{IL} = 0.4V$	-0.1		-10	μA
	I_{ILR}	RST*2	$V_{DD} = 3.6V$, $V_{IL} = 0.3V$	-0.9		-200	μA
	I_{IL}	PA to PD*3, PF0 to PF5*3, PG to PJ*3		$V_{DD} = 3.0V$, $V_{IL} = 2.7V$	-1.0		-20
I/O leakage current	I_{IZ}	PA to PD*3, PE0 to PE5, PF0 to PF5*3, PF7, PG to PJ*3, CS0, SCK0, SI0, EXI2, EXI3, AN0 to AN3, RST*2	$V_{DD} = 3.6V$ $V_I = 0, 3.6V$			± 10	μA

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Supply current*4	I _{DD}	V _{DD}	1/2 frequency dividing clock operation V _{DD} = 3.6V, 12MHz crystal oscillation (C ₁ = C ₂ = 15pF)		10	25	mA
	I _{DDS1}		Sleep mode V _{DD} = 3.6V, 12MHz crystal oscillation (C ₁ = C ₂ = 15pF)		0.5	2.0	mA
	I _{DDS2}		Stop mode V _{DD} = 3.6V, termination of 12MHz crystal oscillation			10	μA
Input capacity	C _{IN}	PA to PD, PE0 to PE5, PF0 to PF5, PF7, PG to PJ, CS ₀ , SCK ₀ , SI0, EXI2, EXI3, AN0 to AN3, EXTAL, RST	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1 $\overline{\text{RST}}$ pin specifies the output voltage only when the power-on reset circuit is selected with mask option.

*2 $\overline{\text{RST}}$ pin specifies the input current when the pull-up resistance is selected, and specifies the leakage current when no resistance is selected.

*3 PA to PD, PF0 to PF5 and PG to PJ pins specify the input current when the pull-up resistance is selected, and specify the leakage current when no resistance is selected.

*4 When all pins are open.

Note) See the Selection Guide for the mask option.

AC Characteristics

(1) Clock timing

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 3.0$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f_c	XTAL EXTAL	Fig. 1, Fig. 2	$V_{DD} = 4.5$ to 5.5V	1	16	MHz
					1	12	
System clock input pulse width	t_{XL} t_{XH}	XTAL EXTAL	Fig. 1, Fig. 2 External clock drive	$V_{DD} = 4.5$ to 5.5V	28		ns
					37.5		
System clock input rise time, fall time	t_{CR} t_{CF}	XTAL EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	t_{EH} t_{EL}	$\overline{\text{EC0}}$ $\overline{\text{EC1}}$	Fig. 3		$t_{\text{sys}} + 50^{*1}$		ns
Event count input clock rise time, fall time	t_{ER} t_{EF}	$\overline{\text{EC0}}$ $\overline{\text{EC1}}$	Fig. 3			20	ms

*1 t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (CLC: 00FEH).

$t_{\text{sys}} [\text{ns}] = 2000/f_c$ (upper two bits = "00"), $4000/f_c$ (upper two bits = "01"), $16000/f_c$ (Upper two bits = "11")

Fig. 1. Clock timing

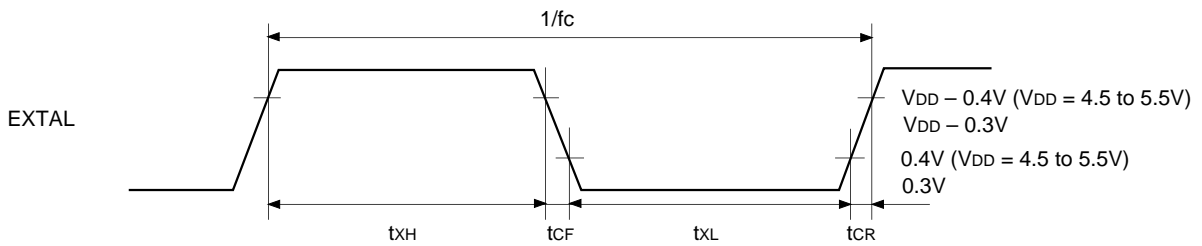


Fig. 2. Clock applied conditions

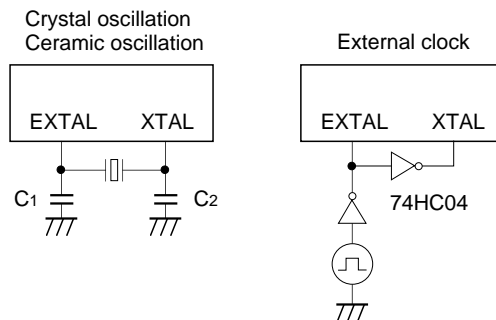
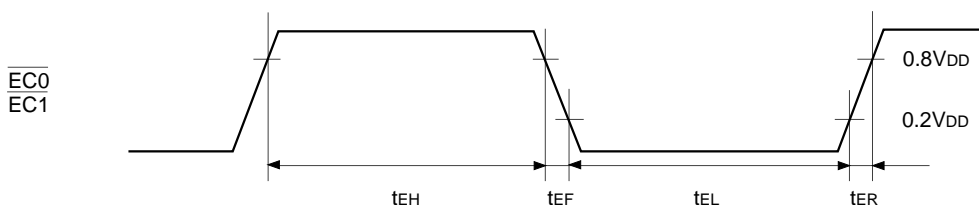


Fig. 3. Event count clock timing



(2) Serial transfer (CH0, CH1)

(Ta = -10 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{CS}\downarrow \rightarrow \overline{SCK}$ delay time	t _{DCSK}	$\overline{SCK0}$ $\overline{SCK1}$	Chip select transfer mode (\overline{SCK} = output mode)		1.5t _{sys} + 200	ns
$\overline{CS}\uparrow \rightarrow \overline{SCK}$ floating delay time	t _{DCSKF}	$\overline{SCK0}$ $\overline{SCK1}$	Chip select transfer mode (\overline{SCK} = output mode)		1.5t _{sys} + 200	ns
$\overline{CS}\downarrow \rightarrow SO$ delay time	t _{DCSO}	SO0 SO1	Chip select transfer mode		1.5t _{sys} + 200	ns
$\overline{CS}\uparrow \rightarrow SO$ floating delay time	t _{DCSOF}	SO0 SO1	Chip select transfer mode		1.5t _{sys} + 200	ns
\overline{CS} High level width	t _{WHCS}	$\overline{CS0}$ $\overline{CS1}$	Chip select transfer mode	t _{sys} + 200		ns
\overline{SCK} cycle time	t _{KCY}	$\overline{SCK0}$ $\overline{SCK1}$	Input mode	2t _{sys} + 200		ns
			Output mode	8000/fc		ns
\overline{SCK} High and Low level widths	t _{KH} t _{KL}	$\overline{SCK0}$ $\overline{SCK1}$	Input mode	t _{sys} + 100		ns
			Output mode	4000/fc - 50		ns
SI input setup time (for $\overline{SCK}\uparrow$)	t _{SIK}	SI0 SI1	\overline{SCK} input mode	-t _{sys} + 100		ns
			\overline{SCK} output mode	200		ns
SI input hold time (for $\overline{SCK}\uparrow$)	t _{KSI}	SI0 SI1	\overline{SCK} input mode	2t _{sys} + 200		ns
			\overline{SCK} output mode	100		ns
$\overline{SCK}\downarrow \rightarrow SO$ delay time	t _{KSO}	SO0 SO1	\overline{SCK} input mode		2t _{sys} + 200	ns
			\overline{SCK} output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC: 00FE_H) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (upper 2 bits = "00"), 4000/fc (upper 2 bits = "01"), 16000/fc (upper 2 bits = "11")

Note 2) \overline{CS} , \overline{SCK} , SI and SO represent $\overline{CS0}$, $\overline{SCK0}$, SI0 and SO0 for CH0; they represent $\overline{CS1}$, $\overline{SCK1}$, SI1 and SO1 for CH1, respectively.

Note 3) The load of \overline{SCK} output mode and SO output delay time is 50pF + 1TTL.

Serial transfer (CH0, CH1)

(Ta = -10 to +75°C, VDD = 3.0 to 3.6V, VSS = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{CS}\downarrow \rightarrow \overline{SCK}$ delay time	t _{D_{CSK}}	$\overline{SCK0}$ $\overline{SCK1}$	Chip select transfer mode (\overline{SCK} = output mode)		1.5t _{sys} + 250	ns
$\overline{CS}\uparrow \rightarrow \overline{SCK}$ floating delay time	t _{D_{CSKF}}	$\overline{SCK0}$ $\overline{SCK1}$	Chip select transfer mode (\overline{SCK} = output mode)		1.5t _{sys} + 200	ns
$\overline{CS}\downarrow \rightarrow SO$ delay time	t _{D_{CSO}}	SO0 SO1	Chip select transfer mode		1.5t _{sys} + 250	ns
$\overline{CS}\uparrow \rightarrow SO$ floating delay time	t _{D_{CSOF}}	SO0 SO1	Chip select transfer mode		1.5t _{sys} + 200	ns
\overline{CS} High level width	t _{WH_{CS}}	$\overline{CS0}$ $\overline{CS1}$	Chip select transfer mode	t _{sys} + 200		ns
\overline{SCK} cycle time	t _{K_{CY}}	$\overline{SCK0}$ $\overline{SCK1}$	Input mode	2t _{sys} + 200		ns
			Output mode	8000/fc		ns
\overline{SCK} High and Low level widths	t _{K_H} t _{K_L}	$\overline{SCK0}$ $\overline{SCK1}$	Input mode	t _{sys} + 100		ns
			Output mode	4000/fc - 100		ns
SI input setup time (for $\overline{SCK}\uparrow$)	t _{SIK}	SI0 SI1	\overline{SCK} input mode	-t _{sys} + 100		ns
			\overline{SCK} output mode	200		ns
SI input hold time (for $\overline{SCK}\uparrow$)	t _{K_{SI}}	SI0 SI1	\overline{SCK} input mode	2t _{sys} + 200		ns
			\overline{SCK} output mode	100		ns
$\overline{SCK}\downarrow \rightarrow SO$ delay time	t _{K_{SO}}	SO0 SO1	\overline{SCK} input mode		2t _{sys} + 250	ns
			\overline{SCK} output mode		125	ns

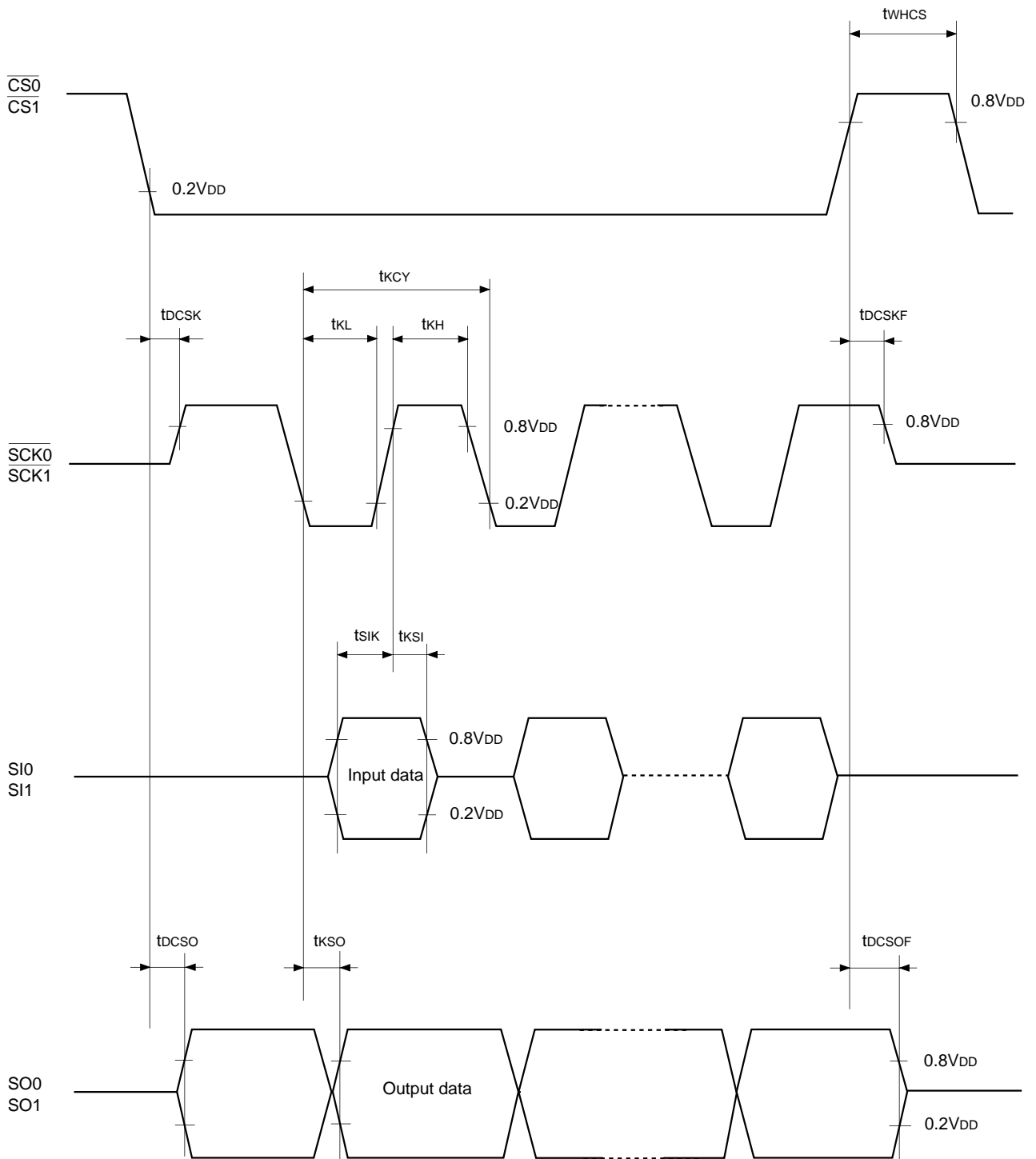
Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC: 00FE_H) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (upper 2 bits = "00"), 4000/fc (upper 2 bits = "01"), 16000/fc (upper 2 bits = "11")

Note 2) \overline{CS} , \overline{SCK} , SI and SO represent $\overline{CS0}$, $\overline{SCK0}$, SI0 and SO0 for CH0; they represent $\overline{CS1}$, $\overline{SCK1}$, SI1 and SO1 for CH1, respectively.

Note 3) The load of \overline{SCK} output mode and SO output delay time is 50pF.

Fig. 4. Serial transfer CH0, CH1 timing



Serial transfer (CH2)

(Ta = -10 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{\text{SCK}}$ cycle time	t_{KCY}	$\overline{\text{SCK2}}$	Input mode	1000		ns
			Output mode	8000/fc		ns
SCK High and Low level widths	t_{KH} t_{KL}	$\overline{\text{SCK2}}$	Input mode	400		ns
			Output mode	4000/fc - 50		ns
SI input setup time (for $\overline{\text{SCK}}\uparrow$)	t_{SIK}	SI2	$\overline{\text{SCK}}$ input mode	100		ns
			$\overline{\text{SCK}}$ output mode	200		ns
SI input hold time (for $\overline{\text{SCK}}\uparrow$)	t_{KSI}	SI2	$\overline{\text{SCK}}$ input mode	200		ns
			$\overline{\text{SCK}}$ output mode	100		ns
SCK \downarrow → SO delay time	t_{KSO}	SO2	$\overline{\text{SCK}}$ input mode		200	ns
			$\overline{\text{SCK}}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC: 00FEH) upper 2 bits (CPU clock selection).

$$t_{\text{sys}} [\text{ns}] = 2000/\text{fc} \text{ (Upper 2 bits = "00")}, 4000/\text{fc} \text{ (Upper 2 bits = "01")}, 16000/\text{fc} \text{ (Upper 2 bits = "11")}$$

Note 2) $\overline{\text{SCK}}$, SI and SO represent $\overline{\text{SCK2}}$, SI2 and SO2 for CH2, respectively.

Note 3) The load of $\overline{\text{SCK2}}$ output mode and SO2 output delay time is 50pF+1TTL.

Serial transfer (CH2)

(Ta = -10 to +75°C, VDD = 3.0 to 3.6V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{\text{SCK}}$ cycle time	t_{KCY}	$\overline{\text{SCK2}}$	Input mode	1000		ns
			Output mode	8000/fc		ns
$\overline{\text{SCK}}$ High and Low level widths	t_{KH} t_{KL}	$\overline{\text{SCK2}}$	Input mode	400		ns
			Output mode	4000/fc - 100		ns
SI input setup time (for $\overline{\text{SCK}}\uparrow$)	t_{SIK}	SI2	$\overline{\text{SCK}}$ input mode	100		ns
			$\overline{\text{SCK}}$ output mode	200		ns
SI input hold time (for $\overline{\text{SCK}}\uparrow$)	t_{KSI}	SI2	$\overline{\text{SCK}}$ input mode	200		ns
			$\overline{\text{SCK}}$ output mode	100		ns
SCK \downarrow → SO delay time	t_{KSO}	SO2	$\overline{\text{SCK}}$ input mode		250	ns
			$\overline{\text{SCK}}$ output mode		125	ns

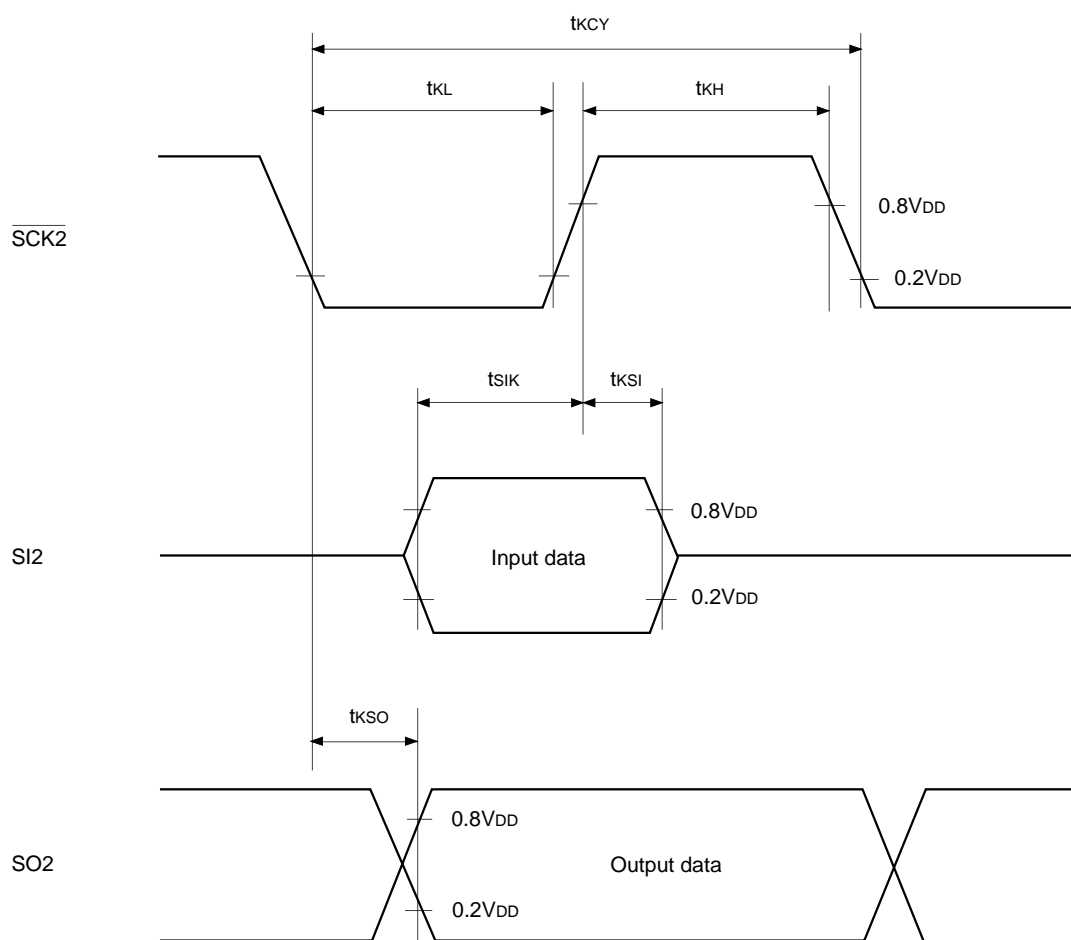
Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC: 00FEH) upper 2 bits (CPU clock selection).

$$t_{\text{sys}} [\text{ns}] = 2000/\text{fc} \text{ (Upper 2 bits = "00")}, 4000/\text{fc} \text{ (Upper 2 bits = "01")}, 16000/\text{fc} \text{ (Upper 2 bits = "11")}$$

Note 2) $\overline{\text{SCK}}$, SI and SO represent $\overline{\text{SCK2}}$, SI2 and SO2 for CH2, respectively.

Note 3) The load of $\overline{\text{SCK2}}$ output mode and SO2 output delay time is 50pF.

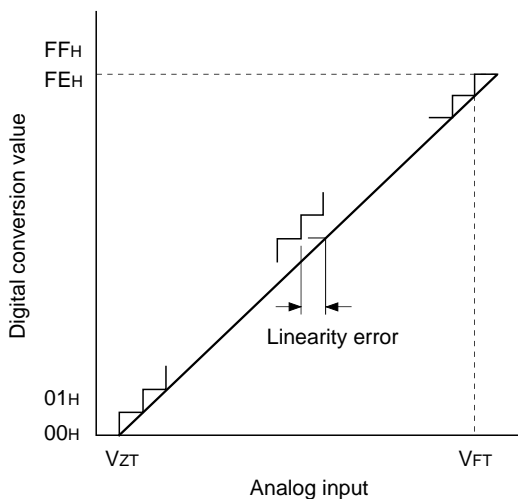
Fig. 5. Serial transfer CH2 timing



(3) A/D converter characteristics (Ta = -10 to +75°C, VDD = AVDD = 3.0 to 5.5V, VSS = AVSS = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit	
Resolution						8	Bits	
Linearity error			Ta = 25°C VDD = AVDD = AVREF = 5.0V VSS = AVSS = 0V			±3	LSB	
Zero transition voltage	VZT*1			-50	10	70	mV	
Full-scale transition voltage	VFT*2			4910	4970	5030	mV	
Linearity error			Ta = 25°C VDD = AVDD = AVREF = 3.3V VSS = AVSS = 0V			±5	LSB	
Zero transition voltage	VZT*1			-10	6.5	70	mV	
Full-scale transition voltage	VFT*2			3215	3280	3345	mV	
Conversion time	tCONV			26/fADC*3			µs	
Sampling time	tSAMP			6/fADC*3			µs	
Reference input voltage	VREF	AVREF	VDD = AVDD = 4.5 to 5.5V	AVDD - 0.5		AVDD	V	
			VDD = AVDD = 3.0 to 3.6V	AVDD - 0.3		AVDD	V	
Analog input voltage	VIAN	AN0 to AN7		0		AVREF	V	
AVREF current	IREF	AVREF	Operation mode	VDD = 5.5V		0.6	1.0	mA
				VDD = 3.6V		0.4	0.7	mA
	IREFS		Sleep mode Stop mode				10	µA

Fig.6. Definition of A/D converter terms



*1 VZT: Value at which the digital conversion value changes from 00H to 01H and vice versa.

*2 VFT: Value at which the digital conversion value changes from FEH to FFH and vice versa.

*3 fADC indicates the below values due to the contents of bit 6 (CKS) of the A/D control register (ADC: 00F9H).

PS1 selected fADC = fc

PS2 selected fADC = fc/2

(4) Interruption, reset input ($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 3.0$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
External interruption High, Low level width	t_{IH} t_{IL}	INT0 INT1 INT2 INT3 INT4 $\overline{\text{NMI}}$		1		μs
Reset input Low level width	t_{RSL}	$\overline{\text{RST}}$		$32/f_c$		μs

Fig. 7. Interruption input timing

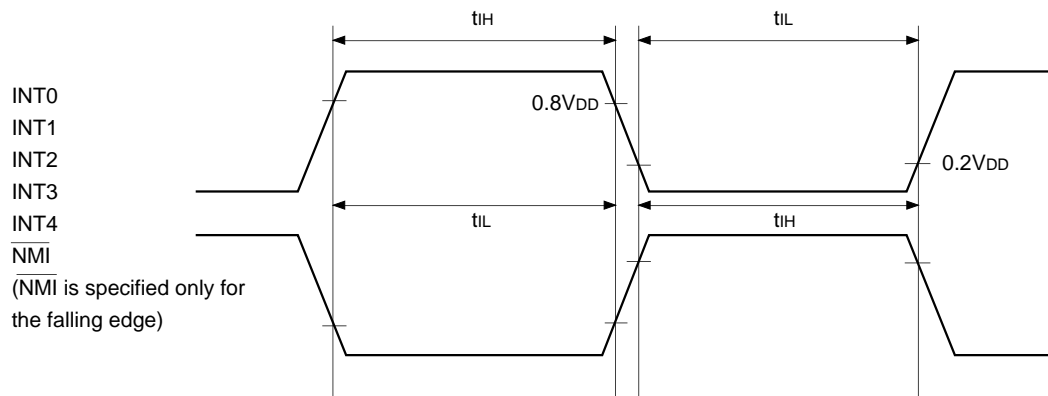
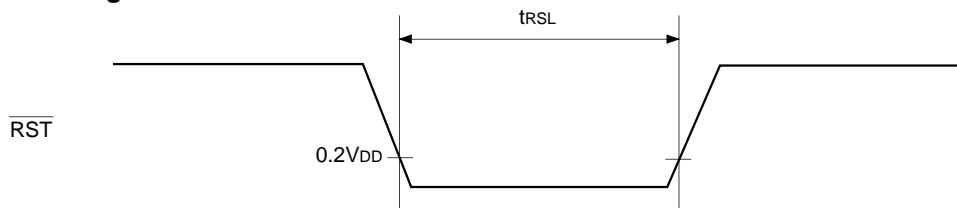


Fig. 8. $\overline{\text{RST}}$ input timing



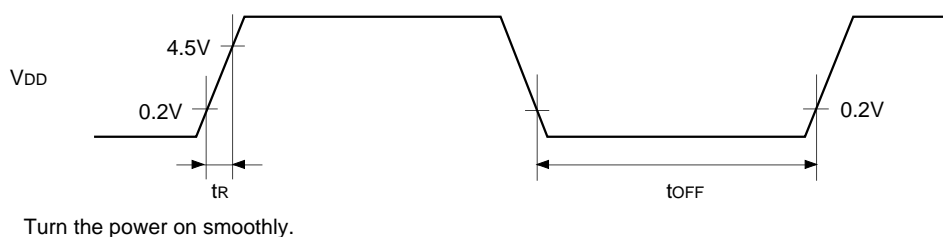
(5) Power-on reset*1

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
Power supply rise time	t_R	V_{DD}	Power-on reset	0.05	50	ms
Power supply cut-off time	t_{OFF}		Repetitive power-on reset	1		ms

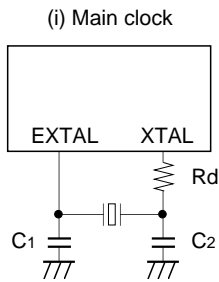
*1 Power-on reset function is selected by the mask option. See the Selection Guide for the mask option.
Power-on reset function can be selected only for the supply voltage range of 4.5 to 5.5V.

Fig. 9. Power-on reset



Appendix

Fig. 10. Recommended oscillation circuit for SPC700 Series



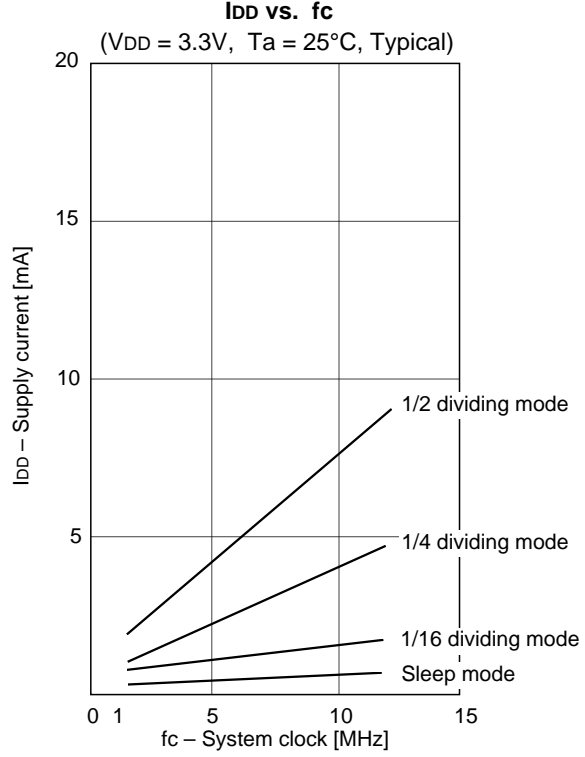
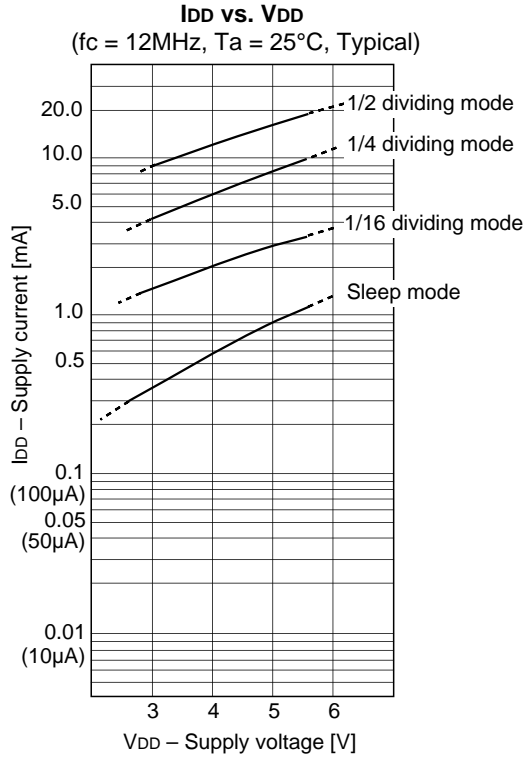
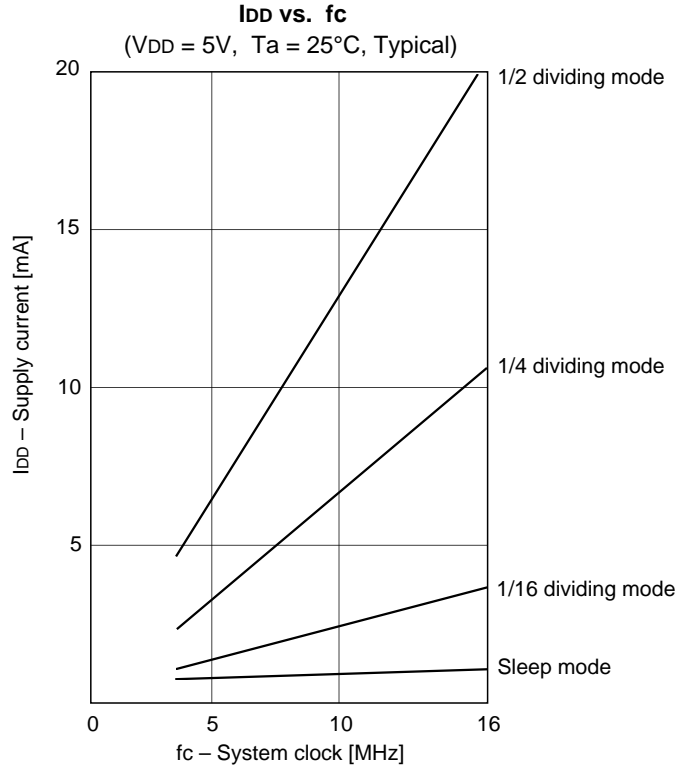
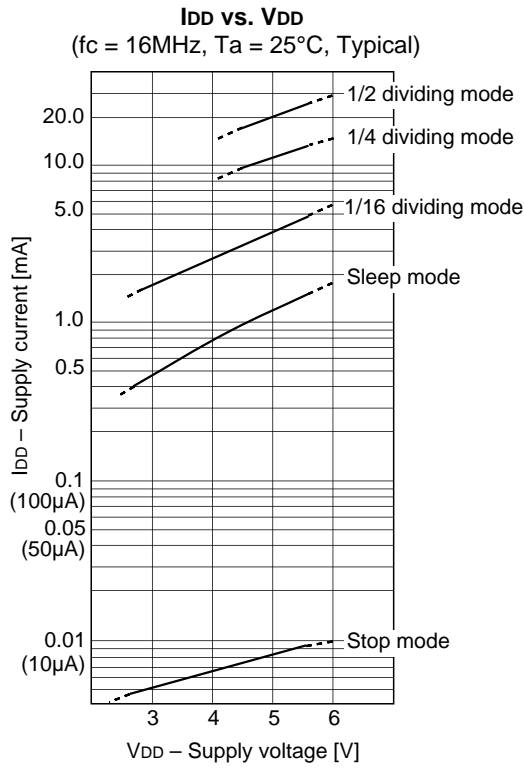
Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00	5	5		
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	22 (15)	22 (15)	0	(i)
		10.00				
		12.00	15	15		
		16.00	12	12		

Selection Guide

Option item	Mask	CXP847P60Q-1-□□□	CXP847P60R-1-□□□
Reset pin pull-up resistor	Non-existent/Existent	Existent	Existent
Power-on reset function	Non-existent/Existent*1	Existent	Existent

*1 Power-on reset function “Existent” is not selected under the using condition in the range of $V_{DD}=3.0$ to 4.5V.

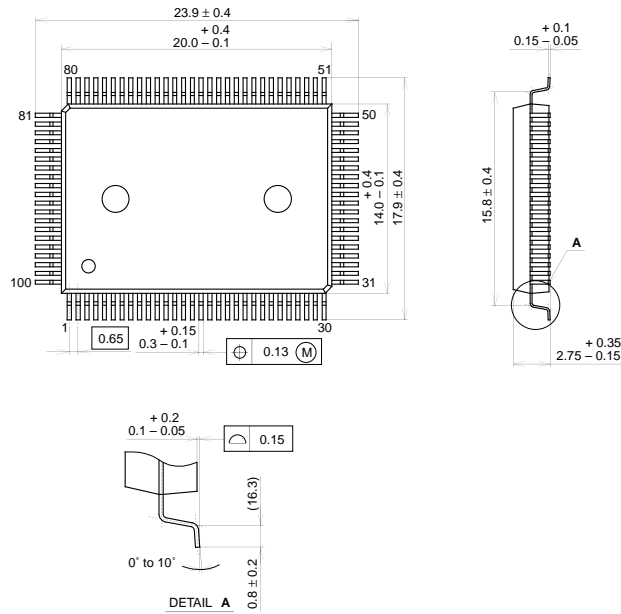
Characteristics Curve (Reference)



Package Outline

Unit: mm

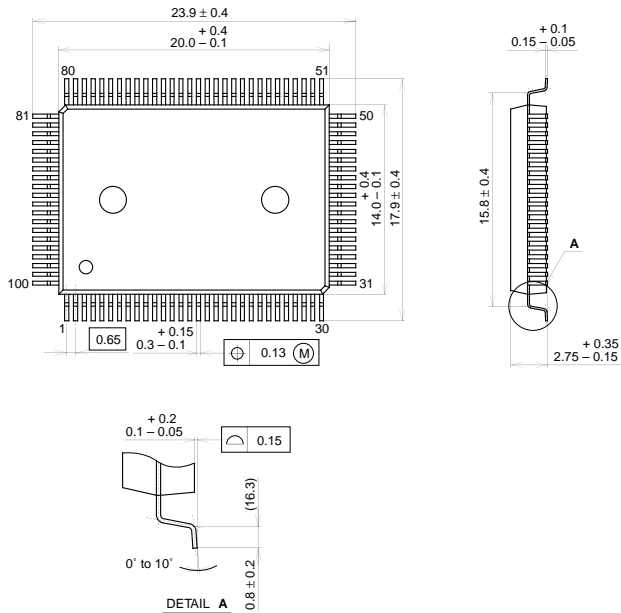
100PIN QFP (PLASTIC)



SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	_____

PACKAGE STRUCTURE	
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

100PIN QFP (PLASTIC)



SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	_____

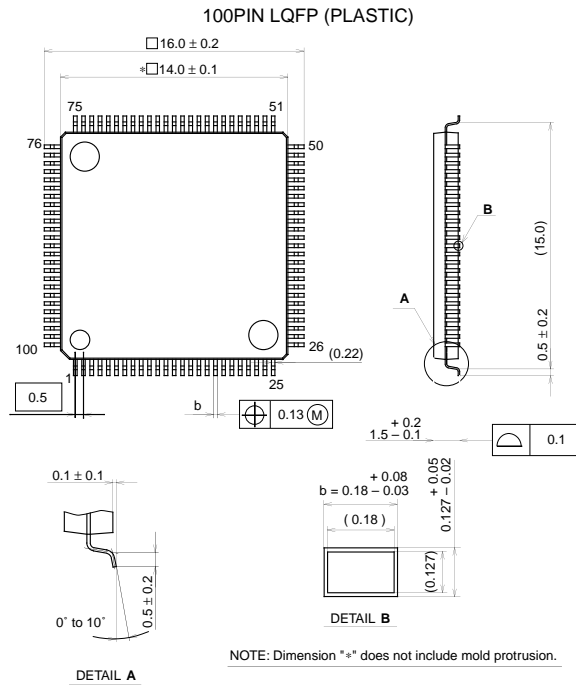
PACKAGE STRUCTURE	
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	42 ALLOY
SOLDER COMPOSITION	Sn-Bi:1-4wt%
PLATING THICKNESS	5-18 μ m

Package Outline

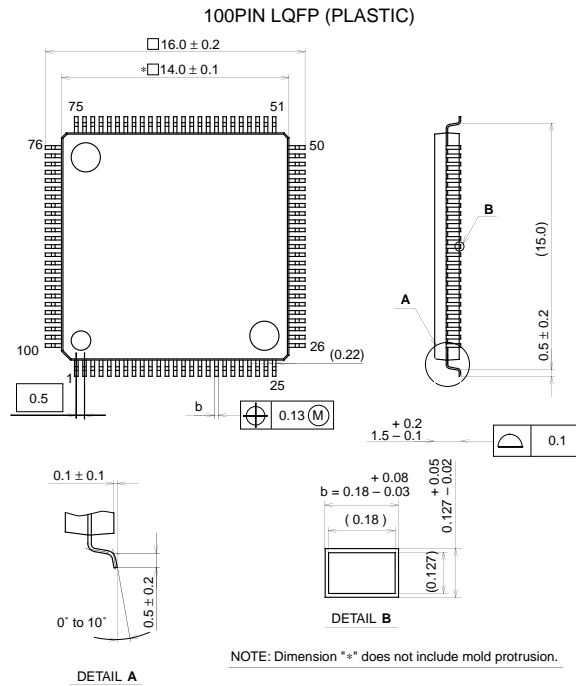
Unit: mm



SONY CODE	LQFP-100P-L01
EIAJ CODE	P-LQFP100-14x14-0.5
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.7g



SONY CODE	LQFP-100P-L01
EIAJ CODE	P-LQFP100-14x14-0.5
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.7g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	42 ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18μm



LittleDiode supplies new, hard to find or obsolete electronic components and semiconductors all over the world.

With over two million different components listed you are sure to find the part you need.

Feel free to visit us today at our online store:

LittleDiode.com

Looking forward to providing you with the best possible service.