SONY

CXP84716/84720/84724

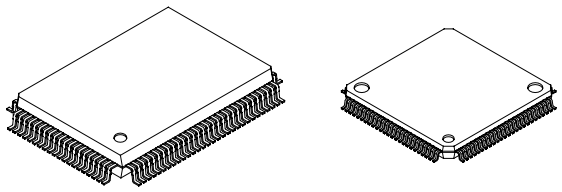
CMOS 8-bit Single Chip Microcomputer

Description

The CXP84716/84720/84724 is a CMOS 8-bit microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time base timer, capture timer/counter, FRC capture unit, high-precision timing pattern generation circuit, PWM output, and the like besides the basic configurations of 8-bit CPU, ROM, RAM, and I/O port.

The CXP84716/84720/84724 also provides the sleep/stop functions that enable to execute the power-on reset function and lower the power consumption.

100 pin QFP (Plastic) 100 pin LQFP (Plastic)



Structure

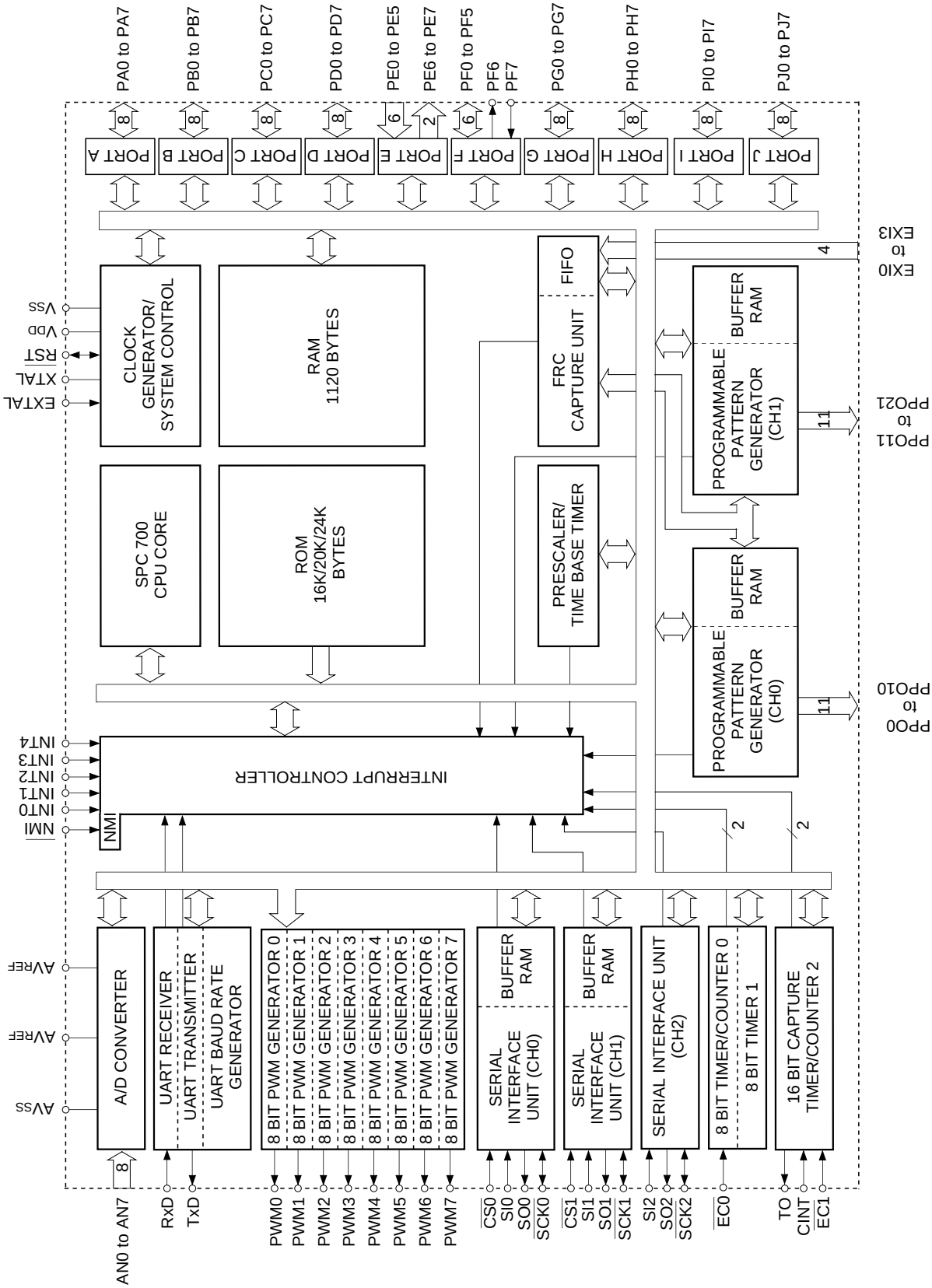
Silicon gate CMOS IC

Features

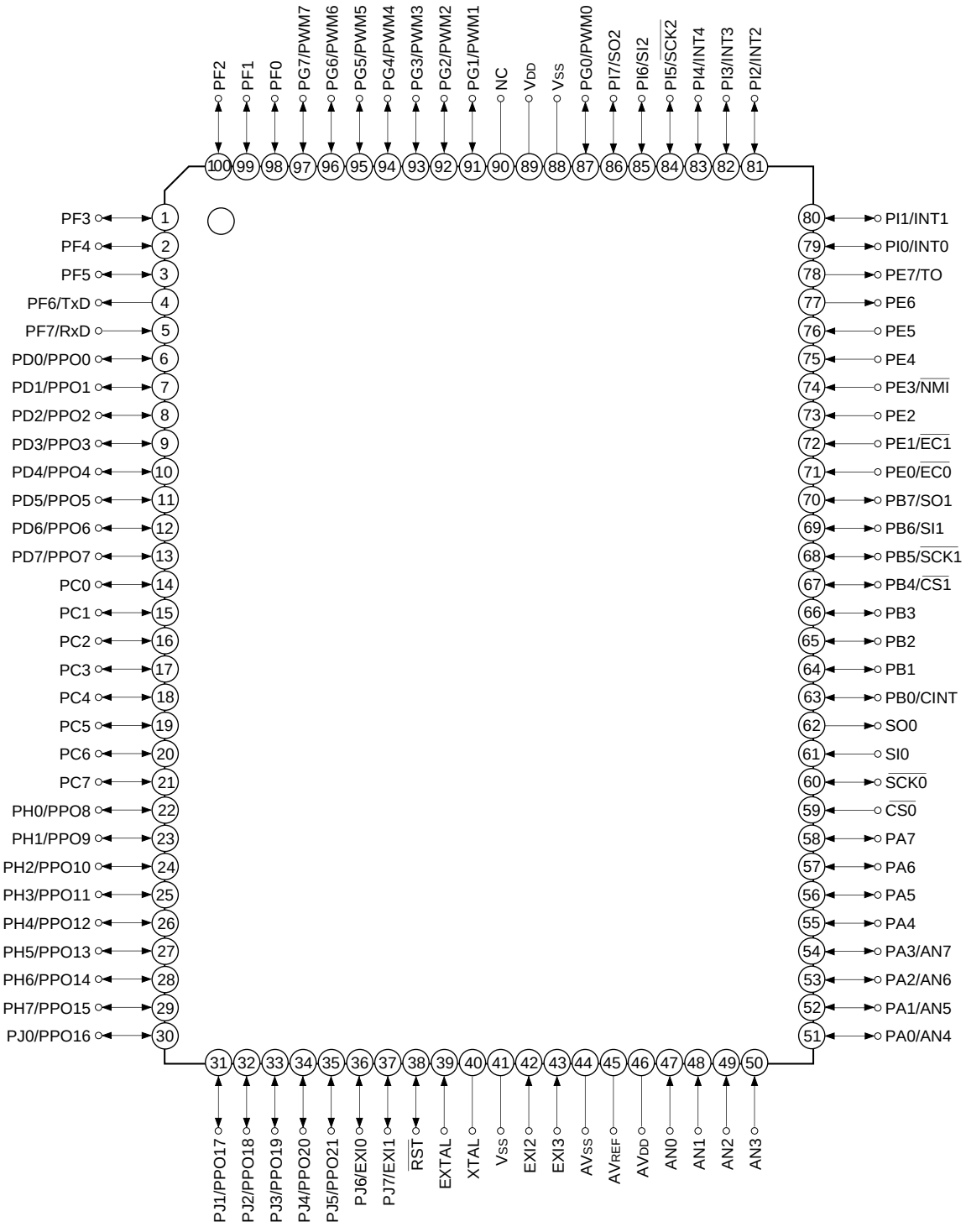
- A wide instruction set (213 instructions) which covers various types of data.
  — 16-bit arithmetic/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle — 250ns at 16MHz operation (4.5 to 5.5V)
  333ns at 12MHz operation (3.0 to 5.5V)
- Incorporated ROM capacity — 16K bytes (CXP84716)
  20K bytes (CXP84720)
  24K bytes (CXP84724)
- Incorporated RAM capacity — 1120 bytes
- Peripheral functions
  — A/D converter — 8 bits, 8 channels, successive approximation method
  (Conversion time 1.6µs at 16MHz)
  — Serial interface — Srart-stop synchronization (UART), 1 channel
  Incorporated buffer RAM (Auto transfer for 1 to 32 bytes), 2 channels
  8-bit clock syncronization (MSB/LSB first selectable), 1 channel
  — Timer — 8-bit timer, 8-bit timer/counter, 19-bit time base timer,
  16-bit capture timer/counter
  — FRC capture unit — Incorporated 24-bit and 6-stage FIFO
  — High-precision timing pattern generation circuit
  PPG: maximum of 11 pins, 16 stages programmable, 2 channels
  — PWM output — 8 bits, 8 channels
- Interruption — 19 factors, 15 vectors, multi-interruption possible
- Standby mode — Sleep/stop
- Package — 100-pin plastic QFP/LQFP
- Piggyback/evaluator — CXP84700

E96Z13B1Y-PS

Block Diagram



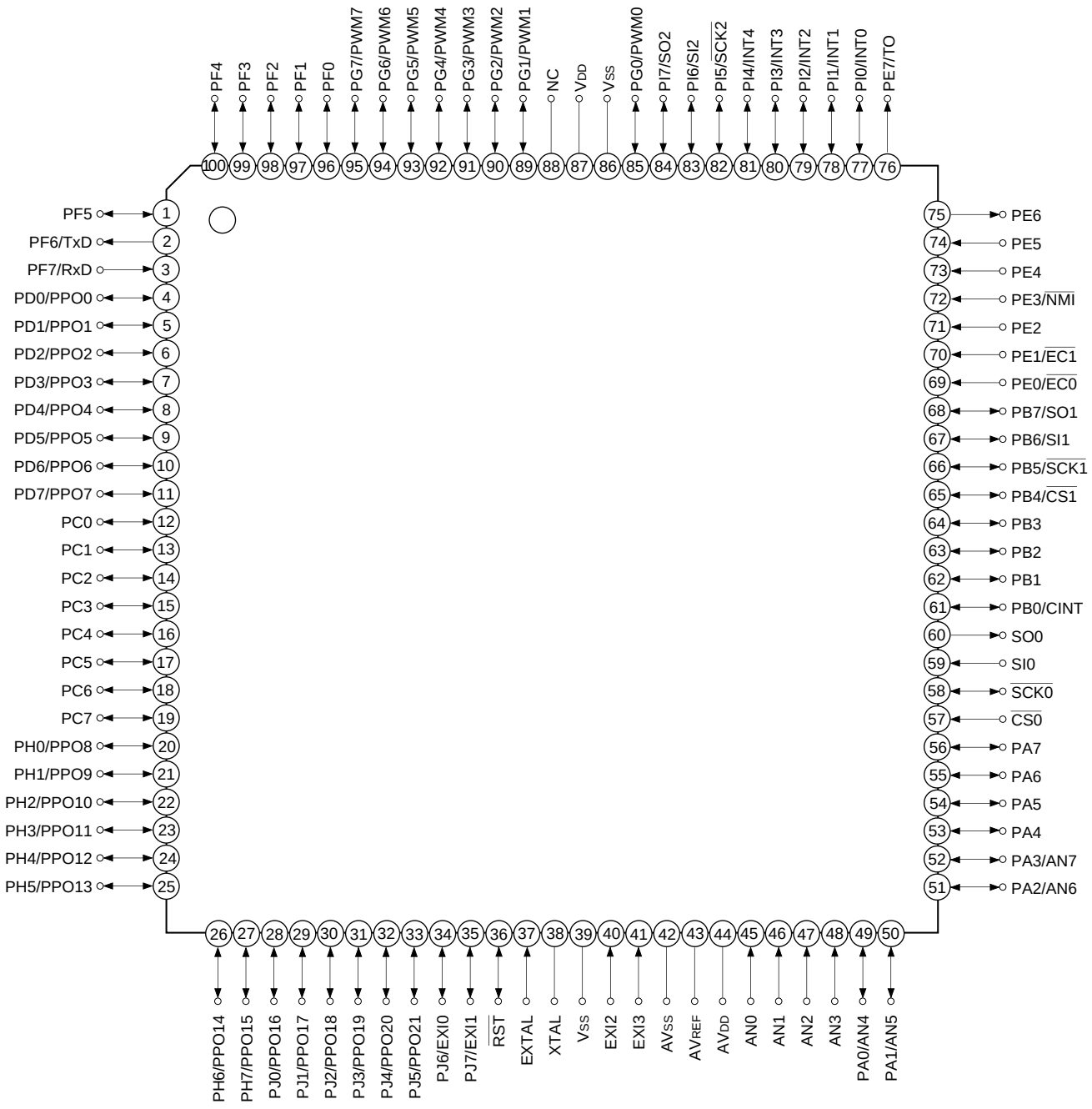
Pin Assignment (Top View) 100-pin QFP package



Note) 1. NC (Pin 90) is left open.

2. VSS (Pins 41 and 88) are both connected to GND.

Pin Assignment (Top View) 100-pin LQFP package



Note) 1. NC (Pin 88) is left open.

2. V_{SS} (Pins 39 and 86) are both connected to GND.

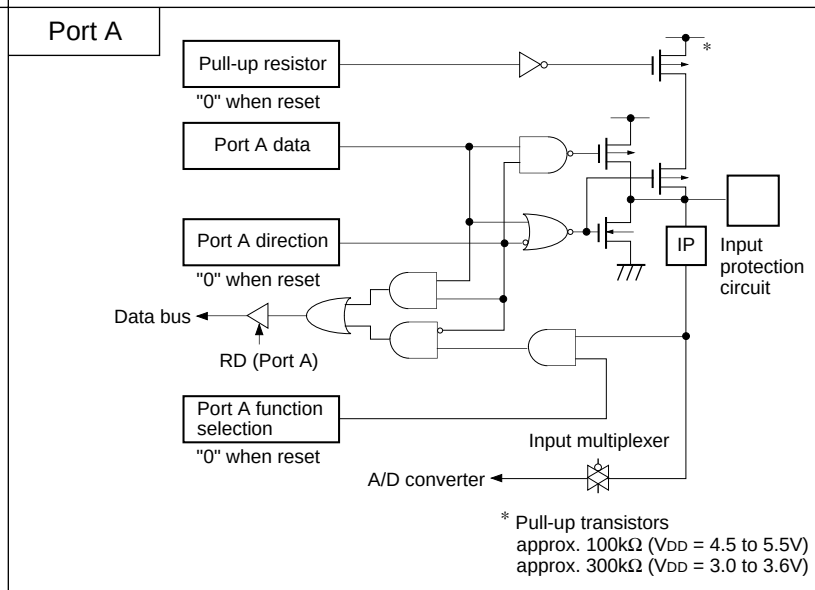
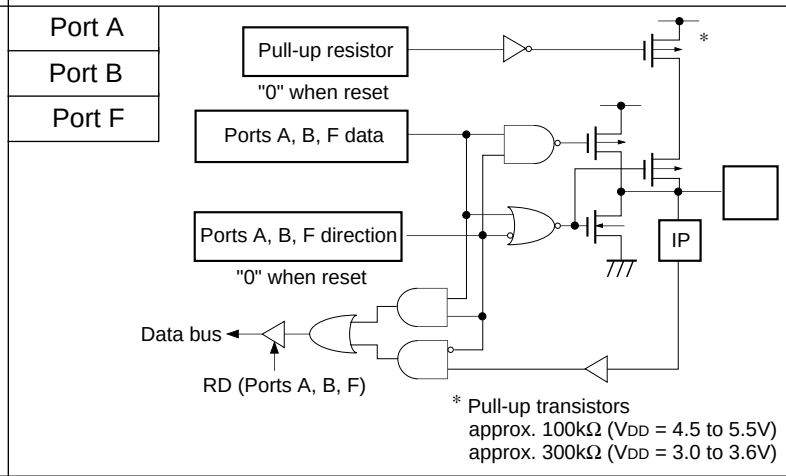
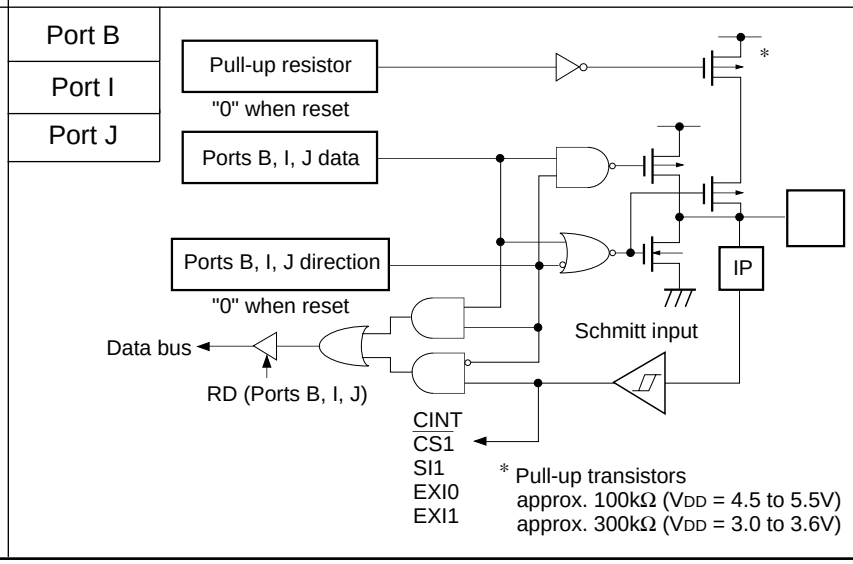
Pin Description

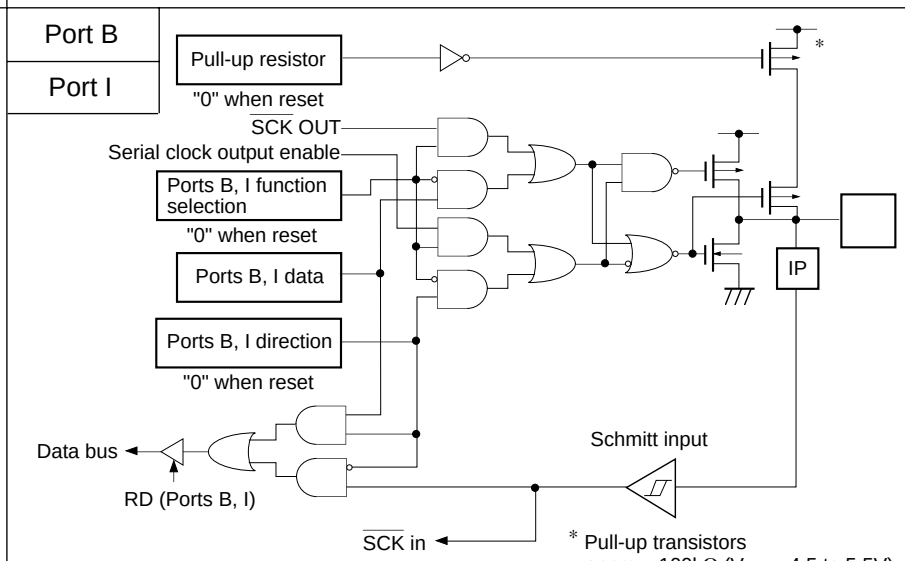
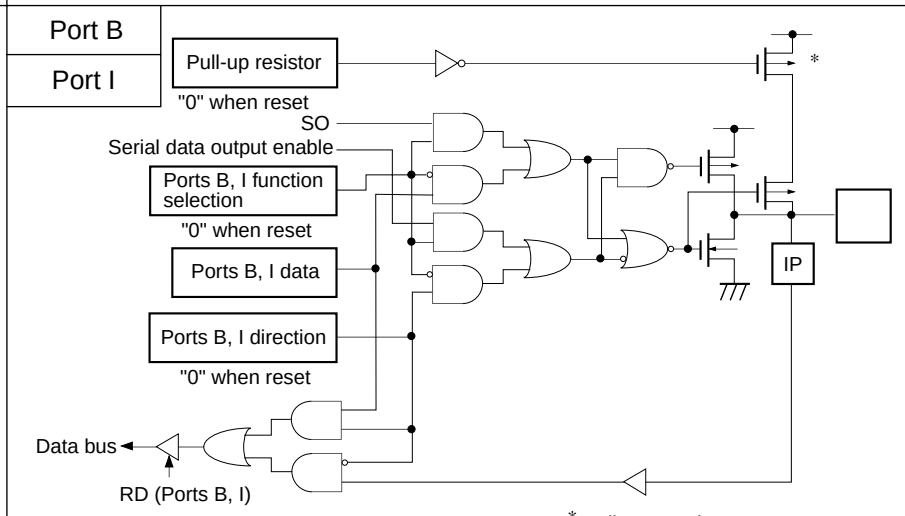
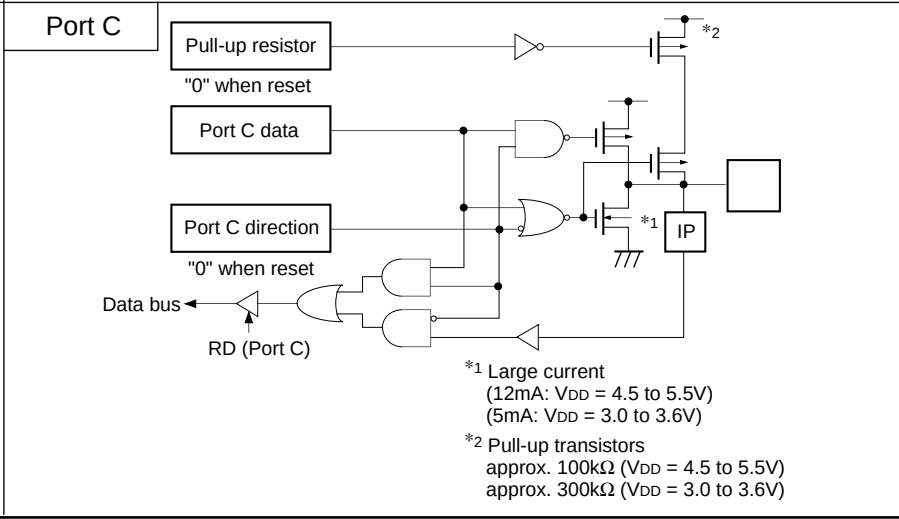
Symbol	I/O	Description	
AN0 to AN3	Input	Analog inputs to A/D converter. (4 pins)	
PA0/AN4 to PA3/AN7	I/O/Input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (4 pins)
PA4 to PA7	I/O		
PB0/CINT	I/O/Input	(Port B) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	External capture input to 16-bit timer/counter.
PB1 to PB3	I/O		
PB4/$\overline{CS1}$	I/O/Input		Chip select input for serial interface (CH1).
PB5/$\overline{SCK1}$	I/O/I/O		Serial clock I/O (CH1).
PB6/SI1	I/O/Input		Serial data input (CH1).
PB7/SO1	I/O/Output		Serial data output (CH1).
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Can drive 12mA sink current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PD0/PPO0 to PD7/PPO7	I/O/Real-time output	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	PPO0 to PPO7 outputs for programmable pattern generator (PPG0). Functions as high-precision real-time pulse output port. (PPG0: 11 pins; PPG1: 11 pins)
PE0/$\overline{EC0}$	Input/Input	(Port E) 8-bit port. Lower 5 bits are for input; upper 2 bits are for output. (8 pins)	External event inputs for timer/counter. (2 pins)
PE1/$\overline{EC1}$	Input/Input		
PE2	Input		
PE3/$\overline{NMI}$	Input/Input		Non-maskable interruption request.
PE4 to PE5	Input		
PE6	Output		
PE7/TO	Output/Output		Rectangular wave output for 16-bit timer/counter.

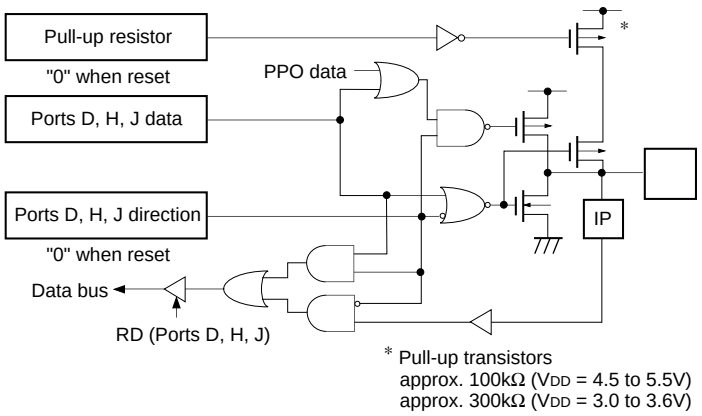
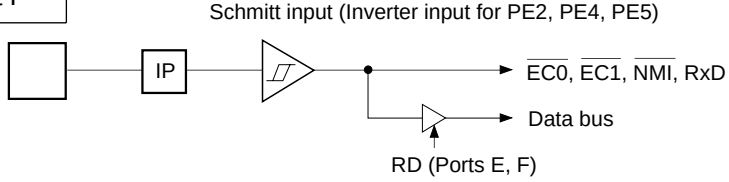
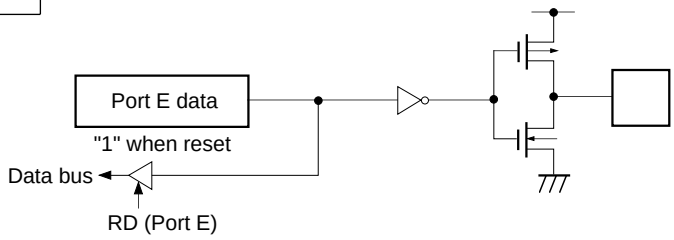
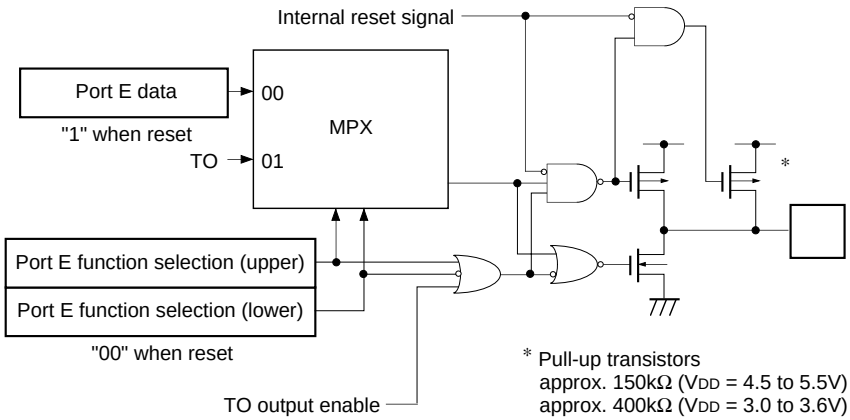
Symbol	I/O	Description	
PF0 to PF5	I/O	(Port F) Lower 6 bits are for I/O. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits (PF0 to PF3) or 2 bits (PF4,PF5) PF6 is for output; PF7 is for input. (8 pins)	
PF6/TxD	Output/Output		UART transmission data output.
PF7/RxD	Input/Input		UART reception data input.
PG0/PWM0 to PG7/PWM7	I/O/Output	(Port G) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	PWM outputs. (8 pins)
PH0/PPO8 to PH7/PPO15	I/O/Real-time output	(Port H) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	PPO8 to PPO11 (PPG0) outputs and PPO12 to PPO15 (PPG1) outputs for programmable pattern generator (PPG0, PPG1). Functions as high-precision real-time pulse output port.
PI0/INT0 to PI4/INT4	I/O/Input	(Port I) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	External interruption request inputs. (5 pins)
PI5/$\overline{SCK2}$	I/O/I/O		Serial clock I/O (CH2).
PI6/SI2	I/O/Input		Serial data input (CH2).
PI7/SO2	I/O/Output		Serial data output (CH2).
PJ0/PPO16 to PJ5/PPO21	I/O/Real-time output	(Port I) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	PPO16 to PPO21 outputs for programmable pattern generator (PPG1). Functions as high-precision real-time pulse output port.
PJ6/EXI0	I/O/Input		External inputs to FRC capture unit. (2 Pins)
PJ7/EXI1	I/O/Input		
EXI2 to EXI3	Input	External inputs to FRC capture unit. (2 pins)	
$\overline{CS0}$	Input	Chip select input for serial interface (CH0).	
$\overline{SCK0}$	I/O	Serial clock I/O (CH0).	
SI0	Input	Serial data input (CH0).	
SO1	I/O/Output	Serial data I/O (CH0).	

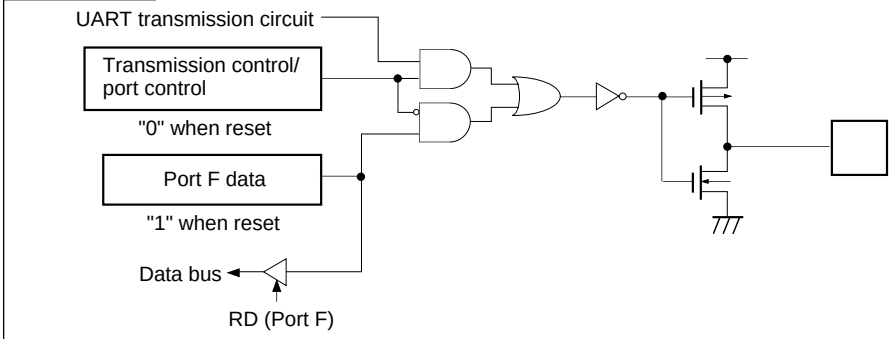
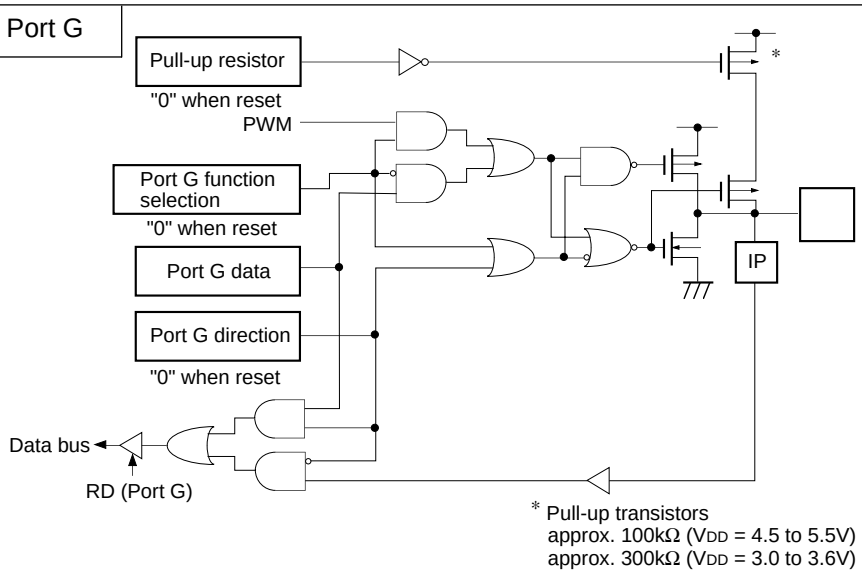
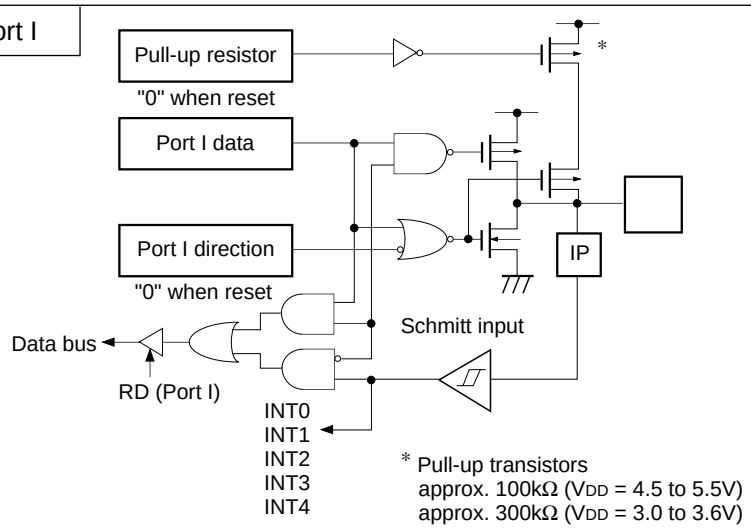
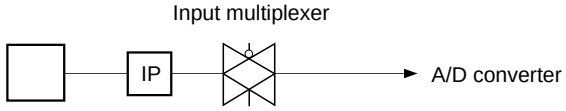
Symbol	I/O	Description
EXTAL	Input	Connects a crystal for system clock oscillation. When a clock is supplied externally, input it to EXTAL pin and input a reversed phase clock to XTAL pin.
XTAL	Output	
$\overline{\text{RST}}$	I/O	System reset; active at Low level. This pin is I/O pin, and outputs Low level at the power on with the power-on reset function is executed. (Mask option)
NC		Not connected. Leave this pin open for normal operation.
AV_{DD}		Positive power supply of A/D converter.
AV_{REF}	Input	Reference voltage input of A/D converter.
AV_{SS}		GND of A/D converter.
V_{DD}		Positive power supply.
V_{SS}		GND.

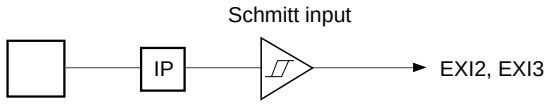
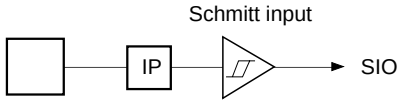
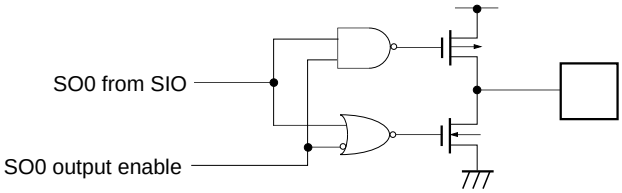
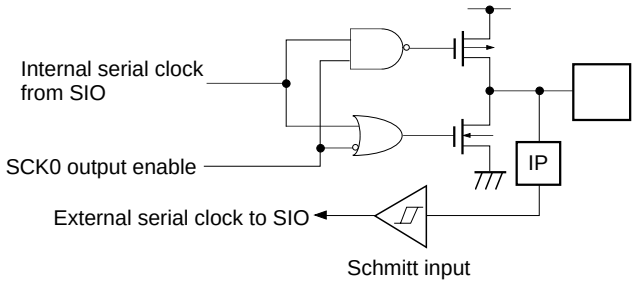
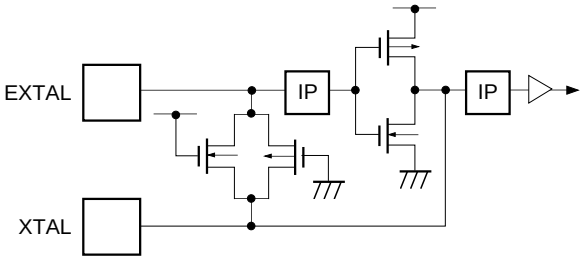
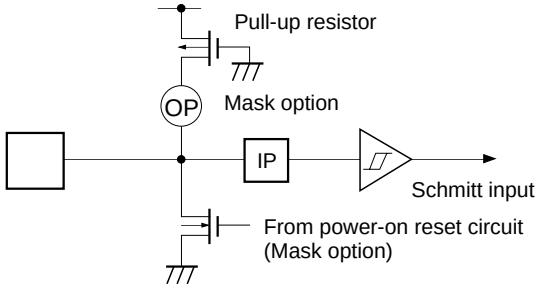
I/O Circuit Format for Pins

Pin	Circuit format	When reset
PA0/AN4 to PA3/AN7 4 pins	Port A 	Hi-Z
PA4 to PA7 PB1 to PB3 PF0 to PF5 13 pins	Port A Port B Port F 	Hi-Z
PB0/CINT PB4/$\overline{CS1}$ PB6/SI1 PI6/SI2 PJ6/EXI0 PJ7/EXI1 6 pins	Port B Port I Port J 	Hi-Z

Pin	Circuit format	When reset
PB5/$\overline{SCK1}$ PI5/$\overline{SCK2}$ 2 pins	 * Pull-up transistors approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 300kΩ (V_{DD} = 3.0 to 3.6V)	Hi-Z
PB7/SO1 PI7/SO2 2 pins	 * Pull-up transistors approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 300kΩ (V_{DD} = 3.0 to 3.6V)	Hi-Z
PC0 to PC7 8 pins	 *1 Large current (12mA: V_{DD} = 4.5 to 5.5V) (5mA: V_{DD} = 3.0 to 3.6V) *2 Pull-up transistors approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 300kΩ (V_{DD} = 3.0 to 3.6V)	Hi-Z

Pin	Circuit format	When reset
PD0/PPO0 to PD7/PPO7 PH0/PPO8 to PH7/PPO15 PJ0/PPO16 to PJ5/PPO21 22 pins	Port D / Port H / Port J 	Hi-Z
PE0/$\overline{EC0}$ PE1/$\overline{EC1}$ PE2 PE3/$\overline{NMI}$ PE4 PE5 PF7/RxD 7 pins	Port E / Port F 	Hi-Z
PE6 1 pin	Port E 	High level
PE7/TO 1 pin	Port E 	High level (with the resistor of pull-up transistor ON for reset)

Pin	Circuit format	When reset
PF6/TxD 1 pin	Port F 	High level
PG0/PWM0 to PG7/PWM7 8 pins	Port G 	Hi-Z
PI0/INT0 to PI4/INT4 5 pins	Port I 	Hi-Z
AN0 to AN3 4 pins		Hi-Z

Pin	Circuit format	When reset
EXI2 EXI3 2 pins		Hi-Z
$\overline{CS0}$ SI0 2 pins		Hi-Z
SO0 1 pin		Hi-Z
$\overline{SCK0}$ 1 pin		Hi-Z
EXTAL XTAL 2 pins		Oscillation
$\overline{RST}$ 1 pin		Low level

Absolute Maximum Ratings (Vss = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
	AV_{DD}	AV_{SS} to +7.0*1	V	
	AV_{SS}	–0.3 to +0.3	V	
	AV_{REF}	AV_{SS} to +7.0	V	
Input voltagte	V_{IN}	–0.3 to +7.0*2	V	
Output voltage	V_{OUT}	–0.3 to +7.0*2	V	
High level output current	I_{OH}	–5	mA	Output (value per pin)
High level total output current	$\sum I_{OH}$	–50	mA	Total for all output pins
	I_{OL}	15	mA	All pins excluding large current outputs (value per pin)
Low level output current	I_{OLC}	20	mA	Large current outputs (value per pin) *3
Low level total output current	$\sum I_{OL}$	100	mA	Total for all output pins
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	QFP package
		380		LQFP package

*1 AV_{DD} and V_{DD} must be set to the same voltage.

*2 V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*3 The large current output pins are Port C (PC).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks	
Supply voltage	V_{DD}	4.5	5.5	V	fc = 16MHz or less	Guaranteed operation range for 1/2 and 1/4 frequency dividing clock.
		3.0	5.5	V	fc = 12MHz or less	
		2.7	5.5	V	Guaranteed operation range for 1/16 frequency dividing clock or sleep mode	
		2.7	5.5	V	Guaranteed data hold operation range during stop mode	
Analog voltage	AV_{DD}	3.0	5.5	V	*1	
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	*2, *5	
		0.8V_{DD}	V_{DD}	V	*2, *6	
	V_{IHS}	0.8V_{DD}	V_{DD}	V	Hysteresis input*3	
	V_{IHEX}	V_{DD} – 0.4	V_{DD} + 0.3	V	EXTAL pin*4, *5	
		V_{DD} – 0.2	V_{DD} + 0.2	V	EXTAL pin*4, *6	
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	*2, *5	
		0	0.2V_{DD}	V	*2, *6	
	V_{ILS}	0	0.2V_{DD}	V	Hysteresis input*3	
	V_{ILEX}	–0.3	0.4	V	EXTAL pin*4, *5	
		–0.3	0.2	V	EXTAL pin*4, *6	
Operating temperature	Topr	–20	+75	°C		

*1 AV_{DD} and V_{DD} must be set to the same voltage.

*2 Normal input port (PA, PB1 to PB3, PB7, PC, PD, PE2, PE4, PE5, PF0 to PF5, PG, PH, PI7, PJ0 to PJ5)

*3 $\overline{RST}$, CINT, $\overline{CS0}$, $\overline{CS1}$, $\overline{SCK0}$, $\overline{SCK1}$, $\overline{SCK2}$, SI0, SI1, SI2, $\overline{EC0}$, $\overline{EC1}$, $\overline{NMI}$, RxD, INT0, INT1, INT2, INT3, INT4, EXI0, EXI1, EXI2 and EXI3

*4 Specifies only when the external clock is input.

*5 This case applies to the range of 4.5 to 5.5V supply voltage (V_{DD}).

*6 This case applies to the range of 3.0 to 5.5V supply voltage (V_{DD}).

Electrical Characteristics

DC Characteristics (V_{DD} = 4.5 to 5.5V) (Ta = –20 to +75°C, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE6, PE7, PF0 to PF6, PG to PJ, SCK0, SO0	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output voltage	V_{OL}	PA to PD, PE6, PE7, PF0 to PF6, PG to PJ, SCK0, SO0, RST*1	V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PC	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{IHT}	TEX	V_{DD} = 5.5V, V_{IL} = 5.5V	0.1		10	µA
	I_{ILT}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.1		–10	µA
	I_{ILR}	RST*2	V_{DD} = 5.5V, V_{IL} = 0.4V	–1.5		–400	µA
	I_{IL}	PA to PD*3, PF0 to PF5*3, PG to PJ*3				–45	µA
			V_{DD} = 4.5V, V_{IL} = 4.0V	–2.78			µA
I/O leakage current	I_{IZ}	PA to PD*3, PE0 to PE5, PF0 to PF5*3, PF7, PG to PJ*3, CS0, SCK0, SI0, EXI2, EXI3, AN0 to AN3 RST*2	V_{DD} = 5.5V V_I = 0, 5.5V			±10	µA

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Supply current*4	I_{DD}	V_{DD}	1/2 frequency dividing clock operation V_{DD} = 5.5V, 16MHz crystal oscillation (C_1 = C_2 = 15pF)		17.5	40	mA
	I_{DDS1}		Sleep mode V_{DD} = 5.5V, 16MHz crystal oscillation (C_1 = C_2 = 15pF)		1.4	8	mA
	I_{DDS2}		Stop mode V_{DD} = 5.5V, termination of 16MHz crystal oscillation			10	µA
Input capacity	C_{IN}	PA to PD, PE0 to PE5, PF0 to PF5, PF7, PG to PJ, $\overline{CS0}$, $\overline{SCK0}$, SI0, EXI2, EXI3, AN0 to AN3, EXTAL, $\overline{RST}$	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1 $\overline{RST}$ pin specifies the output voltage only when the power-on reset circuit is selected with mask option.

*2 $\overline{RST}$ pin specifies the input current when the pull-up resistance is selected, and specifies the leakage current when no resistance is selected.

*3 PA to PD, PF0 to PF5 and PG to PJ pins specify the input current when the pull-up resistance is selected, and specify the leakage current when no resistance is selected.

*4 When all pins are open.

Electrical Characteristics

DC Characteristics (V_{DD} = 3.0 to 3.6V) (Ta = –20 to +75°C, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE6, PE7, PF0 to PF6, PG to PJ, SCK0, SO0	V_{DD} = 3.0V, I_{OH} = –0.15mA	2.7			V
			V_{DD} = 3.0V, I_{OH} = –0.5mA	2.3			V
Low level output voltage	V_{OL}	PA to PD, PE6, PE7, PF0 to PF6, PG to PJ, SCK0, SO0, RST*1	V_{DD} = 3.0V, I_{OL} = 1.2mA			0.3	V
			V_{DD} = 3.0V, I_{OL} = 1.6mA			0.5	V
		PC	V_{DD} = 3.0V, I_{OL} = 5.0mA			1	V
Input current	I_{IHE}	EXTAL	V_{DD} = 3.6V, V_{IH} = 3.6V	0.3		20	µA
	I_{ILE}		V_{DD} = 3.6V, V_{IL} = 0.3V	–0.3		–20	µA
	I_{IHT}	TEX	V_{DD} = 3.6V, V_{IL} = 3.6V	0.1		10	µA
	I_{ILT}		V_{DD} = 3.6V, V_{IL} = 0.4V	–0.1		–10	µA
	I_{ILR}	RST*2	V_{DD} = 3.6V, V_{IL} = 0.3V	–0.9		–200	µA
	I_{IL}	PA to PD*3, PF0 to PF5*3, PG to PJ*3				–20	µA
			V_{DD} = 3.0V, V_{IL} = 2.7V	–1.0			µA
I/O leakage current	I_{IZ}	PA to PD*3, PE0 to PE5, PF0 to PF5*3, PF7, PG to PJ*3, CS0, SCK0, SI0, EXI2, EXI3, AN0 to AN3 RST*2	V_{DD} = 3.6V V_I = 0, 3.6V			±10	µA

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Supply current*4	I_{DD}	V_{DD}	1/2 frequency dividing clock operation V_{DD} = 3.6V, 12MHz crystal oscillation (C_1 = C_2 = 15pF)		6.5	18	mA
	I_{DDS1}		Sleep mode V_{DD} = 3.6V, 12MHz crystal oscillation (C_1 = C_2 = 15pF)		0.5	2.0	mA
	I_{DDS2}		Stop mode V_{DD} = 3.6V, termination of 12MHz crystal oscillation			10	µA
Input capacity	C_{IN}	PA to PD, PE0 to PE5, PF0 to PF5, PF7, PG to PJ, $\overline{CS0}$, $\overline{SCK0}$, SI0, EXI2, EXI3, AN0 to AN3, EXTAL, $\overline{RST}$	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1 $\overline{RST}$ pin specifies the output voltage only when the power-on reset circuit is selected with mask option.

*2 $\overline{RST}$ pin specifies the input current when the pull-up resistance is selected, and specifies the leakage current when no resistance is selected.

*3 PA to PD, PF0 to PF5 and PG to PJ pins specify the input current when the pull-up resistance is selected, and specify the leakage current when no resistance is selected.

*4 When all pins are open.

AC Characteristics

(1) Clock timing (Ta = –20 to +75°C, V_{DD} = 3.0 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2 V_{DD} = 4.5 to 5.5V	1		16	MHz
				1		12	
System clock input pulse width	t_{XL} t_{XH}	XTAL EXTAL	Fig. 1, Fig. 2 V_{DD} = 4.5 to 5.5V	28			ns
			External clock drive	37.5			
System clock input rise time, fall time	t_{CR} t_{CF}	XTAL EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	t_{EH} t_{EL}	$\overline{EC0}$ EC1	Fig. 3	tsys + 50*1			ns
Event count input clock rise time, fall time	t_{ER} t_{EF}	$\overline{EC0}$ EC1	Fig. 3			20	ms

*1 tsys indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (CLC: 00FEh).
tsys [ns] = 2000/fc (upper two bits = “00”), 4000/fc (upper two bits = “01”), 16000/fc (Upper two bits = “11”)

Fig. 1. Clock timing

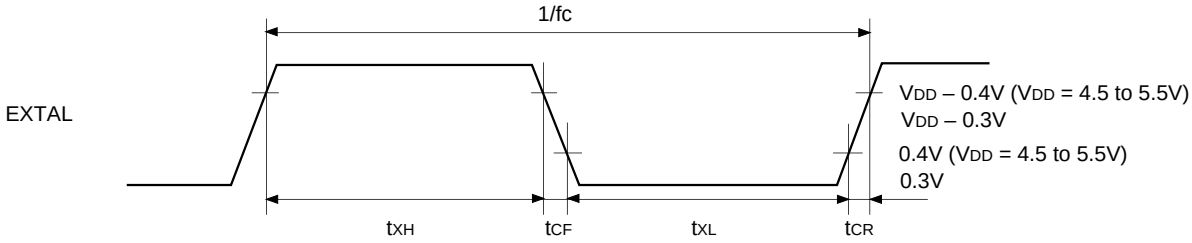


Fig. 2. Clock applied conditions

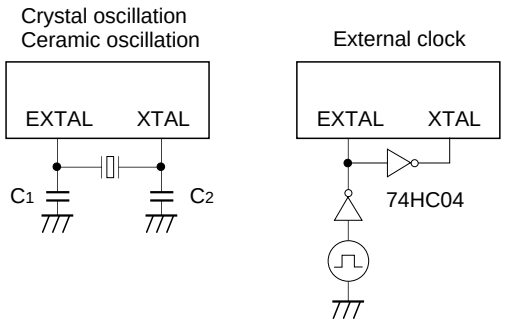
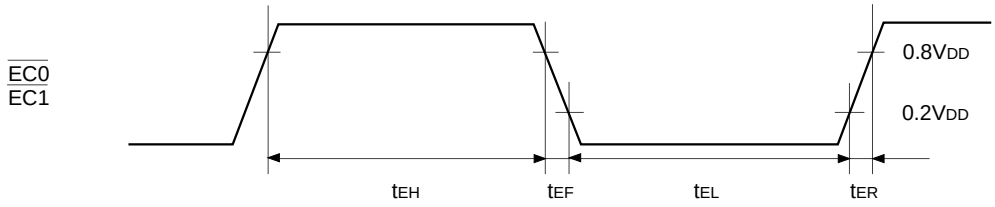


Fig. 3. Event count clock timing



(2) Serial transfer (CH0, CH1) (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{CS}\downarrow \rightarrow \overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$ $\overline{SCK1}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		1.5tsys + 200	ns
$\overline{CS}\uparrow \rightarrow \overline{SCK}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$ $\overline{SCK1}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		1.5tsys + 200	ns
$\overline{CS}\downarrow \rightarrow$ SO delay time	t_{DCSO}	SO0 SO1	Chip select transfer mode		1.5tsys + 200	ns
$\overline{CS}\uparrow \rightarrow$ SO floating delay time	t_{DCSOF}	SO0 SO1	Chip select transfer mode		1.5tsys + 200	ns
$\overline{CS}$ High level width	t_{WHCS}	$\overline{CS0}$ $\overline{CS1}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$ $\overline{SCK1}$	Input mode	2tsys + 200		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ High and Low level width	t_{KH} t_{KL}	$\overline{SCK0}$ $\overline{SCK1}$	Input mode	tsys + 100		ns
			Output mode	4000/fc – 50		ns
SI input setup time (for $\overline{SCK}\uparrow$)	t_{SIK}	SI0 SI1	$\overline{SCK}$ input mode	–tsys + 100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (for $\overline{SCK}\uparrow$)	t_{KSI}	SI0 SI1	$\overline{SCK}$ input mode	2tsys + 200		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK}\downarrow \rightarrow$ SO delay time	t_{KSO}	SO0 SO1	$\overline{SCK}$ input mode		2tsys + 200	ns
			$\overline{SCK}$ output mode		100	ns

Note 1) tsys indicates three values according to the contents of the clock control register (CLC: 00FE$_h$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (upper 2 bits = “00”), 4000/fc (upper 2 bits = “01”), 16000/fc (upper 2 bits = “11”)

Note 2) $\overline{CS}$, $\overline{SCK}$, SI and SO represent $\overline{CS0}$, $\overline{SCK0}$, SI0 and SO0 for CH0; they represent $\overline{CS1}$, $\overline{SCK1}$, SI1 and SO1 for CH1, respectively.

Note 3) The load of $\overline{SCK}$ output mode and SO output delay time is 50pF + 1TTL.

Serial transfer (CH0, CH1) (Ta = –20 to +75°C, V_{DD} = 3.0 to 3.6V, Vss = 0V reference)

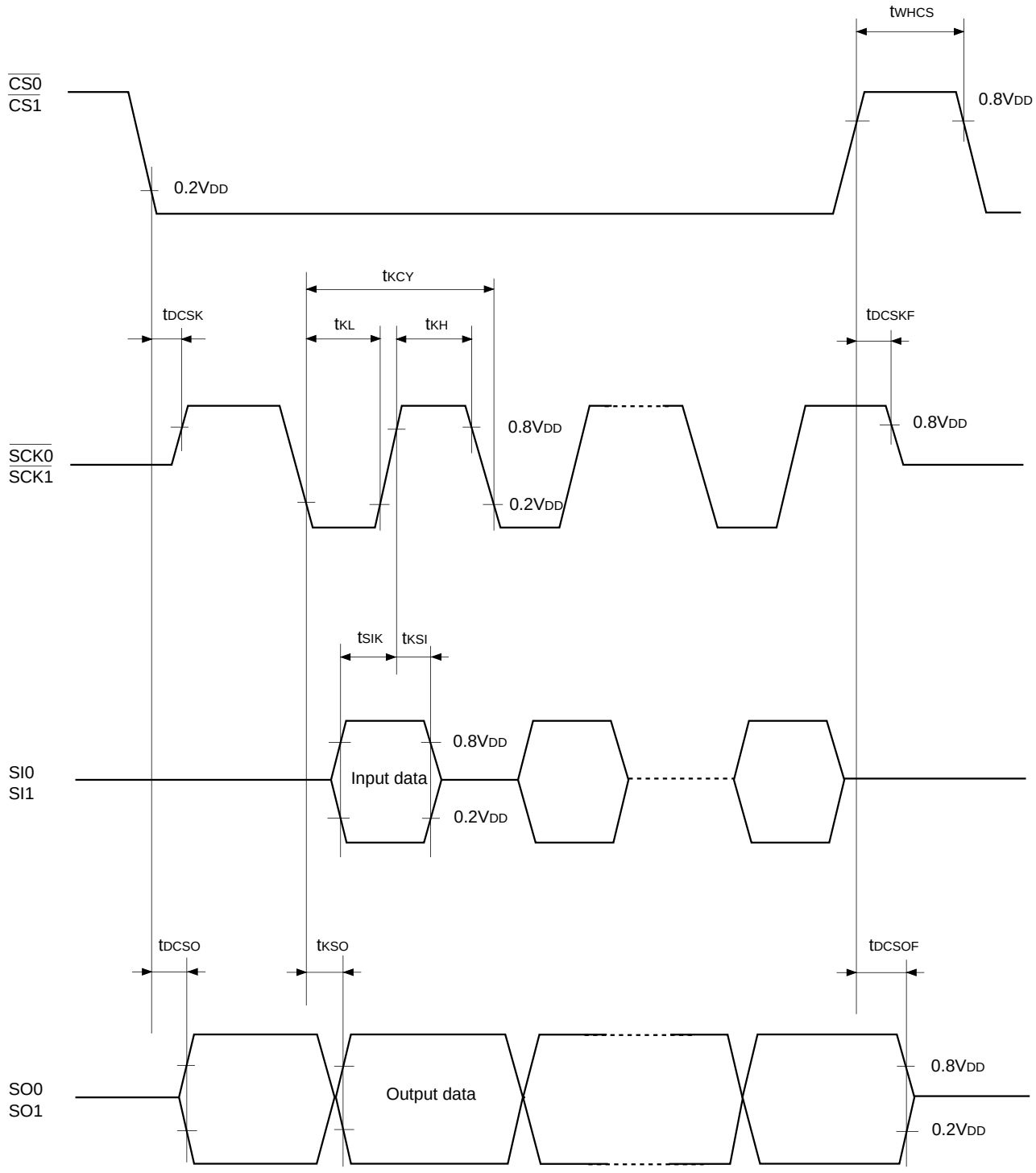
Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{CS}\downarrow \rightarrow \overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$ $\overline{SCK1}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		1.5tsys + 250	ns
$\overline{CS}\uparrow \rightarrow \overline{SCK}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$ $\overline{SCK1}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		1.5tsys + 200	ns
$\overline{CS}\downarrow \rightarrow$ SO delay time	t_{DCSO}	SO0 SO1	Chip select transfer mode		1.5tsys + 250	ns
$\overline{CS}\uparrow \rightarrow$ SO floating delay time	t_{DCSOF}	SO0 SO1	Chip select transfer mode		1.5tsys + 200	ns
$\overline{CS}$ High level width	t_{WHCS}	$\overline{CS0}$ $\overline{CS1}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$ $\overline{SCK1}$	Input mode	2tsys + 200		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ High and Low level widths	t_{KH} t_{KL}	$\overline{SCK0}$ $\overline{SCK1}$	Input mode	tsys + 100		ns
			Output mode	4000/fc – 100		ns
SI input setup time (for $\overline{SCK}\uparrow$)	t_{SIK}	SI0 SI1	$\overline{SCK}$ input mode	–tsys + 100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (for $\overline{SCK}\uparrow$)	t_{KSI}	SI0 SI1	$\overline{SCK}$ input mode	2tsys + 200		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK}\downarrow \rightarrow$ SO delay time	t_{KSO}	SO0 SO1	$\overline{SCK}$ input mode		2tsys + 250	ns
			$\overline{SCK}$ output mode		125	ns

Note 1) tsys indicates three values according to the contents of the clock control register (CLC: 00FE$_h$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (upper 2 bits = “00”), 4000/fc (upper 2 bits = “01”), 16000/fc (upper 2 bits = “11”)

Note 2) $\overline{CS}$, $\overline{SCK}$, SI and SO represent $\overline{CS0}$, $\overline{SCK0}$, SI0 and SO0 for CH0; they represent $\overline{CS1}$, $\overline{SCK1}$, SI1 and SO1 for CH1, respectively.

Note 3) The load of $\overline{SCK}$ output mode and SO output delay time is 50pF.

Fig. 4. Serial transfer CH0, CH1 timing



Serial transfer (CH2) (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK2}$	Input mode	1000		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ High and Low level widths	t_{KH} t_{KL}	$\overline{SCK2}$	Input mode	400		ns
			Output mode	4000/fc – 50		ns
SI input setup time (for $\overline{SCK}\uparrow$)	t_{SIK}	SI2	$\overline{SCK}$ input mode	100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (for $\overline{SCK}\uparrow$)	t_{KSI}	SI2	$\overline{SCK}$ input mode	200		ns
			$\overline{SCK}$ output mode	100		ns
SCK$\downarrow$ $\rightarrow$ SO delay time	t_{KSO}	SO2	$\overline{SCK}$ input mode		200	ns
			$\overline{SCK}$ output mode		100	ns

Note 1) tsys indicates three values according to the contents of the clock control register (CLC: 00FE$_h$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2 bits = “00”), 4000/fc (Upper 2 bits = “01’), 16000/fc (Upper 2 bits = “11”)

Note 2) $\overline{SCK}$, SI and SO represent $\overline{SCK2}$, SI2 and SO2 for CH2, respectively.

Note 3) The load of $\overline{SCK2}$ output mode and SO2 output delay time is 50pF+1TTL.

Serial transfer (CH2) (Ta = –20 to +75°C, V_{DD} = 3.0 to 3.6V, Vss = 0V reference)

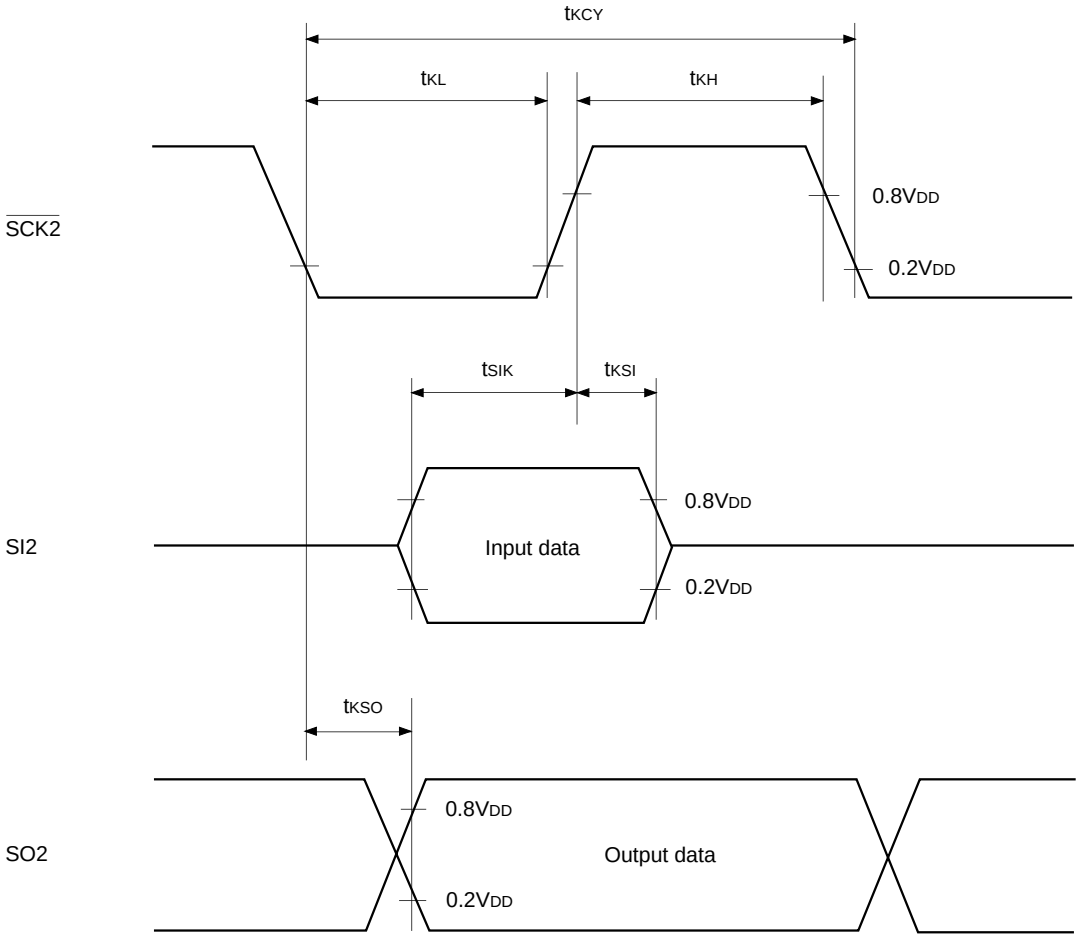
Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK2}$	Input mode	1000		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ High and Low level widths	t_{KH} t_{KL}	$\overline{SCK2}$	Input mode	400		ns
			Output mode	4000/fc – 100		ns
SI input setup time (for $\overline{SCK}\uparrow$)	t_{SIK}	SI2	$\overline{SCK}$ input mode	100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (for $\overline{SCK}\uparrow$)	t_{KSI}	SI2	$\overline{SCK}$ input mode	200		ns
			$\overline{SCK}$ output mode	100		ns
SCK$\downarrow$ $\rightarrow$ SO delay time	t_{KSO}	SO2	$\overline{SCK}$ input mode		250	ns
			$\overline{SCK}$ output mode		125	ns

Note 1) tsys indicates three values according to the contents of the clock control register (CLC: 00FE$_h$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2 bits = “00”), 4000/fc (Upper 2 bits = “01’), 16000/fc (Upper 2 bits = “11”)

Note 2) $\overline{SCK}$, SI and SO represent $\overline{SCK2}$, SI2 and SO2 for CH2, respectively.

Note 3) The load of $\overline{SCK2}$ output mode and SO2 output delay time is 50pF.

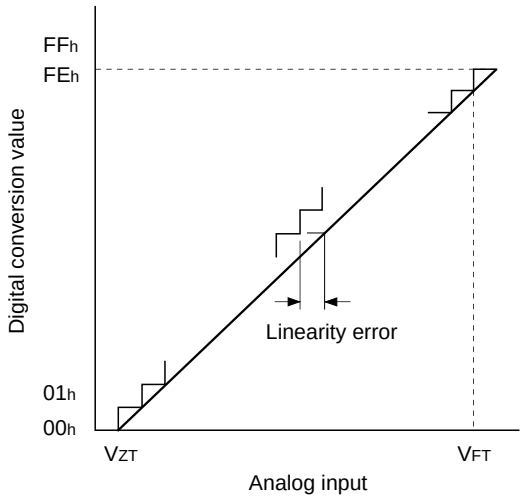
Fig. 5. Serial transfer CH2 timing



(3) A/D converter characteristics (Ta = –20 to +75°C, V_{DD} = AV_{DD} = 3.0 to 5.5V, Vss = AV_{SS} = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity errror			Ta = 25°C V_{DD} = AV_{DD} = AV_{REF} = 5.0V V_{SS} = AV_{SS} = 0V			±3	LSB
Zero transition voltage	V_{ZT}*1			–10	10	70	mV
Full-scale transition voltage	V_{FT}*2			4910	4970	5030	mV
Linearity errror			Ta = 25°C V_{DD} = AV_{DD} = AV_{REF} = 3.3V V_{SS} = AV_{SS} = 0V			±5	LSB
Zero transition voltage	V_{ZT}*1			–10	6.5	70	mV
Full-scale transition voltage	V_{FT}*2			3215	3280	3345	mV
Convertion time	t_{CONV}			26/f_{ADC}*3			µs
Sampling time	t_{SAMP}			6/f_{ADC}*3			µs
Reference input voltage	V_{REF}	AV_{REF}	V_{DD} = AV_{DD} = 4.5 to 5.5V	AV_{DD} – 0.5		AV_{DD}	V
			V_{DD} = AV_{DD} = 3.0 to 3.6V	AV_{DD} – 0.3		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN7		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operation mode, V_{DD} = 5.5V		0.6	1.0	mA
			Operation mode, V_{DD} = 3.6V		0.4	0.7	mA
	I_{REFS}		Sleep mode Stop mode			10	µA

Fig.6. Definition of A/D converter terms



*1 V_{ZT}: Value at which the digital conversion value changes from 00h to 01h and vice versa.

*2 V_{FT}: Value at which the digital conversion value changes from FEh to FFh and vice versa.

*3 f_{ADC} indicates the below values due to the contents of bit 6 (CKS) of the A/D control register (ADC: 00F9h).

PS1 selected f_{ADC} = fc

PS2 selected f_{ADC} = fc/2

(4) Interruption, reset input (Ta = –20 to +75°C, V_{DD} = 3.0 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
External interruption High, Low level width	t_{IH} t_{IL}	INT0 INT1 INT2 INT3 INT4 $\overline{NMI}$		1		µs
Reset input Low level width	t_{RSL}	$\overline{RST}$		32/fc		µs

Fig. 7. Interruption input timing

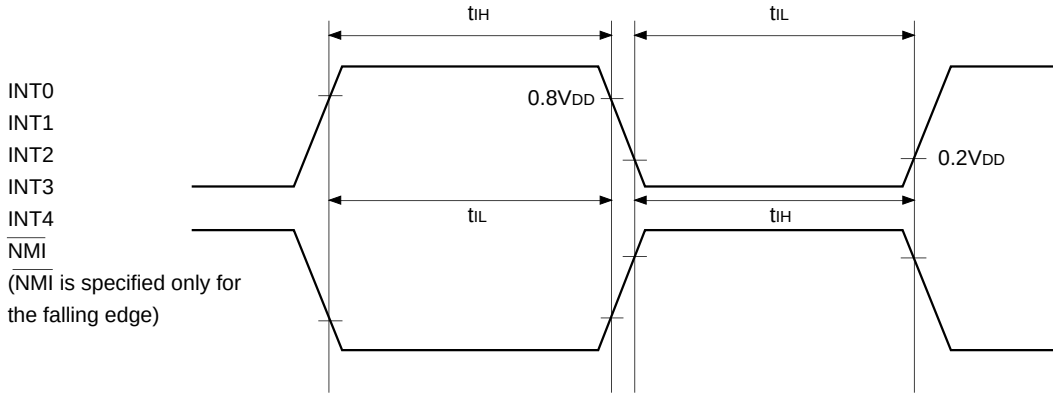
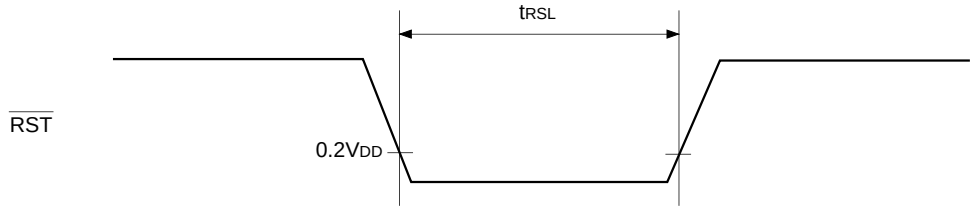


Fig. 8. $\overline{RST}$ input timing

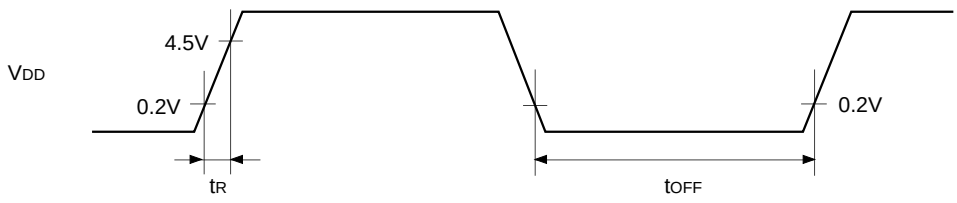


(5) Power-on reset[*1] (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
Power supply rise time	t_R	V_{DD}	Power-on reset	0.05	50	ms
Power supply cut-off time	t_{OFF}		Repetitive power-on reset	1		ms

[*1] Specifies only when the power-on reset function is selected.
Power-on reset function can be selected only for the supply voltage range of 4.5 to 5.5V.

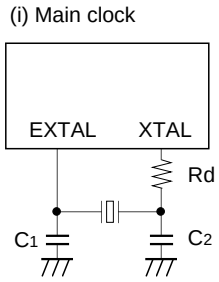
Fig. 9. Power-on reset



Turn the power on smoothly.

Appendix

Fig. 10. Recommended oscillation circuit



Manufacture	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC co., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00	5	5		
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	22 (15)	22 (15)	0	(i)
		10.00				
		12.00	15	15		
		16.00	12	12		

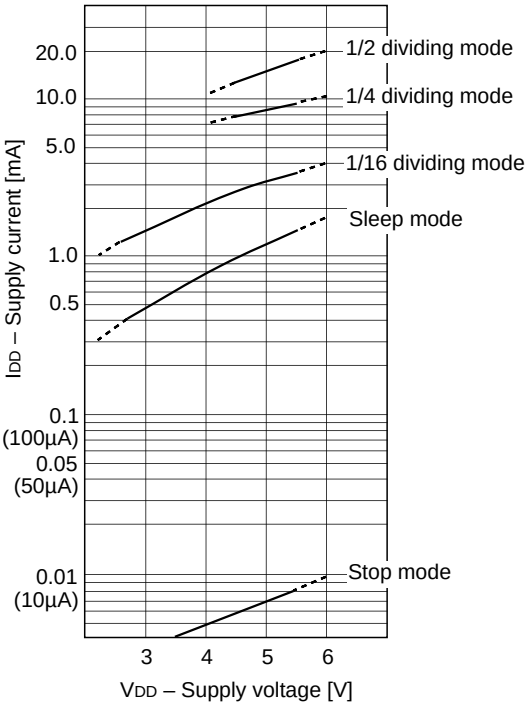
Mask Option Table

Item	Content	
Reset pin pull-up resistor	Non-existent	Existent
Power-on-reset circuit*1	Non-existent	Existent

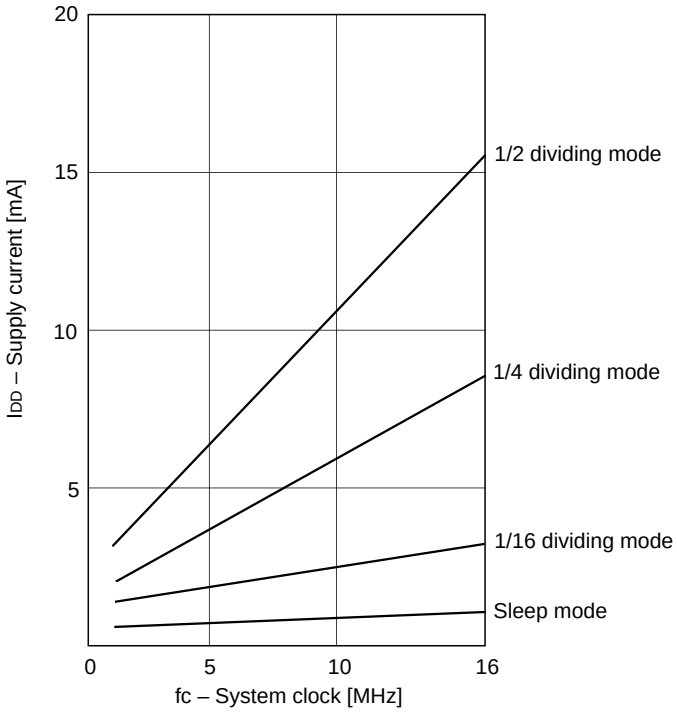
*1 Power-on-reset circuit can not be selected when the supply voltage (V_{DD}) ranges from 3.5 to 4.5V.

Characteristics Curve

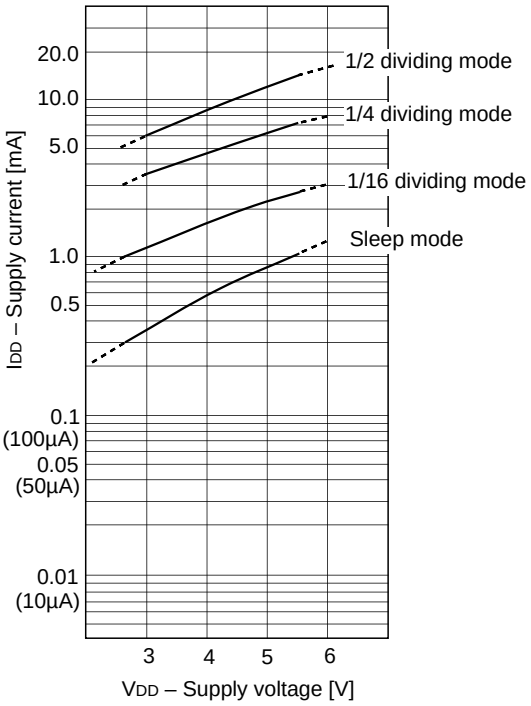
IDD vs. VDD
(fc = 16MHz, Ta = 25°C, Typical)



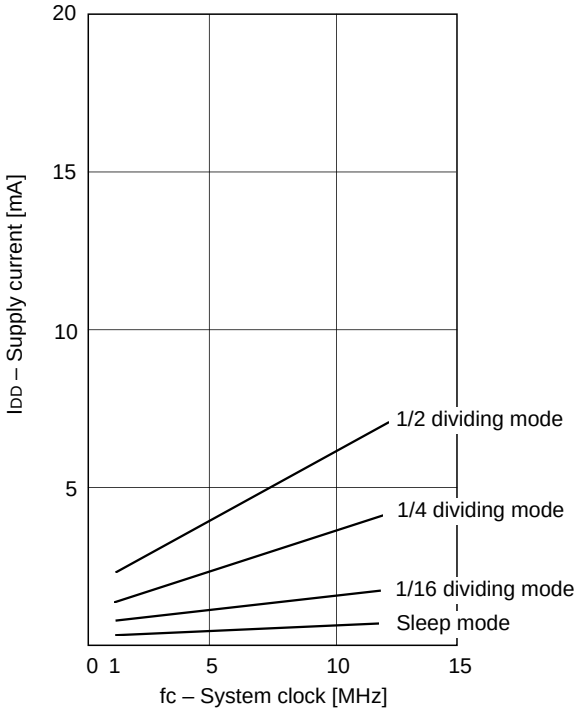
IDD vs. fc
(VDD = 5V, Ta = 25°C, Typical)



IDD vs. VDD
(fc = 12MHz, Ta = 25°C, Typical)



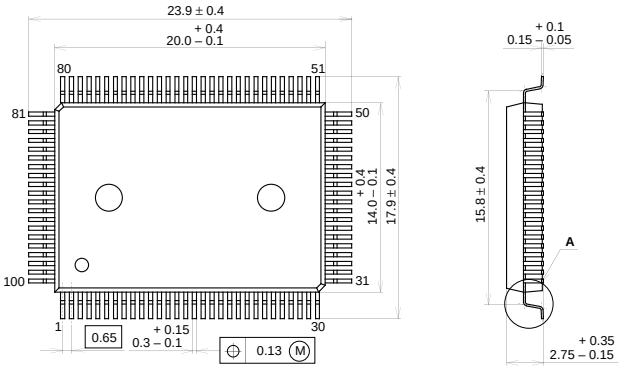
IDD vs. fc
(VDD = 3.3V, Ta = 25°C, Typical)

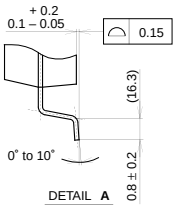


Package Outline

Unit: mm

100PIN QFP (PLASTIC)



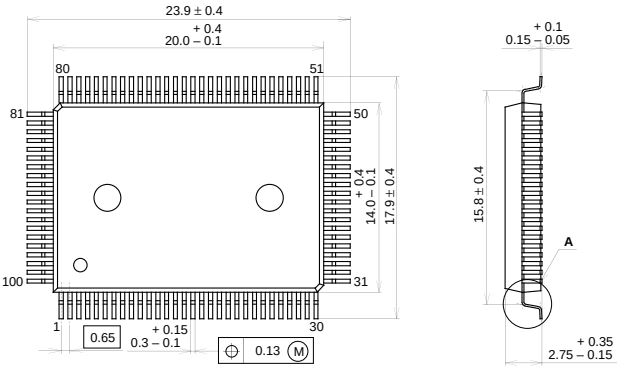


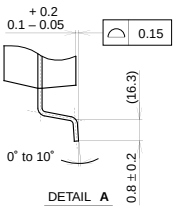
SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

100PIN QFP (PLASTIC)





SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	

PACKAGE STRUCTURE

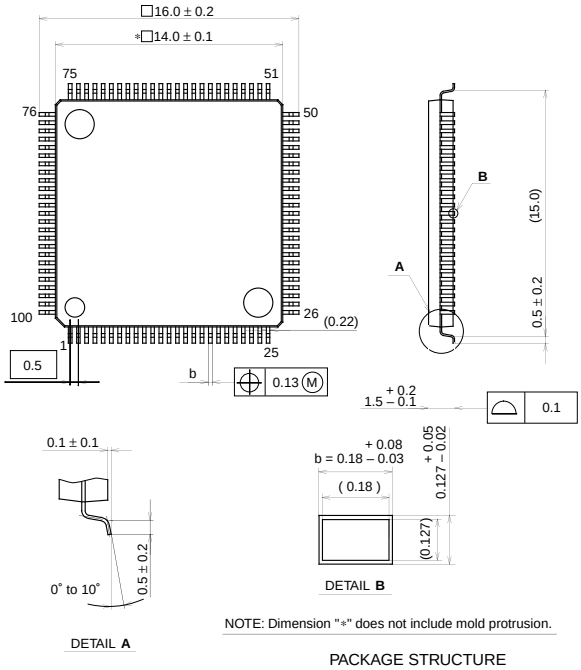
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	42 ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm

Package Outline Unit: mm

100PIN LQFP (PLASTIC)



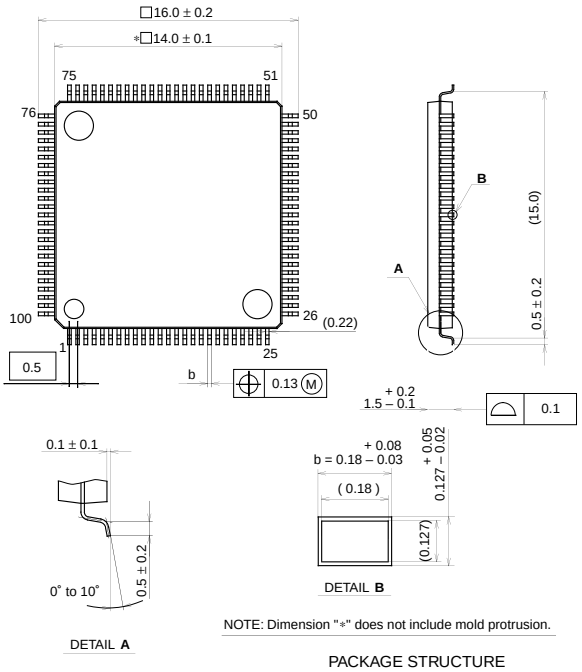
NOTE: Dimension "*" does not include mold protrusion.

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.7g

SONY CODE	LQFP-100P-L01
EIAJ CODE	P-LQFP100-14x14-0.5
JEDEC CODE	————

100PIN LQFP (PLASTIC)



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