SONY

CXP846P48

CMOS 8-bit Single Chip Microcomputer

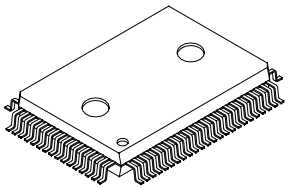
Description

The CXP846P48 is a CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time base timer, capture timer/counter, I²C bus interface, remote control reception circuit, PWM output, and 32kHz timer/counter besides the basic configurations of 8-bit CPU, PROM, RAM, and I/O port.

The CXP846P48 also provides a sleep/stop function that enables lower power consumption.

The CXP846P48 is the PROM-incorporated version of the CXP846P48 with built-in mask ROM. This provides the additional feature of being able to write directly into the program, Thus, it is most suitable for evaluation use during system development and for small-quantity production.

80 pin QFP (Plastic)



Structure

Silicon gate CMOS IC

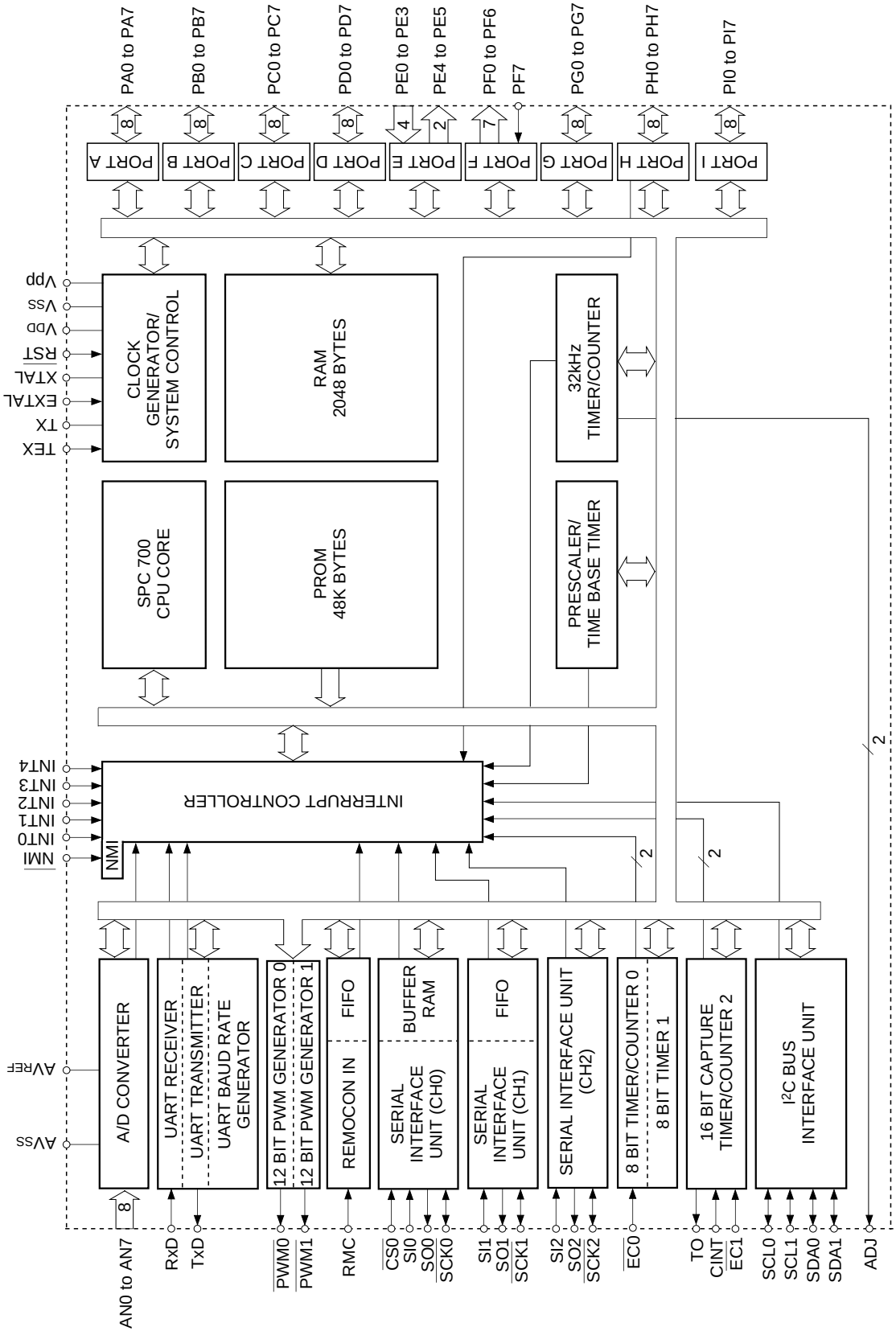
Features

- Wide range instruction system (213 instructions) to cover various of data.
  - 16-bit arithmetic/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle — 250ns at 16MHz operation (4.5 to 5.5V)
  333ns at 12MHz operation (3.0 to 5.5V)
  122µs at 32kHz operation (2.7 to 5.5V)
- Incorporated PROM capacity — 48K bytes
- Incorporated RAM capacity — 2048 bytes
- Peripheral functions
  - A/D converter — 8 bits, 8 channels, successive approximation method
    (Conversion time 20µs/16MHz)
  - Serial interface — Srart-stop synchronization (UART), 1 channel
    Incorporated buffer RAM (Auto transfer for 1 to 32 bytes), 1 channel
    Incorporated 8-bit, 10-stage FIFO
    (Auto transfer for 1 to 10 bytes), 1 channel
    8-bit clock syncronization (MSB/LSB first selectable), 1 channel
  - Timer — 8-bit timer, 8-bit timer/counter, 19-bit time base timer,
    16-bit capture timer/counter, 32kHz timer/counter
  - I²C bus interface
  - Remote control reception circuit — 8-bit pulse measurement counter, 6-stage FIFO
  - PWM output circuit — 12 bits, 2 channels
- Interruption — 21 factors, 15 vectors, multi-interruption possible
- Standby mode — SLEEP/STOP
- Package — 80-pin plastic QFP
- Piggyback/evaluation chip — CXP84600 80-pin ceramic QFP

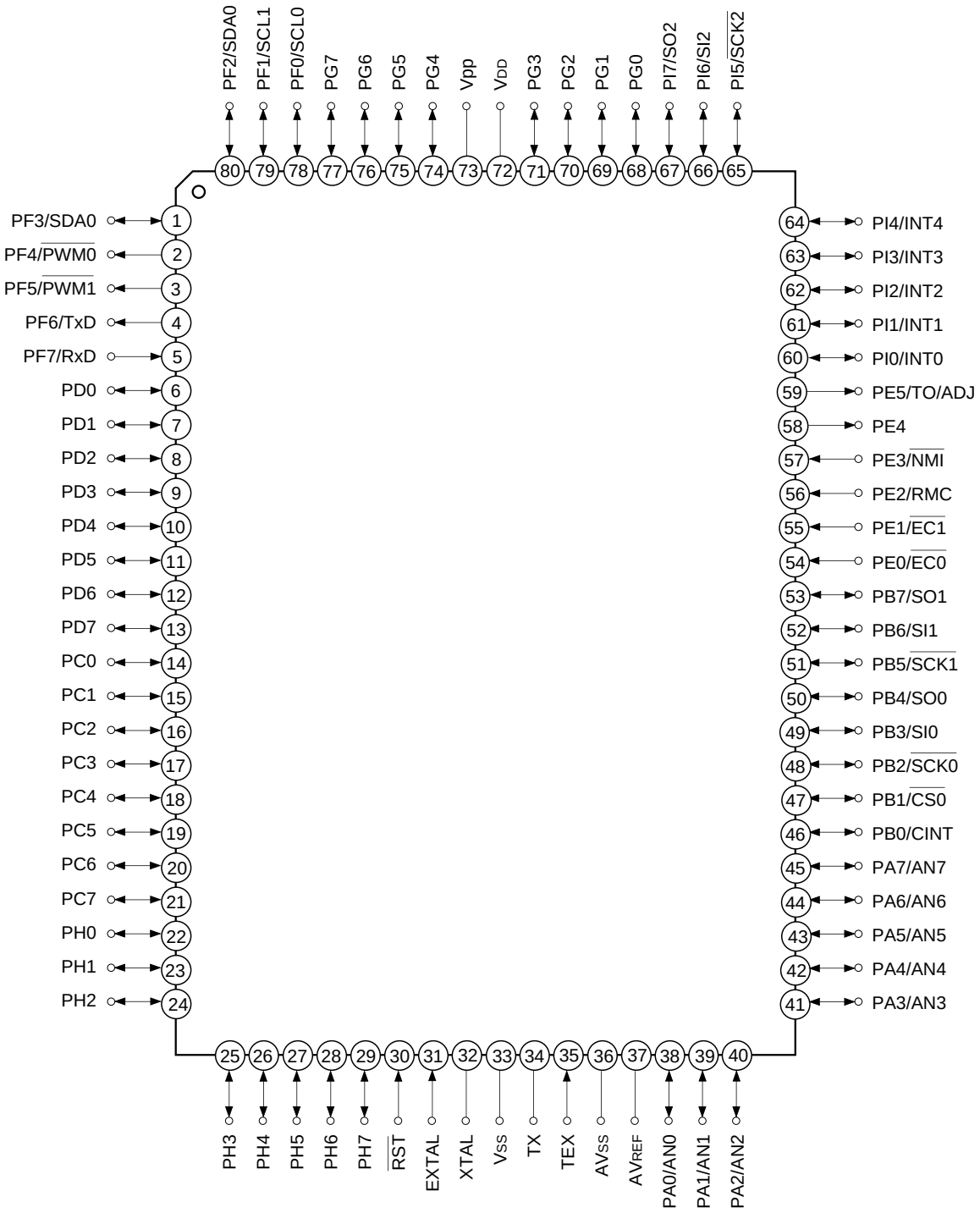
Perchase of Sony's I²C components conveys a licence under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specifications as defined by Philips.

E96308A16-PS

Block Diagram



Pin Assignment (Top View)



Note) Vpp (Pin 73) must be connected V_{DD}.

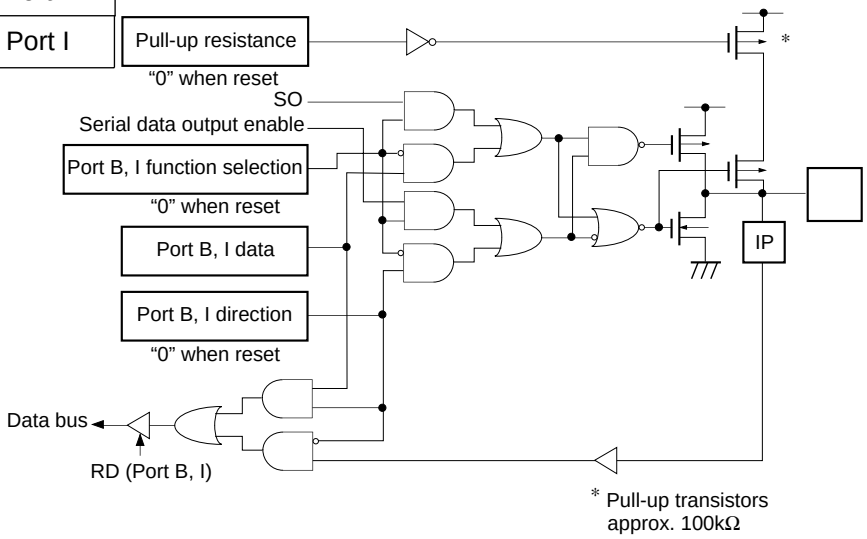
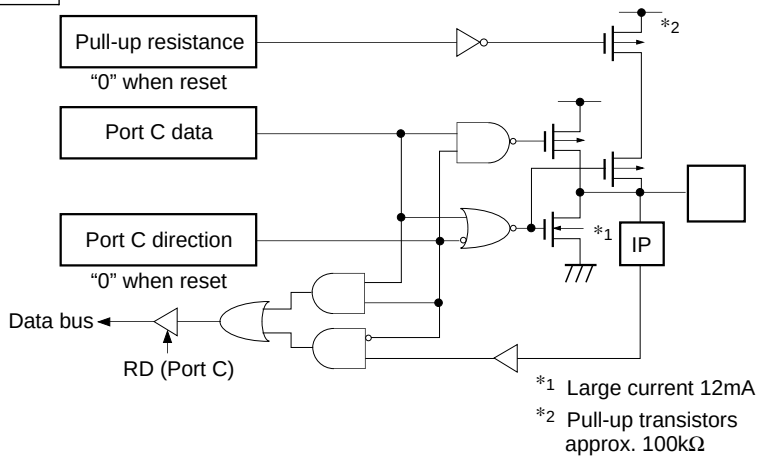
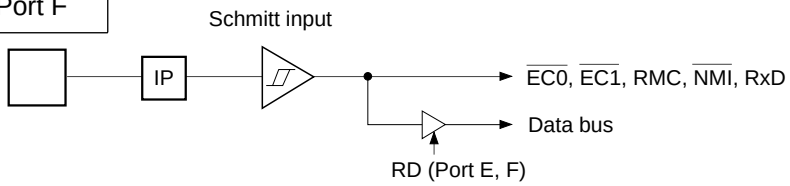
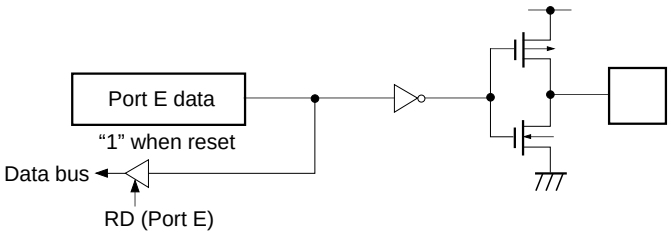
Pin Description

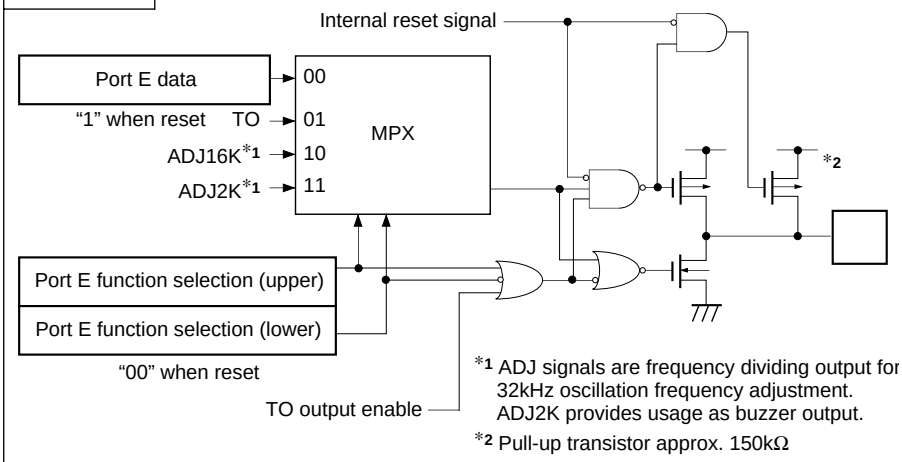
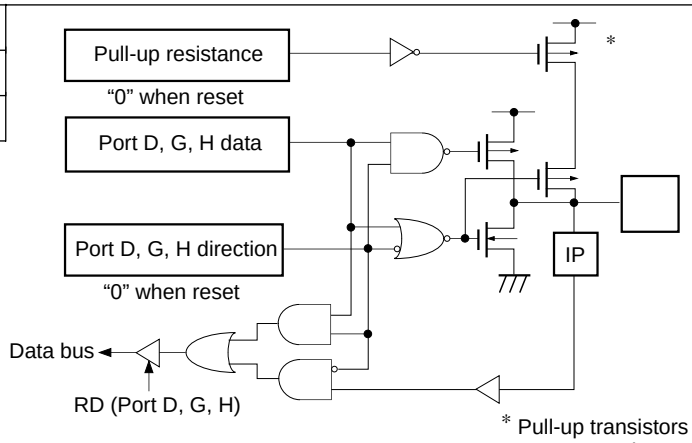
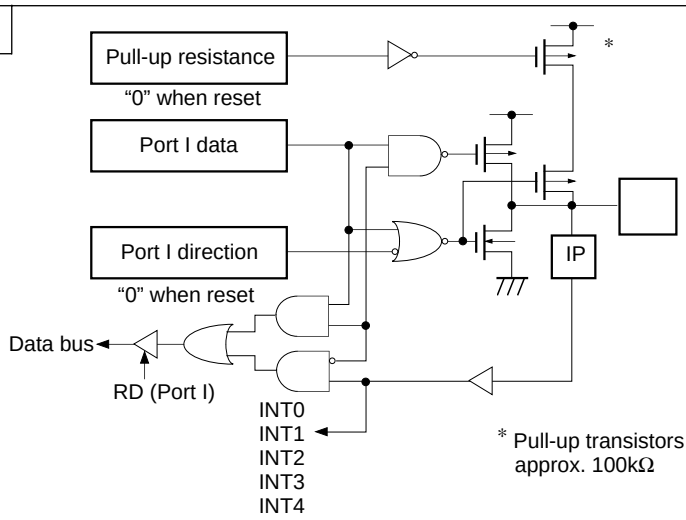
Pin code	I/O	Functions	
PA0/AN0 to PA7/AN7	I/O/Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of signle bits. Incorporation of the pull-up resistance can be set through the software in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (8 pins)
PB0/CINT	I/O/Input	(Port B) I/O can be set in a unit of single bits for lower 7 bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	External capture input to 16-bit timer/counter.
PB1/$\overline{CS0}$	I/O/Input		Chip select input for serial interface (CH0).
PB2/$\overline{SCK0}$	I/O/I/O		Serial clock I/O (CH0).
PB3/SI0	I/O/Input		Serial data input (CH0).
PB4/SO0	I/O/Output		Serial data output (CH0).
PB5/$\overline{SCK1}$	I/O/I/O		Serial clock I/O (CH1).
PB6/SI1	I/O/Input		Serial data input (CH1).
PB7/SO1	I/O/Output		Serial data output (CH1).
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Capable of driving 12mA sync current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PD0 to PD7	I/O	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PE0/$\overline{EC0}$	Input/Input	(Port E) 6-bit port. Lower 4 bits are for inputs; upper 2 bits are for outputs. (6 pins)	External event inputs for timer/counter. (2 pins)
PE1/$\overline{EC1}$	Input/Input		
PE2/RMC	Input/Input		Remote control reception circuit input.
PE3/$\overline{NMI}$	Input/Input		Non-maskable interruption request input.
PE4	Output		
PE5/TO/ ADJ	Output/Output/ Output		Rectangular wave output for 16-bit timer/counter. Output for 32kHz oscillation frequency division.
PF0/SCL0 PF1/SCL1	Output/I/O	(Port F) Lower 7 bits are for output; of which lower 4 bits are large current (12mA) N-ch open drain output. The uppermost bit (PF7) is for input. (8pins)	Transfer clock I/O for I^2C bus interface. (2pins)
PF2/SDA0 PF3/SDA1	Output/I/O		Transfer data I/O for I^2C bus interface. (2pins)
PF4/$\overline{PWM0}$	Output/Output		$\overline{PWM}$ outputs. (2pins)
PF5/$\overline{PWM1}$	Output/Output		
PF6/TxD	Output/Output		UART transmission data output.
PF7/RxD	Input/Input		UART reception data input.

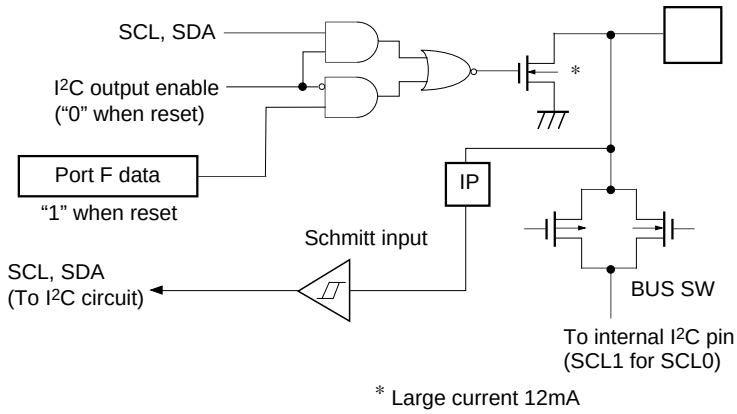
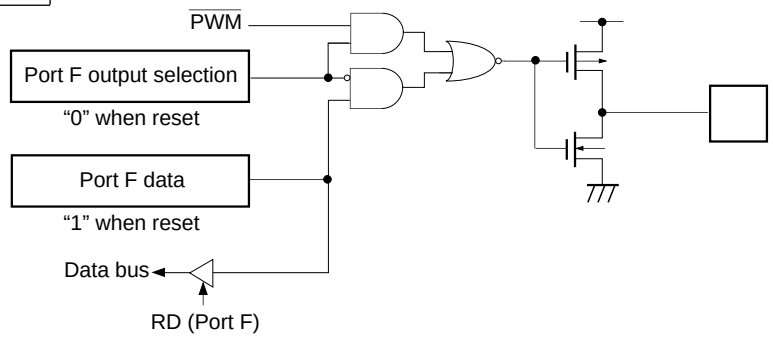
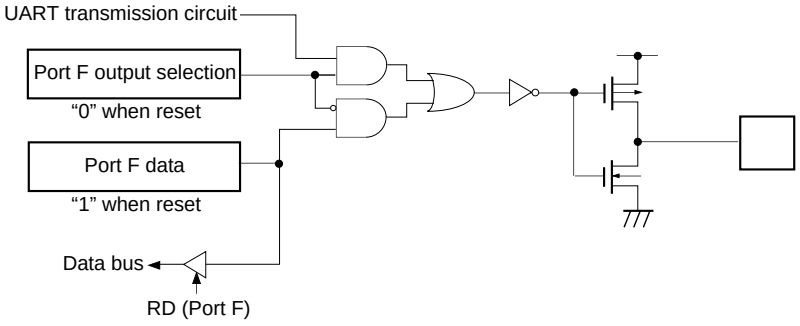
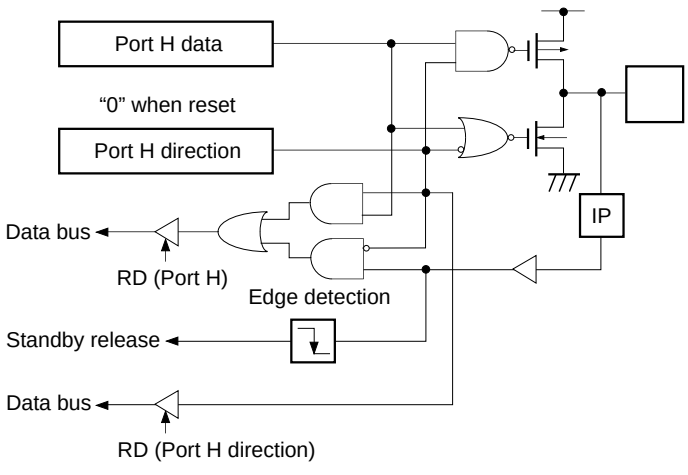
Pin code	I/O	Functions	
PG0 to PG7	I/O	(Port G) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PH0 to PH7	I/O	(Port H) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PI0/INT0 to PI4/INT4	I/O/Input	(Port I) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	External interruption request inputs. (5 pins)
PI5/$\overline{SCK2}$	I/O/I/O		Serial clock I/O. (CH2)
PI6/SI2	I/O/Input		Serial data input. (CH2)
PI7/SO2	I/O/Output		Serial data output. (CH2)
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL	Output		
TEX	Input	Crystal connectors for 32kHz timer/counter clock oscillation. For usage as event counter, input to TEX, and open TX.	
TX	Output		
$\overline{RST}$	Input	Low-level active, system reset.	
Vpp		Positive power supply pin for built-in PROM writing. Connect to V_{DD} for normal operation.	
AV_{REF}	Input	Reference voltage input for A/D converter.	
AVss		A/D converter GND.	
V_{DD}		Positive power supply.	
Vss		GND.	

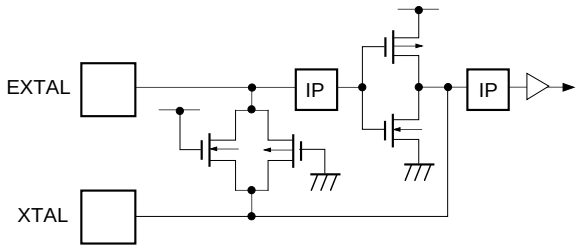
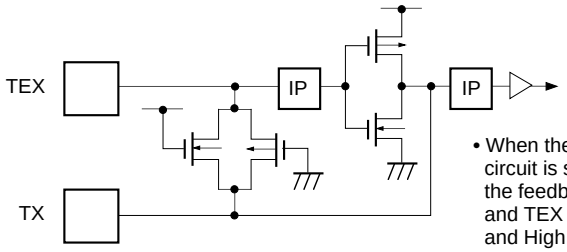
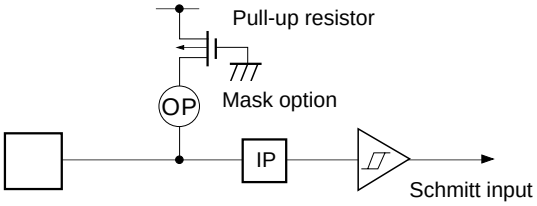
I/O Circuit Format for Pins

Pin	Circuit format	When reset
PA0/AN0 to PA7/AN7 8 pins	Port A Pull-up resistance "0" when reset Port A data Port A direction "0" when reset Data bus RD (Port A) Port A function selection "0" when reset IP Input protection circuit Input multiplexer A/D converter * Pull-up transistors approx. 100kΩ	Hi-Z
PB0/$\overline{\text{CINT}}$ PB1/$\overline{\text{CS0}}$ PB3/SI0 PB6/SI1 PI6/SI2 5 pins	Port B Port I Pull-up resistance "0" when reset Port B, I data Port B, I direction "0" when reset Data bus RD (Port B, I) IP Schmitt input $\overline{\text{CINT}}$ $\overline{\text{CS0}}$ SI0 SI1 * Pull-up transistors approx. 100kΩ	Hi-Z
PB2/$\overline{\text{SCK0}}$ PB5/$\overline{\text{SCK1}}$ PI5/$\overline{\text{SCK2}}$ 3 pins	Port B Port I Pull-up resistance "0" when reset $\overline{\text{SCK}}$ OUT Serial clock output enable Port B, I function selection "0" when reset Port B, I data Port B, I direction "0" when reset Data bus RD (Port B, I) IP Schmitt input $\overline{\text{SCK}}$ in * Pull-up transistors approx. 100kΩ	Hi-Z

Pin	Circuit format	When reset
PB4/SO0 PB7/SO1 PI7/SO2 3 pins	Port B Port I 	Hi-Z
PC0 to PC7 8 pins	Port C 	Hi-Z
PE0/$\overline{EC0}$ PE1/$\overline{EC1}$ PE2/$\overline{RMC}$ PE3/$\overline{NMI}$ PF7/RxD 5 pins	Port E Port F 	Hi-Z
PE4 1 pin	Port E 	High level

Pin	Circuit format	When reset
PE5/TO/ADJ 1 pin	Port E  *1 ADJ signals are frequency dividing output for 32kHz oscillation frequency adjustment. ADJ2K provides usage as buzzer output. *2 Pull-up transistor approx. 150kΩ	High level with approx. 150kΩ resistor when reset
PD0 to PD7 PG0 to PG7 PH0 to PH7 24 pins	Port D Port G Port H  * Pull-up transistors approx. 100kΩ	Hi-Z
PI0/INT0 to PI4/INT4 5 pins	Port I  * Pull-up transistors approx. 100kΩ	Hi-Z

Pin	Circuit format	When reset
PF0/SCL0 PF1/SCL1 PF2/SDA0 PF3/SDA1 4 pins	Port F 	Hi-Z
PF4/$\overline{\text{PWM0}}$ PF5/$\overline{\text{PWM1}}$ 2 pins	Port F 	High level
PF6/TxD 1 pin	Port F 	High level
PH0 to PH7 8 pins	Port H 	Hi-Z

Pin	Circuit format	When reset
EXTAL XTAL 2 pins	 • Diagram shows circuit composition during oscillation. • Feedback resistor is removed during stop, and XTAL becomes High level.	Oscillation
TEX TX 2 pins	 • Diagram shows circuit composition during oscillation. • When the operation of the oscillation circuit is stopped by the software, the feedback resistor is removed, and TEX and TX become Low level and High level respectively.	Oscillation
$\overline{\text{RST}}$ 1 pin		Low level

Absolute Maximum Ratings (Vss = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
	AV_{SS}	–0.3 to +0.3	V	
Input voltagte	V_{IN}	–0.3 to +7.0*1	V	
Output voltage	V_{OUT}	–0.3 to +7.0*1	V	
High level output current	I_{OH}	–5	mA	Output (value per pin)
High level total output current	$\sum I_{OH}$	–50	mA	Total for all output pins
Low level output current	I_{OL}	15	mA	All pins excluding large current outputs (value per pin)
	I_{OLC}	20	mA	Large current outputs (value per pin) *2
Low level total output current	$\sum I_{OL}$	100	mA	Total for all output pins
Operating temperature	Topr	–10 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	

*1 V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*2 The large current output is for each pin of Port C (PC), Port F0 (PF0) to Port 3 (PF3).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks	
Supply voltage	V_{DD}	4.5	5.5	V	fc = 16MHz or less	Guaranteed operation range for 1/2 and 1/4 frequency dividing clock.
		3.0	5.5	V	fc = 12MHz or less	
		2.7	5.5	V	Guaranteed operation range for 1/16 frequency dividing clock or SLEEP mode	
		2.7	5.5	V	Guaranteed operation range by TEX clock	
		2.5	5.5	V	Guaranteed data hold operation range during STOP	
HIgh level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	*1, *5	
		0.8V_{DD}	V_{DD}	V	*1, *6	
	V_{IHS}	0.8V_{DD}	V_{DD}	V	Hysteresis input*2	
	V_{IHEX}	V_{DD} – 0.4	V_{DD} + 0.3	V	EXTAL pin*3, *5 TEX pin*4, *5	
		V_{DD} – 0.2	V_{DD} + 0.2	V	EXTAL pin*3, *6 TEX pin*4, *6	
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	*1, *5	
		0	0.2V_{DD}	V	*1, *6	
	V_{ILS}	0	0.2V_{DD}	V	Hysteresis input*2	
	V_{ILEX}	–0.3	0.4	V	EXTAL pin*3, *5 TEX pin*4, *5	
		–0.3	0.2	V	EXTAL pin*3, *6 TEX pin*4, *6	
Operating temperature	Topr	–10	+75	°C		

*1 Normal input port (each pin of PA, PB4, PB7, PC, PF0 to PF4, PG, PH and PI7)

*2 Each pin of $\overline{RST}$, CINT, $\overline{CS0}$, $\overline{SCK0}$, $\overline{SCK1}$, $\overline{SCK2}$, SI0, SI1, SI2, $\overline{EC0}$, $\overline{EC1}$, RMC, $\overline{NMI}$, RxD, INT0, INT1, INT2, INT3 and INT4

*3 It is specified only when the external clock is input.

*4 It is specified only when the external event count clock is input.

*5 This case applies to the range of 4.5 to 5.5V supply voltage (V_{DD}).

*6 This case applies to the range of 3.0 to 5.5V supply voltage (V_{DD}).

Electrical Characteristics

DC Characteristics

Supply voltage (V_{DD}) 4.5 to 5.5V (Ta = –10 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE4, PE5, PF4, PF5, PF6, PG to PI	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output voltage	V_{OL}		V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PC, PF0 to PF3	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
		PF0 to PF3 (SCL0, SCL1, SDA0, SDA1)	V_{DD} = 4.5V, I_{OL} = 3.0mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 4.0mA			0.6	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{IHT}	TEX	V_{DD} = 5.5V, V_{IL} = 5.5V	0.1		10	µA
	I_{ILT}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$*1	V_{DD} = 5.5V, V_{IL} = 0.4V	–1.5		–400	µA
	I_{IL}	PA to PD*2, PG to PI*2				–45	µA
			V_{DD} = 4.5V, V_{IL} = 4.0V	–2.78			µA
I/O lealage current	I_{IZ}	PA to PD*2, PG to PI*2, $\overline{RST}$*1	V_{DD} = 5.5V V_I = 0, 5.5V			±10	µA
Open drain output leakage current (N-ch Tr off state)	I_{LOH}	PF0 to PF3 (SCL0, SCL1, SDA0, SDA1)	V_{DD} = 5.5V V_{OH} = 5.5V			10	µA
I^2C bus switch connection impedance (Output Tr off state)	R_{BS}	SCL0: SCL1 SDA0: SDA1	V_{DD} = 4.5V V_{SCL0} = V_{SCL1} = 2.25V V_{SDA0} = V_{SDA1} = 2.25V			120	Ω

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Supply current*3	I_{DD1}	V_{DD}	1/2 frequency dividing clock operation V_{DD} = 5.5V, 16MHz crystal oscillation (C_1 = C_2 = 15pF)		31	50	mA
	I_{DD2}		V_{DD} = 3V, 32kHz crystal oscillation; and termination of 16MHz oscillation (C_1 = C_2 = 47pF)		0.6	1.2	mA
	I_{DDS1}		SLEEP mode V_{DD} = 5.5V, 16MHz crystal oscillation (C_1 = C_2 = 15pF)		2.5	10	mA
	I_{DDS2}		V_{DD} = 3V, 32kHz crystal oscillation; and termination of 16MHz oscillation (C_1 = C_2 = 47pF)		8	30	µA
	I_{DDS3}		STOP mode V_{DD} = 5.5V, termination of 16MHz and 32kHz crystal oscillation			30	µA
Input capacity	C_{IN}	PA to PC, PE0 to PE5, PF to PI, EXTAL, TEX, $\overline{RST}$	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1 $\overline{RST}$ specifies the input current when pull-up resistance has been selected; leakage current when no resistance has been selected.

*2 PA to PD, and PG to PI specify the input current when pull-up resistance has been selected; leakage current when no resistance has been selected.

*3 When all pins are open.

Electrical Characteristics

DC Characteristics

Supply voltage (V_{DD}) 3.0 to 3.6V (Ta = –10 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE4, PE5, PF4, PF5, PF6	V_{DD} = 3.0V, I_{OH} = –0.15mA	2.7			V
			V_{DD} = 3.0V, I_{OH} = –0.5mA	2.3			V
Low level output voltage	V_{OL}		V_{DD} = 3.0V, I_{OL} = 1.2mA			0.3	V
			V_{DD} = 3.0V, I_{OL} = 1.6mA			0.5	V
		PC, PF0 to PF3	V_{DD} = 3.0V, I_{OL} = 5.0mA			1	V
		PF0 to PF3 (SCL0, SCL1, SDA0, SDA1)	V_{DD} = 3.0V, I_{OL} = 2.0mA			0.3	V
			V_{DD} = 3.0V, I_{OL} = 2.5mA			0.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 3.6V, V_{IH} = 3.6V	0.3		20	µA
	I_{ILE}		V_{DD} = 3.6V, V_{IL} = 0.3V	–0.3		–20	µA
	I_{IHT}	TEX	V_{DD} = 3.6V, V_{IL} = 3.6V	0.1		10	µA
	I_{ILT}		V_{DD} = 3.6V, V_{IL} = 0.4V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$*1	V_{DD} = 3.6V, V_{IL} = 0.3V	–0.9		–200	µA
	I_{IL}	PA to PD*2, PG to PI*2				–20	µA
			V_{DD} = 3.0V, V_{IL} = 2.7V	–1.0			µA
I/O lealage current	I_{IZ}	PA to PD*2, PG to PI*2, $\overline{RST}$*1	V_{DD} = 3.6V V_I = 0, 3.6V			±10	µA
Open drain output leakage current (N-ch Tr off state)	I_{LOH}	PF0 to PF3 (SCL0, SCL1, SDA0, SDA1)	V_{DD} = 3.6V V_{OH} = 3.6V			10	µA
I^2C bus switch connection impedance (Output Tr off state)	R_{BS}	SCL0: SCL1 SDA0: SDA1	V_{DD} = 3.0V V_{SCL0} = V_{SCL1} = 1.5V V_{SDA0} = V_{SDA1} = 1.5V			300	Ω

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Supply current*3	I_{DD1}	V_{DD}	1/2 frequency dividing clock operation V_{DD} = 3.6V, 12MHz crystal oscillation (C_1 = C_2 = 15pF)		11	25	mA
	I_{DDS1}		SLEEP mode V_{DD} = 3.6V, 12MHz crystal oscillation (C_1 = C_2 = 15pF)		0.5	2.5	mA
	I_{DDS3}		STOP mode V_{DD} = 3.6V, termination of 16MHz and 32kHz crystal oscillation			20	µA
Input capacity	C_{IN}	PA to PC, PE0 to PE5, PF to PI, EXTAL, TEX, $\overline{RST}$	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1 $\overline{RST}$ specifies the input current when pull-up resistance has been selected; leakage current when no resistance has been selected.

*2 PA to PD, and PG to PI specify the input current when pull-up resistance has been selected; leakage current when no resistance has been selected.

*3 When all pins are open.

AC Characteristics

(1) Clock timing

(Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2 V_{DD} = 4.5 to 5.5V	1		16	MHz
				1		12	
System clock input pulse width	t_{XL} t_{XH}	EXTAL	Fig. 1, Fig. 2 V_{DD} = 4.5 to 5.5V	28			ns
			External clock drive	37.5			
System clock input rise time, fall time	t_{CR} t_{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	t_{EH} t_{EL}	$\overline{EC0}$ EC1	Fig. 3	4tsys*1			ns
Event count input clock rise time, fall time	t_{ER} t_{EF}	$\overline{EC0}$ EC1	Fig. 3			20	ms
System clock frequency	f_C	TEX TX	V_{DD} = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count input clock input pulse width	t_{TL} t_{TH}	TEX	Fig. 3	10			µs
Event count input clock rise time, fall time	t_{TR} t_{TF}	TEX	Fig. 3			20	ms

*1 tsys indicates the three values below according to the upper two bits (CPU clock selection) of the control clock register (CLC: 00FE$_H$).

tsys [ns] = 2000/fc (upper two bits = “00”), 4000/fc (upper two bits = “01”), 16000/fc (Upper two bits = “11”)

Fig. 1. Clock timing

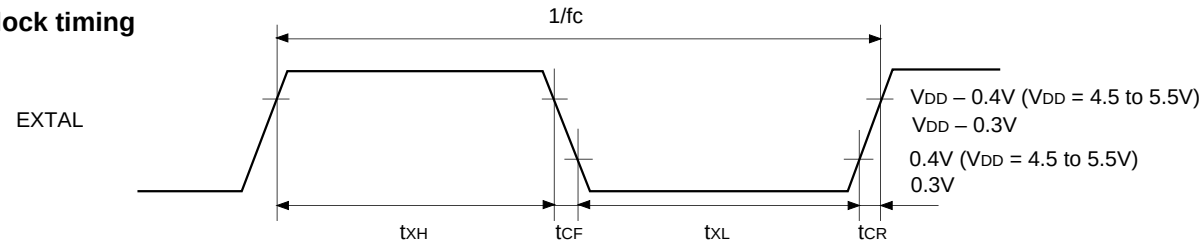


Fig. 2. Clock applied conditions

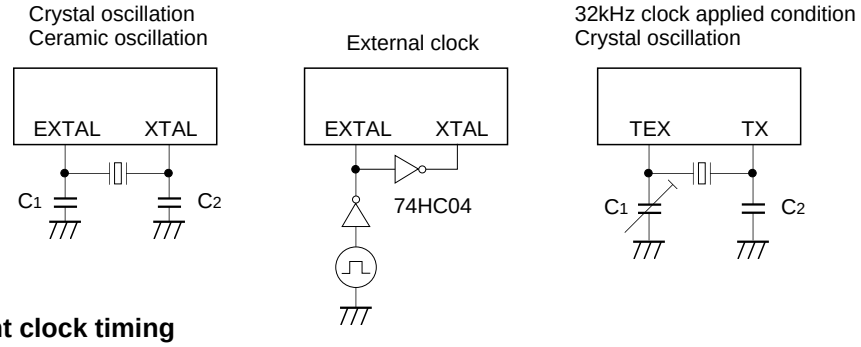
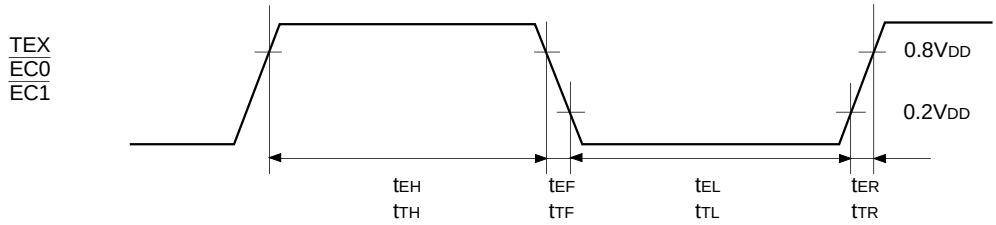


Fig. 3. Event count clock timing



(2) Serial transfer (CH0) (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS}\downarrow \rightarrow \overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		tsys + 200	ns
$\overline{CS}\uparrow \rightarrow \overline{SCK}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		tsys + 200	ns
$\overline{CS}\downarrow \rightarrow$ SO delay time	t_{DCSO}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS}\downarrow \rightarrow$ SO floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS}$ High level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK}$ High and Low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys + 100		ns
			Output mode	8000/fc – 100		ns
SI input setup time (against $\overline{SCK}\uparrow$)	t_{SIK}	SI0	$\overline{SCK}$ input mode	–tsys + 100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (against $\overline{SCK}\uparrow$)	t_{KSI}	SI0	$\overline{SCK}$ input mode	2tsys + 100		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK}\downarrow \rightarrow$ SO delay time	t_{KSO}	SO0	$\overline{SCK}$ input mode		2tsys + 200	ns
			$\overline{SCK}$ output mode		100	ns

Note 1) tsys indicates three values according to the contents of the clock control register (CLC; $00FE_H$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (upper 2 bits = “00”), 4000/fc (upper 2 bits = “01”), 16000/fc (upper 2 bits = “11”)

Note 2) $\overline{CS}$, $\overline{SCK}$, SI and SO represent $\overline{CS0}$, $\overline{SCK0}$, SI0 and SO0, respectively.

Note 3) The load of $\overline{SCK}$ output mode and SO output delay time is 50pF + 1TTL.

Serial transfer (CH0) (Ta = –10 to +75°C, V_{DD} = 3.0 to 3.6V, Vss = 0V reference)

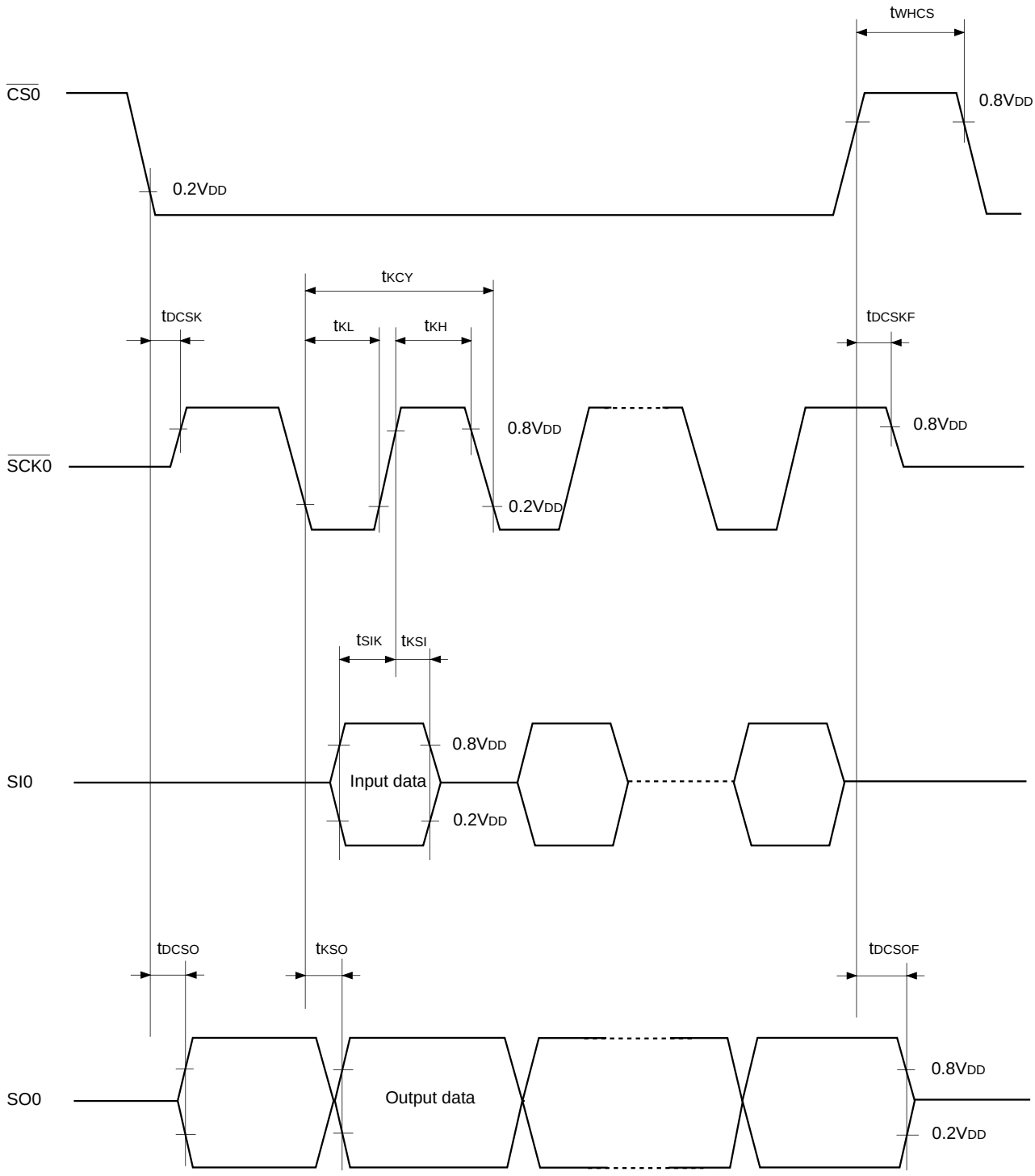
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS}\downarrow \rightarrow \overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		tsys + 250	ns
$\overline{CS}\uparrow \rightarrow \overline{SCK}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		tsys + 200	ns
$\overline{CS}\downarrow \rightarrow$ SO delay time	t_{DCSO}	SO0	Chip select transfer mode		tsys + 250	ns
$\overline{CS}\downarrow \rightarrow$ SO floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS}$ High level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK}$ High and Low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys + 100		ns
			Output mode	8000/fc – 150		ns
SI input setup time (against $\overline{SCK}\uparrow$)	t_{SIK}	SI0	$\overline{SCK}$ input mode	–tsys + 100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (against $\overline{SCK}\uparrow$)	t_{KSI}	SI0	$\overline{SCK}$ input mode	2tsys + 100		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK}\downarrow \rightarrow$ SO delay time	t_{KSO}	SO0	$\overline{SCK}$ input mode		2tsys + 250	ns
			$\overline{SCK}$ output mode		125	ns

Note 1) tsys indicates three values according to the contents of the clock control register (CLC; 00FE$_H$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (upper 2 bits = “00”), 4000/fc (upper 2 bits = “01”), 16000/fc (upper 2 bits = “11”)

Note 2) $\overline{CS}$, $\overline{SCK}$, SI and SO represent $\overline{CS0}$, $\overline{SCK0}$, SI0 and SO0, respectively.

Note 3) The load of $\overline{SCK}$ output mode and SO output delay time is 50pF.

Fig. 4. Serial transfer CH0 timing



Serial transfer (CH1, CH2) (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK1}$ $\overline{SCK2}$	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK}$ High and Low level widths	t_{KH} t_{KL}	$\overline{SCK1}$ $\overline{SCK2}$	Input mode	tsys + 100		ns
			Output mode	8000/fc – 50		ns
SI input setup time (against $\overline{SCK}\uparrow$)	t_{SIK}	SI1 SI2	$\overline{SCK}$ input mode	100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (against $\overline{SCK}\uparrow$)	t_{KSI}	SI1 SI2	$\overline{SCK}$ input mode	tsys + 200		ns
			$\overline{SCK}$ output mode	100		ns
SCK$\downarrow \rightarrow$ SO delay time	t_{KSO}	SO1 SO2	$\overline{SCK}$ input mode		tsys + 200	ns
			$\overline{SCK}$ output mode		100	ns

Note 1) tsys indicates three values according to the contents of the clock control register (CLC; $00FE_H$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2 bits = “00”), 4000/fc (Upper 2 bits = “01”), 16000/fc (Upper 2 bits = “11”)

Note 2) $\overline{SCK}$, SI and SO represent $\overline{SCK1}$, SI1, and SO1, respectively for CH1; they represent $\overline{SCK2}$, SI2 and SO2, respectively for CH2.

Note 3) The load of $\overline{SCK1}$ and $\overline{SCK2}$ output modes and SO1 and SO2 output delay times is 50pF+1TTL.

Serial transfer (CH1, CH2) (Ta = –10 to +75°C, V_{DD} = 3.0 to 3.6V, Vss = 0V reference)

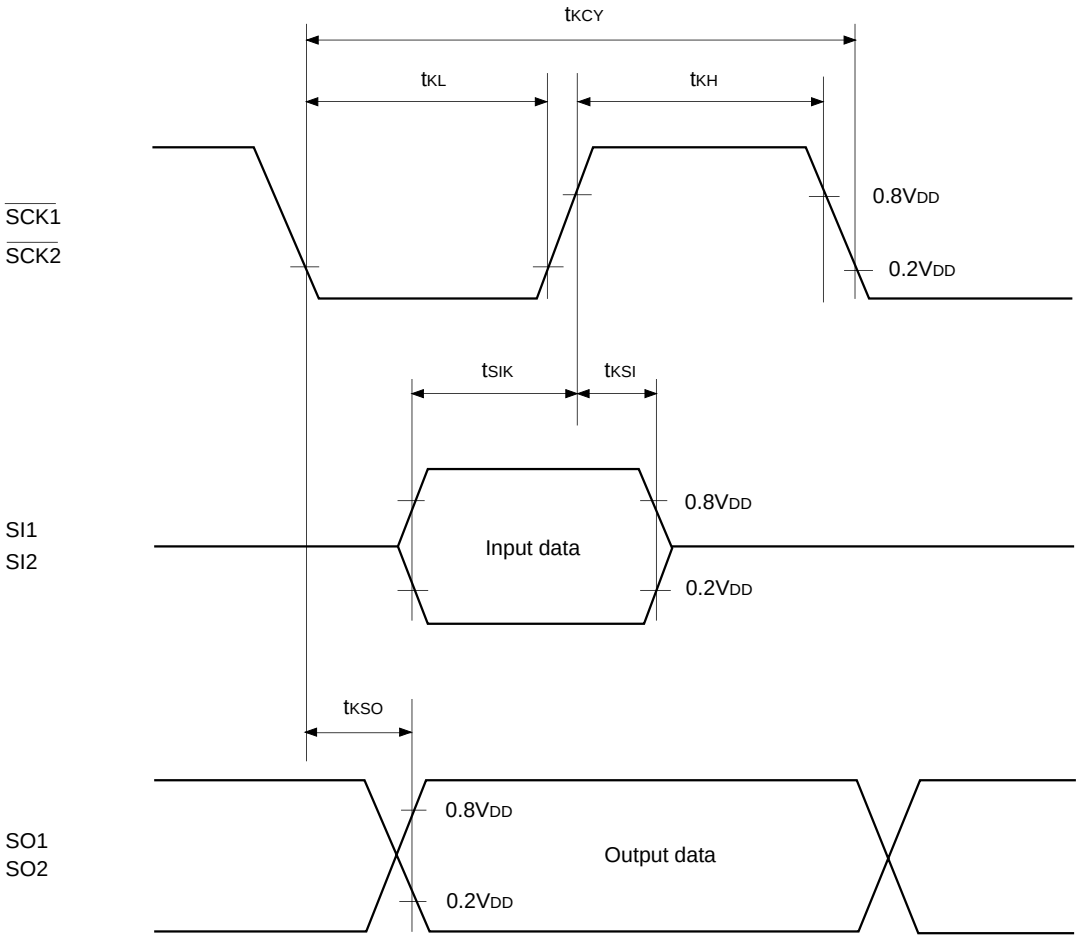
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK1}$ $\overline{SCK2}$	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK}$ High and Low level widths	t_{KH} t_{KL}	$\overline{SCK1}$ $\overline{SCK2}$	Input mode	tsys + 100		ns
			Output mode	8000/fc – 150		ns
SI input setup time (against $\overline{SCK}\uparrow$)	t_{SIK}	SI1 SI2	$\overline{SCK}$ input mode	100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (against $\overline{SCK}\uparrow$)	t_{KSI}	SI1 SI2	$\overline{SCK}$ input mode	tsys + 200		ns
			$\overline{SCK}$ output mode	100		ns
SCK$\downarrow \rightarrow$ SO delay time	t_{KSO}	SO1 SO2	$\overline{SCK}$ input mode		tsys + 250	ns
			$\overline{SCK}$ output mode		125	ns

Note 1) tsys indicates three values according to the contents of the clock control register (CLC; $00FE_H$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2 bits = “00”), 4000/fc (Upper 2 bits = “01”), 16000/fc (Upper 2 bits = “11”)

Note 2) $\overline{SCK}$, SI and SO represent $\overline{SCK1}$, SI1, and SO1, respectively for CH1; they represent $\overline{SCK2}$, SI2 and SO2, respectively for CH2.

Note 3) The load of $\overline{SCK1}$ and $\overline{SCK2}$ output modes and SO1 and SO2 output delay times is 50pF.

Fig. 5. Serial transfer CH1 and CH2 timing

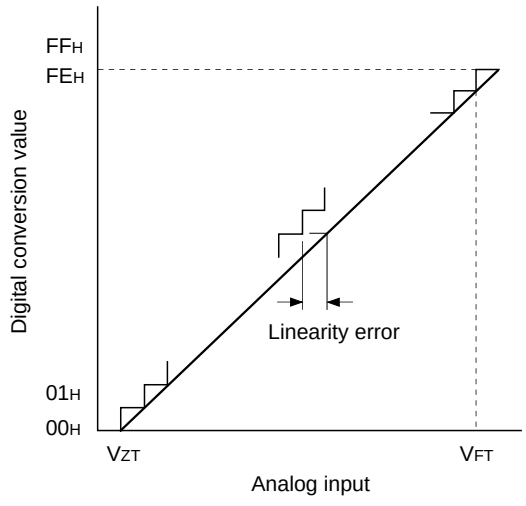


(3) A/D converter characteristics

(Ta = –10 to +75°C, V_{DD} = 3.0 to 5.5V, AV_{REF} = 2.7 to V_{DD}, Vss = AV_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity errror			Ta = 25°C V_{DD} = AV_{REF} = 5.0V V_{SS} = AV_{SS} = 0V			±3	LSB
Zero transition voltage	V_{ZT}*1			–50	10	70	mV
Full-scale transition voltage	V_{FT}*2			4910	4970	5030	mV
Linearity errror			Ta = 25°C V_{DD} = AV_{REF} = 3.3V V_{SS} = AV_{SS} = 0V			±5	LSB
Zero transition voltage	V_{ZT}*1			–10	6.5	110	mV
Full-scale transition voltage	V_{FT}*2			4870	3280	5070	mV
Convertion time	t_{CONV}			160/f_{ADC}*3			µs
Sampling time	t_{SAMP}			12/f_{ADC}*3			µs
Reference input voltage	V_{REF}	AV_{REF}	V_{DD} = 4.5 to 5.5V	V_{DD} – 0.5		V_{DD}	V
			V_{DD} = 3.0 to 3.6V	V_{DD} – 0.3		V_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN7		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operation mode, V_{DD} = 5.5V		0.6	1.0	mA
			Operation mode, V_{DD} = 3.6V		0.4	0.7	mA
	I_{REFS}		SLEEP mode STOP mode 32kHz operation mode			10	µA

Fig.6. Definition of A/D converter terms



*1 V_{ZT}: Value at which the digital conversion value changes from 00H to 01H and vice versa.

*2 V_{FT}: Value at which the digital conversion value changes from FEH to FFH and vice versa.

*3 f_{ADC} indicates the below values due to the contents of bit 6 (CKS) of the A/D control register (ADC: 00F9H) and bits 7 (PCK1) and 6 (PCK0) of the clock control register (CLC: 00FEH).

CKS / PCK1, PCK0	0(ϕ/2 selection)	1(ϕ selection)
00 (ϕ = f_{EX}/2)	f_{ADC} = f_C/2	f_{ADC} = f_C
01 (ϕ = f_{EX}/4)	f_{ADC} = f_C/4	f_{ADC} = f_C/2
11 (ϕ = f_{EX}/16)	f_{ADC} = f_C/16	f_{ADC} = f_C/8

(4) Interruption, reset input (Ta = –10 to +75°C, V_{DD} = 3.0 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption HIgh, Low level width	t_{IH} t_{IL}	INT0 INT1 INT2 INT3 INT4 $\overline{NMI}$		1		µs
Reset input Low level width	t_{RSL}	$\overline{RST}$		32/fc		µs

Fig. 7. Interruption input timing

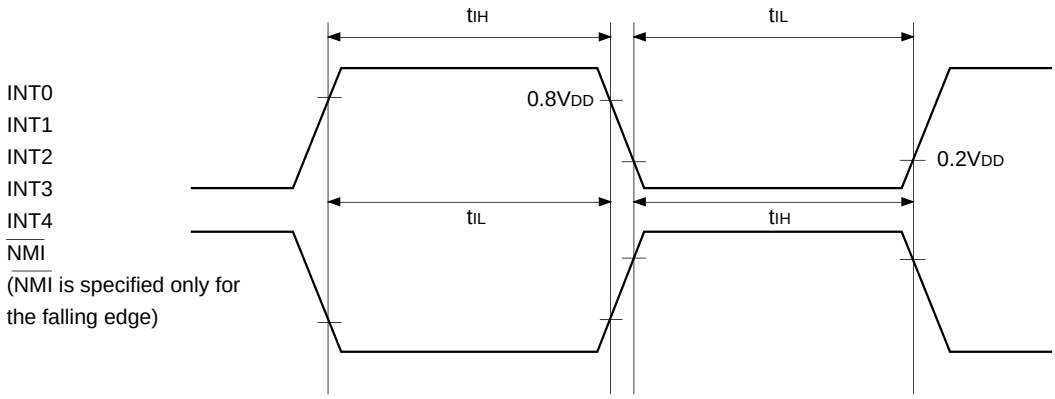
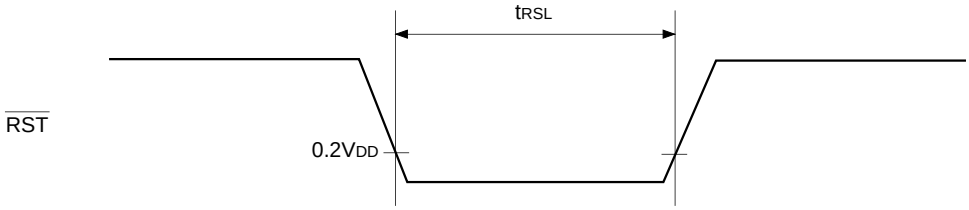


Fig. 8. $\overline{RST}$ input timing



(5) I²C bus timing (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
SCL clock frequency	f_{SLC}	SCL		0	100	kHz
Bus-free time before starting transfer	t_{BUF}	SDA, SCL		4.7		µs
Hold time for starting transfer	$t_{HD;\,STA}$	SDA, SCL		4.0		µs
Clock Low level width	t_{LOW}	SCL		4.7		µs
Clock High level width	t_{HIGH}	SCL		4.0		µs
Setup time for repetitive transfers	$t_{SU;\,STA}$	SDA, SCL		4.7		µs
Data bold time	$t_{HD;\,DAT}$	SDA, SCL		0*1		µs
Data setup time	$t_{SU;\,DAT}$	SDA, SCL		250		ns
SDA, SCL rise time	t_R	SDA, SCL			1	µs
SDA, SCL fall time	t_F	SDA, SCL			300	ns
Setup time for transfer completion	$t_{SU;\,STO}$	SDA, SCL		4.7		µs

*1 The data hold time must exceed 300ns because the SCL rise time (300ns max.) is not taken into consideration.

Fig. 9. I²C bus transfer timing

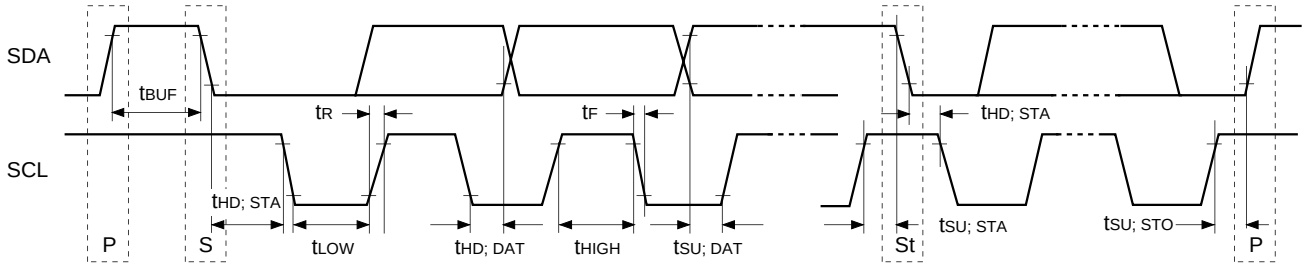
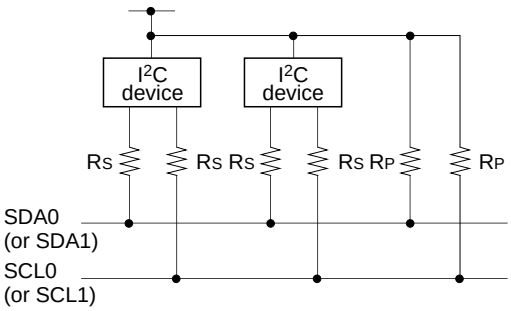


Fig. 10. Recommended circuit example for I²C device



- Pull-up resistors (R_P) must be connected to SDA0 (or SDA1) and SCL0 (or SCL1).
- Serial resistance (Rs = 300Ω or less) of SDA0 (or SDA1) and SCL0 (or SCL1) reduces spike noise caused by CRT flash-over.

Appendix

Fig. 11. SPC700 Series recommended oscillation circuit

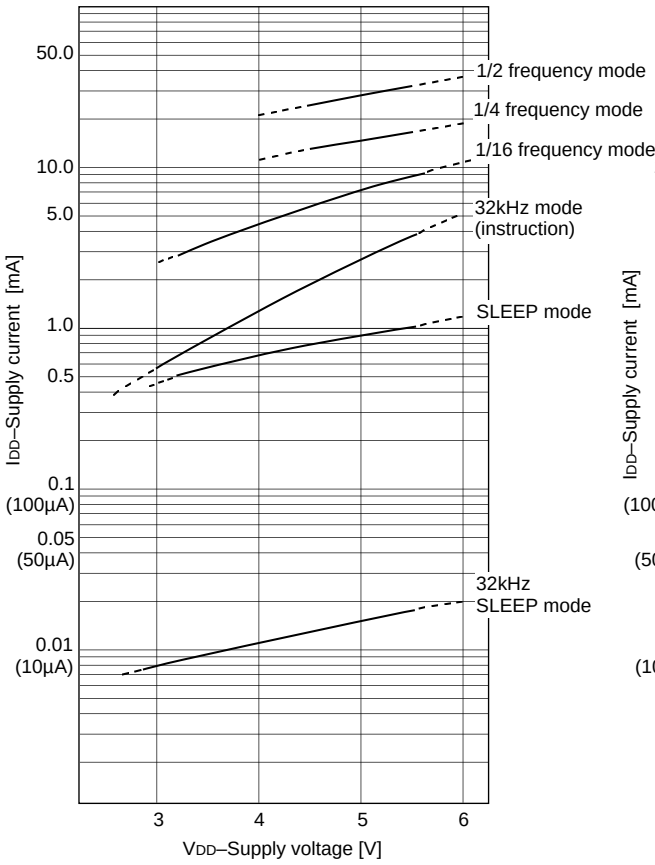
Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00	5	5		
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16 (12)	16 (12)	0	(i)
		10.00	16 (12)	16 (12)		
		12.00	12	12	0	
		16.00	12	12	0	
	P3	32.768kHz	30	18	470k	(ii)

Mask option table

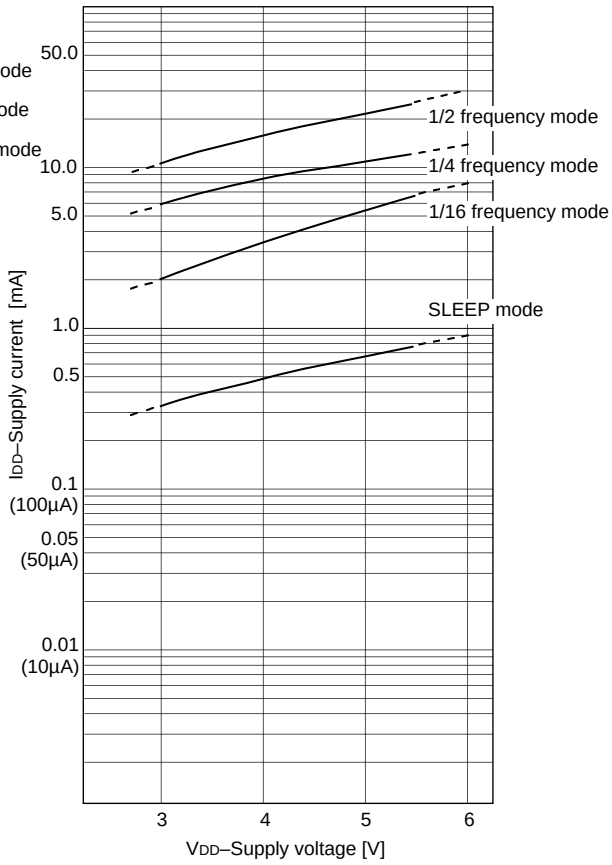
Option item	Mask	CXP846P48-1-□□□
Package	80-pin plastic QFP	80-pin plastic QFP
ROM capacity	32K/40K/48K bytes	PROM 48K bytes
Reset pin pull-up resistance	Existent/Non-existent	Existent

Characteristics Curve

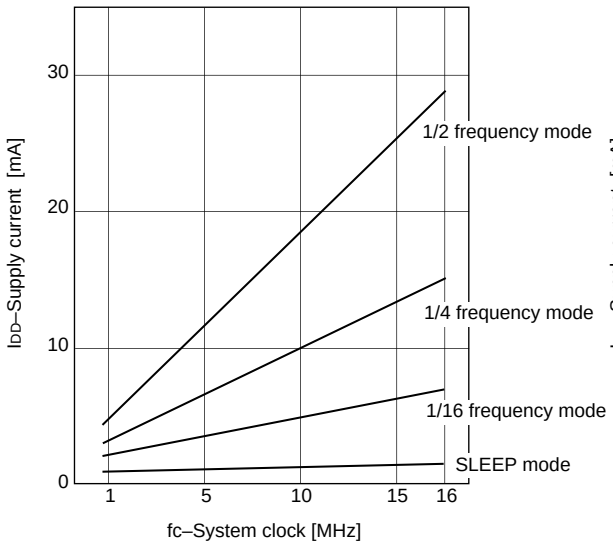
IDD vs. VDD
(fc = 16MHz, Ta = 25°C, Typical)



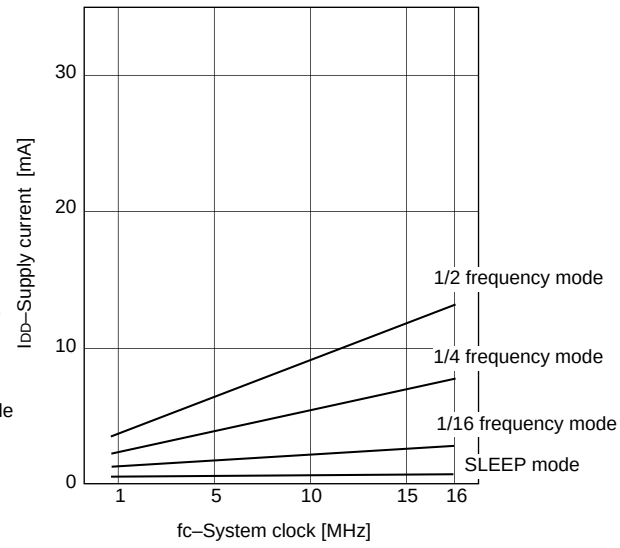
IDD vs. VDD
(fc = 12MHz, Ta = 25°C, Typical)



IDD vs. fc
(VDD = 5.0V, Ta = 25°C, Typical)



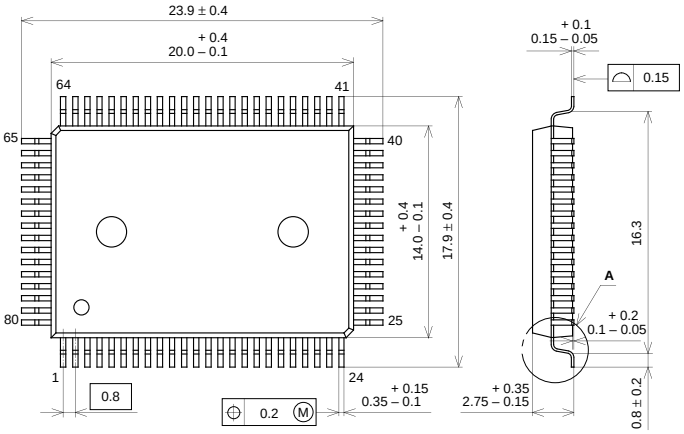
IDD vs. fc
(VDD = 3.3V, Ta = 25°C, Typical)

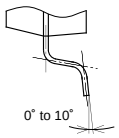


Package Outline

Unit: mm

80PIN QFP (PLASTIC)





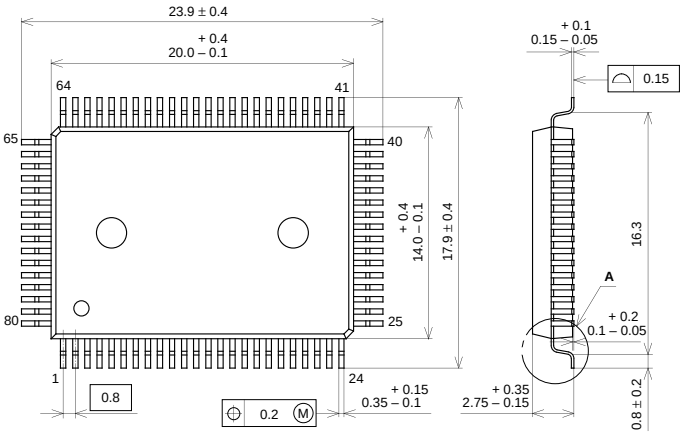
DETAIL **A**

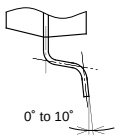
SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g

80PIN QFP (PLASTIC)





DETAIL **A**

SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18µm

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