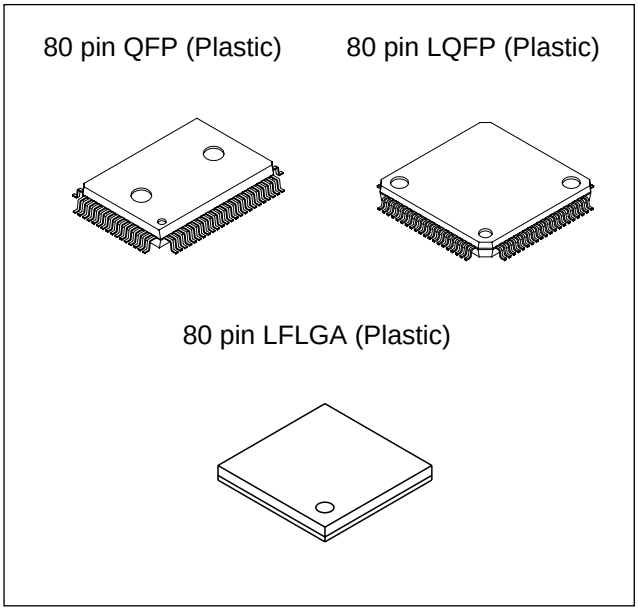
SONY

CXP84540/84548

CMOS 8-bit Single Chip Microcomputer



Description

The CXP84540/84548 is a CMOS 8-bit microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time-base timer, capture timer/counter, PWM output and the like besides the basic configurations of 8-bit CPU, ROM, RAM and I/O port.

The CXP84540/84548 also provide a sleep/stop functions that enable to execute the power-on reset function or lower the power consumption.

Features

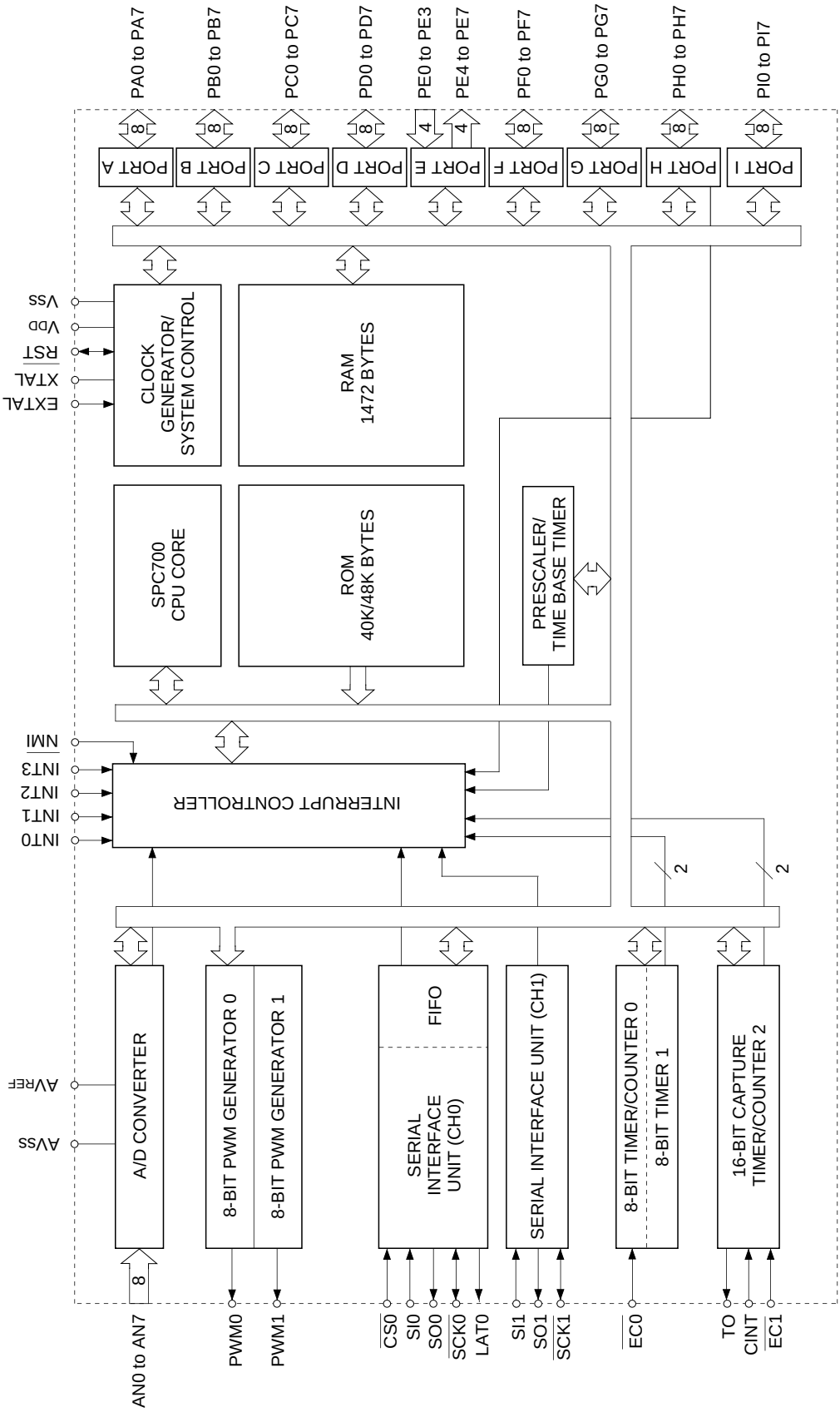
- Wide range instruction system (213 instructions) which covers various of data
  - — 16-bit arithmetic/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle — 143ns at 28MHz operation (4.5 to 5.5V)
  200ns at 20kHz operation (3.0 to 5.5V)
- Incorporated ROM capacity — 40K bytes (CXP84540)
  48K bytes (CXP84548)
- Incorporated RAM capacity — 1472 bytes
- Peripheral functions
  - — A/D converter — 8 bits, 8 channels, successive approximation method (Conversion time of 1.93µs / at 28MHz, 2.7µs / at 20MHz)
  - — Serial interface — Incorporated 8-bit, 8-stage FIFO (Auto transfer for 1 to 8 bytes, latch output function, MSB/LSB first selectable), 1 channel
    8-bit clock syncronization, 1 channel
  - — Timer — 8-bit timer
    8-bit timer/counter
    19-bit time-base timer
    16-bit capture time/counter
  - — PWM output — 8 bits, 2 channels
- Interruption — 14 factors, 14 vectors, multi-interruption possible
- Standby mode — Sleep/Stop
- Package — 80-pin plastic QFP/LQFP
  80-pin plastic LFLGA
- Piggyback/evaluator — CXP84500

Structure

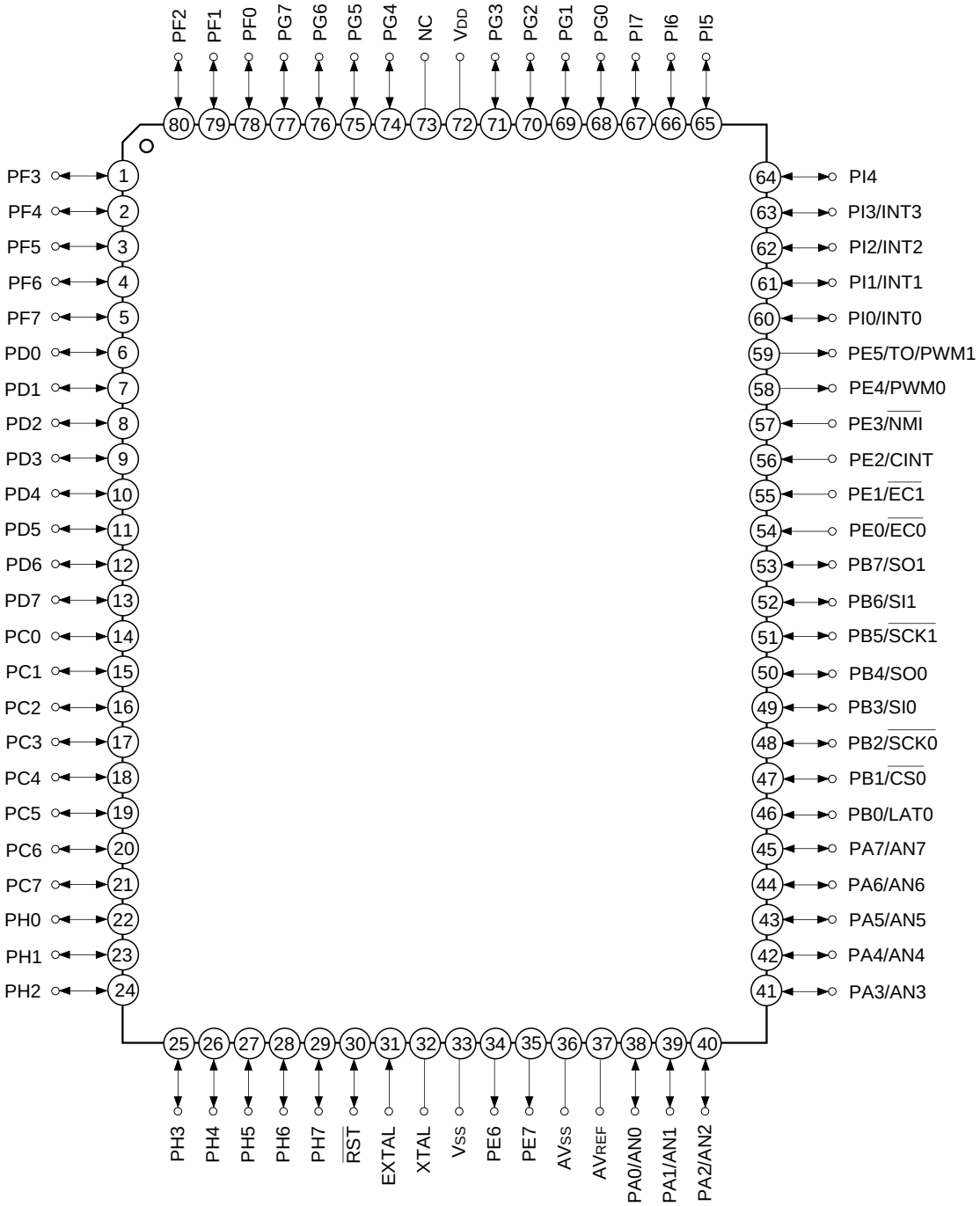
Silicon gate CMOS IC

E96528C15-PS

Block Diagram

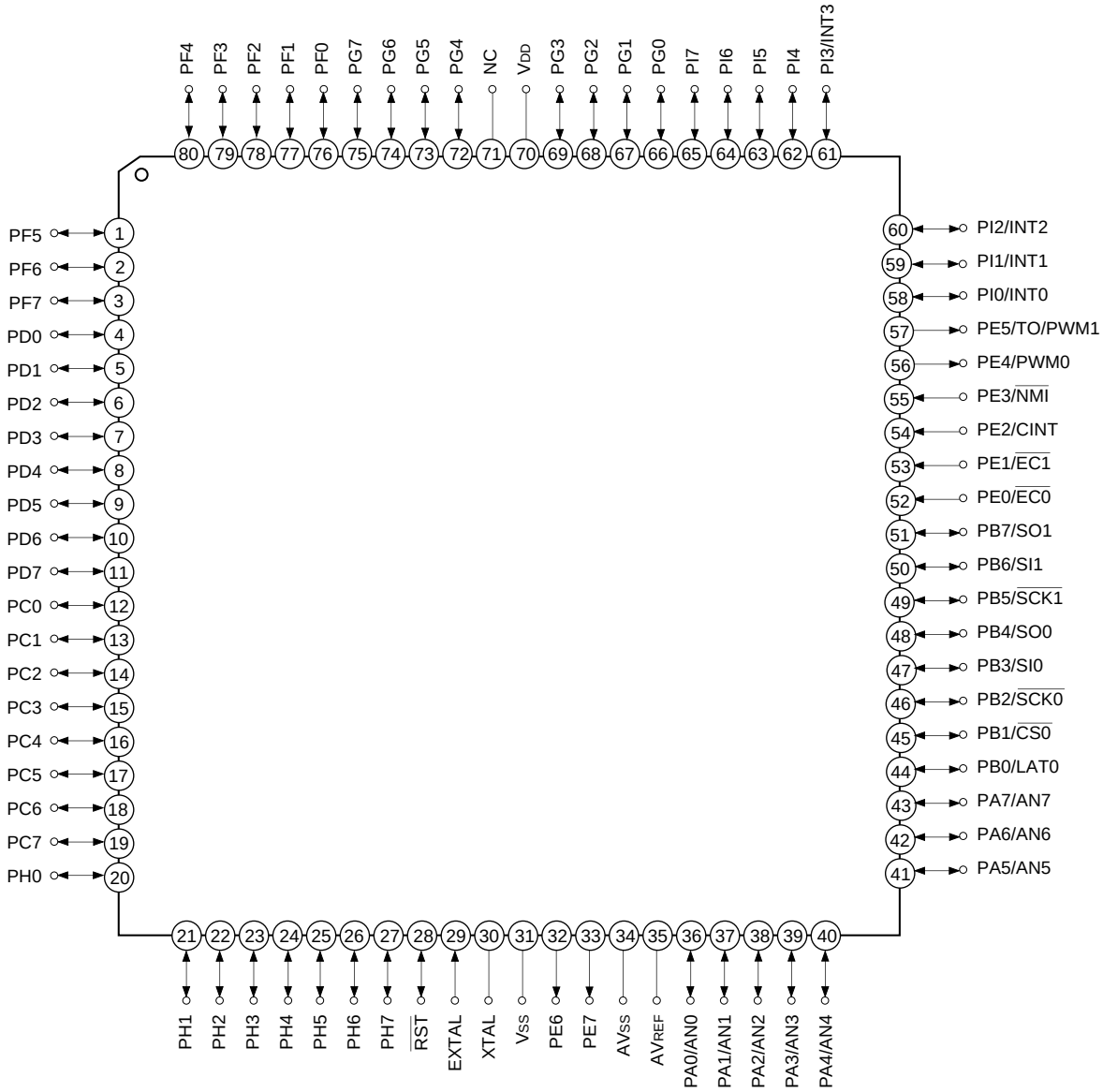


Pin Assignment (Top View) 80-pin QFP package



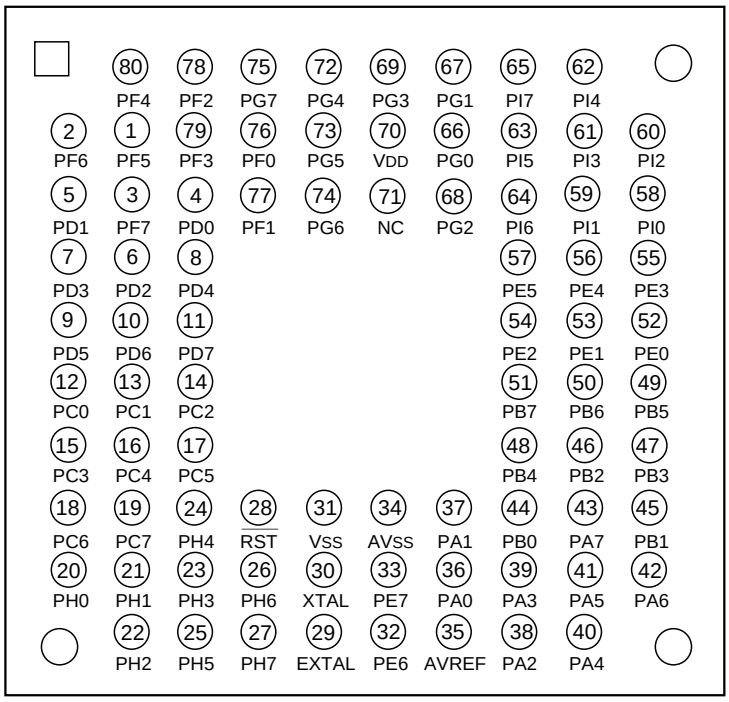
Note) NC (Pin 73) is left open. However, this pin is used for the Flash EEPROM incorporated version (CXP845F60).

Pin Assignment (Top View) 80-pin LQFP package



Note) NC (Pin 73) is left open.

Pin Assignment (Top View) 80-pin LFLGA package



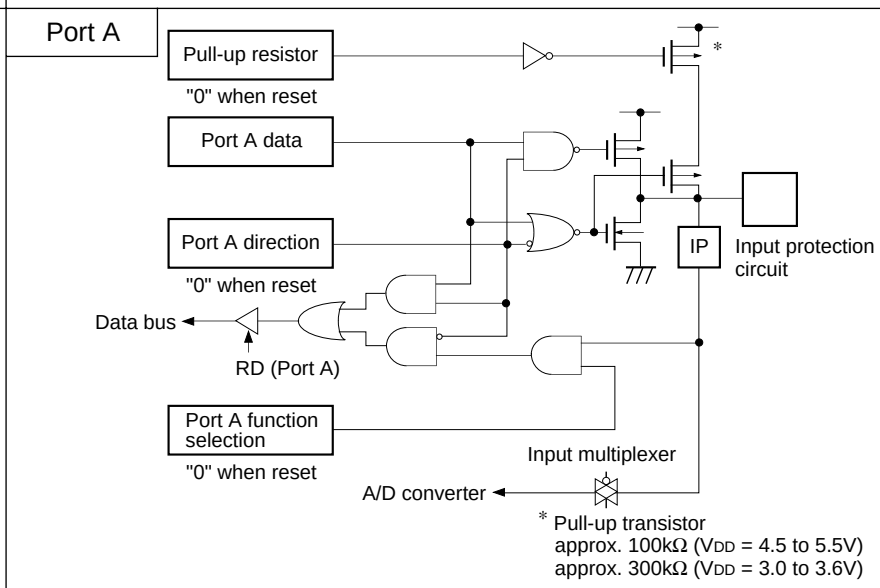
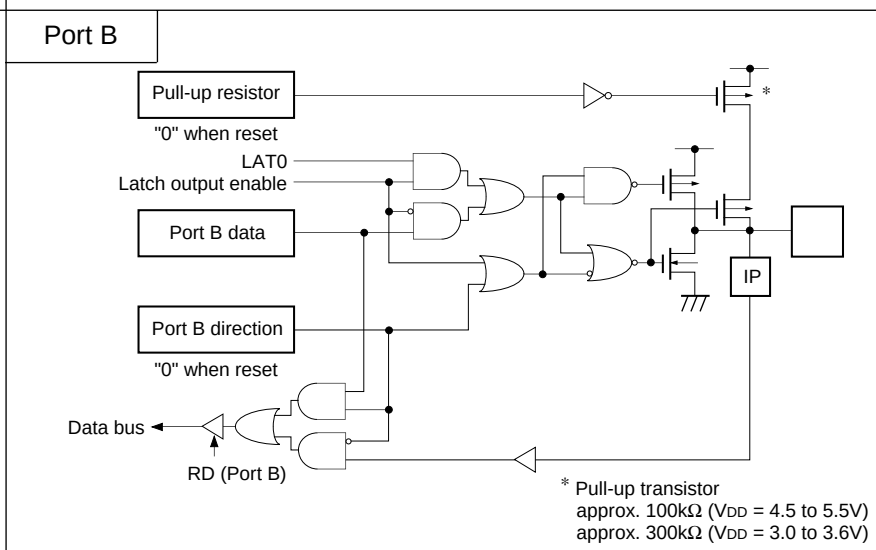
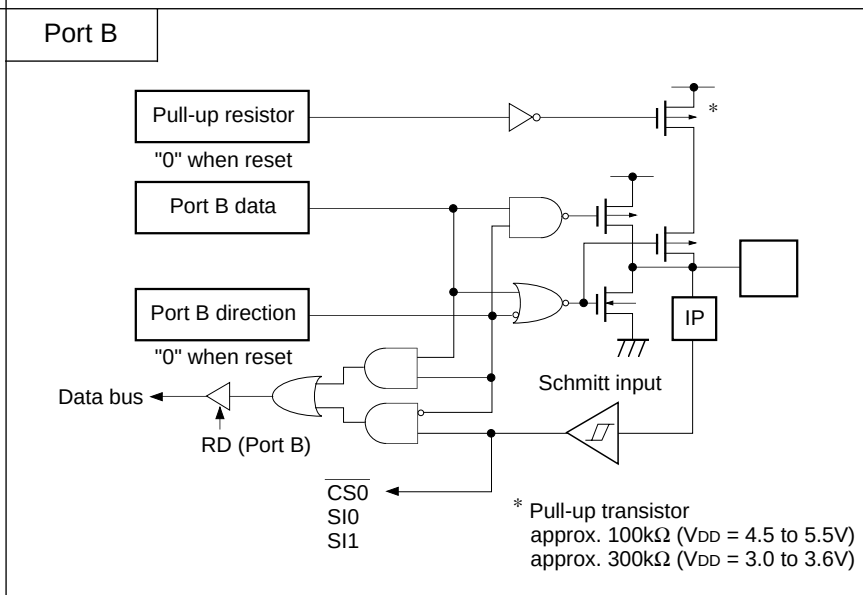
Note) NC (Pin 71) is left open.

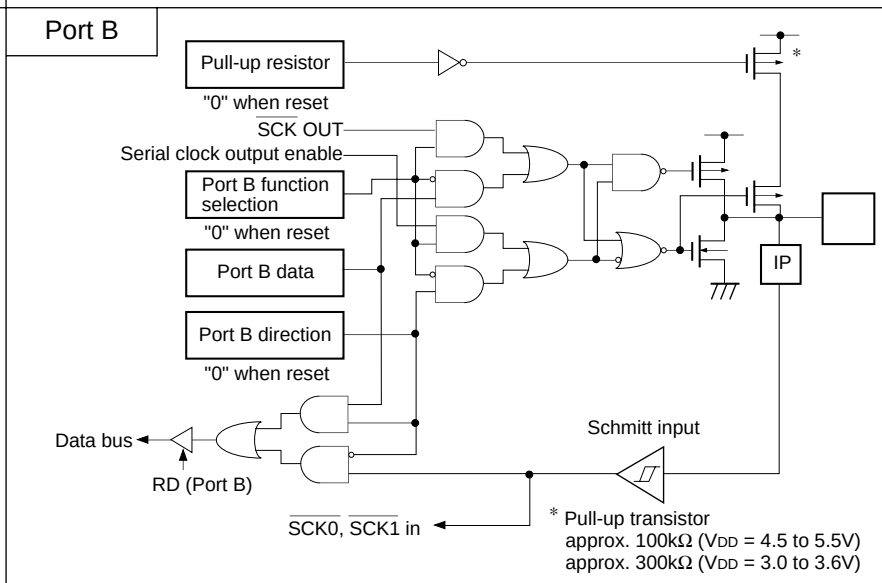
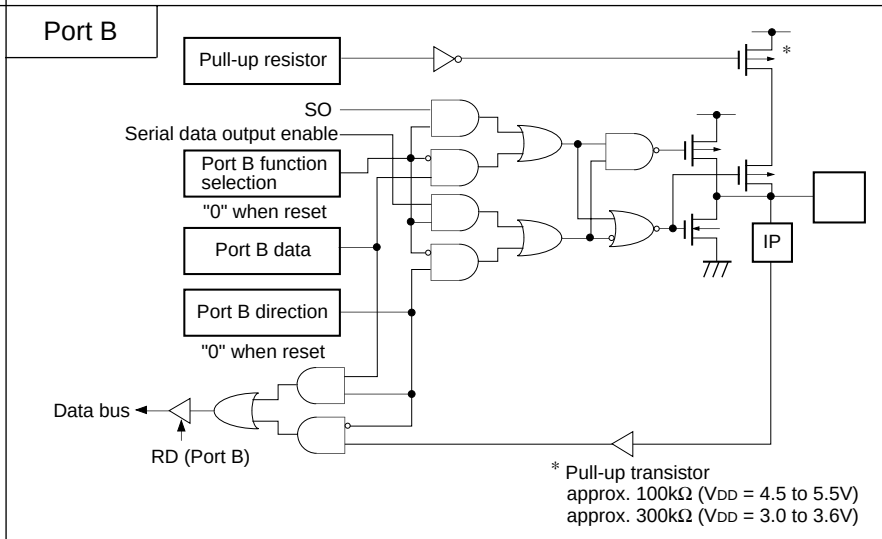
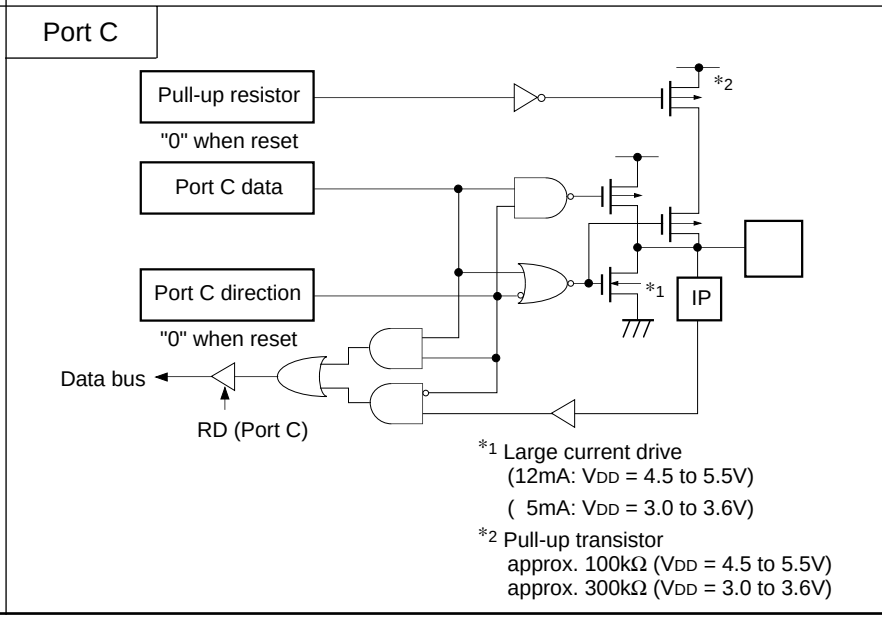
Pin Description

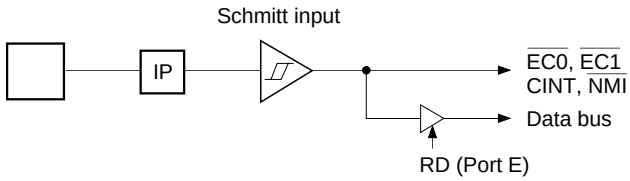
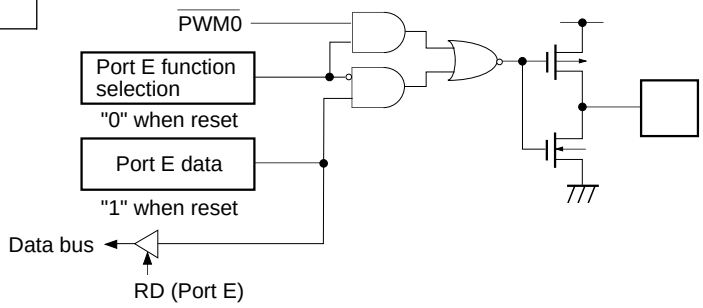
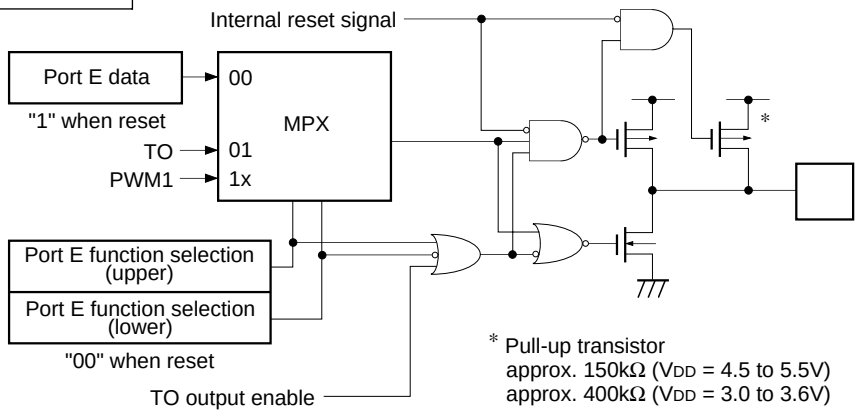
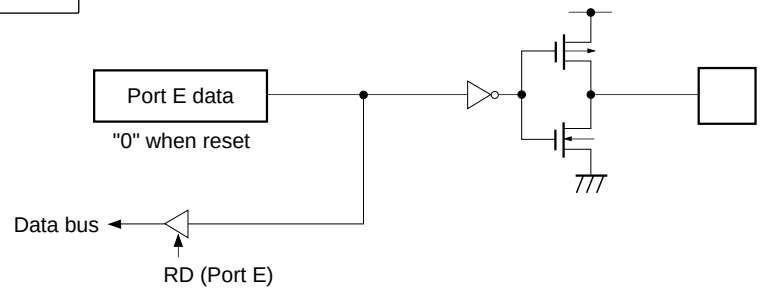
Symbol	I/O	Description	
PA0/AN0 to PA7/AN7	I/O/Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of the pull-up resistance can be set through the software in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (8 pins)
PB0/LAT0	I/O/Output	(Port B) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Latch output for serial interface (CH0).
PB1/$\overline{CS0}$	I/O/Input		Chip select input for serial interface (CH0).
PB2/$\overline{SCK0}$	I/O/I/O		Serial clock I/O (CH0).
PB3/SI0	I/O/Input		Serial data input (CH0).
PB4/SO0	I/O/Output		Serial data output (CH0).
PB5/$\overline{SCK1}$	I/O/I/O		Serial clock I/O (CH1).
PB6/SI1	I/O/Input		Serial data input (CH1).
PB7/SO1	I/O/Output		Serial data output (CH1).
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Can drive 12mA sync current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PD0 to PD7	I/O	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PE0/$\overline{EC0}$	Input/Input	(Port E) 8-bit port. Lower 4 bits are for inputs; upper 4 bits are for outputs. (8 pins)	External event inputs for timer/counter. (2 pins)
PE1/$\overline{EC1}$	Input/Input		
PE2/CINT	Input/Input		Capture trigger input.
PE3/$\overline{NMI}$	Input/Input		Non-maskable interruption request input.
PE4/PWM0	Output/Output		8-bit PWM0 output.
PE5/TO/ PWM1	Output/Output/ Output		Rectangular wave output for 16-bit timer/ counter and 8-bit PWM1 output.
PE6	Output		
PE7	Output		
PF0 to PF7	I/O	(Port F) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	

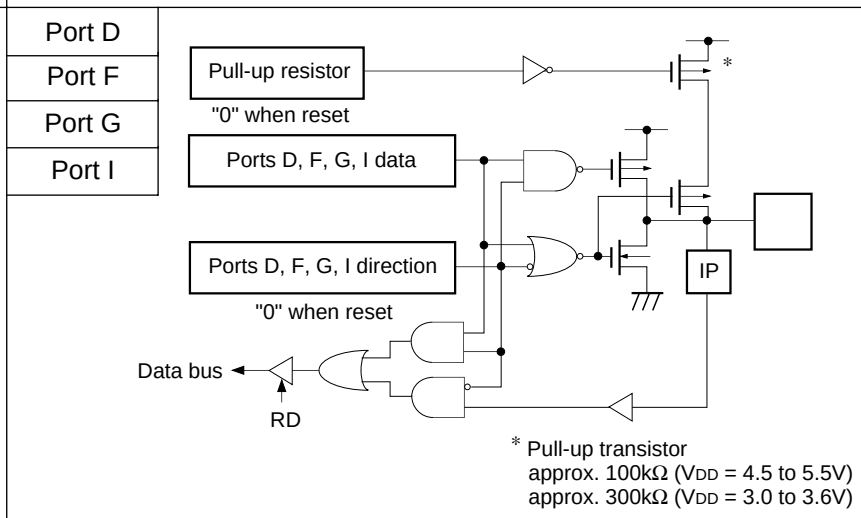
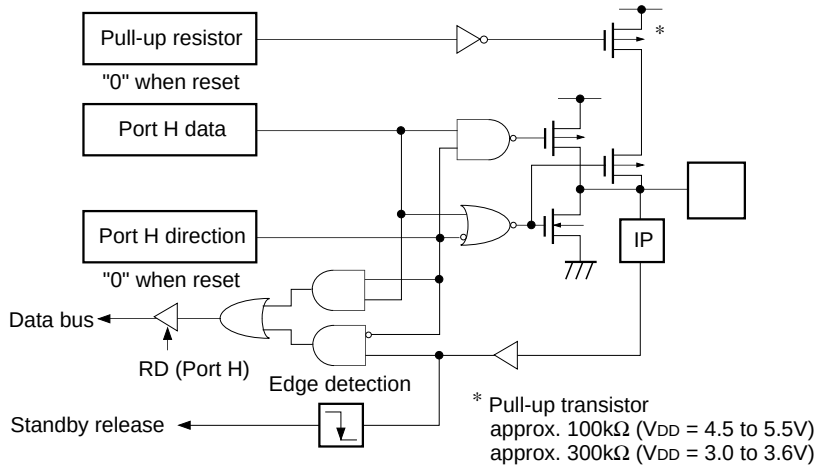
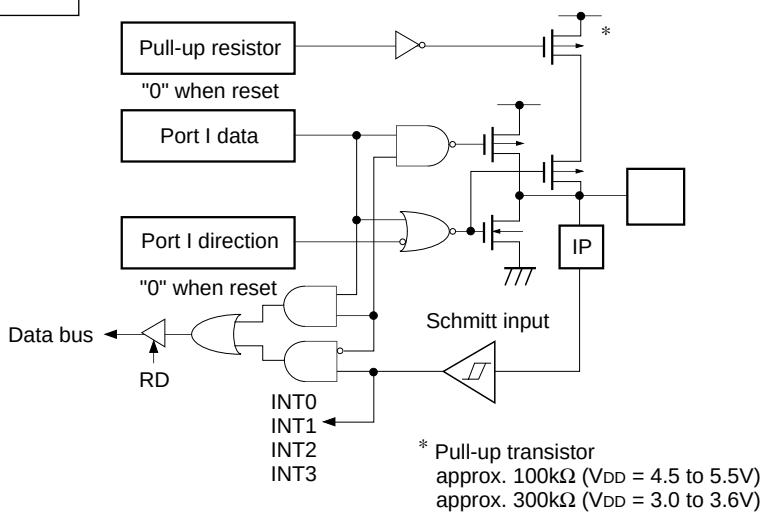
Symbol	I/O	Description
PG0 to PG7	I/O	(Port G) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)
PH0 to PH7	I/O	(Port H) 8-bit I/O port. I/O and standby release input function can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)
PI0/INT0 to PI3/INT3	I/O/Input	(Port I) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins) External interruption request inputs. (4 pins)
PI4 to PI7	I/O	
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input it to EXTAL; opposite phase clock should be input to XTAL.
XTAL	Output	
$\overline{\text{RST}}$	I/O	System reset for active at Low level. This pin is I/O pin, and outputs Low level at the power on with the power-on reset function executed. (Mask option)
NC		No connected. Leave this pin open. However, this is used for the Flash EEPROM incorporated version (CXP845F60).
AV_{REF}	Input	Reference voltage input for A/D converter.
AVss		A/D converter GND.
V_{DD}		Positive power supply.
Vss		GND

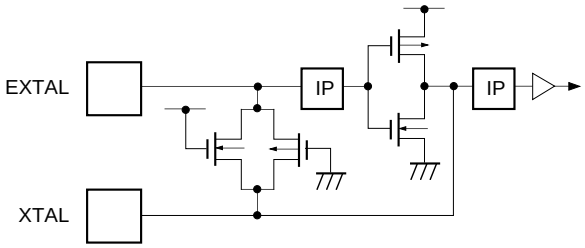
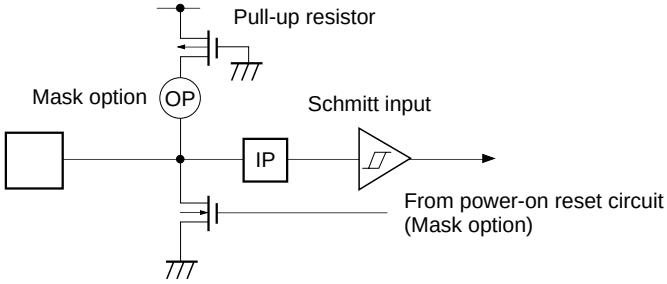
Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
PA0/AN0 to PA7/AN7 8 pins		Hi-Z
PB0/LAT0 1 pin		Hi-Z
PB1/$\overline{CS0}$ PB3/SI0 PB6/SI1 3 pins		Hi-Z

Pin	Circuit format	When reset
PB2/$\overline{SCK0}$ PB5/$\overline{SCK1}$ 2 pins		Hi-Z
PB4/SO0 PB7/SO1 2 pins		Hi-Z
PC0 to PC7 8 pins		Hi-Z

Pin	Circuit format	When reset
PE0/$\overline{EC0}$ PE1/$\overline{EC1}$ PE2/$\overline{CINT}$ PE3/$\overline{NMI}$ 4 pins	Port E 	Hi-Z
PE4/PWM0 1 pin	Port E 	High level
PE5/TO/ PWM1 1 pin	Port E 	High level (with resistor of pull-up transistor ON for reset)
PE6, PE7 2 pins	Port E 	Low level

Pin	Circuit format	When reset
PD0 to PD7 PF0 to PF7 PG0 to PG7 PI4 to PI7 28 pins	Port D / Port F / Port G / Port I 	Hi-Z
PH0 to PH7 8 pins	Port H 	Hi-Z
PI0/INT0 to PI3/INT3 4 pins	Port I 	Hi-Z

Pin	Circuit format	When reset
EXTAL XTAL 2 pins	 • Diagram shows the circuit composition during oscillation. • Feedback resistor is removed during stop mode and XTAL becomes High level.	Oscillation
$\overline{\text{RST}}$ 1 pin		Low level

Absolute Maximum Ratings (Vss = 0V reference)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
	AV_{SS}	–0.3 to +0.3	V	
Input voltage	V_{IN}	–0.3 to +7.0*1	V	
Output voltage	V_{OUT}	–0.3 to +7.0*1	V	
High level output current	I_{OH}	–5	mA	Output (value per pin)
High level total output current	$\sum I_{OH}$	–50	mA	Total of all output pins
Low level output current	I_{OL}	15	mA	Pins excluding large current outputs (value per pin)
	I_{OLC}	20	mA	Large current outputs (value per pin*2)
Low level total output current	$\sum I_{OL}$	100	mA	Total of all output pins
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	QFP-80P-L01
		380	mW	LQFP-80P-L01
		500	mW	LFLGA-80P-02

*1 V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*2 The large current drive transistor is the N-ch transistor of Port C (PC)

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage*1	V_{DD}	4.5 (3.0)	5.5	V	Guaranteed operation range for 1/2 and 1/4 frequency dividing clocks
		3.5 (2.7)	5.5		Guaranteed operation range for 1/16 frequency dividing clock and sleep mode
		2.0	5.5		Guaranteed data hold range during stop mode
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	*2
	V_{IHS}	0.8V_{DD}	V_{DD}	V	Hysteresis input*3
	V_{IHEX}	0.9V_{DD}	V_{DD} + 0.3	V	EXTAL*4
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	*2
	V_{ILS}	0	0.2V_{DD}	V	Hysteresis input*3
	V_{ILEX}	–0.3	0.1V_{DD}	V	EXTAL*4
Operating temperature	Topr	–20	+75	°C	

*1 Specifies values in parenthesis for 1 to 20MHz system clock operation.

*2 Normal input ports (PA, PB0, PB4, PB7, PC, PE0 to PE3, PD, PF to PH, PI4 to PI7)

*3 $\overline{RST}$, CINT, $\overline{CS0}$, $\overline{SCK0}$, $\overline{SCK1}$, $\overline{EC0}$, $\overline{EC1}$, SI0, SI1, $\overline{NMI}$, INT0, INT1, INT2, INT3

*4 Specifies only during external clock input.

Electrical Characteristics

DC Characteristics (V_{DD} 4.5 to 5.5V) (Ta = –20 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE4 to PE7, PF to PI, $\overline{RST}$ (only V_{OL})*1	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output voltage	V_{OL}		V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PC	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.1		25	µA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.1		–25	µA
	I_{ILR}	$\overline{RST}$*2	V_{DD} = 5.5V, V_{IL} = 4.0V	–1.5		–400	µA
	I_{IL}	PA to PD*3 PF to PI*3				–50	µA
			V_{DD} = 4.5V, V_{IL} = 4.0V	–2.78			µA
I/O leakage current	I_{IZ}	PA to PD*3 PF to PI*3 PE0 to PE3, $\overline{RST}$*2	V_{DD} = 5.5V, V_I = 0, 5.5V			±10	µA
Supply current *4	I_{DD1}	V_{DD}	1/2 frequency dividing clock operation		28	58	mA
	I_{DD2}		V_{DD} = 5.5V, 28MHz crystal oscillation (C_1 = C_2 = 5pF)				
	I_{DDS1}		Sleep mode		4.0	10	mA
	I_{DDS2}		V_{DD} = 5.5V, 28MHz crystal oscillation (C_1 = C_2 = 5pF)				
	I_{DDS3}		Stop mode			10	µA
			V_{DD} = 5.5V, termination of 28MHz crystal oscillation				
Input capacity	C_{IN}	PA to PD, PE0 to PE3, PF to PI, EXTAL, $\overline{RST}$	Clock 1MHz 0V for no-measured pins		10	20	pF

*1 Specifies $\overline{RST}$ pin when the power-on reset circuit is selected with mask option.

*2 For $\overline{RST}$ pin, specifies the input current when pull-up resistance is selected; leakage current when no resistance is selected.

*3 For PA to PD and PF to PI pins, specifies the input current when pull-up resistance is selected; leakage current when no resistance is selected.

*4 When all pins are open.

DC Characteristics (V_{DD} = 3.0 to 3.6V) (Ta = –20 to +75°C, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE4 to PE7, PF to PI, $\overline{RST}$ (only V_{OL})*1	V_{DD} = 3.0V, I_{OH} = –0.15mA	2.7			V
			V_{DD} = 3.0V, I_{OH} = –0.5mA	2.3			V
Low level output voltage	V_{OL}		V_{DD} = 3.0V, I_{OL} = 1.2mA			0.3	V
			V_{DD} = 3.0V, I_{OL} = 1.6mA			0.5	V
		PC	V_{DD} = 3.0V, I_{OL} = 5mA			1.0	V
Input current	I_{IHE}	EXTAL	V_{DD} = 3.6V, V_{IH} = 3.6V	0.05		15	µA
	I_{ILE}		V_{DD} = 3.6V, V_{IL} = 0.3V	–0.05		–15	µA
	I_{ILR}	$\overline{RST}$*2	V_{DD} = 3.6V, V_{IL} = 2.7V	–0.7		–200	µA
	I_{IL}	PA to PD*3 PF to PI*3				–30	µA
			V_{DD} = 3.0V, V_{IL} = 2.7V	–1.0			µA
I/O leakage current	I_{IZ}	PA to PD*3 PF to PI*3 PE0 to PE3, $\overline{RST}$*2	V_{DD} = 3.6V, V_I = 0, 3.6V			±5	µA
Supply current*4	I_{DD1}	V_{DD}	1/2 frequency dividing clock operation		13.5	30	mA
	I_{DD2}		V_{DD} = 3.6V, 20MHz crystal oscillation (C_1 = C_2 = 10pF)				
	I_{DDS1}		Sleep mode		1.2	4.0	mA
	I_{DDS2}		V_{DD} = 3.6V, 20MHz crystal oscillation (C_1 = C_2 = 10pF)				
	I_{DDS3}		Stop mode			5	µA
			V_{DD} = 3.6V, termination of 20MHz crystal oscillation				

*1 Specifies $\overline{RST}$ pin when the power-on reset circuit is selected with mask option.

*2 For $\overline{RST}$ pin, specifies the input current when pull-up resistance is selected; leakage current when no resistance is selected.

*3 For PA to PD and PF to PI pins, specifies the input current when pull-up resistance is selected; leakage current when no resistance is selected.

*4 When all pins are open.

AC Characteristics

(1) Clock timing

(Ta = –20 to +75°C, V_{DD} = 3.0 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Conditions		Min.	Typ.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	V_{DD} = 4.5 to 5.5V	1		28	MHz
					1		20	
System clock input pulse width	t_{XL}, t_{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	V_{DD} = 4.5 to 5.5V	15.6			ns
					23			
System clock input rise time, fall time	t_{CR}, t_{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive				100	ns
Event count input clock pulse width	t_{EH}, t_{EL}	$\overline{EC0}$ $\overline{EC1}$	Fig. 3		$t_{sys} + 50$*1			ns
Event count input clock rise time, fall time	t_{ER}, t_{EF}	$\overline{EC0}$ $\overline{EC1}$	Fig. 3				20	ns

*1 tsys indicates three values according to the contents of the clock control register (CLC: 00FEh) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

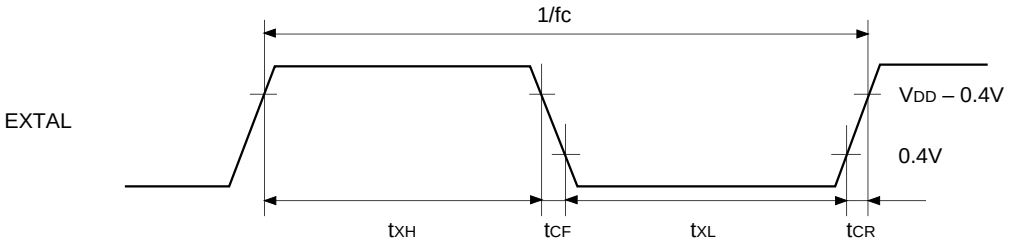


Fig. 1. Clock timing

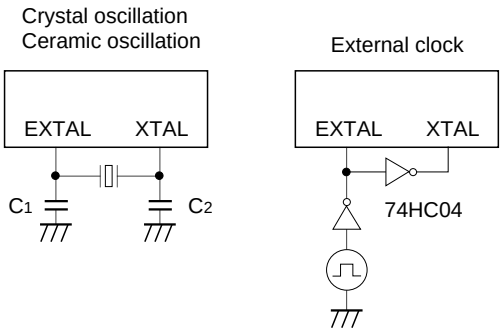


Fig. 2. Clock applied conditions

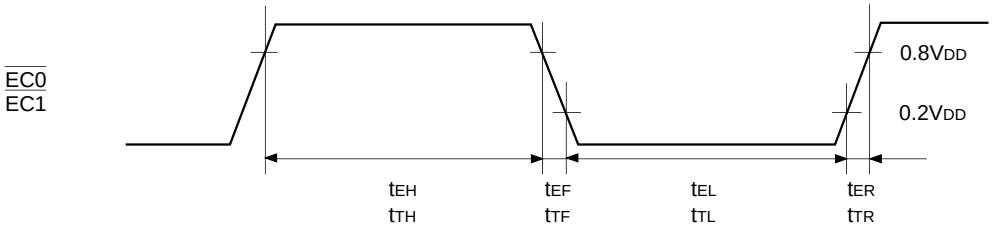


Fig. 3. Event count clock timing

(2) Serial transfer (CH0) (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		1.5tsys + 100	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ float delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		1.5tsys + 100	ns
$\overline{CS0} \downarrow \rightarrow$ SO0 delay time	t_{DCSO}	SO0	Chip select transfer mode		1.5tsys + 100	ns
$\overline{CS0} \uparrow \rightarrow$ SO0 float delay time	t_{DCSOF}	SO0	Chip select transfer mode		1.5tsys + 100	ns
$\overline{CS0}$ High level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys + 150		ns
$\overline{SCK0}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys + 200		ns
			Output mode	8000/fc		ns
$\overline{SCK0}$ High, Low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys + 90		ns
			Output mode	4000/fc – 25		ns
SI0 input setup time (for $\overline{SCK0} \uparrow$)	t_{SIK}	SI0	$\overline{SCK0}$ input mode	50		ns
			$\overline{SCK0}$ output mode	100		ns
SI0 input hold time (for $\overline{SCK0} \uparrow$)	t_{KSI}	SI0	$\overline{SCK0}$ input mode	tsys + 100		ns
			$\overline{SCK0}$ output mode	50		ns
$\overline{SCK0} \downarrow \rightarrow$ SO0 delay time	t_{KSO}	SO0	$\overline{SCK0}$ input mode		tsys + 100	ns
			$\overline{SCK0}$ output mode		50	ns
$\overline{SCK0} \downarrow \rightarrow$ LAT0 output delay time	t_{LADLY}	LAT0	Latch output mode ($\overline{SCK0}$ = output mode)	t_{KCY}	t_{KCY} + 50	ns
LAT0 data pulse width	t_{LAPLS}	LAT0	Latch output mode ($\overline{SCK0}$ = output mode)	t_{KCY} – 10	t_{KCY} + 50	ns

Note 1) tsys indicates three values according to the ccontents of the clock control register (CLC: 00FEh) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) The load condition for the $\overline{SCK0}$ output mode, SO0 output delay time is 50pF + 1TTL.

Serial transfer (CH0) (Ta = –20 to +75°C, V_{DD} = 3.0 to 3.6V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		1.5tsys + 200	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ float delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		1.5tsys + 200	ns
$\overline{CS0} \downarrow \rightarrow$ SO0 delay time	t_{DCSO}	SO0	Chip select transfer mode		1.5tsys + 200	ns
$\overline{CS0} \uparrow \rightarrow$ SO0 float delay time	t_{DCSOF}	SO0	Chip select transfer mode		1.5tsys + 200	ns
$\overline{CS0}$ High level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK0}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys + 200		ns
			Output mode	8000/fc		ns
$\overline{SCK0}$ High, Low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys + 80		ns
			Output mode	4000/fc – 50		ns
SI0 input setup time (for $\overline{SCK0} \uparrow$)	t_{SIK}	SI0	$\overline{SCK0}$ input mode	80		ns
			$\overline{SCK0}$ output mode	150		ns
SI0 input hold time (for $\overline{SCK0} \uparrow$)	t_{KSI}	SI0	$\overline{SCK0}$ input mode	tsys + 120		ns
			$\overline{SCK0}$ output mode	70		ns
$\overline{SCK0} \downarrow \rightarrow$ SO0 delay time	t_{KSO}	SO0	$\overline{SCK0}$ input mode		tsys + 200	ns
			$\overline{SCK0}$ output mode		80	ns
$\overline{SCK0} \downarrow \rightarrow$ LAT0 output delay time	t_{LADLY}	LAT0	Latch output mode ($\overline{SCK0}$ = output mode)	t_{KCY}	t_{KCY} + 100	ns
LAT0 data pulse width	t_{LAPLS}	LAT0	Latch output mode ($\overline{SCK0}$ = output mode)	t_{KCY} – 10	t_{KCY} + 100	ns

Note 1) tsys indicates three values according to the contents of the clock control register (CLC: 00FEh) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) The load condition for the $\overline{SCK0}$ output mode, SO0 output delay time is 50pF + 1TTL.

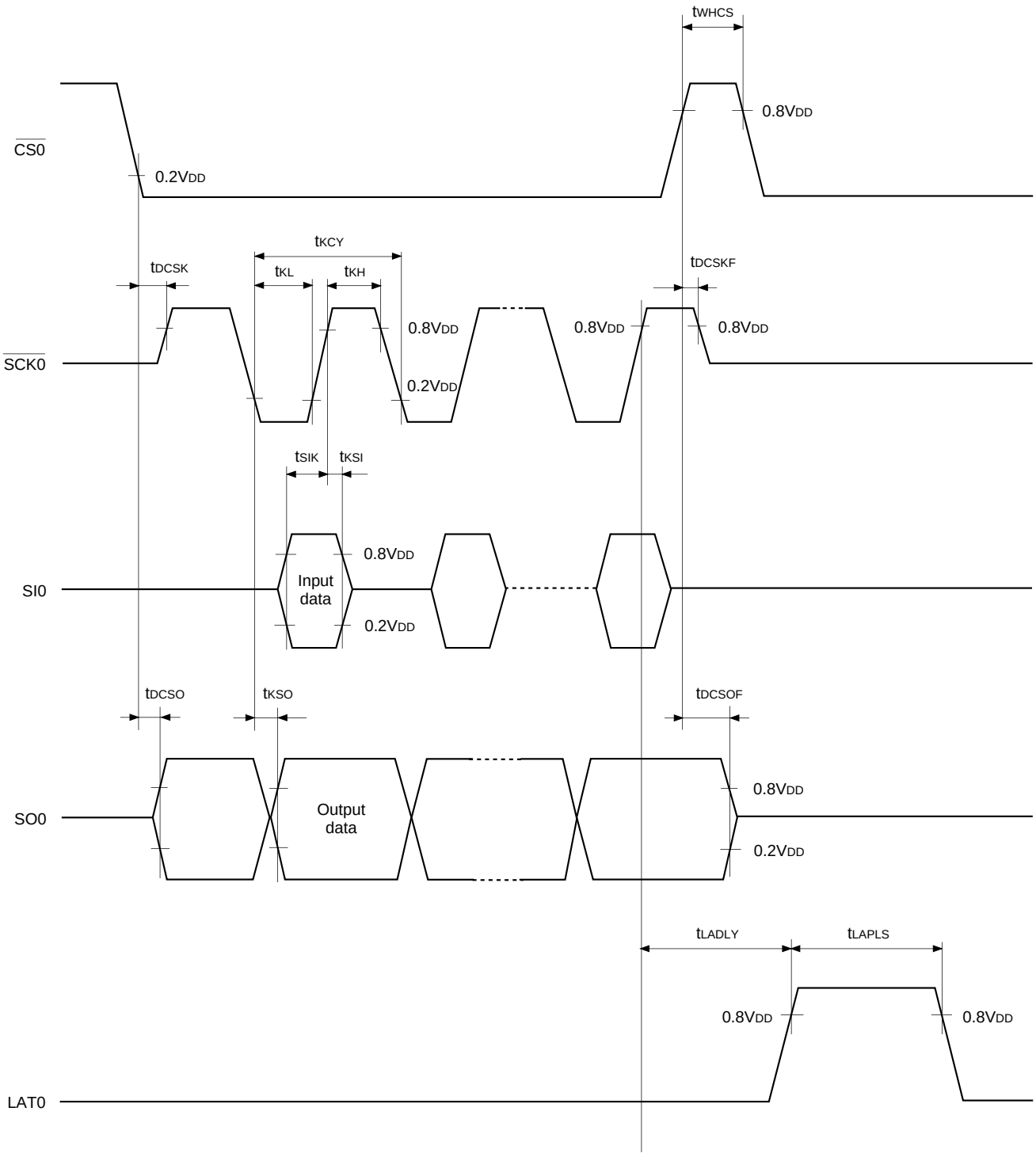


Fig. 4. Serial transfer CH0 timing

(3) Serial transfer (CH1) (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	500		ns
			Output mode	8000/fc		ns
$\overline{SCK1}$ High, Low level widths	t_{KH} t_{KL}	$\overline{SCK1}$	Input mode	200		ns
			Output mode	4000/fc – 25		ns
SI1 input set-up time (for $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	50		ns
			$\overline{SCK1}$ output mode	100		ns
SI1 input hold time (for $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ output mode	50		ns
$\overline{SCK1}$ ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		100	ns
			$\overline{SCK1}$ output mode		50	ns

Note) The load condition for the $\overline{SCK1}$ output mode, SO1 output delay time is 50pF + 1TTL.

(Ta = –20 to +75°C, V_{DD} = 3.0 to 3.6V, V_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	700		ns
			Output mode	8000/fc		ns
$\overline{SCK1}$ High, Low level widths	t_{KH} t_{KL}	$\overline{SCK1}$	Input mode	300		ns
			Output mode	4000/fc – 50		ns
SI1 input set-up time (for $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	70		ns
			$\overline{SCK1}$ output mode	150		ns
SI1 input hold time (for $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	150		ns
			$\overline{SCK1}$ output mode	70		ns
$\overline{SCK1}$ ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		150	ns
			$\overline{SCK1}$ output mode		80	ns

Note) The load condition for the $\overline{SCK1}$ output mode, SO1 output delay time is 50pF.

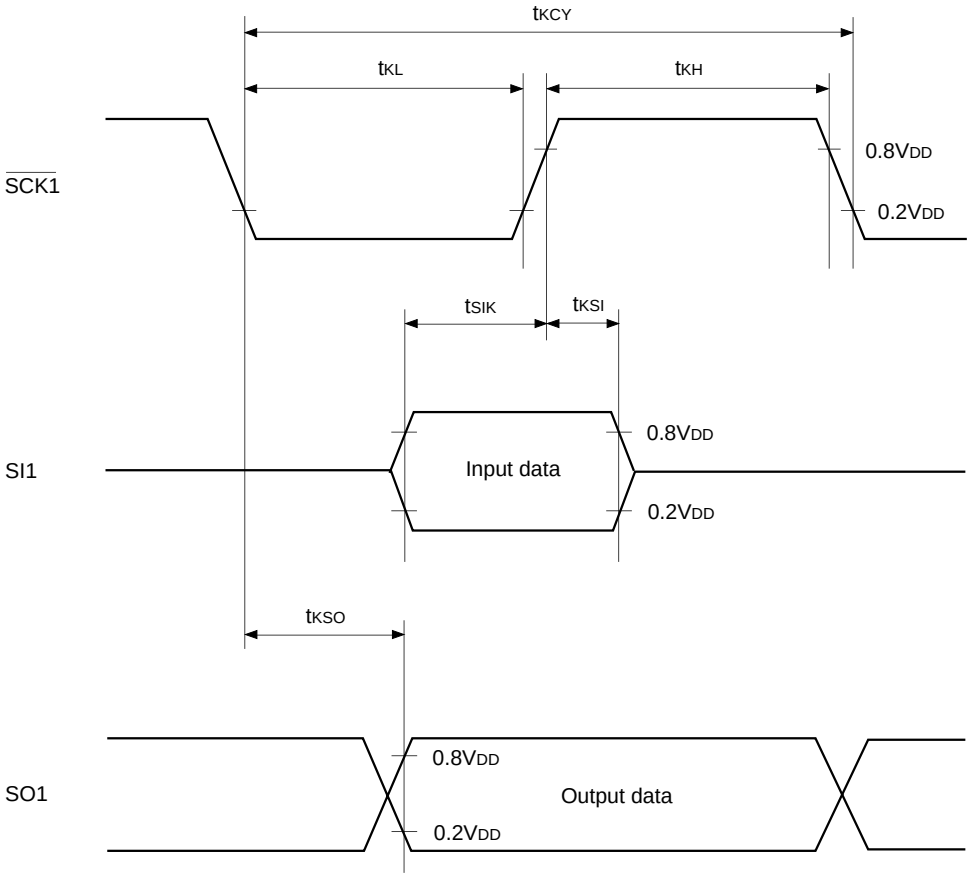


Fig. 5. Serial transfer CH1 timing

(4) A/D converter characteristics (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, AV_{REF} = 4.0 to V_{DD}, Vss = AV_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V_{DD} = AV_{REF} = 5.0V Vss = AV_{SS} = 0V			±4	LSB
Zero transition voltage	V_{ZT}*1			–10	10	70	mV
Full-scale transition voltage	V_{FT}*2			4910	4970	5030	mV
Conversion time	t_{CONV}			27/f_{ADC}*3			µs
Sampling time	t_{SAMP}			6/f_{ADC}*3			µs
Reference input voltage	V_{REF}	AV_{REF}		V_{DD} – 0.5		V_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN7		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operation mode		0.6	1.0	mA
	I_{REFS}		Sleep mode Stop mode			10	µA

(Ta = –20 to +75°C, V_{DD} = 3.0 to 3.6V, AV_{REF} = 2.7 to V_{DD}, Vss = AV_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V_{DD} = AV_{REF} = 3.3V Vss = AV_{SS} = 0V			±5	LSB
Zero transition voltage	V_{ZT}*1			–10	6.5	70	mV
Full-scale transition voltage	V_{FT}*2			3216	3280.5	3345	mV
Conversion time	t_{CONV}			27/f_{ADC}*3			µs
Sampling time	t_{SAMP}			6/f_{ADC}*3			µs
Reference input voltage	V_{REF}	AV_{REF}		V_{DD} – 0.3		V_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN7		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operation mode		0.4	0.7	mA
	I_{REFS}		Sleep mode Stop mode			5	µA

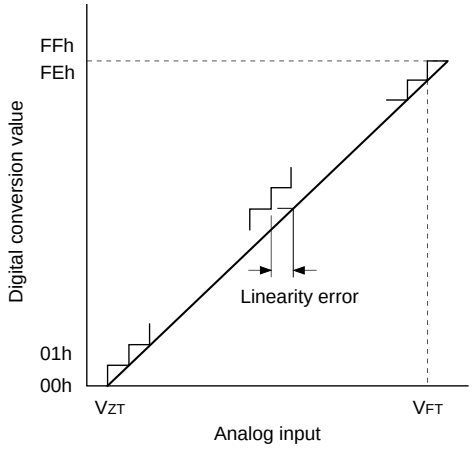


Fig. 6. Definition of A/D converter terms

*1 V_{ZT}: Value at which the digital conversion value changes from 00h to 01h and vice versa.

*2 V_{FT}: Value at which the digital conversion value changes from FEh to FFh and vice versa.

*3 f_{ADC} indicates the values below due to the contents of bit 6 (CKS) of the A/D control register (ADC: 00F9h).

f_{ADC} = fc (CKS = "0"), fc/2 (CKS = "1")

However, the selection for f_{ADC} = fc (CKS = "0") is limited in the clock range of fc = 1 to 14MHz (V_{DD} 4.5 to 5.5V) and fc = 1 to 10MHz (V_{DD} = 3.0 to 4.5V).

(4) Interruption, reset input (Ta = –20 to +75°C, V_{DD} = 3.0 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption High, Low level widths	t_{IH} t_{IL}	INT0 INT1 INT2 INT3 $\overline{NMI}$		1		µs
Reset input Low level width	t_{RSL}	$\overline{RST}$		32/fc		µs

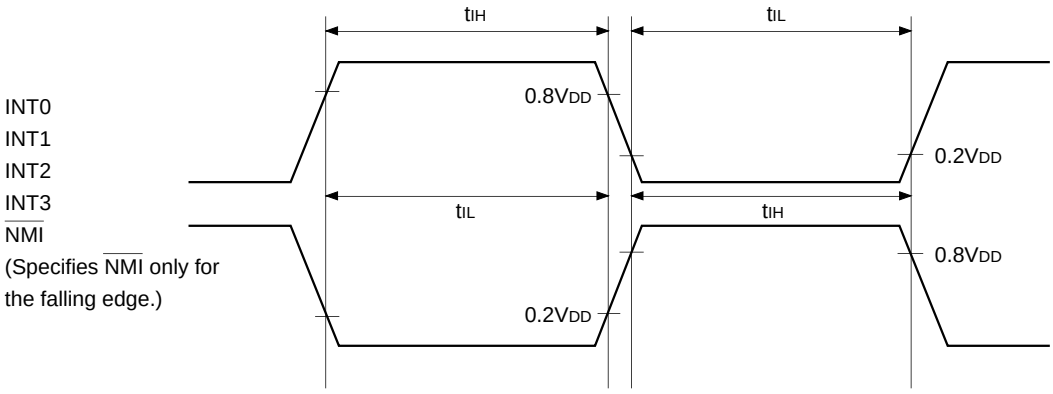


Fig 7. Interruption input timing

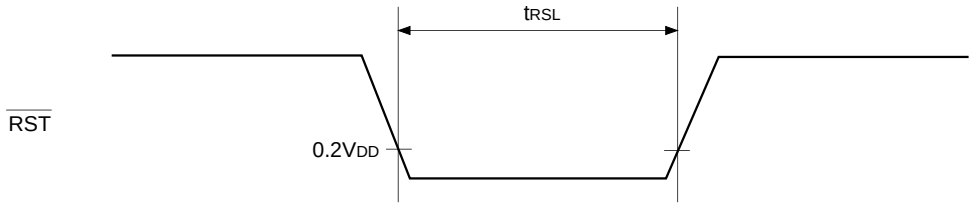
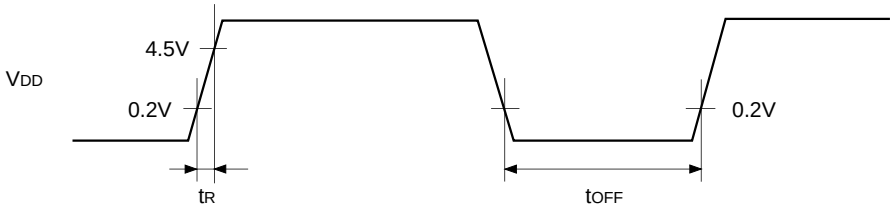


Fig. 8. $\overline{RST}$ input timing

(5) Power-on reset[*1] (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rise time	t_R	V_{DD}	Power-on reset	0.05	50	ms
Power supply cut-off time	t_{OFF}		Repetitive power-on reset	1		ms

[*1] Specifies only when the power-on reset function is selected.
Power-on reset function can be selected only for the supply voltage range of 4.5 to 5.5V.



Take care when turning the power on.

Fig. 9. Power-on reset

Appendix

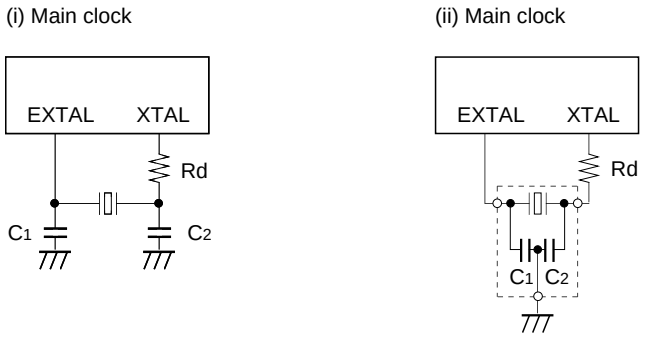


Fig. 10. SPC700 Series recommended oscillation circuit

Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
MURATA MFG CO., LTD.	CSA8.00MTZ	8.00	30	30	0	(i)
	CSA10.0MTZ	10.00				
	CSA12.00MTZ	12.00				
	CST8.00MTW*	8.00				(ii)
	CST10.0MT*	10.00				
	CST12.0MTW*	12.00				
	CSA16.00MXZ040	16.00	5	5	0	(i)
	CST16.00MXZ0C1*	16.00	5	5	0	(ii)
	CSA20.00MXZ040	20.00	OPEN	OPEN	0	(i)
	CSA24.00MXZ040	24.00	3	3	0	
	CSA28.00MXZ040	28.00	3	3	0	
TDK CORPORATION.	CCR20.0MC6*	20.00	16	16	0	(ii)
	CCR24.0MC6*	24.00	16	16	0	
KINSEKI LTD.	HC49/U-S	28.00	1	1	220	(i)
	CX-11F	28.00	1	1	220	

Models with an asterisk (*) have the built-in ground capacitance (C_1, C_2).

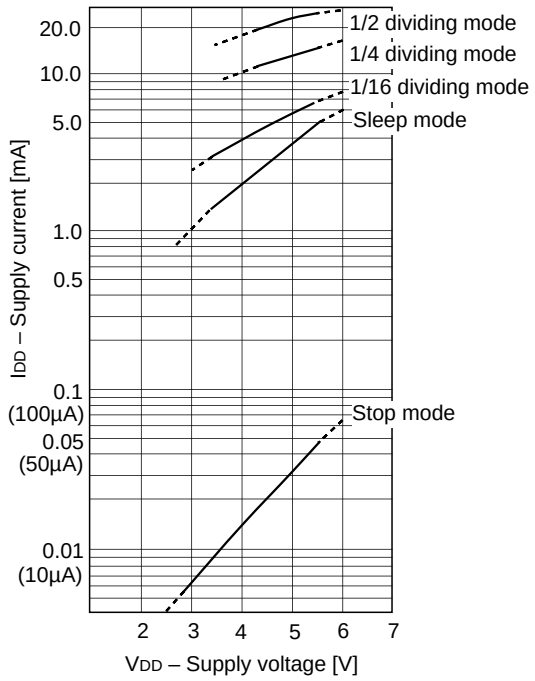
Mask option table

Item	Contents	
Reset pin pull-up resistor	Non-existent	Existent
Power-on reset circuit *1	Non-existent	Existent

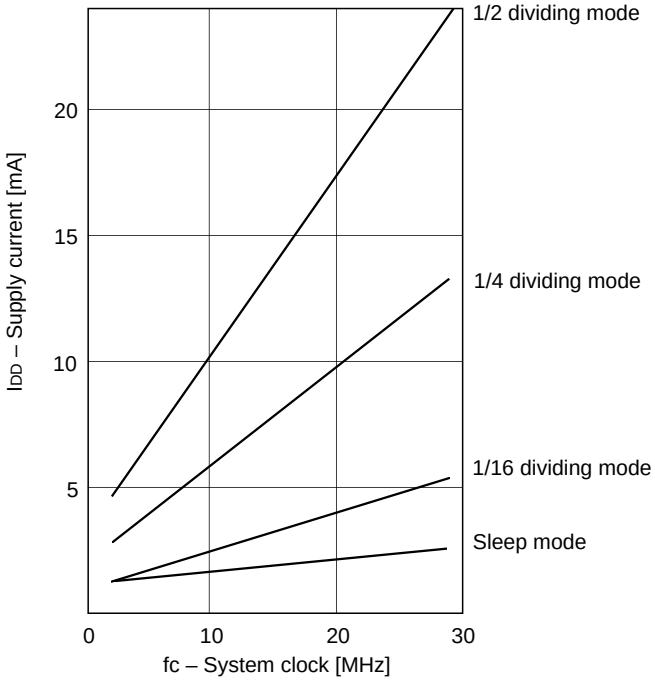
*1 "Existent" for power-on reset circuit cannot be selected when the supply voltage V_{DD} of 3.0 to 4.5V.

Characteristics Curves

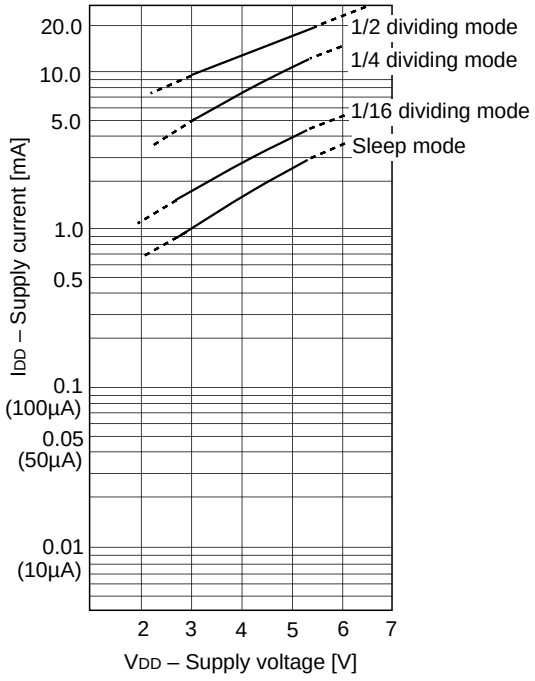
IDD vs. VDD
(fc = 28MHz, Ta = 25°C, Typical)



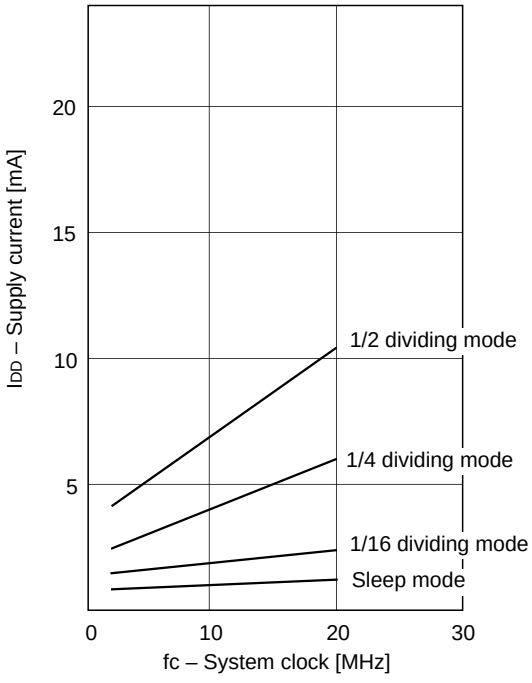
IDD vs. fc
(VDD = 5V, Ta = 25°C, Typical)



IDD vs. VDD
(fc = 20MHz, Ta = 25°C, Typical)



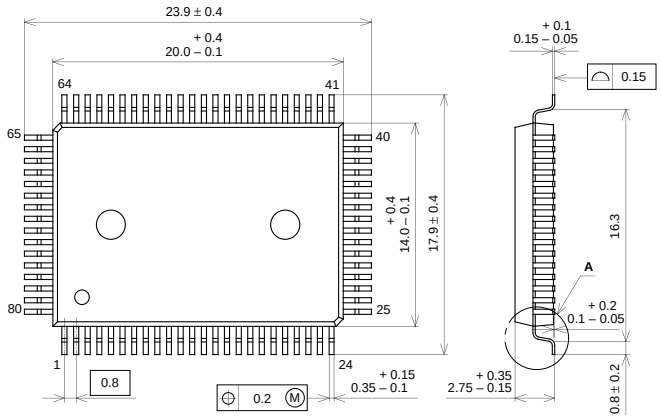
IDD vs. fc
(VDD = 3.3V, Ta = 25°C, Typical)

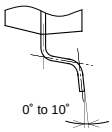


Package Outline

Unit: mm

80PIN QFP (PLASTIC)





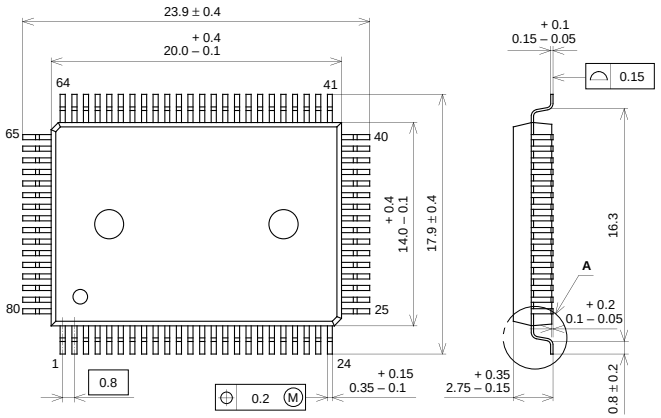
DETAIL **A**

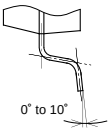
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g

SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	————

80PIN QFP (PLASTIC)





DETAIL **A**

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g

SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	————

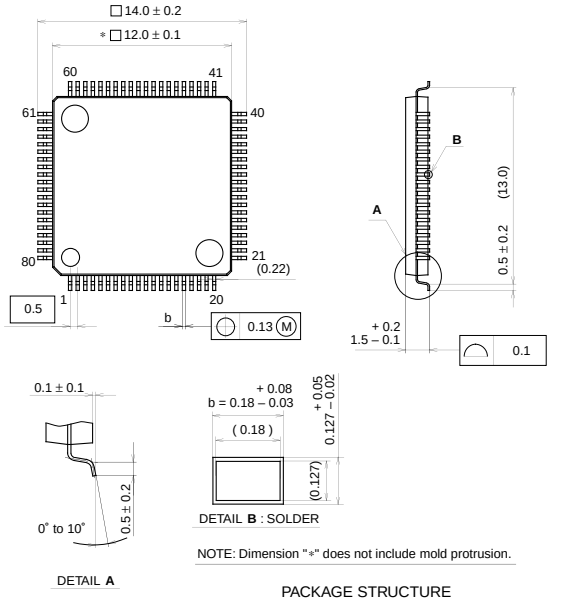
LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18µm

Package Outline

Unit: mm

80PIN LQFP (PLASTIC)



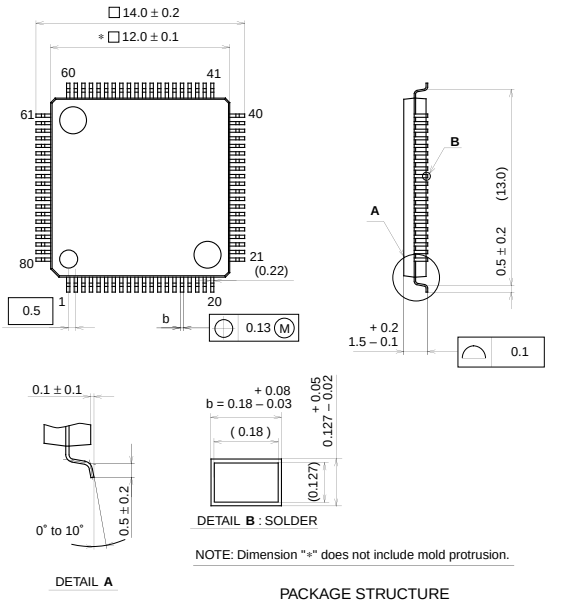
NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-80P-L01
EIAJ CODE	P-LQFP80-12x12-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.5g

80PIN LQFP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-80P-L01
EIAJ CODE	P-LQFP80-12x12-0.5
JEDEC CODE	————

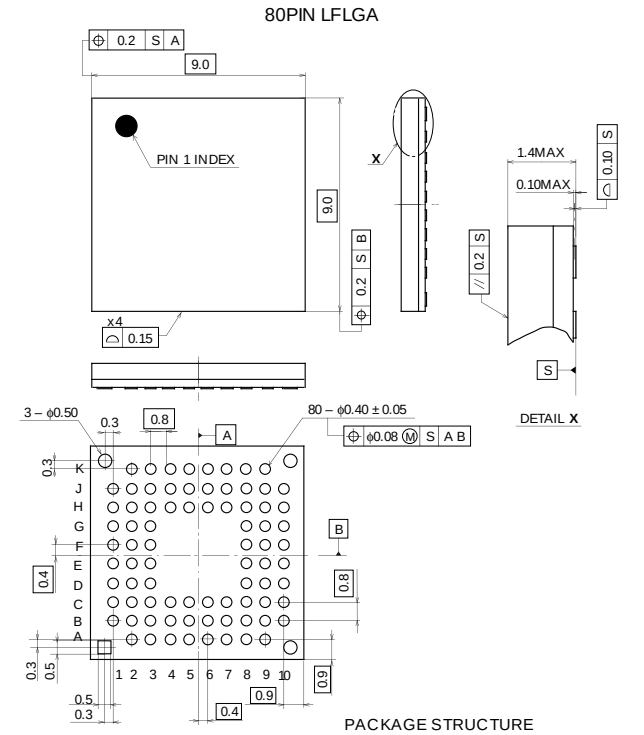
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.5g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18μm

Package Outline Unit: mm



PACKAGE STRUCTURE

SONY CODE	LFLGA-80P-02
EIAJ CODE	P-LFLGA80-9x9-0.8
JEDEC CODE	

PACKAGE MATERIAL	ORGANIC SUBSTRATE
TERMINAL TREATMENT	GOLD PLATING
TERMINAL MATERIAL	NICKEL PLATING
PACKAGE MASS	0.3g

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