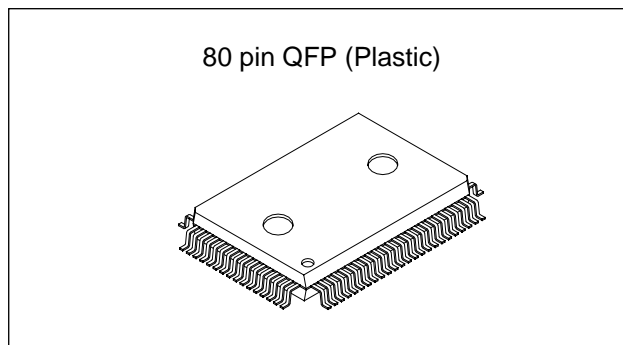


CMOS 8-bit Single Chip Microcomputer**Description**

CXP84332M/84340M is a CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time base timer, capture timer/counter, remote control reception circuit, PWM output, and 32kHz timer/counter besides the basic configurations of 8-bit CPU, ROM, RAM, and I/O port.

The CXP84332M/84340M also provides a sleep/stop function that enables lower power consumption.

**Features**

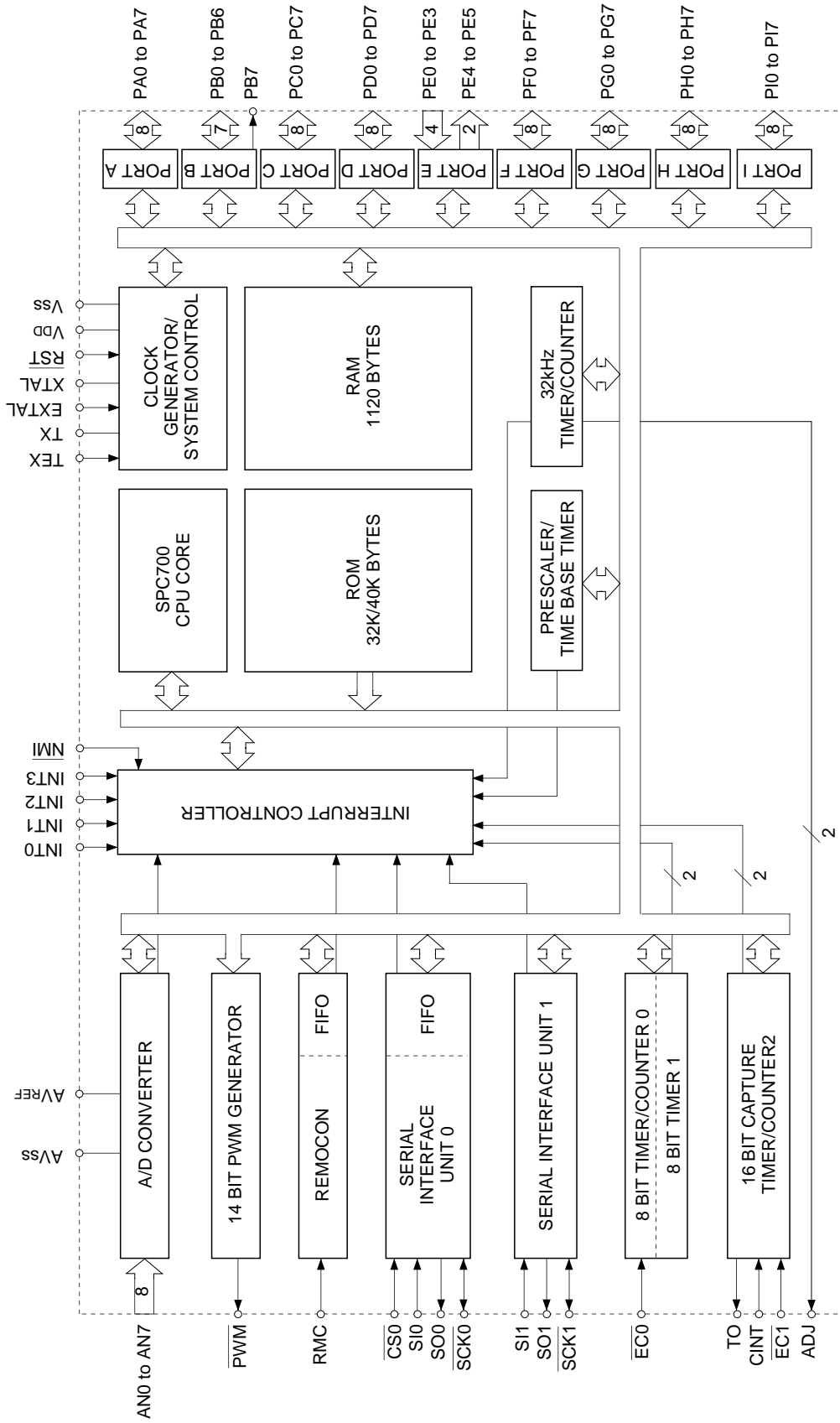
- Wide-range instruction system (213 instructions) to cover various types of data
 - 16-bit arithmetic/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle
 - 200ns at 20MHz operation
 - 122μs at 32kHz operation
- Incorporated ROM capacity
 - 32K bytes (CXP84332M)
 - 40K bytes (CXP84340M)
- Incorporated RAM capacity
 - 1120 bytes
- Peripheral functions
 - A/D converter
 - 8 bits, 8 channels, successive approximation method
(Conversion time of 16μs/20MHz)
 - Serial interface
 - 8-bit, 8-stage FIFO incorporated
(Auto transfer for 1 to 8 bytes), 1 channel
 - 8-bit clock synchronization, 1 channel
 - Timers
 - 8-bit timer
 - 8-bit timer/counter
 - 19-bit time base timer
 - 16-bit capture timer/counter
 - 32kHz timer/counter
 - Remote control reception circuit
 - 8-bit pulse measuring counter, 6-stage FIFO
 - PWM output
 - 14 bits, 1 channel
- Interruption
 - 15 factors, 15 vectors, multi-interruption possible
- Standby mode
 - SLEEP/STOP
- Package
 - 80-pin plastic QFP
- Piggyback/evaluation chip
 - CXP84300 80-pin ceramic QFP

Structure

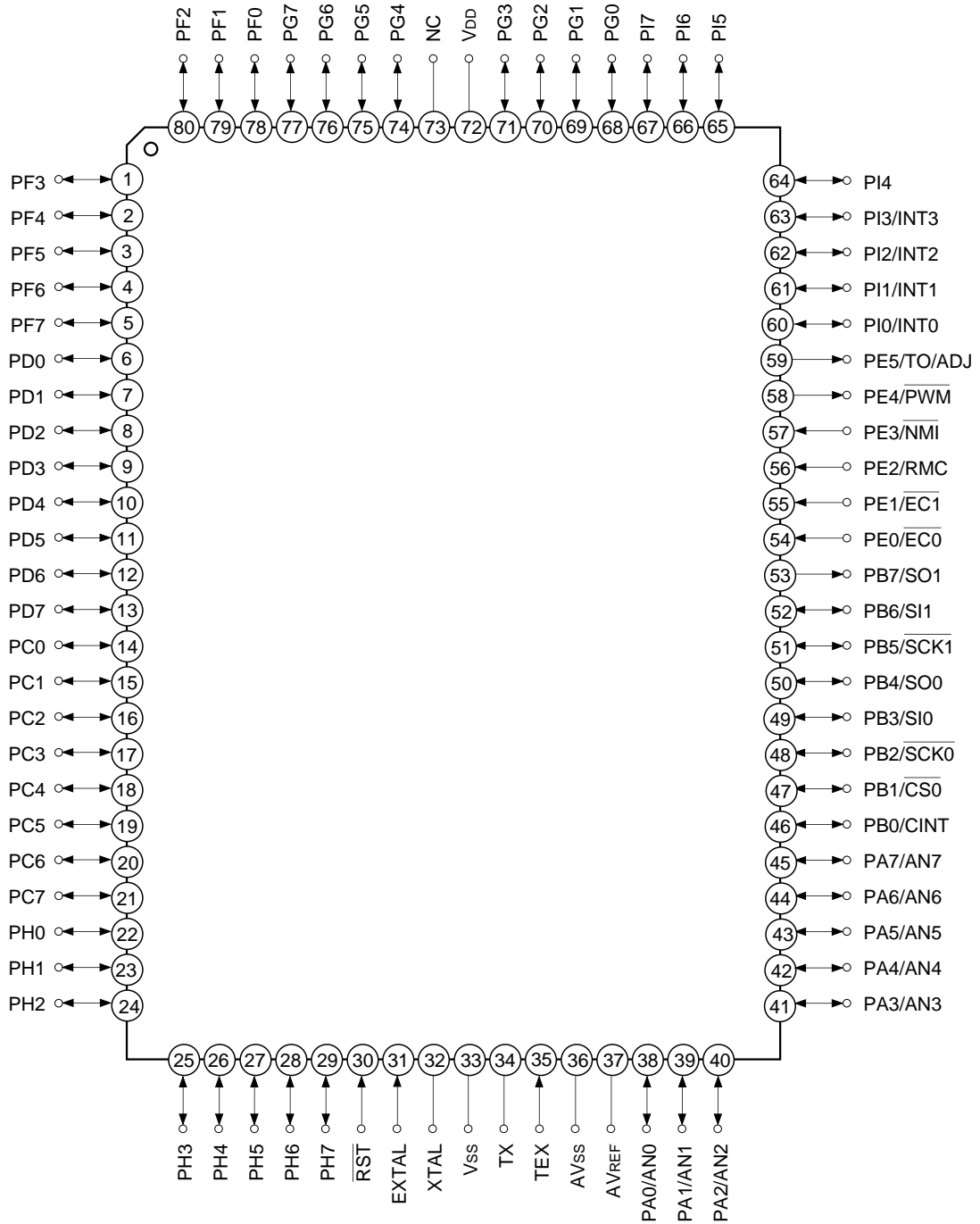
Silicon gate CMOS IC

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Block Diagram



Pin Assignment (Top View)



Note NC (Pin 73) must be connected to VDD.

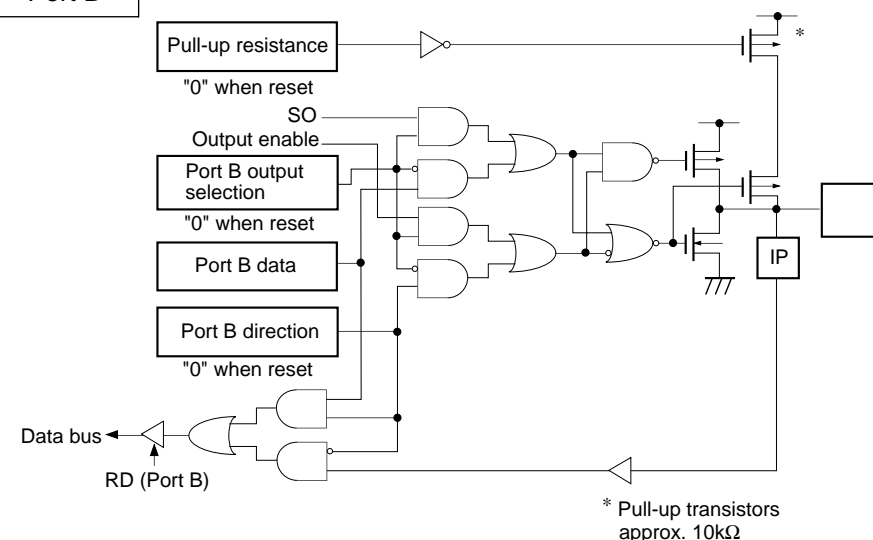
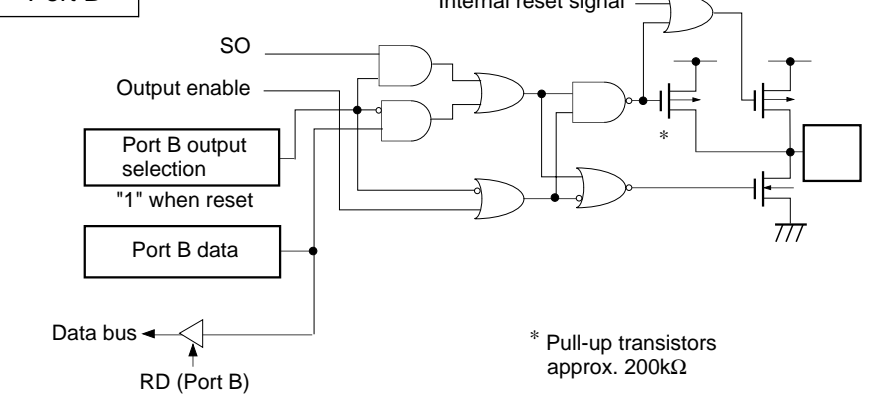
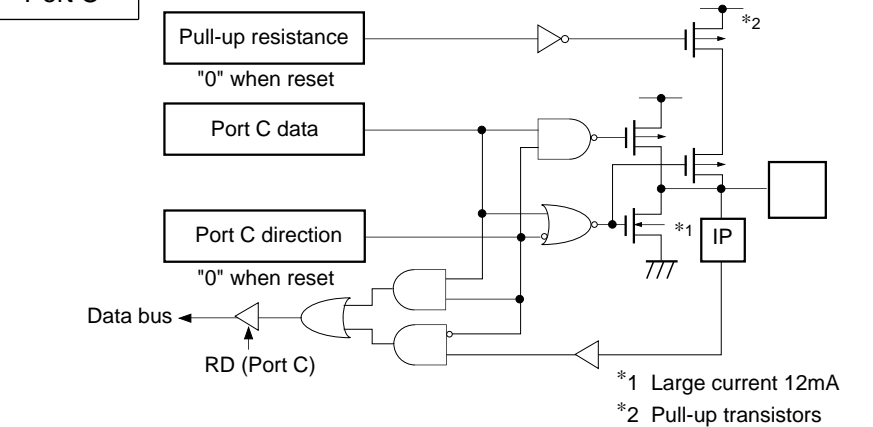
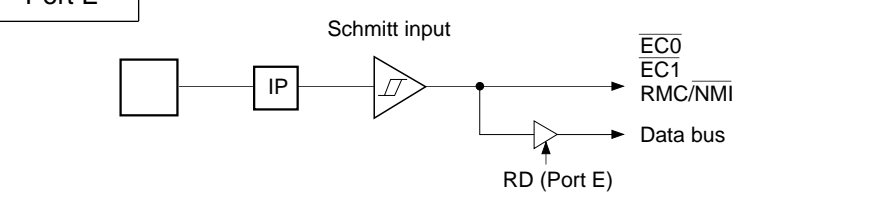
Pin Description

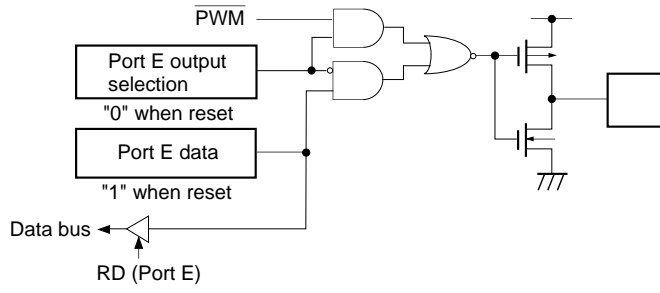
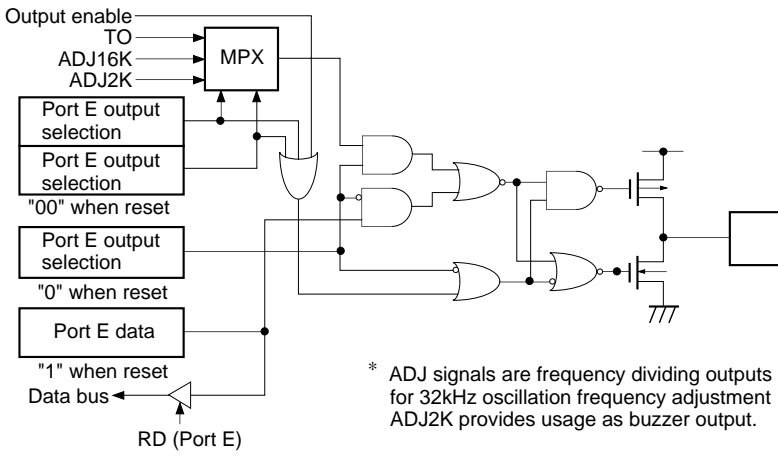
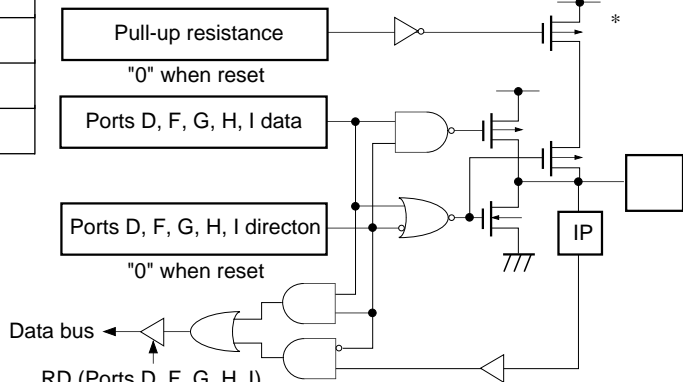
Pin code	I/O	Functions	
PA0/AN0 to PA7/AN7	I/O/Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of the pull-up resistance can be set through the software in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (8 pins)
PB0/CINT	I/O/Input	(Port B) Lower 7-bit I/O port in which I/O can be set in a unit of single bits. Also, an uppermost bit (PB7) exclusively for output. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	External capture input to 16-bit timer/counter.
PB1/ $\overline{\text{CS}}_0$	I/O/Input		Chip select input for serial interface (CH0).
PB2/ $\overline{\text{SCK}}_0$	I/O/I/O		Serial clock I/O (CH0).
PB3/SI0	I/O/Input		Serial data input (CH0).
PB4/SO0	I/O/Output		Serial data output (CH0).
PB5/ $\overline{\text{SCK}}_1$	I/O/I/O		Serial clock I/O (CH1).
PB6/SI1	I/O/Input		Serial data input (CH1).
PB7/SO1	Output/Output		Serial data output (CH1).
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Capable of driving 12mA sync current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PD0 to PD7	I/O	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PE0/ $\overline{\text{EC}}_0$	Input/Input	(Port E) 6-bit port. Lower 4 bits are for inputs; upper 2 bits are for outputs. (6 pins)	External event inputs for timer/counter. (2 pins)
PE1/ $\overline{\text{EC}}_1$	Input/Input		
PE2/RMC	Input/Input		Remote control reception circuit input.
PE3/ $\overline{\text{NMI}}$	Input/Input		Non-maskable interruption request input.
PE4/ $\overline{\text{PWM}}$	Output/Output		14-bit PWM output.
PE5/TO/ADJ Output	Output/Output/ Output		Rectangular wave output for 16-bit timer/counter and output for 32kHz oscillation frequency demultiplication.
PF0 to PF7	I/O	(Port F) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	

Pin code	I/O	Functions	
PG0 to PG7	I/O	(Port G) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PH0 to PH7	I/O	(Port H) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PI0/INT0 to PI3/INT3	I/O/Input	(Port I) 8-bit I/O ports. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	External interruption request inputs. (4 pins)
PI4 to PI7	I/O		
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL	Output		
TEX	Input	Crystal connectors for 32kHz timer/counter clock oscillaton circuit. For usage as event counter, input to TEX, and open TX.	
TX	Output		
$\overline{\text{RST}}$	Input	Low-level active, system reset.	
NC		NC. Under normal operating conditions, connect to V _{DD} .	
AV _{REF}	Input	Reference voltage input for A/D converter.	
AV _{SS}		A/D converter GND.	
V _{DD}		V _{CC} supply.	
V _{SS}		GND	

I/O Circuit Format for Pins

Pin	Circuit format	When reset
<p>PA0/AN0 to PA7/AN7</p> <p>8 pins</p>	<p>Port A</p> <p>Pull-up resistance "0" when reset</p> <p>Port A data</p> <p>Port A direction "0" when reset</p> <p>Data bus ←</p> <p>RD (Port A)</p> <p>Port A input selection "0" when reset</p> <p>A/D converter</p> <p>Input multiplexer</p> <p>IP Input protection circuit</p> <p>* Pull-up transistors approx. 10kΩ</p>	<p>Hi-Z</p>
<p>PB0/CINT PB1/$\overline{CS0}$ PB3/SI0 PB6/SI1</p> <p>4 pins</p>	<p>Port B</p> <p>Pull-up resistance "0" when reset</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus ←</p> <p>RD (Port B)</p> <p>Schmitt input</p> <p>CINT CS0 SI0 SI1</p> <p>IP</p> <p>* Pull-up transistors approx. 10kΩ</p>	<p>Hi-Z</p>
<p>PB2/$\overline{SCK0}$ PB5/$\overline{SCK1}$</p> <p>2 pins</p>	<p>Port B</p> <p>Pull-up resistance "0" when reset</p> <p>SCK OUT Output enable</p> <p>Port B output selection "0" when reset</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus ←</p> <p>RD (Port B)</p> <p>Schmitt input</p> <p>SCK in</p> <p>IP</p> <p>* Pull-up transistors approx. 10kΩ</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PB4/SO0</p> <p>1 pin</p>	<p>Port B</p>  <p>* Pull-up transistors approx. 10kΩ</p>	<p>Hi-Z</p>
<p>PB7/SO1</p> <p>1 pin</p>	<p>Port B</p>  <p>* Pull-up transistors approx. 200kΩ</p>	<p>High level (with approx. 200kΩ resistor when reset)</p>
<p>PC0 to PC7</p> <p>8 pins</p>	<p>Port C</p>  <p>*1 Large current 12mA *2 Pull-up transistors approx. 10kΩ</p>	<p>Hi-Z</p>
<p>PE0/EC0 PE1/EC1 PE2/RMC PE3/NMI</p> <p>4 pins</p>	<p>Port E</p> 	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PE4/PWM</p> <p>1 pin</p>	<p>Port E</p> 	<p>High level</p>
<p>PE5/TO/ADJ</p> <p>1 pin</p>	<p>Port E</p>  <p>* ADJ signals are frequency dividing outputs for 32kHz oscillation frequency adjustment ADJ2K provides usage as buzzer output.</p>	<p>High level</p>
<p>PD0 to PD7 PF0 to PF7 PG0 to PG7 PH0 to PH7 PI4 to PI7</p> <p>36 pins</p>	<p>Port D Port F Port G Port H Port I</p>  <p>* Pull-up transistors approx. 10kΩ</p>	<p>Hi-Z</p>

Absolute Maximum Ratings

(V_{SS} = 0V reference)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V _{DD}	-0.3 to +7.0	V	
	AV _{SS}	-0.3 to +0.3	V	
Input voltage	V _{IN}	-0.3 to +7.0*1	V	
Output voltage	V _{OUT}	-0.3 to +7.0*1	V	
High level output current	I _{OH}	-5	mA	Output per pin
High level total output current	∑I _{OH}	-50	mA	Total for all output pins
Low level output current	I _{OL}	15	mA	Value per pin, excluding large current outputs
	I _{OLC}	20	mA	Value per pin*2 for large current outputs
Low level total output current	∑I _{OL}	100	mA	Total for all output pins
Operating temperature	T _{opr}	-20 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	600	mW	

*1) V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*2) The large current drive transistor is the N-ch transistor of Port C (PC).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	4.5	5.5	V	Guaranteed operation range for high speed mode*1
		3.5	5.5		Guaranteed operation range for low speed mode*1
		2.7	5.5		Guaranteed operation range with TEX clock
		2.5	5.5		Guaranteed data hold range during STOP
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*2
	V _{IHS}	0.8V _{DD}	V _{DD}	V	Hysteresis input*3
	V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL*4
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	*2
	V _{ILS}	0	0.2V _{DD}	V	Hysteresis input*3
	V _{ILEX}	-0.3	0.4	V	EXTAL*4
Operating temperature	T _{opr}	-20	+75	°C	

*1) High speed mode is 1/2 frequency dividing clock selection; low-speed mode is 1/16 frequency dividing clock selection.

*2) Value for each pin of normal input ports (PA, PB3, PB4, PB6, PC, PD, PF to PH, PI4 to PI7).

*3) Value of the following pins: \overline{RST} , CINT, $\overline{CS0}$, $\overline{SCK0}$, $\overline{SCK1}$, $\overline{EC0}$, $\overline{EC1}$, RMC, $\overline{NM1}$, INT0, INT1, INT2, INT3.

*4) Specifies only during external clock input.

Electrical Characteristics

DC Characteristics

(Ta = -20 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit	
High level output current	V _{OH}	PA to PD, PE4, PE5, PF to PI	V _{DD} = 4.5V, I _{OH} = -0.5mA	4.0			V	
			V _{DD} = 4.5V, I _{OH} = -1.2mA	3.5			V	
V _{OL}	V _{DD} = 4.5V, I _{OL} = 1.8mA				0.4		V	
	V _{DD} = 4.5V, I _{OL} = 3.6mA				0.6		V	
Low level output current	V _{OL}	PC	V _{DD} = 4.5V, I _{OL} = 12.0mA			1.5	V	
		Input current	EXTAL	I _{IHE}	V _{DD} = 5.5V, V _{IH} = 5.5V	0.5		40
I _{ILE}	V _{DD} = 5.5V, V _{IL} = 0.4V			-0.5		-40	μA	
TEX	I _{IHT}		V _{DD} = 5.5V, V _{IL} = 5.5V	0.1		10	μA	
	I _{ILT}			-0.1		-10	μA	
I _{ILR}	$\overline{\text{RST}}^{*1}$		V _{DD} = 5.5V, V _{IL} = 0.4V	-1.5		-400	μA	
I _{IL}	PA to PD ^{*2} , PF to PI ^{*2}					-2.0	mA	
			V _{DD} = 4.5V, V _{IL} = 4.0V	-10			μA	
I/O leakage current	I _{Iz}	PE0 to PE3, $\overline{\text{RST}}^{*1}$	V _{DD} = 5.5V, V _I = 0, 5.5V			±10	μA	
Power supply current ^{*3}	I _{DD1}	V _{DD}	High-speed mode operation (1/2 frequency dividing clock)		32	52	mA	
			V _{DD} = 5.5V, 20MHz crystal oscillation (C ₁ = C ₂ = 15pF)					
	I _{DD2}		V _{DD} = 3V, 32kHz crystal oscillation (C ₁ = C ₂ = 47pF)		38	100	μA	
	I _{DDS1}		SLEEP mode					
			V _{DD} = 5.5V, 20MHz crystal oscillation (C ₁ = C ₂ = 15pF)		1.4	10	mA	
I _{DDS2}	V _{DD} = 3V, 32kHz crystal oscillation (C ₁ = C ₂ = 47pF)		9	30	μA			
I _{DDS3}	STOP mode							
			V _{DD} = 5.5V, termination of 20MHz and 32kHz crystal oscillation			10	μA	
Input capacity	C _{IN}	PA, PB0 to PB6, PC, PD, PE0 to PE3, PF to PI, EXTAL, XTAL, TEX, TX, $\overline{\text{RST}}$	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF	

*1) $\overline{\text{RST}}$ specifies the input current when pull-up resistance has been selected; leakage current when no resistance has been selected.

*2) PA to PD, and PF to PI pins specify the input current when pull-up resistance has been selected; leakage current when no resistance has been selected. (Excludes output PB7)

*3) When all pins are open.

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	1		20	MHz
System clock input pulse width	t _{XL} , t _{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	23.0			ns
System clock input rise time, fall time	t _{CR} , t _{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	t _{EH} , t _{EL}	$\overline{\text{EC0}}$ EC1	Fig. 3	t _{sys} + 50*1			ns
Event count input clock rise time, fall time	t _{ER} , t _{EF}	$\overline{\text{EC0}}$ EC1	Fig. 3			20	ms
System clock frequency	fc	TEX TX	VDD = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count input clock input pulse width	t _{TL} , t _{TH}	TEX	Fig. 3	10			μs
Event count input clock rise time, fall time	t _{TR} , t _{TF}	TEX	Fig. 3			20	ms

*1) t_{sys} indicates the three values below according to the upper two bits (CPU clock selected) of the control clock register (address: 00FEH).

t_{sys} (ns) = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Fig. 1. Clock timing

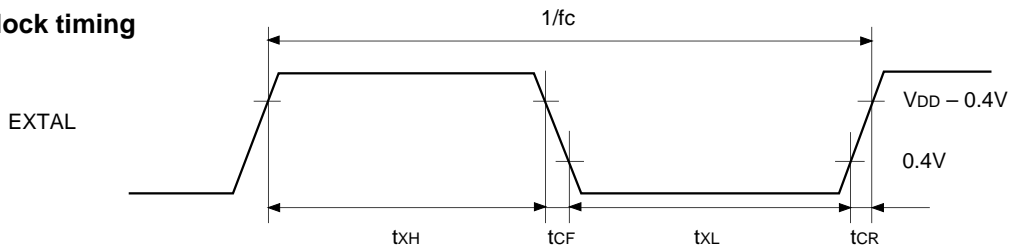


Fig. 2. Clock applied conditions

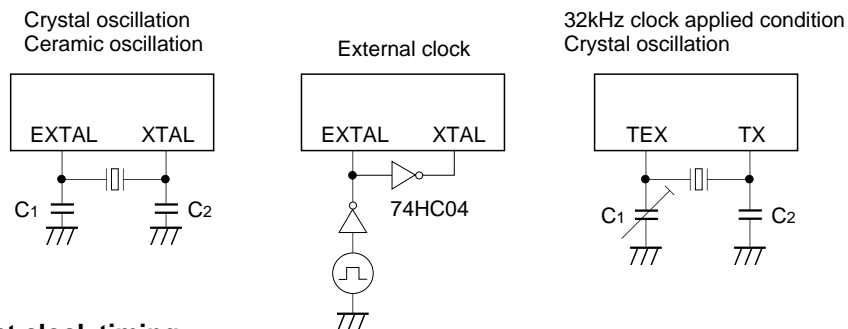
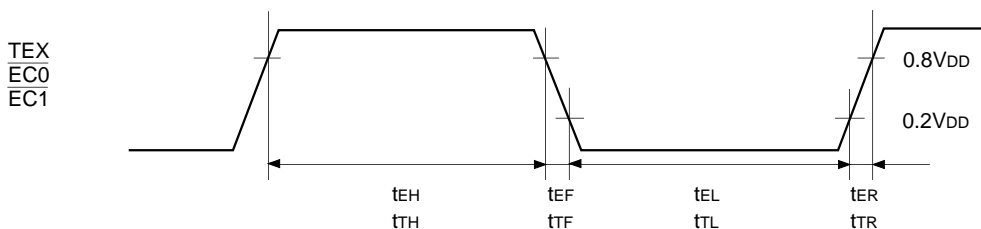


Fig. 3. Event count clock timing



(2) Serial transfer (CH0)

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, Vss reference)

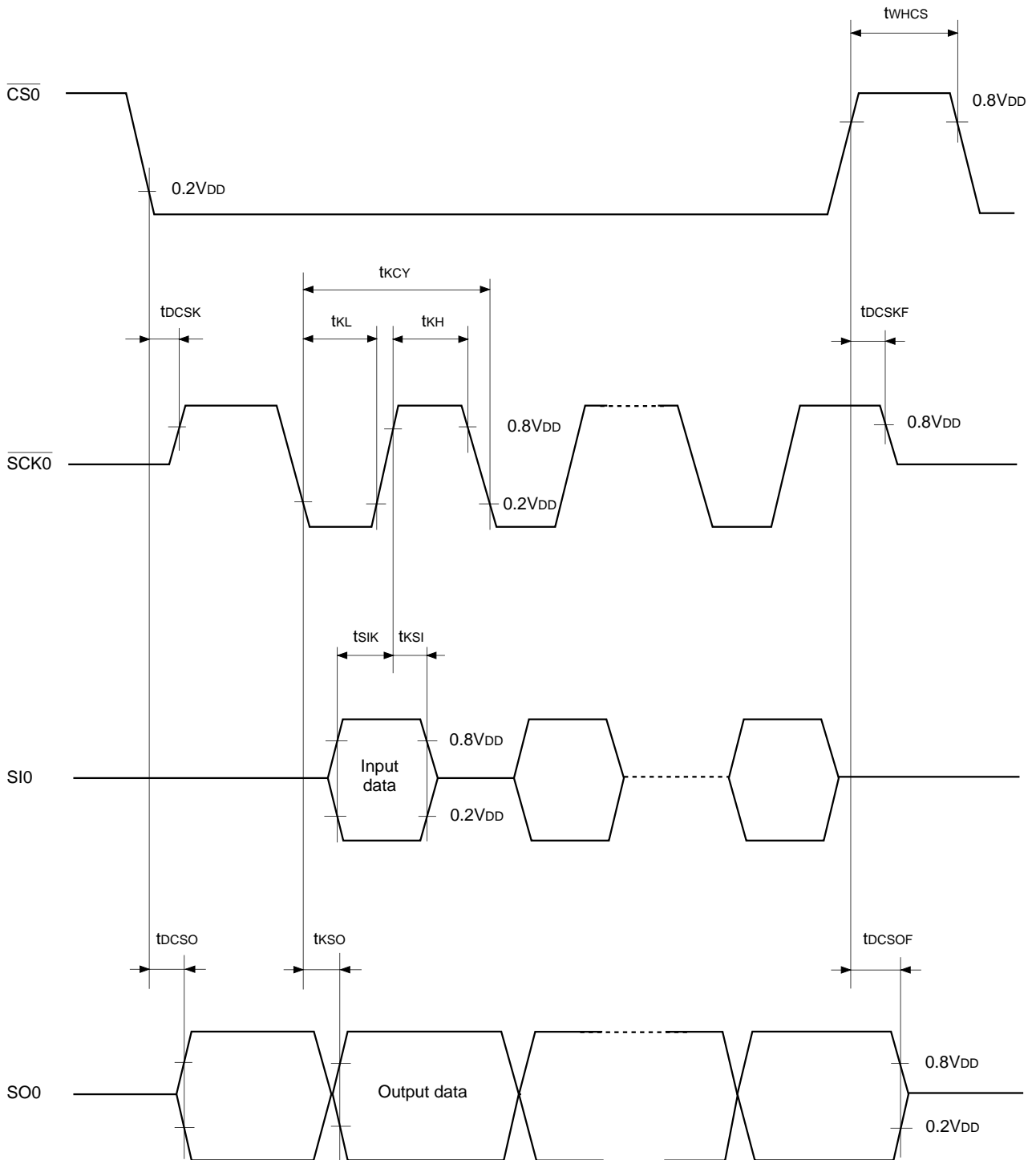
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ delay time	t _{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		t _{sys} + 200	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ float delay time	t _{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		t _{sys} + 200	ns
$\overline{CS0} \downarrow \rightarrow SO0$ delay time	t _{DCSO}	SO0	Chip select transfer mode		t _{sys} + 200	ns
$\overline{CS0} \uparrow \rightarrow SO0$ float delay time	t _{DCSOF}	SO0	Chip select transfer mode		t _{sys} + 200	ns
$\overline{CS0}$ High level width	t _{WHCS}	$\overline{CS0}$	Chip select transfer mode	t _{sys} + 200		ns
$\overline{SCK0}$ cycle time	t _{KCY}	$\overline{SCK0}$	Input mode	2t _{sys} + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ High, Low level width	t _{KH} t _{KL}	$\overline{SCK0}$	Input mode	t _{sys} + 100		ns
			Output mode	8000/fc - 50		ns
SI0 input set-up time (for $\overline{SCK0} \uparrow$)	t _{SIK}	SI0	$\overline{SCK0}$ input mode	100		ns
			$\overline{SCK0}$ output mode	200		ns
SI0 input hold time (for $\overline{SCK0} \uparrow$)	t _{KSI}	SI0	$\overline{SCK0}$ input mode	t _{sys} + 200		ns
			$\overline{SCK0}$ output mode	100		ns
$\overline{SCK0} \downarrow \rightarrow SO0$ delay time	t _{KSO}	SO0	$\overline{SCK0}$ input mode		t _{sys} +200	ns
			$\overline{SCK0}$ output mode		100	ns

Note 1) t_{sys} indicates the three values below according to the upper two bits (CPU clock selected) of the control clock register (address: 00FEH).

t_{sys} (ns) = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Note 2) The load condition for the $\overline{SCK0}$ output mode, SO0 output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer CH0 timing



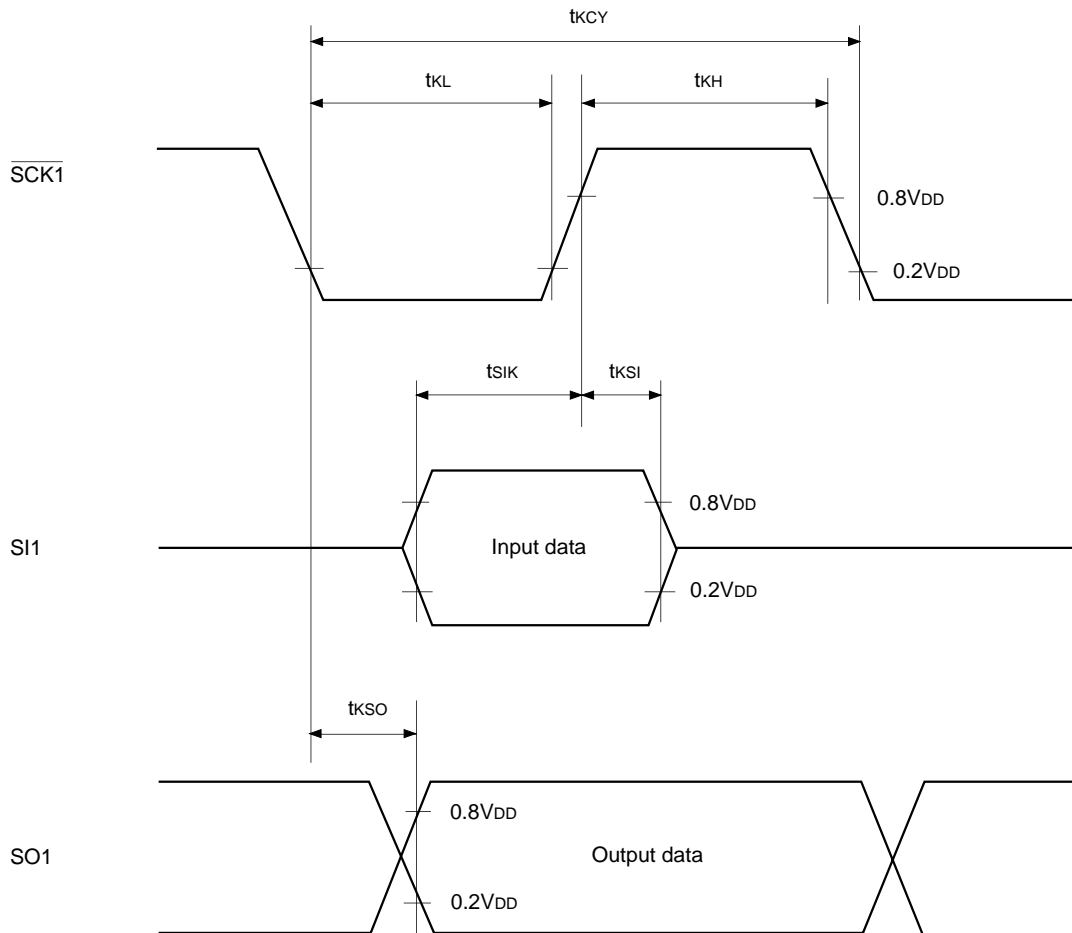
Serial transfer (CH1)

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY}	$\overline{\text{SCK1}}$	Input mode	1000		ns
			Output mode	$16000/f_c$		ns
$\overline{\text{SCK1}}$ High, Low level width	t_{KH} t_{KL}	$\overline{\text{SCK1}}$	Input mode	400		ns
			Output mode	$8000/f_c - 50$		ns
SI1 input set-up time (for $\overline{\text{SCK1}} \uparrow$)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (for $\overline{\text{SCK1}} \uparrow$)	t_{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	200		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}} \downarrow \rightarrow \text{SO1}$ delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		200	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

Note) The load condition for the $\overline{\text{SCK1}}$ output mode, SO1 output delay time is $50\text{pF} + 1\text{TTL}$.

Fig. 5. Serial transfer CH1 timing

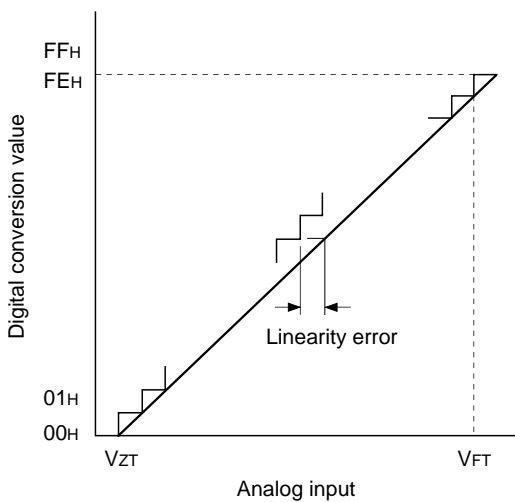


(3) A/D converter characteristics

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $AV_{REF} = 4.0$ to V_{DD} , $V_{SS} = AV_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error						± 5	LSB
Zero transition voltage	V_{ZT}^{*1}		$T_a = 25^\circ\text{C}$ $V_{DD} = AV_{REF} = 5.0\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$	-10	10	110	mV
Full-scale transition voltage	V_{FT}^{*2}			4870	4970	5070	mV
Conversion time	t_{CONV}			$160/f_{ADC}^{*3}$			μs
Sampling time	t_{SAMP}			$12/f_{ADC}^{*3}$			μs
Reference input voltage	V_{REF}	AV_{REF}		$V_{DD} - 0.5$		V_{DD}	V
Analog input voltage	V_{IAN}	$AN0$ to $AN7$		0		AV_{REF}	V
AVREF current	I_{REF}	AV_{REF}	Operation mode		0.6	1.0	mA
	I_{REFS}		SLEEP mode STOP mode 32kHz operation mode			10	μA

Fig. 6. Definition of A/D converter terms



*1) V_{ZT} : Value at which the digital transfer value changes from 00H to 01H and vice versa.

*2) V_{FT} : Value at which the digital transfer value changes from FEH to FFH and vice versa.

*3) f_{ADC} indicates the values below due to the contents of bit 6 (CKS) of the A/D control register (ADC: 00F9H) and bits 7 (PCK1) and 6 (PCK0) of the clock control register (CLC: 00FEH).

PCK1, 0 \ CKS	0 ($\phi/2$ selection)	1 (ϕ selection)
	00 ($\phi = f_{EX}/2$)	$f_{ADC} = f_c/2$
01 ($\phi = f_{EX}/4$)	$f_{ADC} = f_c/4$	$f_{ADC} = f_c/2$
11 ($\phi = f_{EX}/16$)	$f_{ADC} = f_c/16$	$f_{ADC} = f_c/8$

(4) Interruption, reset input (Ta = -20 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption High, Low level width	t _{IH} t _{IL}	INT0 INT1 INT2 INT3 $\overline{\text{NMI}}$		1		μs
Reset input Low level width	t _{RSL}	$\overline{\text{RST}}$		32/fc		μs

Fig 7. Interruption input timing

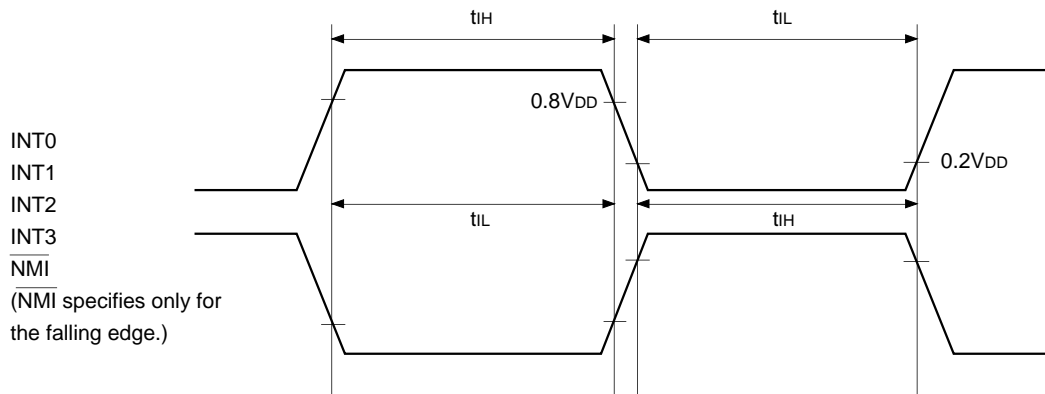
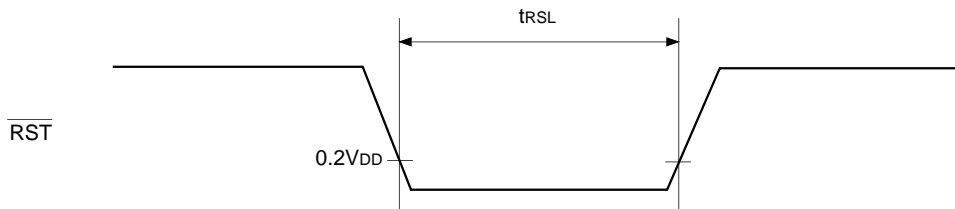


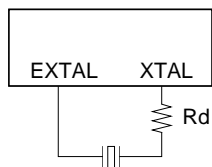
Fig. 8. $\overline{\text{RST}}$ input timing



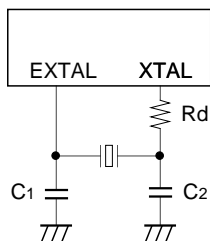
Appendix

Fig. 9. Recommended oscillation circuit

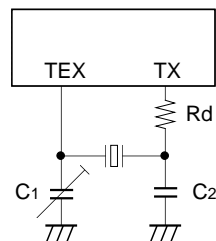
(i) Main clock



(ii) Main clock



(iii) Sub clock



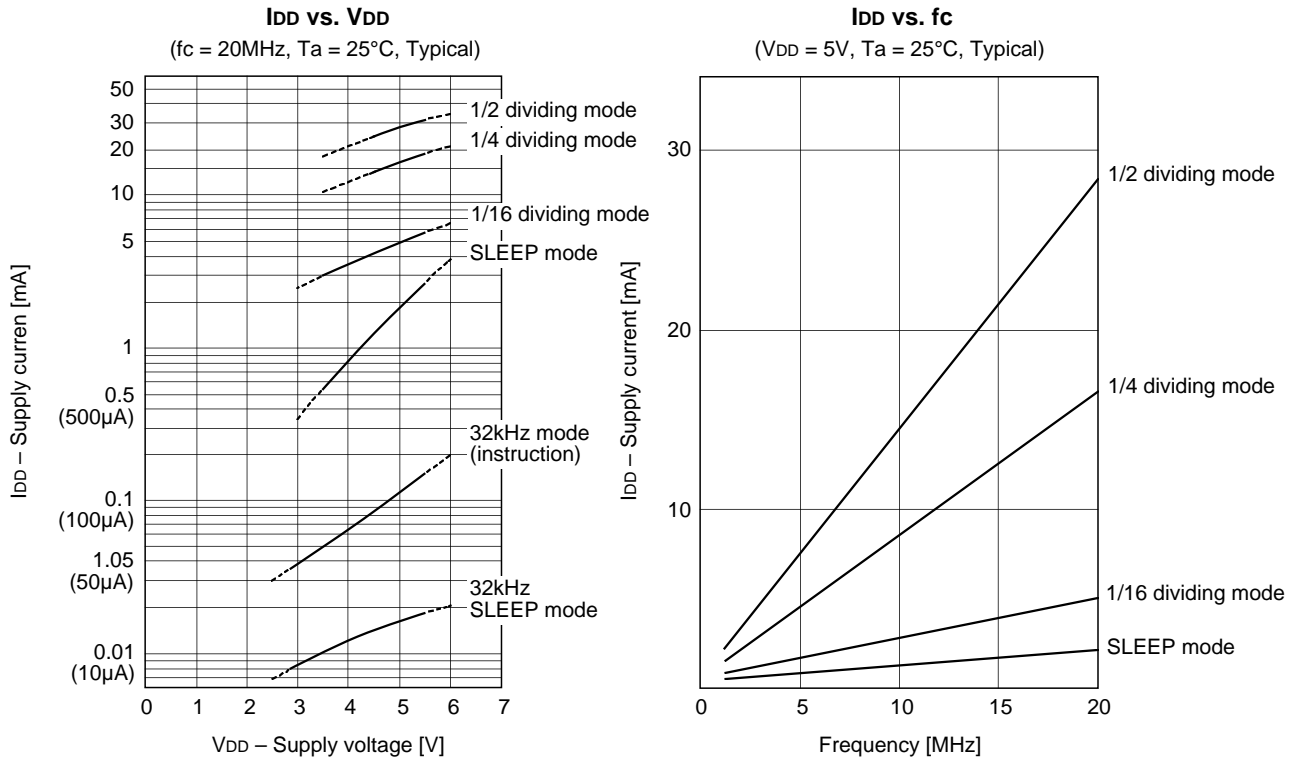
Products List

Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example
MURATA MFG CO., LTD.	CSA16.00MXZ072	16.00	0	0	0	(i)
	CSA20.00MXZ046	20.00				
RIVER ELETEC CO., LTD.	HC-49/U03	16.00	8	8	0	(ii)
		20.00	6	6		
KINSEKI LTD.	P3	32.768kHz	50	22	1M	(iii)

Mask option table

Item	Content	
	Reset pin pull-up resistance	Non-existent

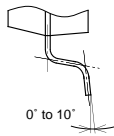
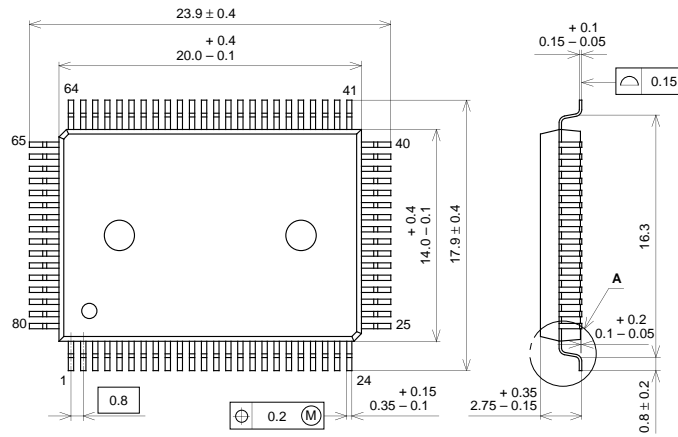
Example of Representative Characteristics



Package Outline

Unit: mm

80PIN QFP (PLASTIC)

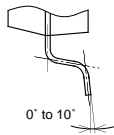
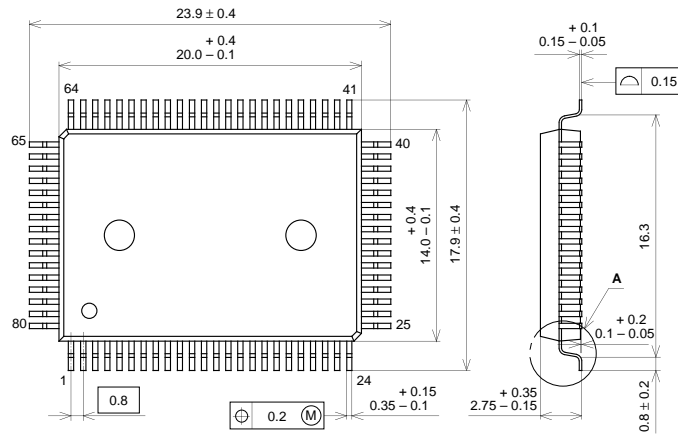


DETAIL A

SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	

PACKAGE STRUCTURE	
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g

80PIN QFP (PLASTIC)



DETAIL A

SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	

PACKAGE STRUCTURE	
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	1.6g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	42 ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18μm



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