

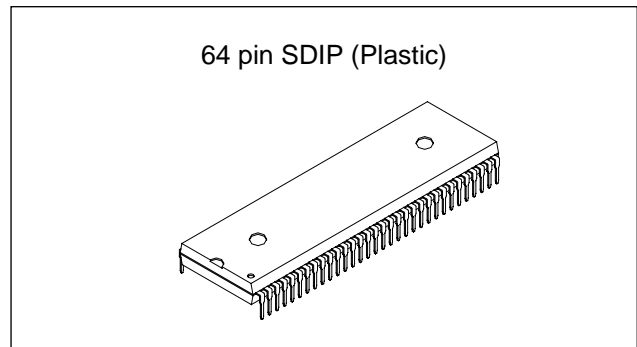
## CMOS 8-bit Single Chip Microcomputer

### Description

The CXP842P24 is a CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time base timer, capture timer/counter, and remote control reception circuit besides the basic configurations of 8-bit CPU, ROM, RAM, and I/O port.

The CXP842P24 also provides a power-on reset function and a sleep/stop function that enables lower power consumption.

This IC is the PROM-incorporated version of the CXP84224 with built-in mask ROM. This provides the additional feature of being able to write directly into the program. Thus, it is most suitable for evaluation use during system development and for small-quantity production.



### Structure

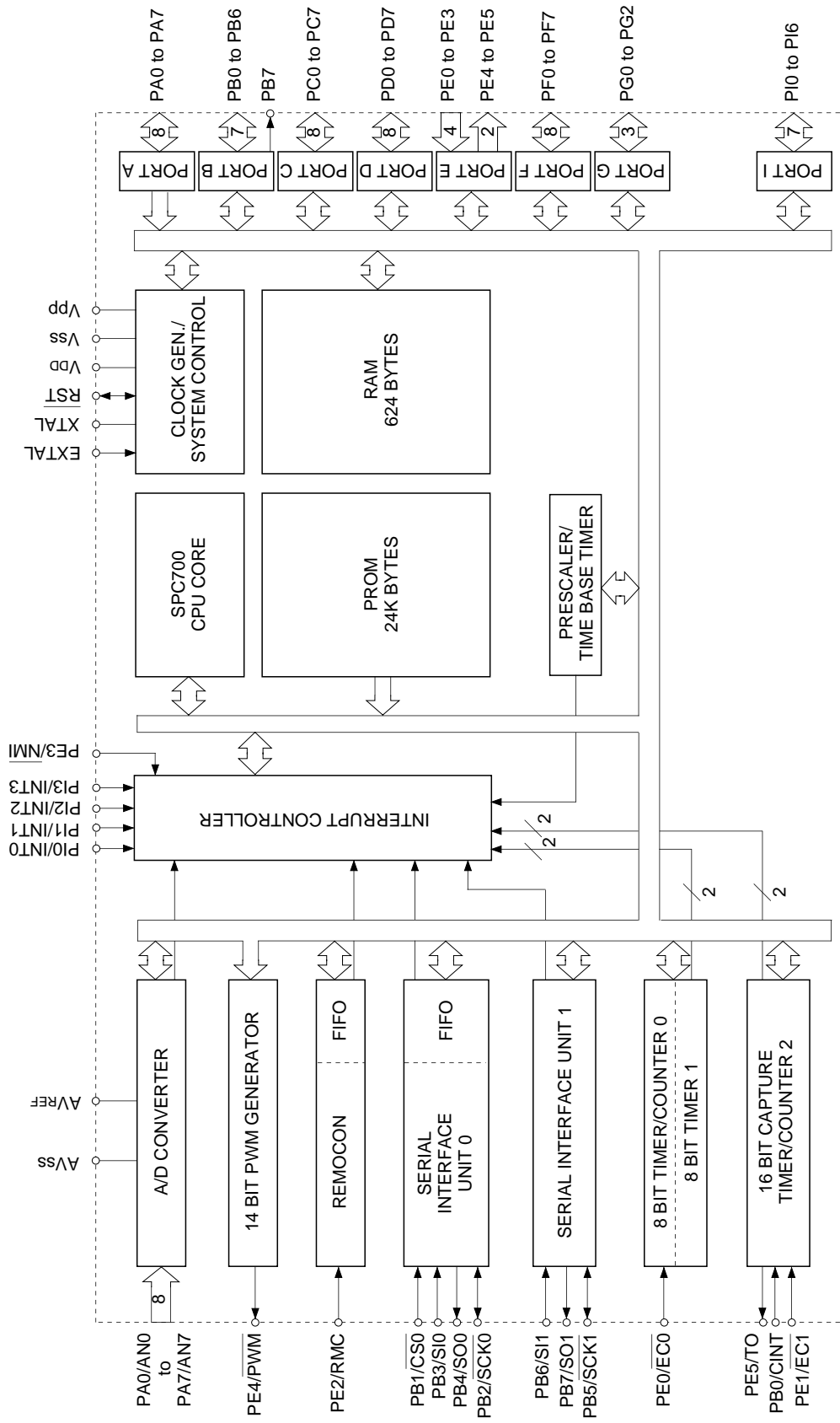
Silicon gate CMOS IC

### Features

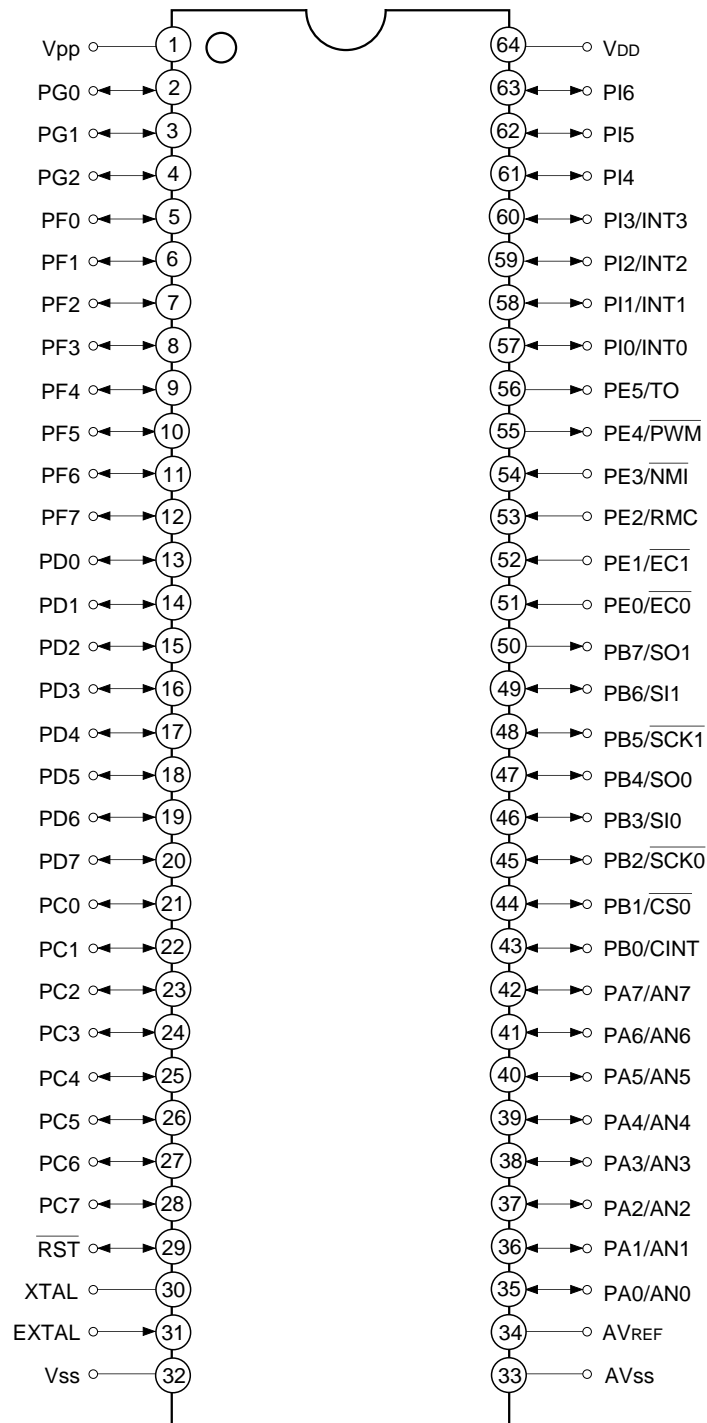
- Wide-range instruction system (213 instructions) to cover various types of data
  - 16-bit arithmetic/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle                      400ns at 10MHz operation
- Incorporated PROM capacity                      24K bytes
- Incorporated RAM capacity                        624 bytes
- Peripheral functions
  - A/D converter                                      8 bits, 8 channels, successive approximation method  
(Conversion time of 32 $\mu$ s/10MHz)
  - Serial interface                                    Incorporated 8-bit, 8-stage FIFO  
(Auto transfer for 1 to 8 bytes), 1 channel  
8-bit clock synchronization, 1 channel
  - Timer    8-bit timer  
8-bit timer/counter  
19-bit time base timer  
16-bit capture timer/counter
  - Remote control reception circuit            8-bit pulse measuring counter, 6-stage FIFO
  - PWM output                                        14 bits, 1 channel
- Interruption                                         14 factors, 14 vectors, multi-interruption possible
- Standby mode                                        Sleep/stop
- Package     64-pin plastic SDIP

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Block Diagram



Pin Assignment (Top View)



**Note)** Vpp (Pin 1) is always connected to VDD.

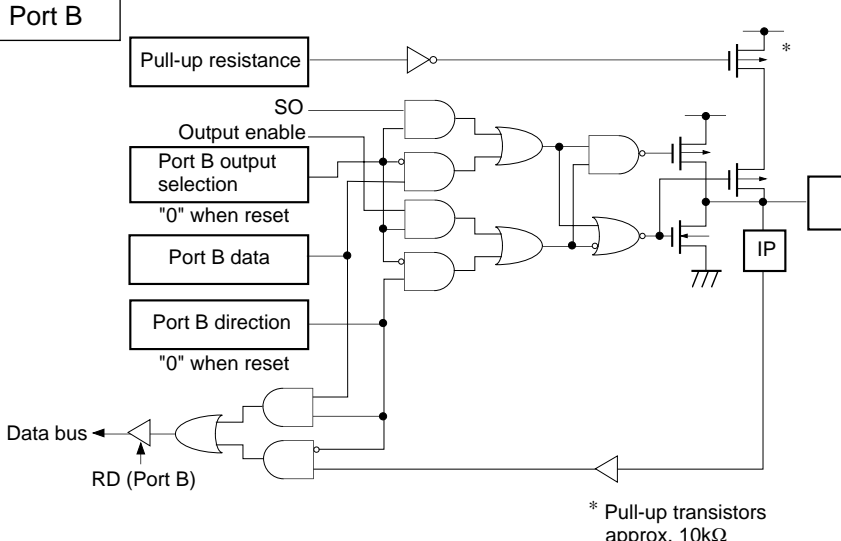
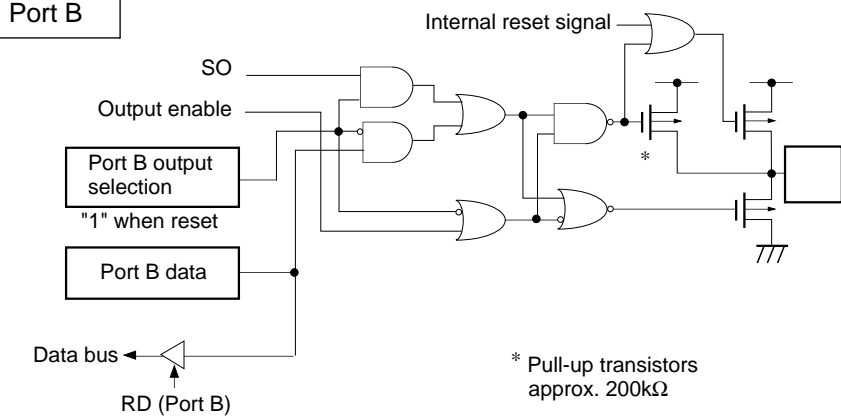
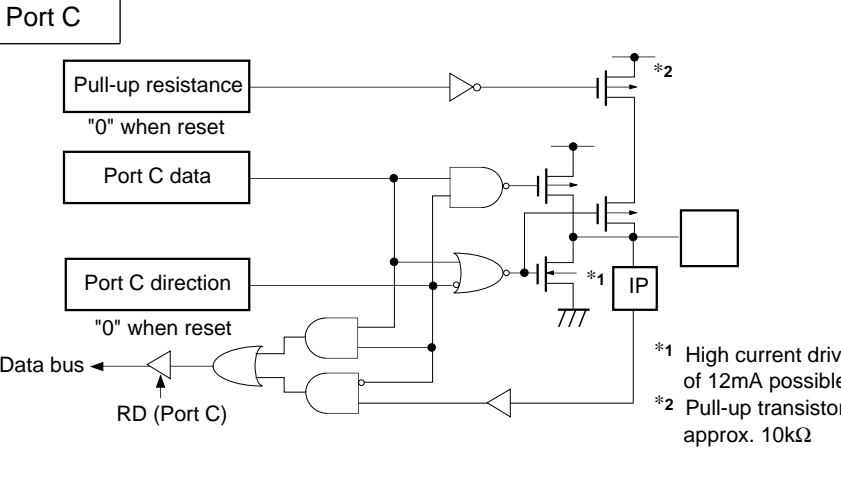
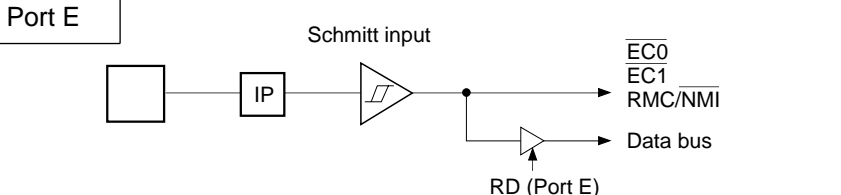
Pin Description

Symbol	I/O	Description	
PA0/AN0 to PA7/AN7	I/O/Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of the pull-up resistance can be set through the software in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (8 pins)
PB0/CINT	I/O/Input	(Port B) Lower 7-bit I/O port in which I/O can be set in a unit of single bits. Also, an uppermost bit (PB7) exclusively for output. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	External capture input to 16-bit timer/counter.
PB1/ $\overline{\text{CS}}_0$	I/O/Input		Chip select input for serial interface (CH0).
PB2/ $\overline{\text{SCK}}_0$	I/O/I/O		Serial clock I/O (CH0).
PB3/SI0	I/O/Input		Serial data input (CH0).
PB4/SO0	I/O/Output		Serial data output (CH0).
PB5/ $\overline{\text{SCK}}_1$	I/O/I/O		Serial clock I/O (CH1).
PB6/SI1	I/O/Input		Serial data input (CH1).
PB7/SO1	Output/Output		Serial data output (CH1).
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Capable of driving 12mA sink current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PD0 to PD7	I/O	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PE0/ $\overline{\text{EC}}_0$	Input/Input	(Port E) 6-bit port. Lower 4 bits are for inputs; upper 2 bits are for outputs. Incorporation of pull-up resistor can be set through the software. (6 pins)	External event inputs for timer/counter. (2 pins)
PE1/ $\overline{\text{EC}}_1$	Input/Input		
PE2/RMC	Input/Input		Remote control reception circuit input.
PE3/ $\overline{\text{NMI}}$	Input/Input		Non-maskable interruption request input.
PE4/ $\overline{\text{PWM}}$	Output/Output		14-bit PWM output.
PE5/TO	Output/Output		Rectangular wave output for 16-bit timer/counter (duty output 50%).
PF0 to PF7	I/O	(Port F) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	

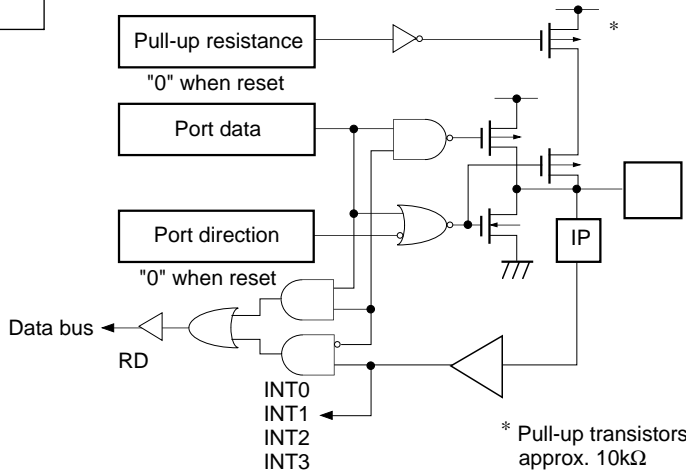
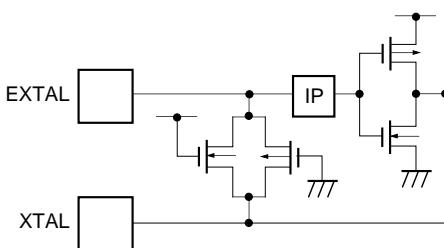
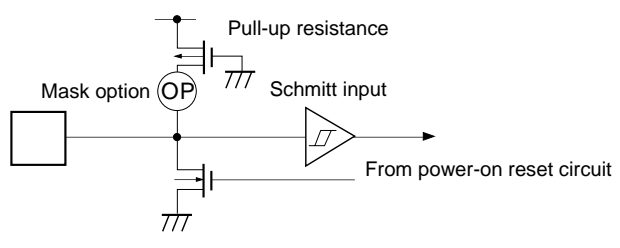
Symbol	I/O	Description	
PG0 to PG2	I/O	(Port G) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (3 pins)	
PI0/INT0 to PI3/INT3	I/O/Input	(Port I) 7-bit I/O ports. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (7 pins)	External interruption request inputs.
PI4 to PI6	I/O		
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL	Output		
$\overline{\text{RST}}$	I/O	Low-level active, system reset.	
AVREF	Input	Reference voltage input for A/D converter.	
AVss		A/D converter GND.	
VDD		Positive power supply.	
Vpp		Positive power supply for incorporated PROM writing. Connect to VDD during normal operation.	
Vss		GND	

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
<p>PA0/AN0 to PA7/AN7</p> <p>8 pins</p>	<p>Port A</p> <p>Pull-up resistance "0" when reset</p> <p>Port A data</p> <p>Port A direction "0" when reset</p> <p>Data bus ←</p> <p>RD (Port A)</p> <p>Port A input selection "0" when reset</p> <p>Input multiplexer</p> <p>A/D converter</p> <p>* Pull-up transistors approx. 10kΩ</p>	<p>Hi-Z</p>
<p>PB0/CINT PB1/CS0 PB3/SI0 PB6/SI1</p> <p>4 pins</p>	<p>Port B</p> <p>Pull-up resistance "0" when reset</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus ←</p> <p>RD (Port B)</p> <p>Schmitt input</p> <p>CINT CS0 SI0 SI1</p> <p>* Pull-up transistors approx. 10kΩ</p>	<p>Hi-Z</p>
<p>PB2/SCK0 PB5/SCK1</p> <p>2 pins</p>	<p>Port B</p> <p>Pull-up resistance "0" when reset</p> <p>SCK OUT</p> <p>Output enable</p> <p>Port B output selection "0" when reset</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus ←</p> <p>RD (Port B)</p> <p>Schmitt input</p> <p>SCK in</p> <p>* Pull-up transistors approx. 10kΩ</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PB4/SO0</p> <p>1 pin</p>	<p>Port B</p>  <p>* Pull-up transistors approx. 10kΩ</p>	<p>Hi-Z</p>
<p>PB7/SO1</p> <p>1 pin</p>	<p>Port B</p>  <p>* Pull-up transistors approx. 200kΩ</p>	<p>High level</p>
<p>PC0 to PC7</p> <p>8 pins</p>	<p>Port C</p>  <p>*1 High current drive of 12mA possible *2 Pull-up transistors approx. 10kΩ</p>	<p>Hi-Z</p>
<p>PE0/EC0 PE1/EC1 PE2/RMC PE3/NMI</p> <p>4 pins</p>	<p>Port E</p> 	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PE4/PWM</p> <p>1 pin</p>	<p>Port E</p>	<p>High level</p>
<p>PE5/TO</p> <p>1 pin</p>	<p>Port E</p>	<p>High level</p>
<p>PD0 to PD7 PF0 to PF7 PG0 to PG2 PI4 to PI6</p> <p>22 pins</p>	<p>Port D Port F Port G Port I</p> <p>* Pull-up transistors approx. 10kΩ</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PI0/INT0 to PI3/INT3</p> <p>4 pins</p>	<p>Port I</p>  <p>* Pull-up transistors approx. 10kΩ</p>	<p>Hi-Z</p>
<p>EXTAL XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> <li>• Diagram shows circuit composition during oscillation.</li> <li>• Feedback resistor is removed during stop.</li> </ul>	<p>Oscillation</p>
<p><math>\overline{\text{RST}}</math></p> <p>1 pin</p>	 <p>Pull-up resistance</p> <p>Mask option OP</p> <p>Schmitt input</p> <p>From power-on reset circuit</p>	<p>Low level</p>

## Absolute Maximum Ratings

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V <sub>DD</sub>	-0.3 to +7.0	V	
	V <sub>pp</sub>	-0.3 to +13.0	V	Incorporated PROM
	AV <sub>SS</sub>	-0.3 to +0.3	V	
Input voltage	V <sub>IN</sub>	-0.3 to +7.0*1	V	
Output voltage	V <sub>OUT</sub>	-0.3 to +7.0*1	V	
High level output current	I <sub>OH</sub>	-5	mA	Output per pin
High level total output current	∑I <sub>OH</sub>	-50	mA	Total for all output pins
Low level output current	I <sub>OL</sub>	15	mA	Value per pin, excluding large current outputs
	I <sub>OLC</sub>	20	mA	Value per pin*2 for large current outputs
Low level total output current	∑I <sub>OL</sub>	100	mA	Total for all output pins
Operating temperature	T <sub>opr</sub>	-10 to +75	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	
Allowable power dissipation	P <sub>D</sub>	1000	mW	

\*1 V<sub>IN</sub> and V<sub>OUT</sub> must not exceed V<sub>DD</sub> + 0.3V.

\*2 The high current drive transistor is the N-ch transistor of Port C (PC).

**Note)** Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

## Recommended Operating Conditions

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V <sub>DD</sub>	4.5	5.5	V	High-speed mode guaranteed operation range* <sup>1</sup>
		3.5	5.5		Low-speed mode guaranteed operation range* <sup>1</sup>
		2.5	5.5		Guaranteed data hold range during stop
	V <sub>pp</sub>	V <sub>pp</sub> = V <sub>DD</sub>		V	* <sup>5</sup>
High level input voltage	V <sub>IH</sub>	0.7V <sub>DD</sub>	V <sub>DD</sub>	V	* <sup>2</sup>
	V <sub>IHS</sub>	0.8V <sub>DD</sub>	V <sub>DD</sub>	V	Hysteresis input* <sup>3</sup>
	V <sub>IHEX</sub>	V <sub>DD</sub> - 0.4	V <sub>DD</sub> + 0.3	V	EXTAL* <sup>4</sup>
Low level input voltage	V <sub>IL</sub>	0	0.3V <sub>DD</sub>	V	* <sup>2</sup>
	V <sub>ILS</sub>	0	0.2V <sub>DD</sub>	V	Hysteresis input* <sup>3</sup>
	V <sub>ILEX</sub>	-0.3	0.4	V	EXTAL* <sup>4</sup>
Operating temperature	Topr	-10	+75	°C	

\*<sup>1</sup> High-speed mode is 1/2 frequency demultiplication clock selection; low-speed mode is 1/16 frequency demultiplication clock selection.

\*<sup>2</sup> Value for each pin of normal input ports (PA, PB3, PB4, PB6, PC, PD, PF, PG, PI4 to PI6).

\*<sup>3</sup> Value of the following pins:  $\overline{\text{RST}}$ , CINT,  $\overline{\text{CS0}}$ ,  $\overline{\text{SCK0}}$ ,  $\overline{\text{SCK1}}$ ,  $\overline{\text{EC0}}$ ,  $\overline{\text{EC1}}$ , RMC,  $\overline{\text{NMI}}$ , INT0, INT1, INT2, INT3.

\*<sup>4</sup> Specifies only during external clock input.

\*<sup>5</sup> V<sub>pp</sub> and V<sub>DD</sub> should be set to the same voltage.

**Electrical Characteristics**

**DC Characteristics**

(Ta = -10 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit	
High level output voltage	V <sub>OH</sub>	PA to PD, PE4, PE5, PF, PG, PI	V <sub>DD</sub> = 4.5V, I <sub>OH</sub> = -0.5mA	4.0			V	
			V <sub>DD</sub> = 4.5V, I <sub>OH</sub> = -1.2mA	3.5			V	
V <sub>OL</sub>	V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 1.8mA				0.4	V		
	V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 3.6mA				0.6	V		
Low level output voltage	V <sub>OL</sub>	PC	V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 12.0mA			1.5	V	
		I <sub>IHE</sub>	EXTAL	V <sub>DD</sub> = 5.5V, V <sub>IH</sub> = 5.5V	0.5		40	μA
				V <sub>DD</sub> = 5.5V, V <sub>IL</sub> = 0.4V	-0.5		-40	μA
		I <sub>ILR</sub>	$\overline{\text{RST}}$	V <sub>DD</sub> = 5.5V, V <sub>IL</sub> = 0.4V	-1.5		-400	μA
I <sub>IL</sub>	PA to PD* <sup>1</sup> , PF, PG, PI* <sup>1</sup>				V <sub>DD</sub> = 4.5V, V <sub>IL</sub> = 4.0V	-10		-2.0
I/O leakage current	I <sub>Iz</sub>	PE0 to PE3	V <sub>DD</sub> = 5.5V, V <sub>I</sub> = 0, 5.5V			±10	μA	
Power supply current* <sup>2</sup>	I <sub>DD1</sub>	V <sub>DD</sub>	High-speed mode operation (1/2 frequency demultiplier clock) V <sub>DD</sub> = 5.5V, 10MHz crystal oscillation (C <sub>1</sub> = C <sub>2</sub> = 15pF)		18	40	mA	
	I <sub>DDS1</sub>		Sleep mode V <sub>DD</sub> = 5.5V, 10MHz crystal oscillation (C <sub>1</sub> = C <sub>2</sub> = 15pF)		1.1	8	mA	
	I <sub>DDS3</sub>		Stop mode V <sub>DD</sub> = 5.5V, termination of 10MHz crystal oscillation .			30	μA	
Input capacity	C <sub>IN</sub>	Pins other than PB7, PE4, PE5, AV <sub>REF</sub> , V <sub>DD</sub> , V <sub>SS</sub>	Clock 1MHz 0V for no-measured pins		10	20	pF	

\*<sup>1</sup> Pins PA to PD, and PF, PG, PI specify the input current when pull-up resistance has been selected; leakage current when no resistance has been selected. (Excludes output PB7)

\*<sup>2</sup> When all pins are open.

AC Characteristics

(1) Clock timing

( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	$f_c$	XTAL EXTAL	Fig. 1, Fig. 2	1		10	MHz
System clock input pulse width	$t_{XL}$ , $t_{XH}$	EXTAL	Fig. 1, Fig. 2 External clock drive	37.5			ns
System clock input rise time, fall time	$t_{CR}$ , $t_{CF}$	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	$t_{EH}$ , $t_{EL}$	$\overline{\text{EC0}}$ EC1	Fig. 3	$t_{\text{sys}} + 50^{*1}$			ns
Event count input clock rise time, fall time	$t_{ER}$ , $t_{EF}$	$\overline{\text{EC0}}$ EC1	Fig. 3			20	ms

\*1  $t_{\text{sys}}$  indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: 00FEH).

$t_{\text{sys}} [\text{ns}] = 2000/f_c$  (upper two bits = "00"),  $4000/f_c$  (upper two bits = "01"),  $16000/f_c$  (upper two bits = "11")

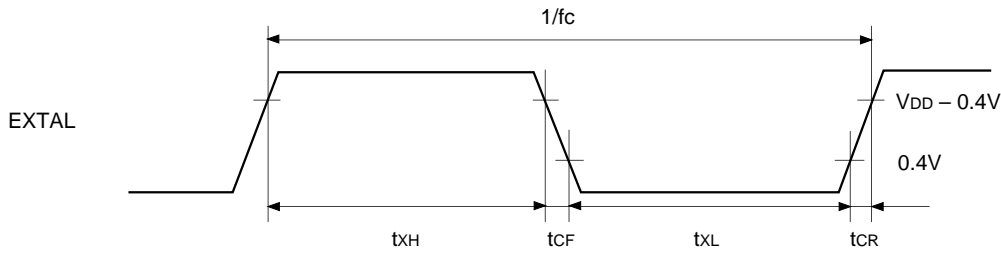


Fig. 1. Clock timing

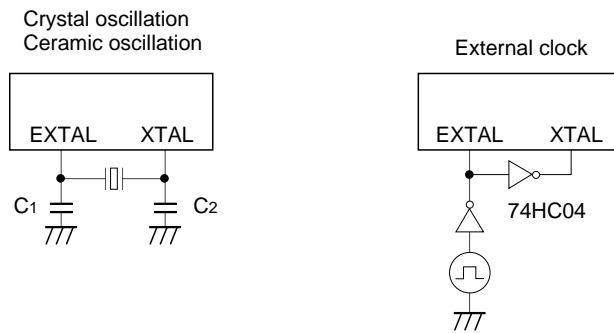


Fig. 2. Clock applied condition

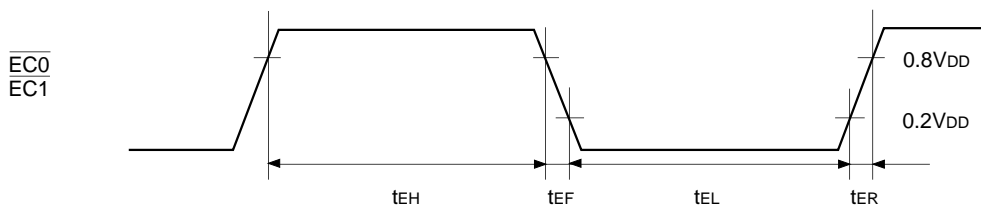


Fig. 3. Event count clock timing

## (2) Serial transfer (CH0)

(Ta = -10 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{CS0}} \downarrow \rightarrow \overline{\text{SCK0}}$ delay time	t <sub>DCSK</sub>	$\overline{\text{SCK0}}$	Chip select transfer mode ( $\overline{\text{SCK0}}$ = output mode)		t <sub>sys</sub> + 200	ns
$\overline{\text{CS0}} \uparrow \rightarrow \overline{\text{SCK0}}$ float delay time	t <sub>DCSKF</sub>	$\overline{\text{SCK0}}$	Chip select transfer mode ( $\overline{\text{SCK0}}$ = output mode)		t <sub>sys</sub> + 200	ns
$\overline{\text{CS0}} \downarrow \rightarrow \text{SO0}$ delay time	t <sub>DCSO</sub>	SO0	Chip select transfer mode		t <sub>sys</sub> + 200	ns
$\overline{\text{CS0}} \uparrow \rightarrow \text{SO0}$ float delay time	t <sub>DCSOF</sub>	SO0	Chip select transfer mode		t <sub>sys</sub> + 200	ns
$\overline{\text{CS0}}$ High level width	t <sub>WHCS</sub>	$\overline{\text{CS0}}$	Chip select transfer mode	t <sub>sys</sub> + 200		ns
$\overline{\text{SCK0}}$ cycle time	t <sub>KCY</sub>	$\overline{\text{SCK0}}$	Input mode	2t <sub>sys</sub> + 200		ns
			Output mode	16000/fc		ns
$\overline{\text{SCK0}}$ High and Low level widths	t <sub>KH</sub> t <sub>KL</sub>	$\overline{\text{SCK0}}$	Input mode	t <sub>sys</sub> + 100		ns
			Output mode	8000/fc - 50		ns
SI0 input setup time (for $\overline{\text{SCK0}} \uparrow$ )	t <sub>SIK</sub>	SI0	$\overline{\text{SCK0}}$ input mode	100		ns
			$\overline{\text{SCK0}}$ output mode	200		ns
SI0 input hold time (for $\overline{\text{SCK0}} \uparrow$ )	t <sub>KSI</sub>	SI0	$\overline{\text{SCK0}}$ input mode	t <sub>sys</sub> + 200		ns
			$\overline{\text{SCK0}}$ output mode	100		ns
$\overline{\text{SCK0}} \downarrow \rightarrow \text{SO0}$ delay time	t <sub>KSO</sub>	SO0	$\overline{\text{SCK0}}$ input mode		t <sub>sys</sub> + 200	ns
			$\overline{\text{SCK0}}$ output mode		100	ns

**Note 1)** t<sub>sys</sub> indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: 00FE<sub>H</sub>).

t<sub>sys</sub> [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

**Note 2)** The load condition for the  $\overline{\text{SCK0}}$  output mode, SO0 output delay time is 50pF + 1TTL.

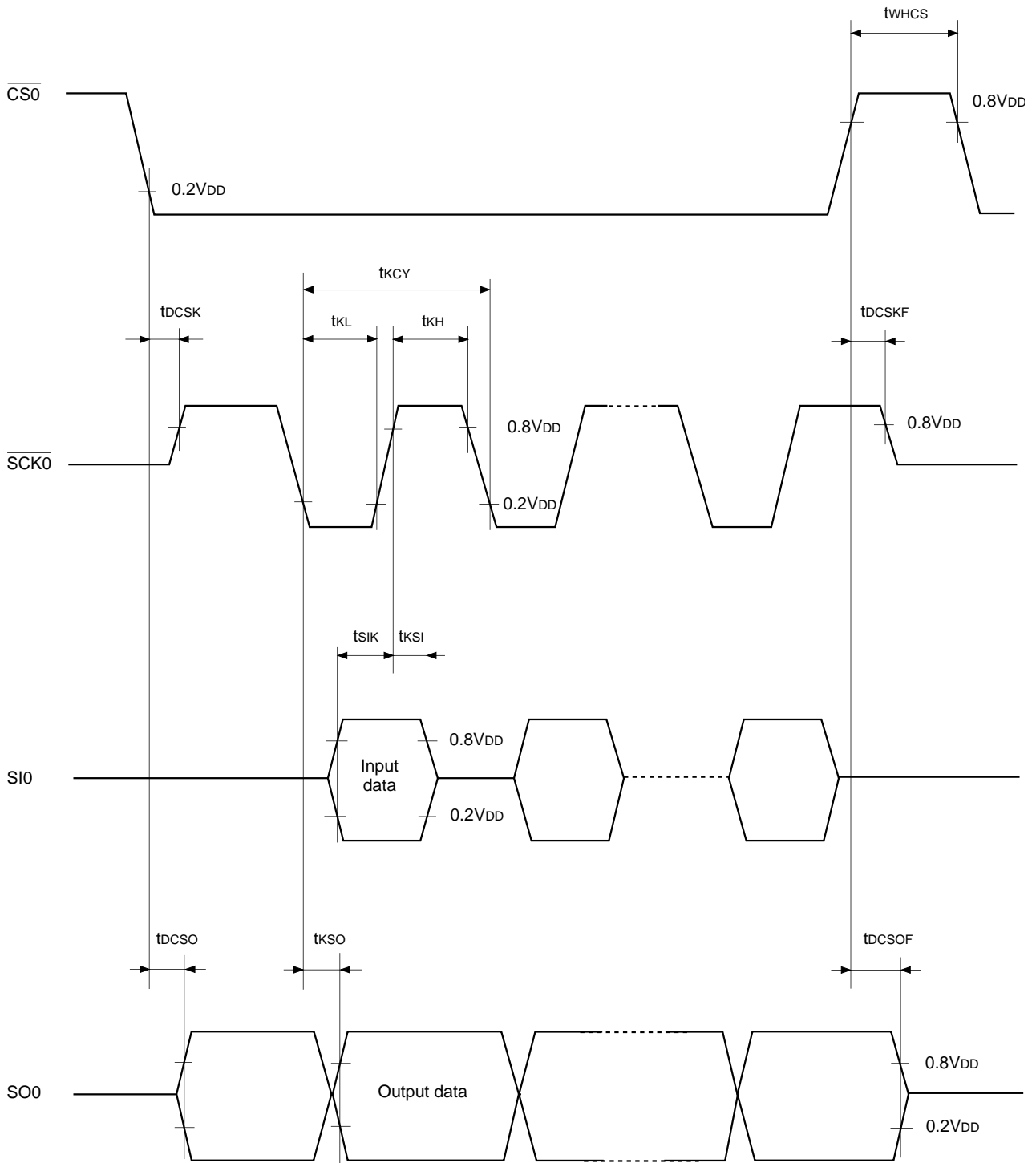


Fig. 4. Serial transfer CH0 timing

Serial transfer (CH1)

( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	$t_{\text{KCY}}$	$\overline{\text{SCK1}}$	Input mode	1000		ns
			Output mode	$16000/f_c$		ns
$\overline{\text{SCK1}}$ High and Low level widths	$t_{\text{KH}}$ $t_{\text{KL}}$	$\overline{\text{SCK1}}$	Input mode	400		ns
			Output mode	$8000/f_c - 50$		ns
SI1 input setup time (for $\overline{\text{SCK1}} \uparrow$ )	$t_{\text{SIK}}$	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (for $\overline{\text{SCK1}} \uparrow$ )	$t_{\text{KSI}}$	SI1	$\overline{\text{SCK1}}$ input mode	200		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}} \downarrow \rightarrow \text{SO1}$ delay time	$t_{\text{KSO}}$	SO1	$\overline{\text{SCK1}}$ input mode		200	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

**Note)** The load condition for the  $\overline{\text{SCK1}}$  output mode, SO1 output delay time is  $50\text{pF} + 1\text{TTL}$ .

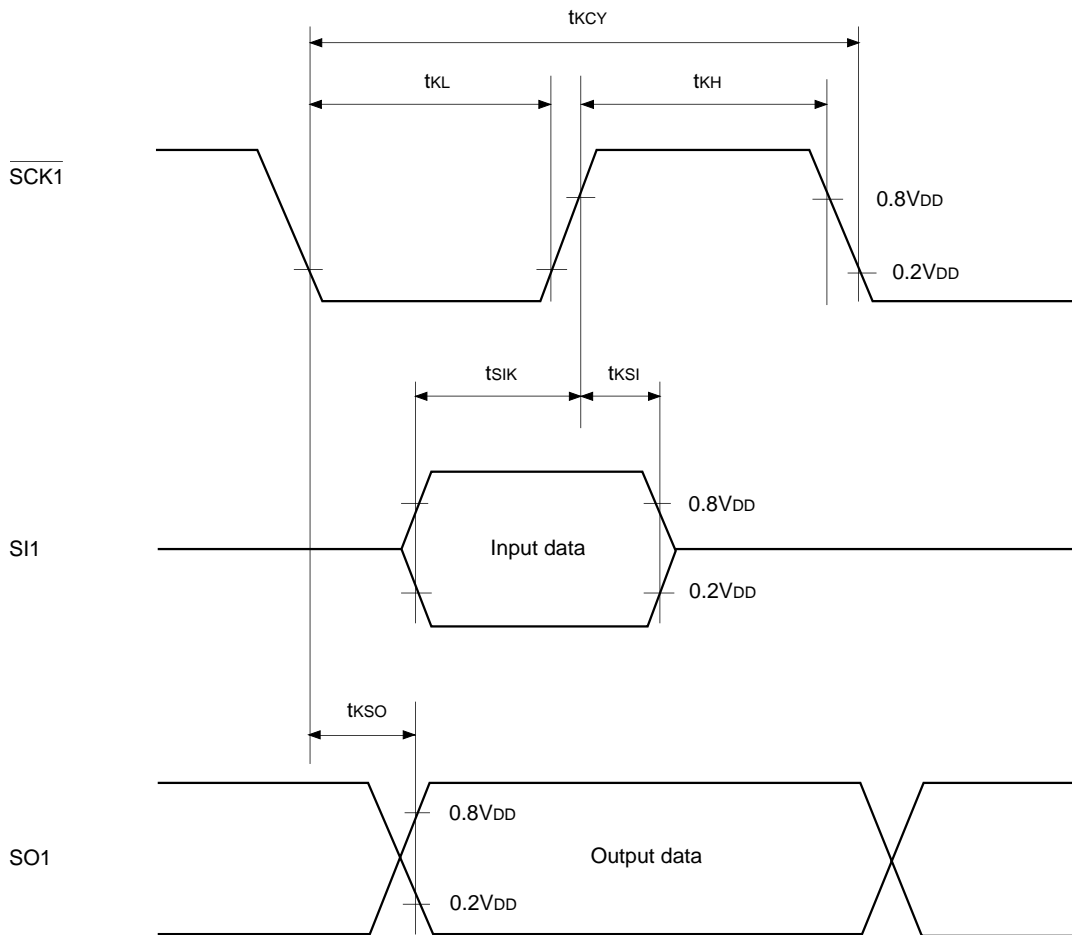
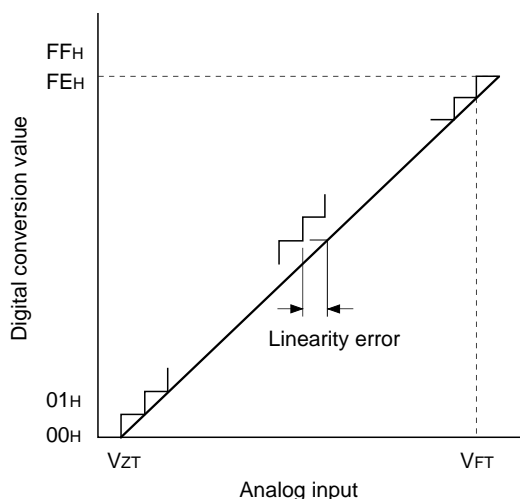


Fig. 5. Serial transfer CH1 timing

**(3) A/D converter characteristics**

( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $AV_{REF} = 4.0$  to  $AV_{DD}$ ,  $V_{SS} = AV_{SS} = 0\text{V}$  reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error						$\pm 3$	LSB
Zero transition voltage	$V_{ZT}^{*1}$		$T_a = 25^\circ\text{C}$ $V_{DD} = 5.0\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$	-10	70	150	mV
Full-scale transition voltage	$V_{FT}^{*2}$			4930	5050	5120	mV
Conversion time	$t_{CONV}$			$160/f_{ADC}^{*3}$			$\mu\text{s}$
Sampling time	$t_{SAMP}$			$12/f_{ADC}^{*3}$			$\mu\text{s}$
Reference input voltage	$V_{REF}$	$AV_{REF}$		$V_{DD} - 0.5$		$V_{DD}$	V
Analog input voltage	$V_{IAN}$	$AN0$ to $AN7$		0		$AV_{REF}$	V
$AV_{REF}$ current	$I_{REF}$	$AV_{REF}$	Operation mode		0.6	1.0	mA
	$I_{REFS}$		Sleep mode Stop mode			10	$\mu\text{A}$

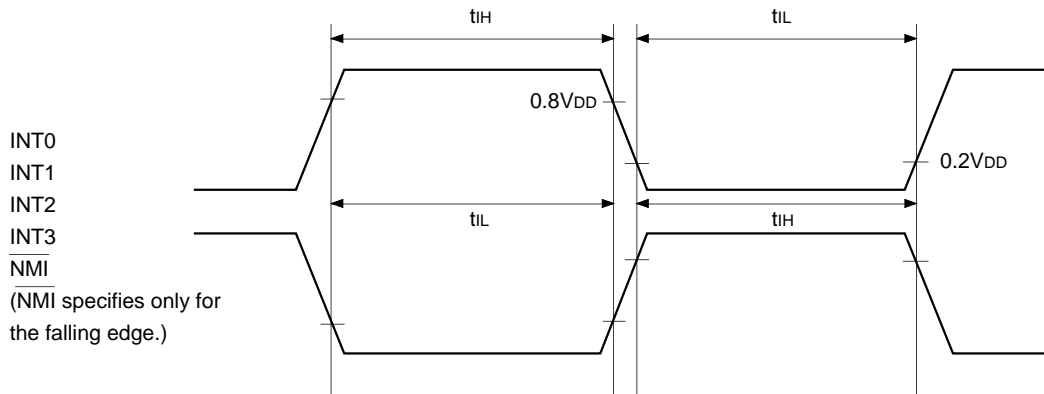


- \*1  $V_{ZT}$  : Value at which the digital conversion value changes from 00H to 01H and vice versa.
- \*2  $V_{FT}$  : Value at which the digital conversion value changes from FEH to FFH and vice versa.
- \*3  $f_{ADC}$  indicates the below values due to ADC operation clock selection.  
 During PS2 selection,  $f_{ADC} = f_c/2$   
 During PS1 selection,  $f_{ADC} = f_c$

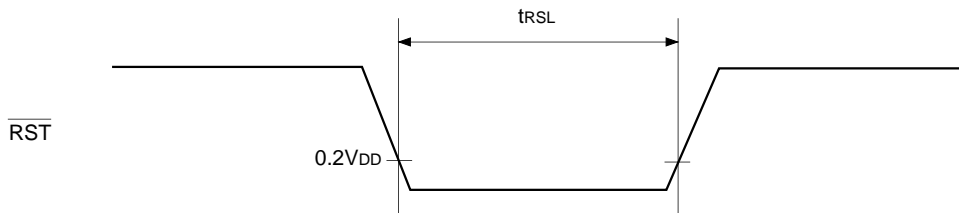
**Fig. 6. Definition of A/D converter terms**

**(4) Interruption, reset input** (Ta = -10 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption High and Low level widths	t <sub>IH</sub> t <sub>IL</sub>	INT0 INT1 INT2 INT3 $\overline{\text{NMI}}$		1		μs
Reset input Low level width	t <sub>RSL</sub>	$\overline{\text{RST}}$		32/fc		μs



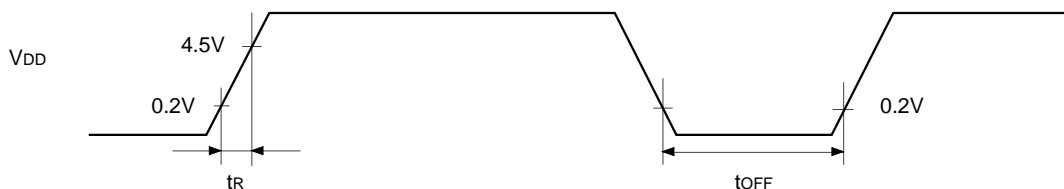
**Fig 7. Interruption input timing**



**Fig. 8.  $\overline{\text{RST}}$  input timing**

**(5) Power-on reset** (Ta = -10 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rising time	t <sub>R</sub>	V <sub>DD</sub>	Power-on reset	0.05	50	ms
Power supply cut-off time	t <sub>OFF</sub>		Repetitive power-on reset	1		ms



The power supply should rise smoothly.

**Fig. 9. Power-on reset**

Appendix

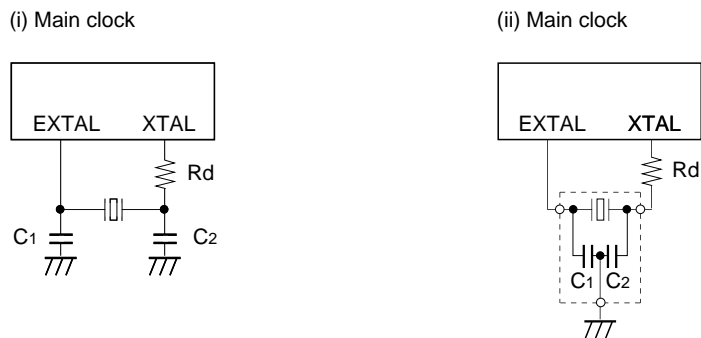


Fig. 10. SPC700 series recommended oscillation circuit

Manufacturer	Model	fc (MHz)	C <sub>1</sub> (pF)	C <sub>2</sub> (pF)	R <sub>d</sub> (Ω)	Circuit example
MURATA MFG CO., LTD.	CSA4.19MG	4.19	30	30	0	(i)
	CSA8.00MTZ	8.00				
	CSA10.0MTZ	10.00				
	CST4.19MGW*	4.19				(ii)
	CST8.00MTW*	8.00				
	CST10.0MTW*	10.00				
RIVER ELETEC CORPORATION	HC-49/U03	4.19	12	12	0	(i)
		8.00				
		10.00				
KINSEKI LTD.	HC-49/U (-S)	4.19	27	27	0	
		8.00				
		10.00	20	20		

Those marked with an asterisk (\*) signify types with built-in ground capacitance (C<sub>1</sub>, C<sub>2</sub>).

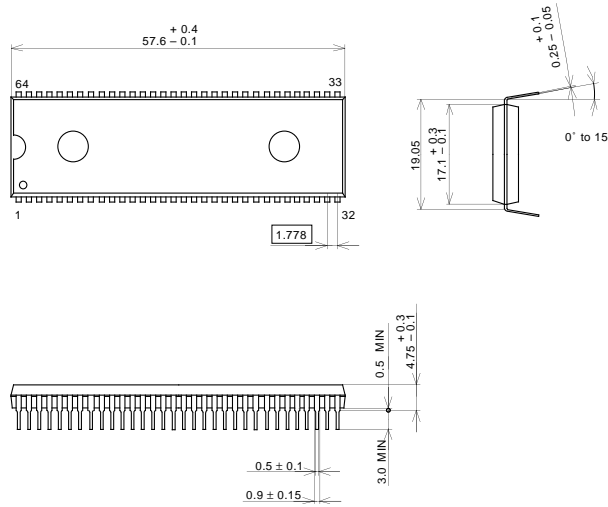
Product List

Optional item	Mask	CXP842P24Q-1-□□□
Package	64-pin plastic SDIP	64-pin plastic SDIP
ROM capacity	20K bytes/24K bytes	PROM 24K bytes
Reset pin pull-up resistor	Existent/non existent	Existent
Power-on reset circuit	Existent/non existent	Existent

Package Outline

Unit: mm

64PIN SDIP (PLASTIC)

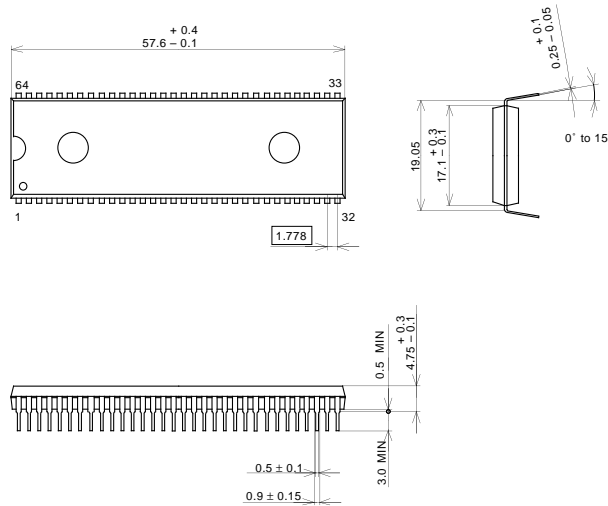


PACKAGE STRUCTURE

SONY CODE	SDIP-64P-01
EIAJ CODE	P-SDIP64-17.1x57.6-1.778
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	8.6g

64PIN SDIP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SDIP-64P-01
EIAJ CODE	P-SDIP64-17.1x57.6-1.778
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	8.6g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18µm



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