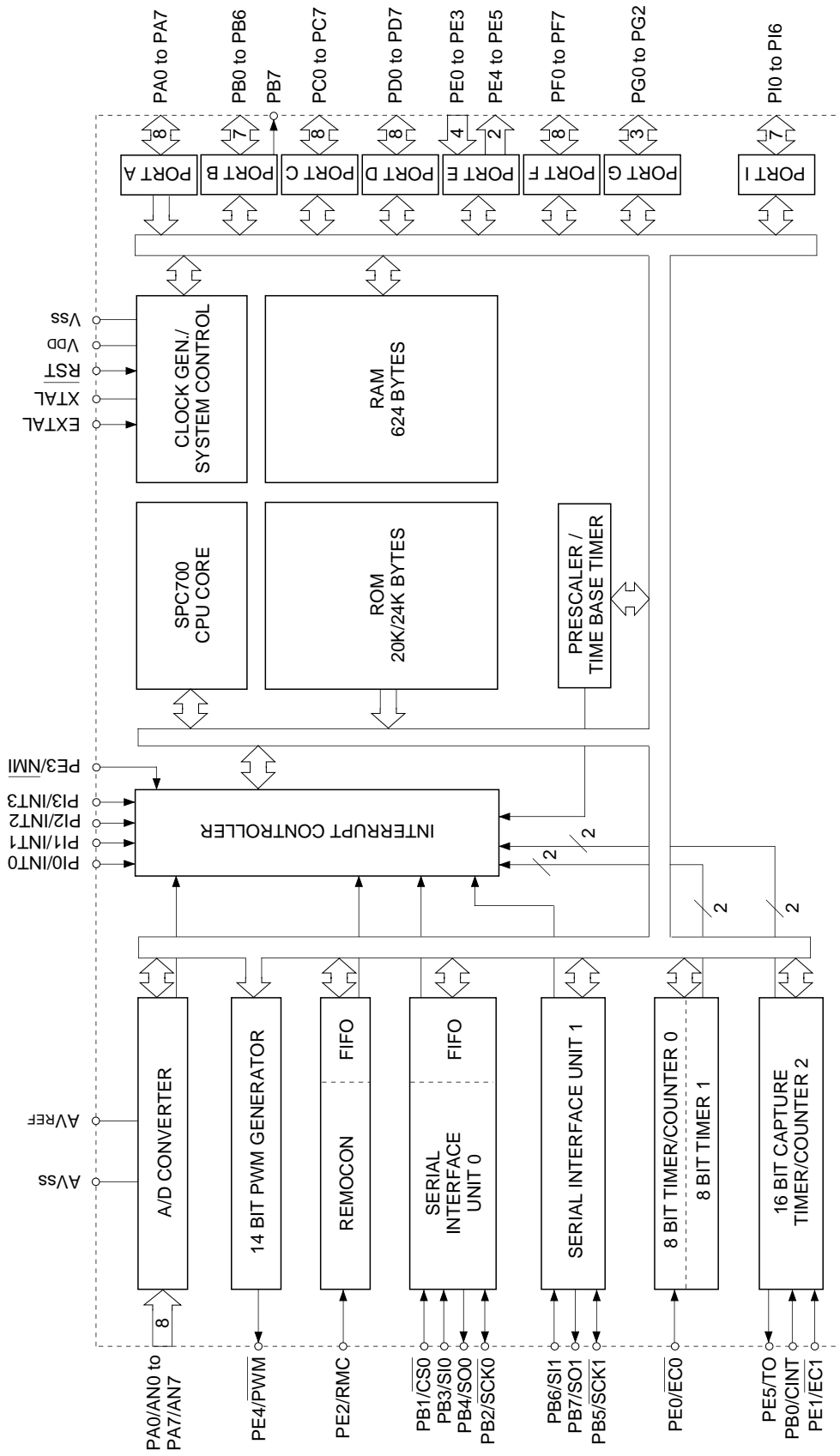
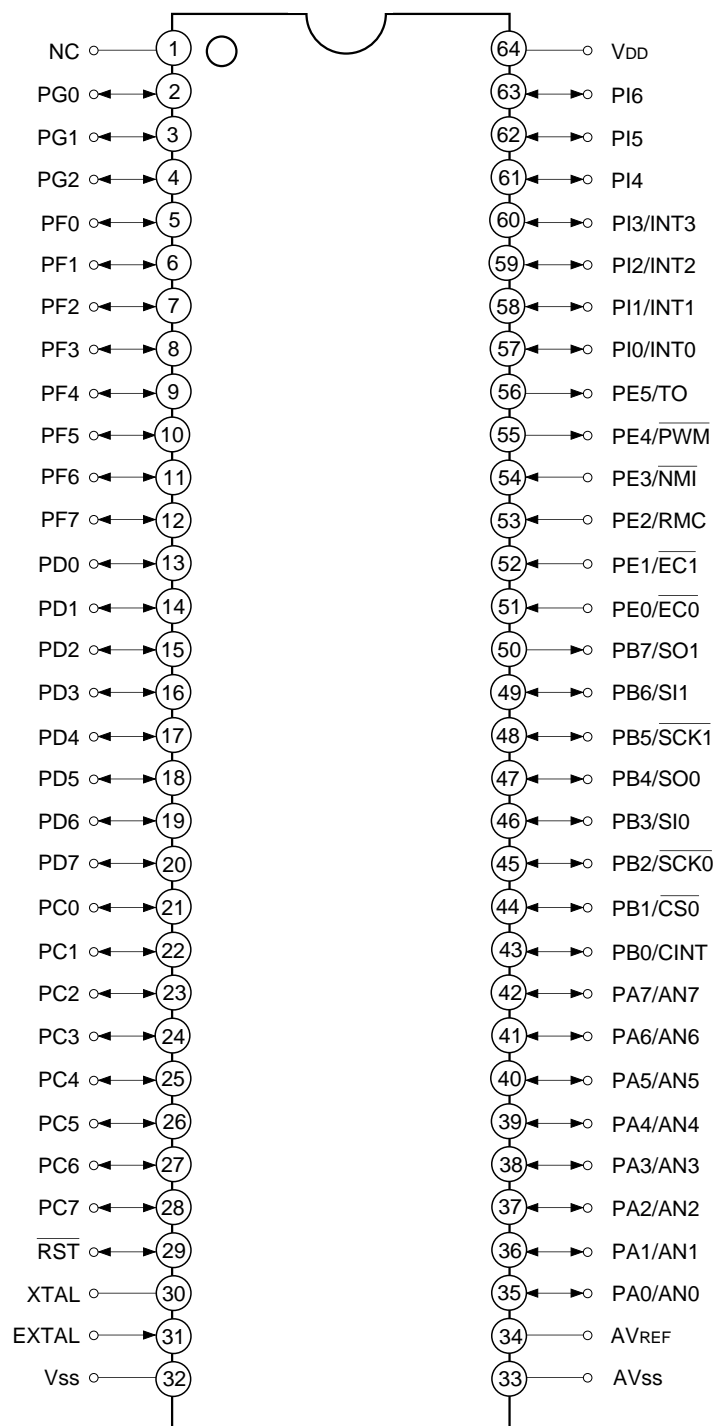


Block Diagram



Pin Assignment (Top View)



Note NC (Pin 1) is always connected to V_{DD}.

Pin Description

Pin code	I/O	Description	
PA0/AN0 to PA7/AN7	I/O/Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bit. Incorporation of the pull-up resistance can be set through the software in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (8 pins)
PB0/CINT	I/O/Input	(Port B) 7-bit I/O port in which I/O can be set in a unit of single bit. Also, an uppermost bit (PB7) exclusively for output. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	External capture input to 16-bit timer/counter.
PB1/ $\overline{\text{CS}}_0$	I/O/Input		Chip select input for serial interface (CH0).
PB2/ $\overline{\text{SCK}}_0$	I/O/I/O		Serial clock I/O (CH0).
PB3/SI0	I/O/Input		Serial data input (CH0).
PB4/SO0	I/O/Output		Serial data output (CH0).
PB5/ $\overline{\text{SCK}}_1$	I/O/I/O		Serial clock I/O (CH1).
PB6/SI1	I/O/Input		Serial data input (CH1).
PB7/SO1	Output/Output		Serial data output (CH1).
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bit. Capable of driving 12mA sink current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PD0 to PD7	I/O	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PE0/ $\overline{\text{EC}}_0$	Input/Input	(Port E) 6-bit port. Lower 4 bits are for inputs; upper 2 bits are for outputs. (6 pins)	External event inputs for timer/counter. (2 pins)
PE1/ $\overline{\text{EC}}_1$	Input/Input		
PE2/RMC	Input/Input		Remote control reception circuit input.
PE3/ $\overline{\text{NMI}}$	Input/Input		Non-maskable interruption request input.
PE4/ $\overline{\text{PWM}}$	Output/Output		14-bit PWM output.
PE5/TO	Output/Output		Rectangular wave output for 16-bit timer/counter.
PF0 to PF7	I/O	(Port F) 8-bit output port. I/O can be set in a unit of single bit. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PG0 to PG2	I/O	(Port G) 8-bit I/O port. I/O can be set in a unit of single bit. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (3 pins)	

Pin code	I/O	Description	
PI0/INT0 to PI3/INT3	I/O/Input	(Port I) 7-bit output ports. I/O can be set in a unit of single bit. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (7 pins)	External interruption request inputs.
PI4 to PI6	I/O		
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL	Output		
$\overline{\text{RST}}$	I/O	Low-level active, system reset.	
NC		NC. Under normal operating conditions, connect to V _{DD} .	
AVREF	Input	Reference voltage input for A/D converter.	
AVss		A/D converter GND.	
V _{DD}		Positive power supply.	
V _{SS}		GND	

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
<p>PA0/AN0 to PA7/AN7</p> <p>8 pins</p>	<p>Port A</p> <p>Pull-up resistance "0" when reset</p> <p>Port A data</p> <p>Port A direction "0" when reset</p> <p>Data bus ← RD (Port A)</p> <p>Port A input selection "0" when reset</p> <p>Input multiplexer</p> <p>A/D converter</p> <p>IP Input protection circuit</p> <p>* Pull-up transistors approx. 10kΩ</p>	<p>Hi-Z</p>
<p>PB0/CINT PB1/CS0 PB3/SI0 PB6/SI1</p> <p>4 pins</p>	<p>Port B</p> <p>Pull-up resistance "0" when reset</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus ← RD (Port B)</p> <p>Schmitt input</p> <p>CINT CS0 SI0 SI1</p> <p>IP</p> <p>* Pull-up transistors approx. 10kΩ</p>	<p>Hi-Z</p>
<p>PB2/SCK0 PB5/SCK1</p> <p>2 pins</p>	<p>Port B</p> <p>Pull-up resistance "0" when reset</p> <p>SCK OUT Output enable</p> <p>Port B output selection "0" when reset</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus ← RD (Port B)</p> <p>Schmitt input</p> <p>SCK in</p> <p>IP</p> <p>* Pull-up transistors approx. 10kΩ</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PB4/SO0</p> <p>1 pin</p>	<p>Port B</p> <p>* Pull-up transistors approx. 10kΩ</p>	<p>Hi-Z</p>
<p>PB7/SO1</p> <p>1 pin</p>	<p>Port B</p> <p>* Pull-up transistors approx. 200kΩ</p>	<p>High level</p>
<p>PC0 to PC7</p> <p>8 pins</p>	<p>Port C</p> <p>*1 Large current drive of 12mA possible</p> <p>*2 Pull-up transistors approx. 10kΩ</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
PE0/ $\overline{EC0}$ PE1/ $\overline{EC1}$ PE2/RMC PE3/NMI 4 pins		Hi-Z
PE4/ \overline{PWM} 1 pin		High level
PE5/ \overline{TO} 1 pin		High level
PD0 to PD7 PF0 to PF7 PG0 to PG2 PI4 to PI6 22 pins	<p>* Pull-up transistors approx. 10kΩ</p>	Hi-Z

Pin	Circuit format	When reset
<p>PI0 to PI3</p> <p>4 pins</p>	<p>Port I</p> <p>Pull-up resistance "0" when reset</p> <p>Port data</p> <p>Port direction "0" when reset</p> <p>Data bus ← RD</p> <p>INT0 INT1 INT2 INT3</p> <p>* Pull-up transistors approx. 10kΩ</p>	<p>Hi-Z</p>
<p>EXTAL XTAL</p> <p>2 pins</p>	<p>EXTAL</p> <p>XTAL</p> <ul style="list-style-type: none"> • Diagram shows circuit composition during oscillation • Feedback resistor is removed during stop. 	<p>Oscillation</p>
<p>$\overline{\text{RST}}$</p> <p>1 pin</p>	<p>Mask option OP</p> <p>Pull-up resistor</p> <p>IP</p> <p>Schmitt input Power-on reset function (Mask option)</p>	<p>Low level</p>

Absolute Maximum Ratings

(V_{SS} = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	-0.3 to +7.0	V	
	AV _{SS}	-0.3 to +0.3	V	
Input voltage	V _{IN}	-0.3 to +7.0* ¹	V	
Output voltage	V _{OUT}	-0.3 to +7.0* ¹	V	
High level output current	I _{OH}	-5	mA	Output per pin
High level total output current	∑I _{OH}	-50	mA	Total for all output pins
Low level output current	I _{OL}	15	mA	Value per pin, excluding large current outputs
	I _{OLC}	20	mA	Value per pin* ² for large current outputs
Low level total output current	∑I _{OL}	100	mA	Total for all output pins
Operating temperature	T _{opr}	-20 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	1000	mW	

*¹ V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*² The large current drive transistor is the N-ch transistor of Port C (PC).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	4.5	5.5	V	High-speed mode guaranteed operation range* ¹
		3.5	5.5		Low-speed mode guaranteed operation range* ¹
		2.5	5.5		Guaranteed data hold range during stop
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	* ²
	V _{IHS}	0.8V _{DD}	V _{DD}	V	Hysteresis input* ³
	V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL* ⁴
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	* ²
	V _{ILS}	0	0.2V _{DD}	V	Hysteresis input* ³
	V _{ILEX}	-0.3	0.4	V	EXTAL* ⁴
Operating temperature	T _{opr}	-20	+75	°C	

*¹ High-speed mode is 1/2 frequency demultiplication clock selection; low-speed mode is 1/16 frequency demultiplication clock selection.

*² Value for each pin of normal input ports (PA, PB3, PB4, PB6, PC, PD, PF, PG, PI4 to PI6).

*³ Value of the following pins: RST, CINT, CS0, SCK0, SCK1, EC0, EC1, RMC, NMI, INT0, INT1, INT2, INT3.

*⁴ Specifies only during external clock input.

Electrical Characteristics

DC Characteristics

(Ta = -20 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit	
High level output voltage	V _{OH}	PA to PD, PE4, PE5, PF, PG, PI	V _{DD} = 4.5V, I _{OH} = -0.5mA	4.0			V	
			V _{DD} = 4.5V, I _{OH} = -1.2mA	3.5			V	
V _{OL}	V _{DD} = 4.5V, I _{OL} = 1.8mA				0.4	V		
	V _{DD} = 4.5V, I _{OL} = 3.6mA				0.6	V		
Low level output voltage	V _{OL}	PC	V _{DD} = 4.5V, I _{OL} = 12.0mA			1.5	V	
		I _{IHE}	EXTAL	V _{DD} = 5.5V, V _{IH} = 5.5V	0.5		40	μA
				V _{DD} = 5.5V, V _{IL} = 0.4V	-0.5		-40	μA
		I _{ILR}	$\overline{\text{RST}}^{*1}$	V _{DD} = 5.5V V _{IL} = 0.4V	-1.5		-400	μA
I _{IL}	PA to PD* ² , PF, PG, PI* ²		V _{DD} = 5.5V V _{IL} = 0.4V			-2.0	mA	
		V _{DD} = 4.5V, V _{IL} = 4.0V	-10			μA		
I/O leakage current	I _{Iz}	PE0 to PE3, RST* ¹	V _{DD} = 5.5V V _I = 0, 5.5V			±10	μA	
Supply current* ³	I _{DD1}	V _{DD}	High-speed mode operation (1/2 frequency demultiplier clock) V _{DD} = 5.5V, 10MHz crystal oscillation (C ₁ = C ₂ = 15pF)		18	40	mA	
			Sleep mode V _{DD} = 5.5V, 10MHz crystal oscillation (C ₁ = C ₂ = 15pF)		1.1	8	mA	
			Stop mode V _{DD} = 5.5V, termination of 10MHz crystal oscillation			10	μA	
Input capacity	C _{IN}	Pins other than PB7, PE4, PE5, AV _{REF} , AV _{SS} , V _{DD} , V _{SS}	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF	

*¹ $\overline{\text{RST}}$ specifies the input current when pull-up resistance has been selected; leakage current when no resistance has been selected.

*² Pins PA to PD, and PF, PG, PI specify the input current when pull-up resistance has been selected; leakage current when no resistance has been selected. (Excludes output PB7)

*³ When all pins are open.

AC Characteristics

(1) Clock timing

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f_c	XTAL EXTAL	Fig. 1, Fig. 2	1		10	MHz
System clock input pulse width	t_{XL} t_{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	37.5			ns
System clock input rise time, fall time	t_{CR} t_{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	t_{EH} t_{EL}	$\overline{\text{EC0}}$ EC1	Fig. 3	$t_{\text{sys}} + 50^{*1}$			ns
Event count input clock rise time, fall time	t_{ER} t_{EF}	$\overline{\text{EC0}}$ EC1	Fig. 3			20	ms

*1 t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: 00FEH).

t_{sys} [ns] = $2000/f_c$ (upper two bits = "00"), $4000/f_c$ (upper two bits = "01"), $16000/f_c$ (upper two bits = "11")

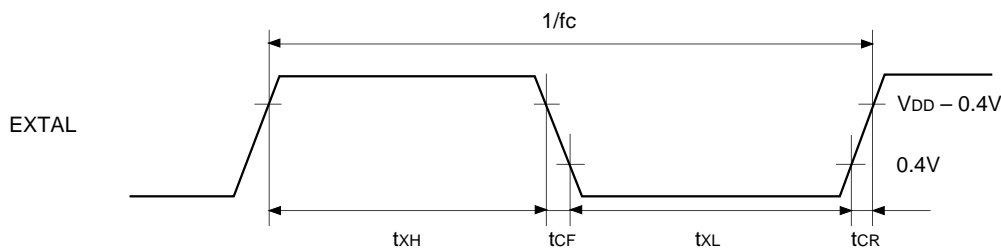


Fig. 1. Clock timing

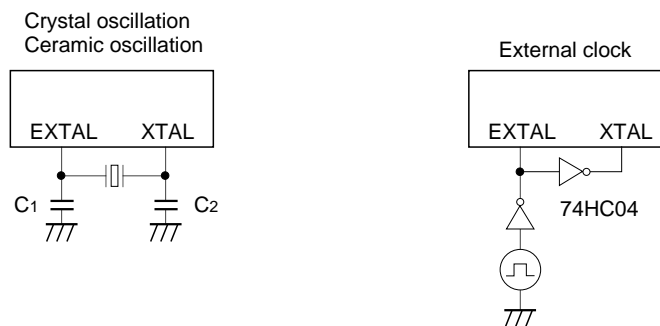


Fig. 2. Clock applied condition

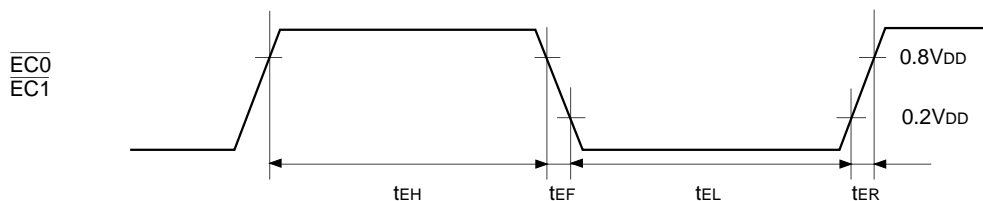


Fig. 3. Event count clock timing

(2) Serial transfer (CH0)

(Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{CS0}} \downarrow \rightarrow \overline{\text{SCK0}}$ delay time	t _{DCSK}	$\overline{\text{SCK0}}$	Chip select transfer mode ($\overline{\text{SCK0}}$ = output mode)		t _{sys} + 200	ns
$\overline{\text{CS0}} \uparrow \rightarrow \overline{\text{SCK0}}$ float delay time	t _{DCSKF}	$\overline{\text{SCK0}}$	Chip select transfer mode ($\overline{\text{SCK0}}$ = output mode)		t _{sys} + 200	ns
$\overline{\text{CS0}} \downarrow \rightarrow \text{SO0}$ delay time	t _{DCSO}	SO0	Chip select transfer mode		t _{sys} + 200	ns
$\overline{\text{CS0}} \uparrow \rightarrow \text{SO0}$ float delay time	t _{DCSOF}	SO0	Chip select transfer mode		t _{sys} + 200	ns
$\overline{\text{CS0}}$ High level width	t _{WHCS}	$\overline{\text{CS0}}$	Chip select transfer mode	t _{sys} + 200		ns
$\overline{\text{SCK0}}$ cycle time	t _{KCY}	$\overline{\text{SCK0}}$	Input mode	2t _{sys} + 200		ns
			Output mode	16000/fc		ns
$\overline{\text{SCK0}}$ High, Low level width	t _{KH} t _{KL}	$\overline{\text{SCK0}}$	Input mode	t _{sys} + 100		ns
			Output mode	8000/fc - 50		ns
SI0 input setup time (for $\overline{\text{SCK0}} \uparrow$)	t _{SIK}	SI0	$\overline{\text{SCK0}}$ input mode	100		ns
			$\overline{\text{SCK0}}$ output mode	200		ns
SI0 input hold time (for $\overline{\text{SCK0}} \uparrow$)	t _{KSI}	SI0	$\overline{\text{SCK0}}$ input mode	t _{sys} + 200		ns
			$\overline{\text{SCK0}}$ output mode	100		ns
$\overline{\text{SCK0}} \downarrow \rightarrow \text{SO0}$ delay time	t _{KSO}	SO0	$\overline{\text{SCK0}}$ input mode		t _{sys} + 200	ns
			$\overline{\text{SCK0}}$ output mode		100	ns

Note 1) t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: 00FEH).

t_{sys} [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Note 2) The load condition for the $\overline{\text{SCK0}}$ output mode, SO0 output delay time is 50pF + 1TTL.

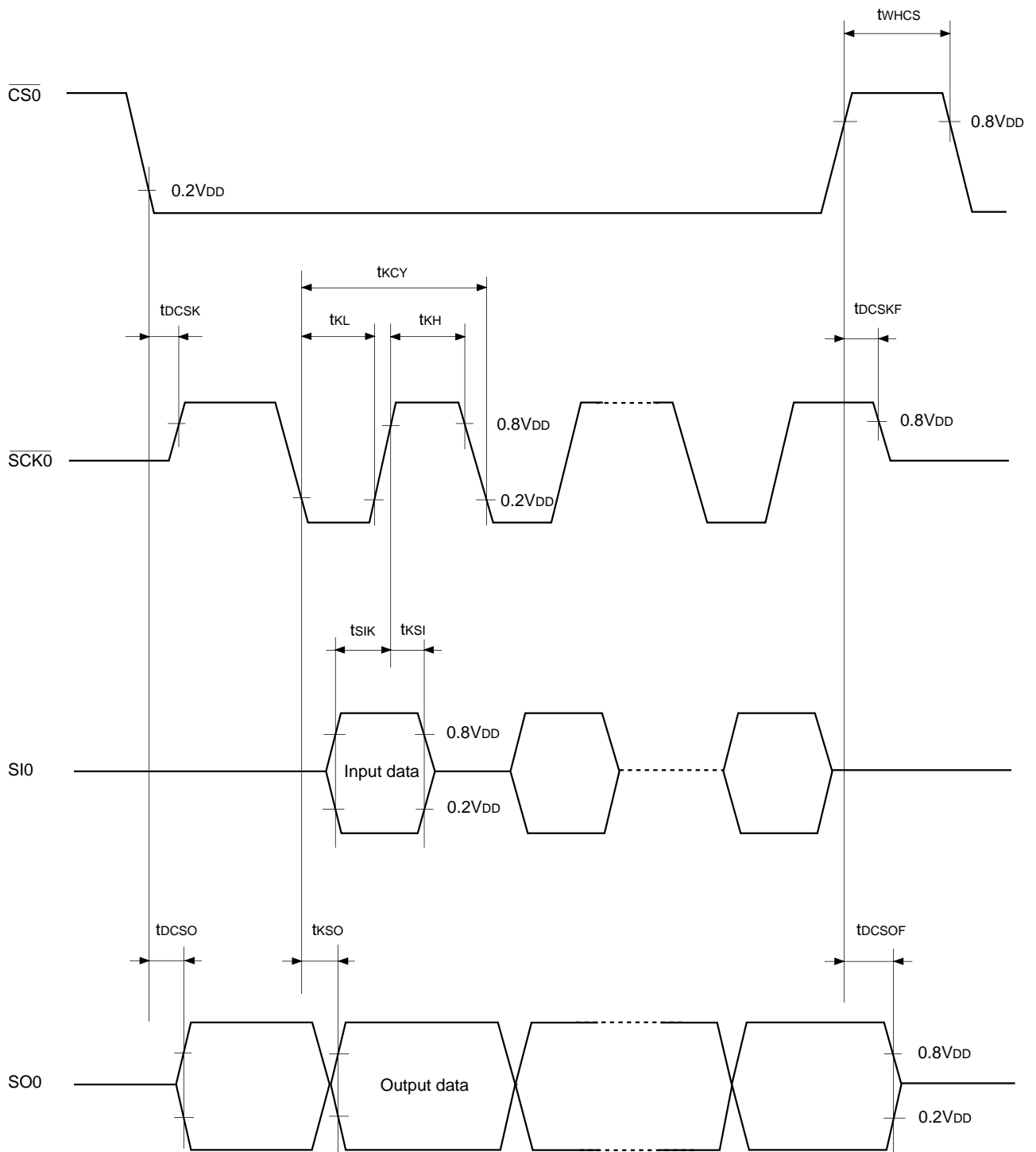


Fig. 4. Serial transfer CH0 timing

Serial transfer (CH1)

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{CY}	$\overline{\text{SCK1}}$	Input mode	1000		ns
			Output mode	$16000/f_c$		ns
$\overline{\text{SCK1}}$ High, Low level width	t_{KH} t_{KL}	$\overline{\text{SCK1}}$	Input mode	400		ns
			Output mode	$8000/f_c - 50$		ns
SI1 input setup time (for $\overline{\text{SCK1}} \uparrow$)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (for $\overline{\text{SCK1}} \uparrow$)	t_{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	200		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}} \downarrow \rightarrow \text{SO1}$ delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		200	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

Note) The load condition for the $\overline{\text{SCK1}}$ output mode, SO1 output delay time is $50\text{pF} + 1\text{TTL}$.

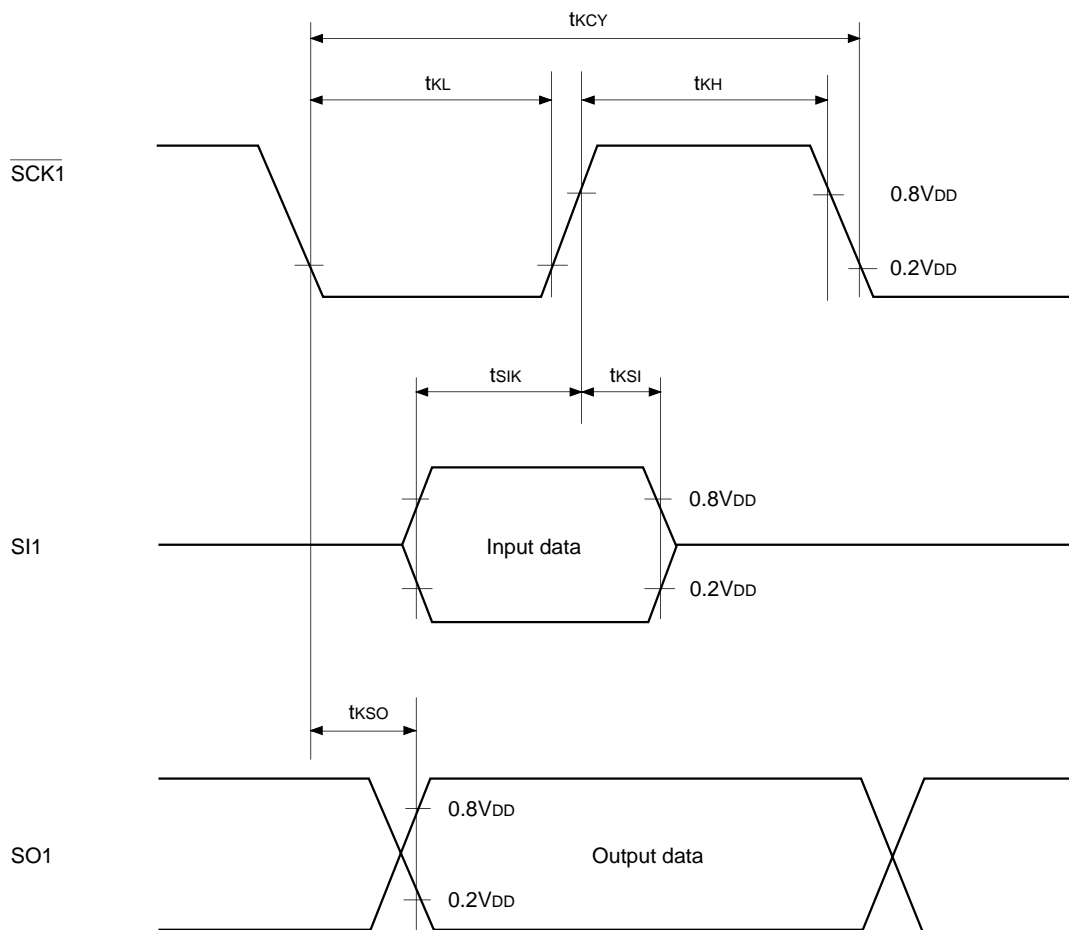
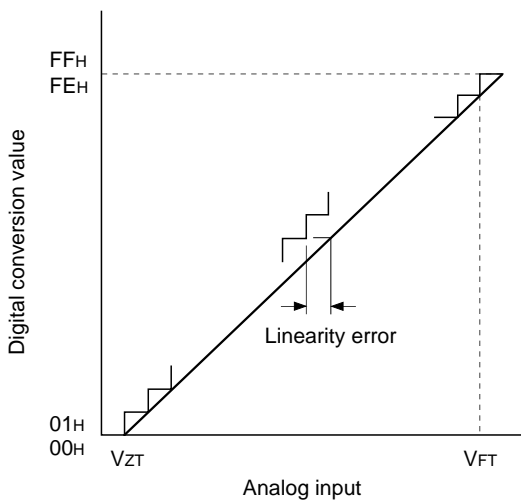


Fig. 5. Serial transfer CH1 timing

(3) A/D converter characteristics

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $AV_{REF} = 4.0$ to AV_{DD} , $V_{SS} = AV_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error						± 3	LSB
Zero transition voltage	V_{ZT}^{*1}		$T_a = 25^\circ\text{C}$ $V_{DD} = 5.0\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$	-10	70	150	mV
Full-scale transition voltage	V_{FT}^{*2}			4930	5050	5120	mV
Conversion time	t_{CONV}			$160/f_{ADC}^{*3}$			μs
Sampling time	t_{SAMP}			$12/f_{ADC}^{*3}$			μs
Reference input voltage	V_{REF}	AV_{REF}		$V_{DD} - 0.5$		V_{DD}	V
Analog input voltage	V_{IAN}	$AN0$ to $AN7$		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operation mode		0.6	1.0	mA
	I_{REFS}		Sleep mode Stop mode			10	μA



- *1 V_{ZT} : Value at which the digital conversion value changes from 00H to 01H and vice versa.
- *2 V_{FT} : Value at which the digital conversion value changes from FEH to FFH and vice versa.
- *3 f_{ADC} indicates the below values due to ADC operation clock selection.
 During PS2 selection, $f_{ADC} = f_c/2$
 During PS1 selection, $f_{ADC} = f_c$

Fig. 6. Definition of A/D converter terms

(4) Interruption, reset input

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption High, Low level width	t_{IH} t_{IL}	INT0 INT1 INT2 INT3 NMI		1		μs
Reset input Low level width	t_{RSL}	$\overline{\text{RST}}$		$8/f_c$		μs

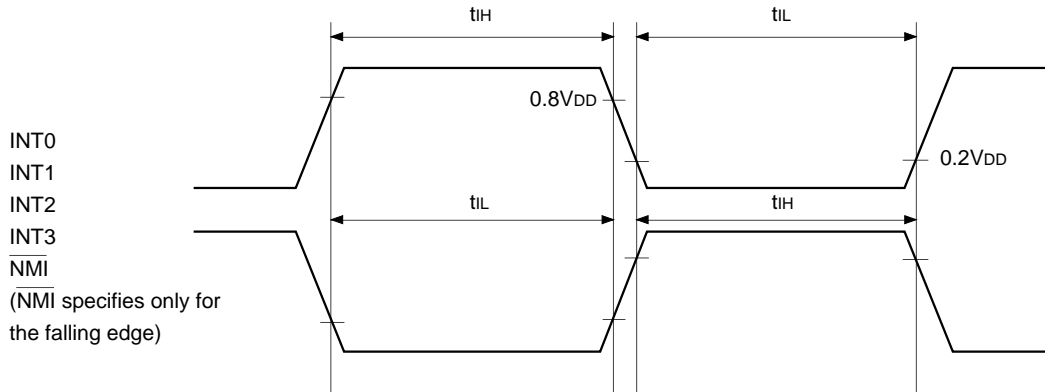


Fig. 7. Interruption input timing

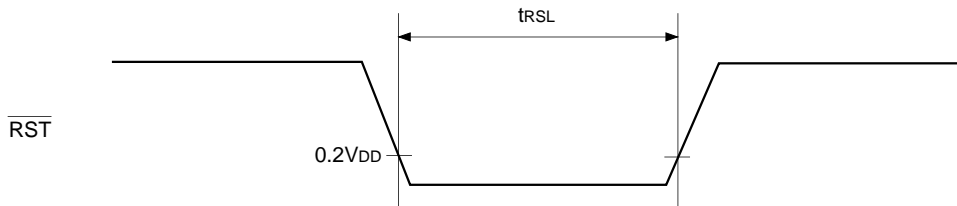


Fig. 8. RST input timing

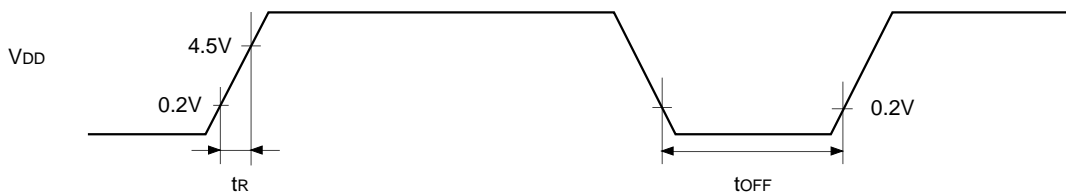
(5) Power-on reset

Power-on reset*

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rising time	t_R	V_{DD}	Power-on reset	0.05	50	ms
Power supply cut-off time	t_{OFF}		Repetitive power-on reset	1		ms

* Specifies only when power-on reset function is selected.



The power supply should be rise smoothly.

Fig. 9. Power-on reset

Appendix

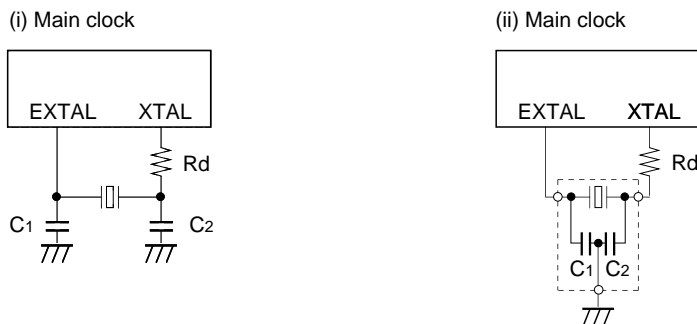


Fig. 10. SPC700 Series recommended oscillation circuit

Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example
MURATA MFG CO., LTD.	CSA4.19MG	4.19	30	30	0	(i)
	CSA8.00MTZ	8.00				
	CSA10.0MTZ	10.00				
	CST4.19MGW*	4.19				(ii)
	CST8.00MTW*	8.00				
	CST10.0MTW*	10.00				
RIVER ELETEC CORPORATION	HC-49/U03	4.19	12	12	0	(i)
		8.00				
		10.00				
KINSEKI LTD.	HC-49/U (-S)	4.19	27	27	0	
		8.00				
		10.00	20	20		

Those marked with an asterisk (*) signify types with built-in ground capacitance (C1, C2).

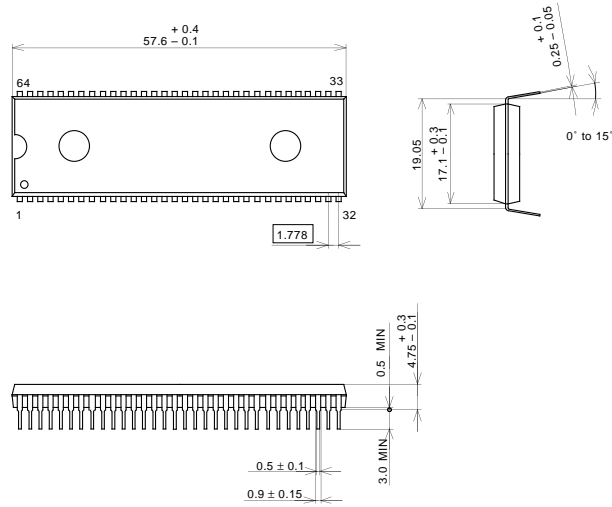
Mask option table

Item	Content	
Reset pin pull-up resistance	Non-existent	Existent
Power-on reset circuit	Non-existent	Existent

Package Outline

Unit: mm

64PIN SDIP (PLASTIC)

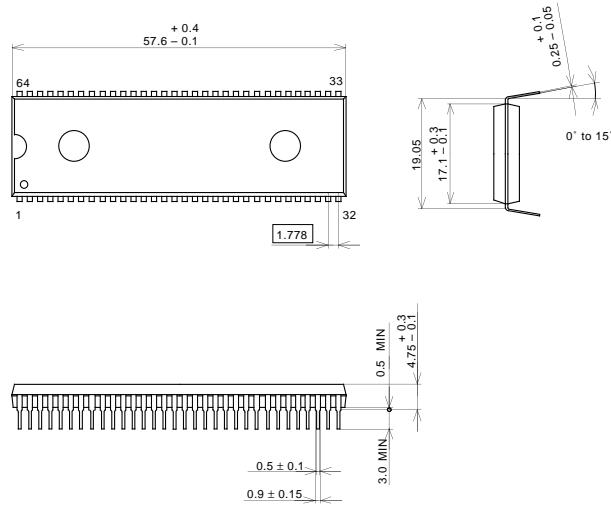


PACKAGE STRUCTURE

SONY CODE	SDIP-64P-01
EIAJ CODE	P-SDIP64-17.1x57.6-1.778
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	8.6g

64PIN SDIP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SDIP-64P-01
EIAJ CODE	P-SDIP64-17.1x57.6-1.778
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	8.6g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18 μ m



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