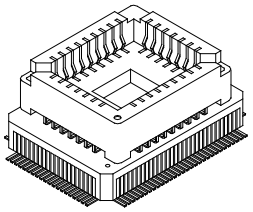
SONY

CXP83200A

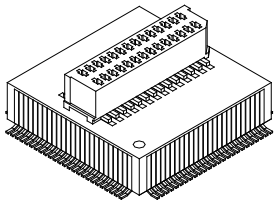
CMOS 8-bit Single Chip Microcomputer

Piggyback/ evaluator type

100 pin PQFP (Ceramic)



QFP supported



LQFP supported

Description

The CXP83200A is a CMOS 8-bit single chip microcomputer of piggyback/evaluator combined type, which is developed for evaluating the function of the CXP83120A/83124A and CXP83232/83240.

Features

- Wide-range instruction system (213 instructions) to cover various types of data
  - 16-bit operation/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle 400ns at 10MHz operation
  8µs at 500kHz operation
  122µs at 32kHz operation
- Applicable EPROM LCC type 27C512
  (Maximum 40K bytes are available.)
- Incorporated RAM capacity 1120 bytes (Including LCD display data area)
- Peripheral functions
  - A/D converter 8-bit, 8-channel, successive approximation method
    (Conversion time of 32µs/10 MHz)
  - Serial interface Incorporated 8-bit, 8-stage FIFO
    (Auto transfer for 1 to 8 bytes), 1 channel
    8-bit clock sync type, 1 channel
  - Timer 8-bit timer
    8-bit timer/counter
    19-bit time base timer
    16-bit capture timer/counter
    32kHz timer/counter
  - LCD controller/driver Maximum 160 segment display possible (for 1/4 duty)
    4 lines for common output, 40 lines for segment output
    Display method static: 1/2, 1/3, 1/4 duty
    Bias method: 1/2, 1/3 bias
  - Remote control reception circuit 8-bit pulse measurement counter with on-chip 6-stage FIFO
  - PWM output 14 bits, 1 channel
- Interruption 15 factors, 15 vectors, multi-interruption possible
- Standby mode SLEEP/STOP
- Package 100-pin ceramic PQFP

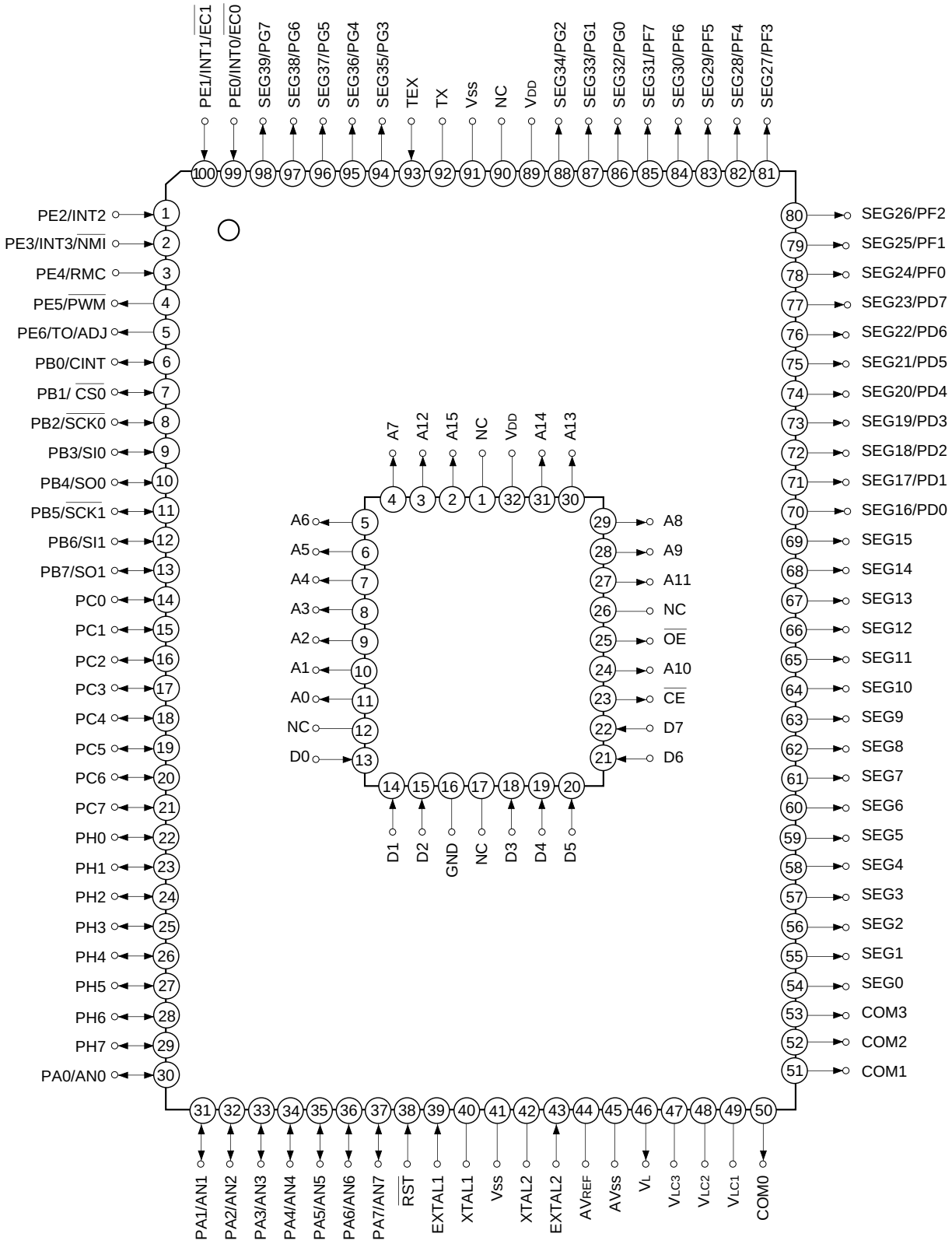
Note) Mask option depends on the type of the CXP83200A. Refer to the Products List for details.

Structure

Silicon gate CMOS IC

E94831A68-PS

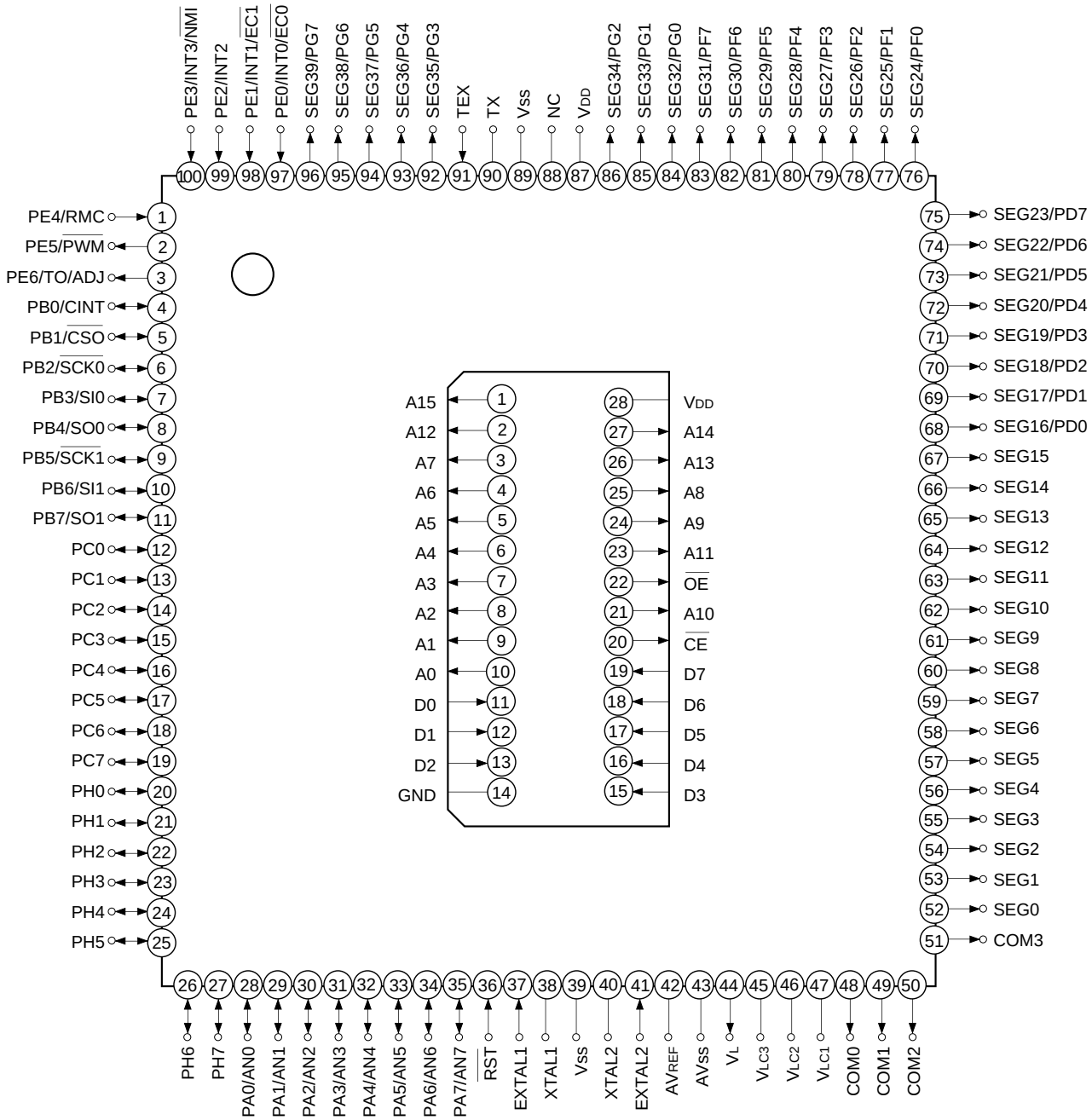
Pin Configuration in Piggyback Mode (QFP package)



Note) 1. NC (Pin 90) is always connected to V_{DD}.

2. Vss (Pins 41 and 91) are both connected to GND.

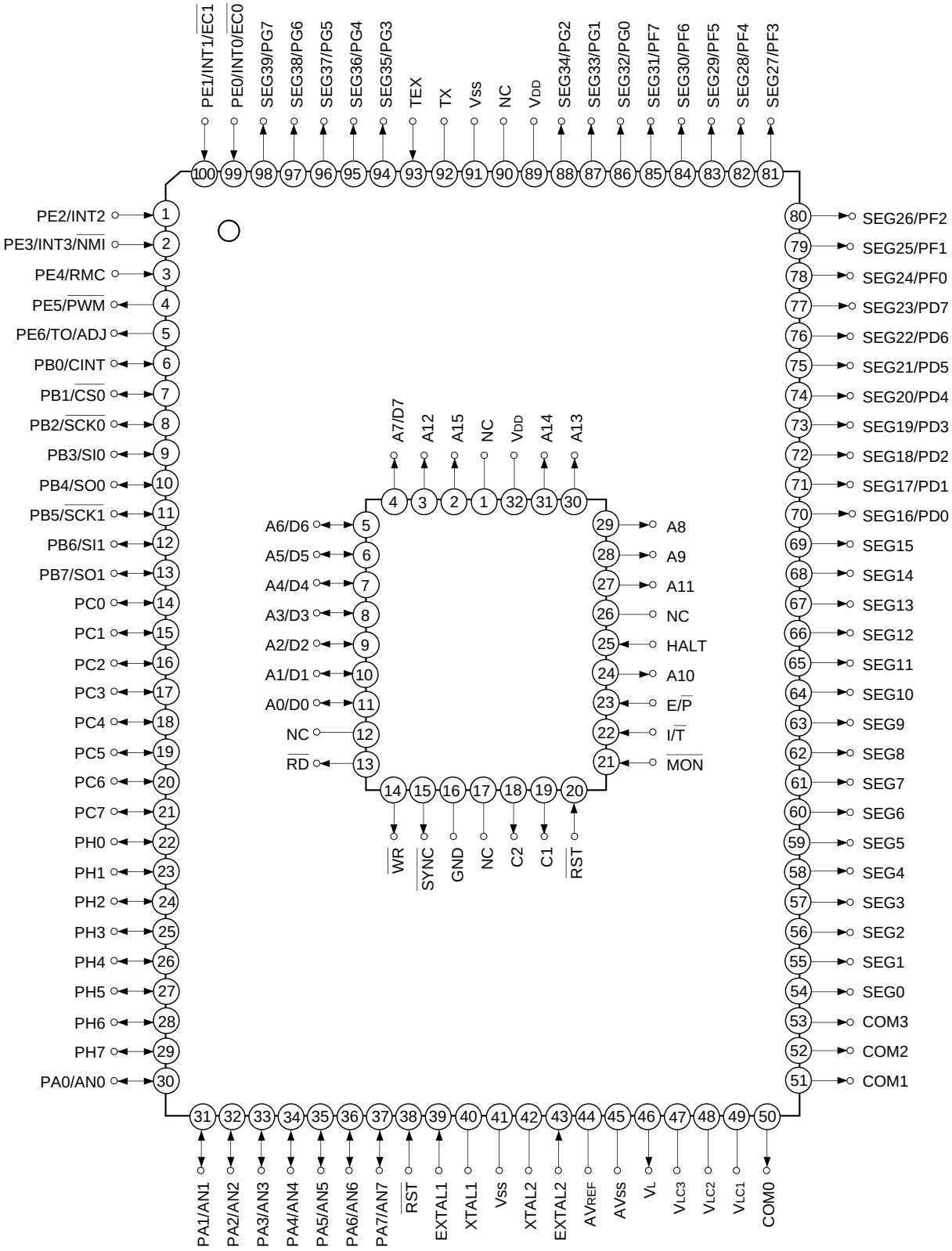
Pin Configuration in Piggyback Mode (LQFP package)



Note) 1. NC (Pin 88) is always connected to V_{DD}.

2. Vss (Pins 39 and 89) are both connected to GND.

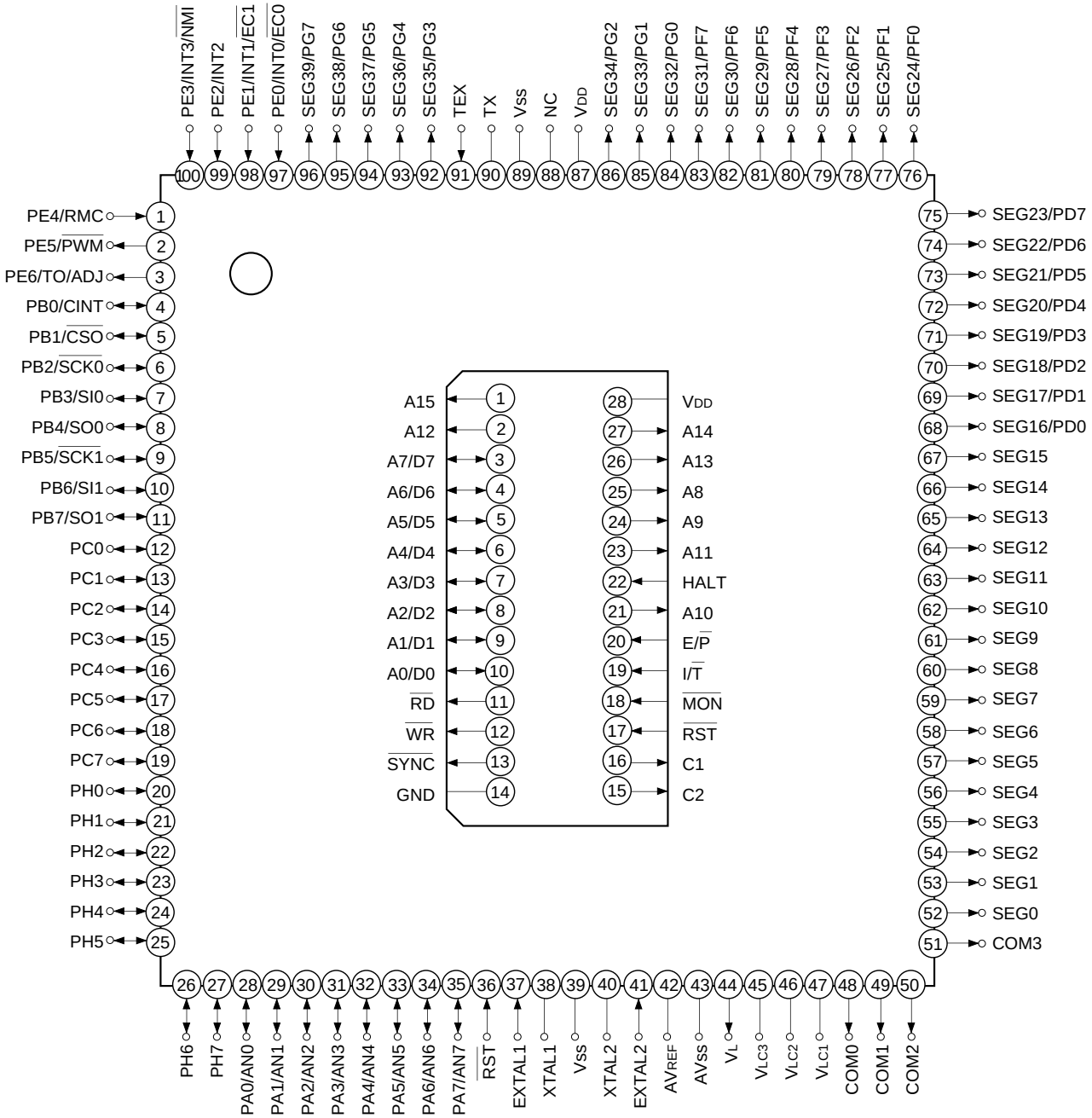
Pin Configuration in Evaluator Mode (QFP package)



Note) 1. NC (Pin 90) is always connected to V_{DD}.

2. Vss (Pins 41 and 91) are both connected to GND.

Pin Configuration in Evaluator Mode (LQFP package)



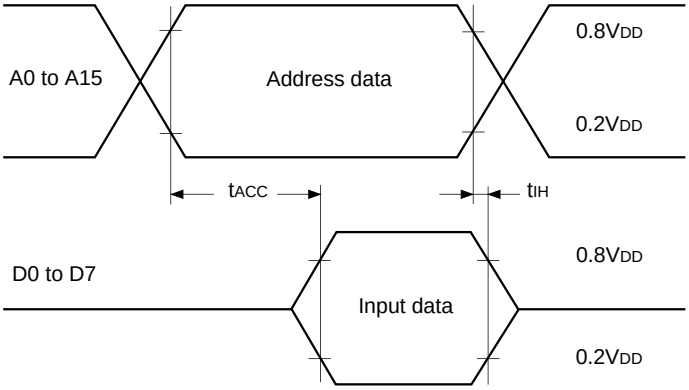
Note) 1. NC (Pin 88) is always connected to V_{DD}.

2. Vss (Pins 39 and 89) are both connected to GND.

EPROM Read Timing

(Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

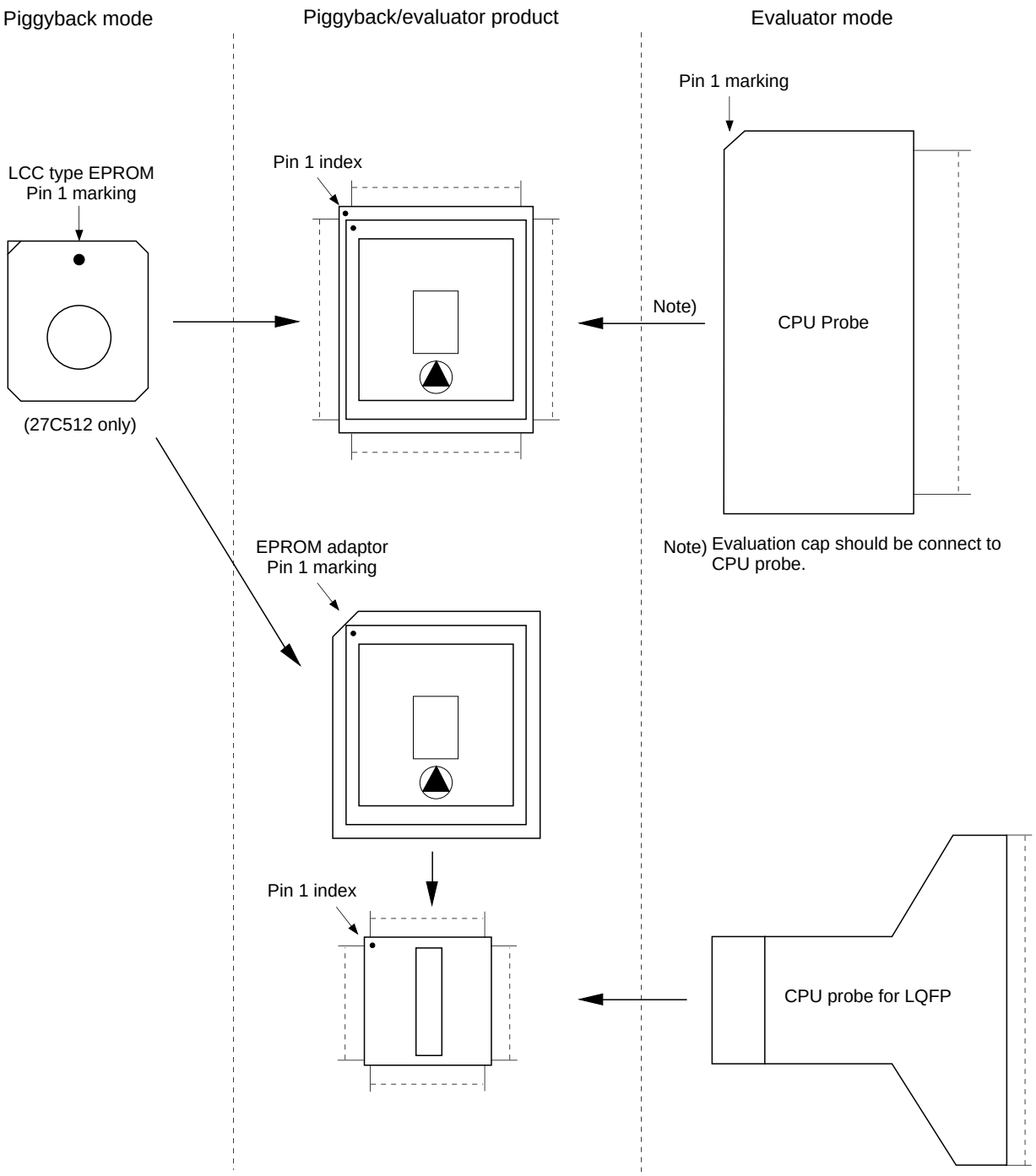
Item	Symbol	Pins	Min.	Max.	Unit
Address → Data input delay time	t_{ACC}	A0 to A15 D0 to D7		120	ns
Address → Data Hold time	t_{IH}	A0 to A15 D0 to D7	0		ns



Products List

Option item	Products				
	Mask type				Piggyback/evaluator type
	CXP83120A	CXP83124A	CXP83232A	CXP83240A	CXP83200A-U01Q CXP83200A-U01R
Package	100-pin plastic QFP/LQFP				100-pin ceramic PQFP
Rom capacitance	20K bytes	24K bytes	32K bytes	40K bytes	EPROM 40K bytes
RAM capacitance	644 bytes		1120bytes		1120 bytes
Pull-up resistance for reset	Existent/Non-existent				Existent

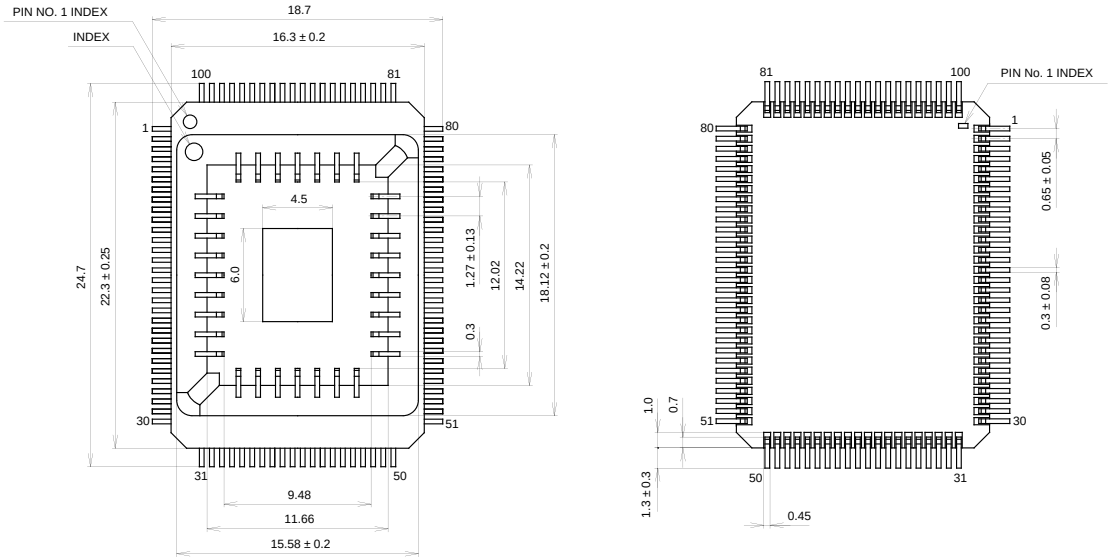
Piggyback mode/evaluator mode can be switched as shown below.

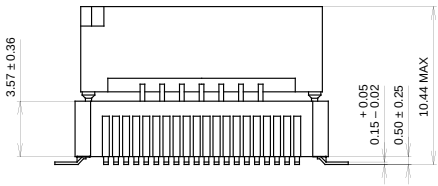


Note) Evaluation cap should be connect to CPU probe.

Package Outline Unit: mm

100PIN PQFP (CERAMIC)



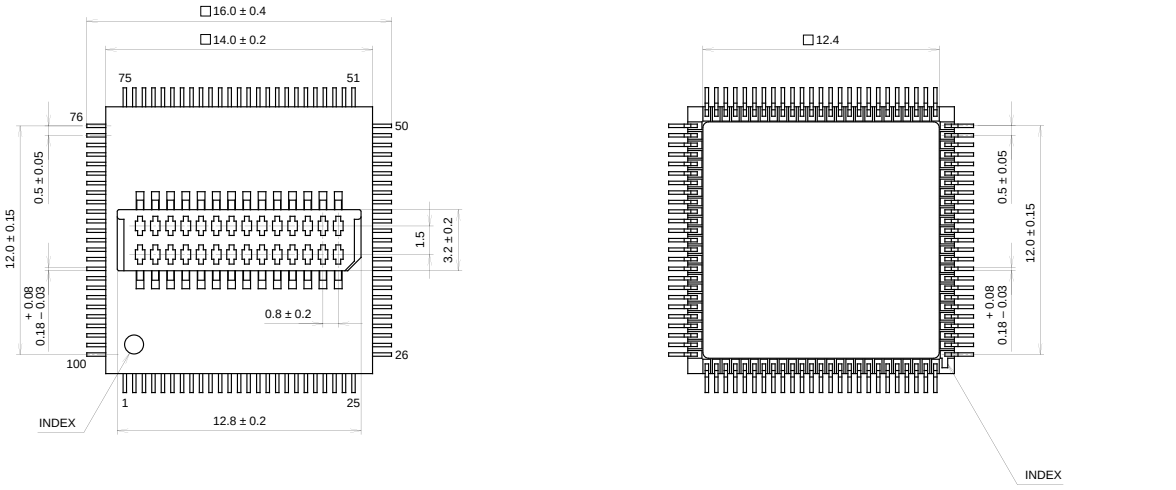


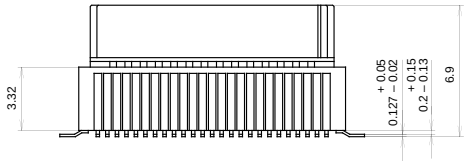
PACKAGE STRUCTURE

SONY CODE	PQFP-100C-L01
EIAJ CODE	AQFP100-C-0000-A
JEDEC CODE	————

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	5.7g

100PIN PQFP (CERAMIC)





PACKAGE STRUCTURE

SONY CODE	PQFP-100C-L02
EIAJ CODE	AQFP100-C-1414-A
JEDEC CODE	————

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	2.2g

littlediode
COMPONENTS FOR ALL

Littlediode supplies new, hard to find or obsolete electronic components and semiconductors all over the world.

With over two million different components listed you are sure to find the part you need.

Feel free to visit us today at our online store:

LittleDiode.com

Looking forward to providing you with the best possible service.