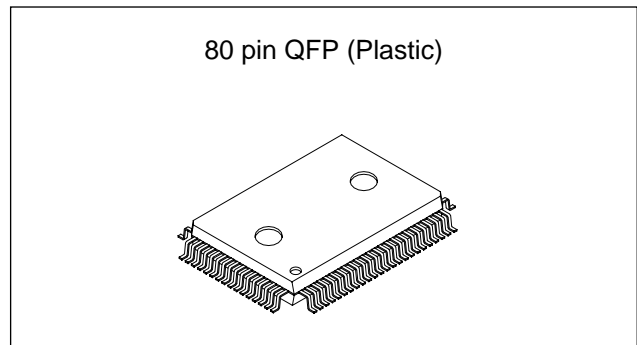


## CMOS 8-bit Single Chip Microcomputer

### Description

The CXP82940/82948/82952/82960 is a CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time base timer, fluorescent display panel controller/driver, I<sup>2</sup>C bus interface, remote control transmission circuit, remote control reception circuit, and 32kHz timer/counter besides the basic configurations of 8-bit CPU, ROM, RAM, and I/O port.



### Features

- Wide-range instruction system (213 instructions) to cover various types of data

- 16-bit arithmetic/multiplication and division/boolean bit operation instructions

- Minimum instruction cycle

250ns at 16MHz operation  
(122µs at 32kHz operation)

- Incorporated ROM capacity

40K bytes (CXP82940)  
48K bytes (CXP82948)  
52K bytes (CXP82952)  
60K bytes (CXP82960)

- Incorporated RAM capacity

2048 bytes (including fluorescent display area)

- Peripheral functions

- A/D converter

8-bit, 8-channel, successive approximation method  
(Conversion time of 20µs/16MHz)

- Serial interface

Buffer RAM incorporated (Auto transfer for 1 to 32 bytes), 1 channel  
8-bit, 8-stage FIFO incorporated  
(Auto transfer for 1 to 8 bytes), 1 channel

- Timers

8-bit timer, 8-bit timer/counter, 19-bit time base timer  
32kHz timer/counter

- Fluorescent display panel controller/driver

Maximum of 196 segments display possible  
1 to 16-digit dynamic display

Dimmer function  
High voltage drive output (40V)  
Incorporated pull-down resistor (Mask option)  
Hardware key scan function  
Maximum of 12 x 8 key matrix supportable

- I<sup>2</sup>C bus interface

- Remote control transmission circuit

Auto transmission for 1 to 32 bytes,  
restart function, carrier output function

- Remote control reception circuit

8-bit pulse measurement counter, 6-stage FIFO  
16 factors, 15 vectors, multi-interruption possible

- Interruption

SLEEP/STOP

- Standby mode

- Package

80-pin plastic QFP

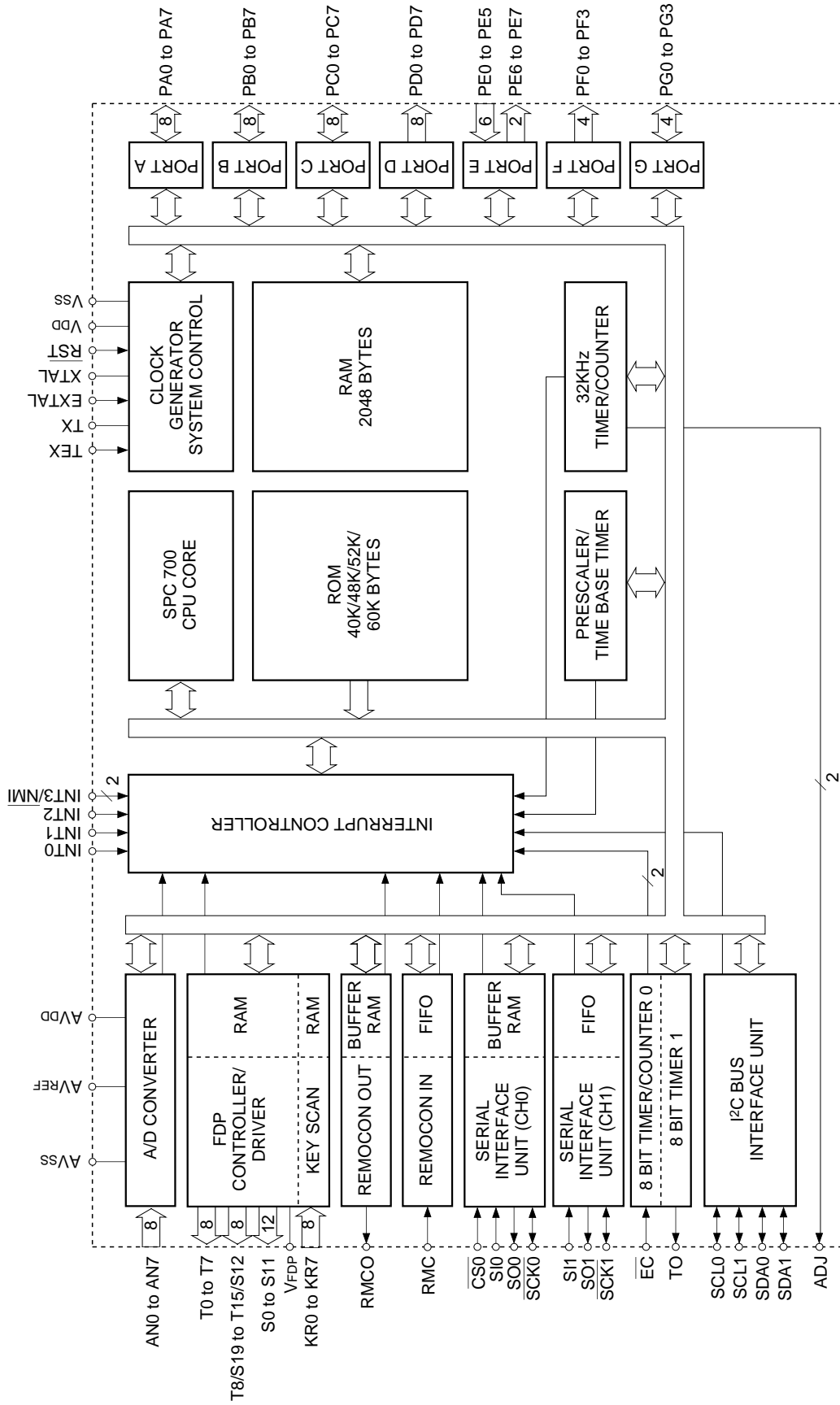
- Piggyback/evaluation chip

CXP82900 80-pin ceramic QFP

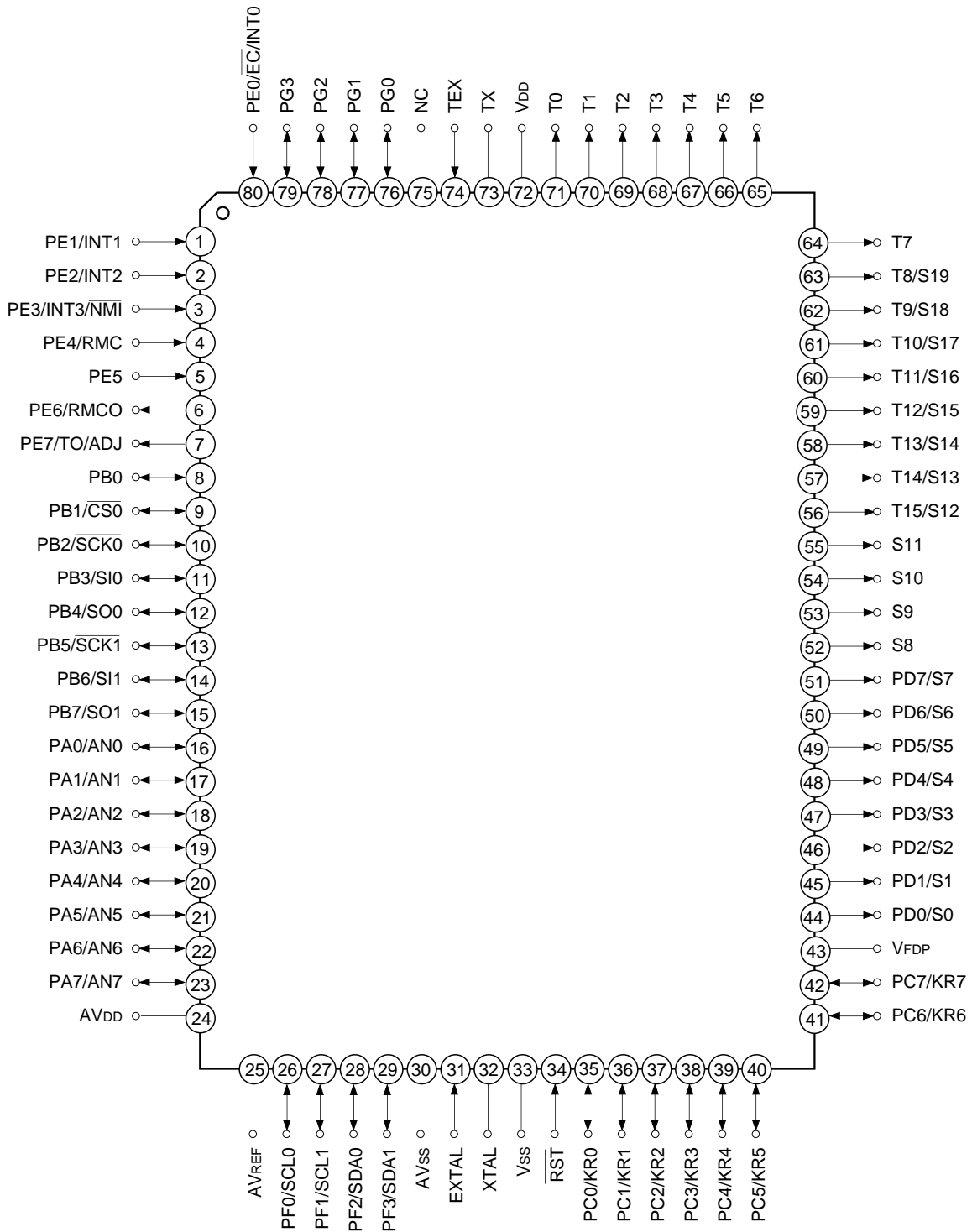
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Block Diagram



Pin Assignment (Top View)



**Note)** NC (Pin 75) must be connected to VDD.

Pin Description

Pin code	I/O	Functions		
PA0/AN0 to PA7/AN7	I/O/ Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (8 pins)	
PB0	I/O	(Port B) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Chip select input for serial interface (CH0).	
PB1/ $\overline{CS0}$	I/O/Input		Serial clock I/O (CH0).	
PB2/ $\overline{SCK0}$	I/O/I/O		Serial data input (CH0).	
PB3/SI0	I/O/Input		Serial data output (CH0).	
PB4/SO0	I/O/Output		Serial clock I/O (CH1).	
PB5/ $\overline{SCK1}$	I/O/I/O		Serial data input (CH1).	
PB6/SI1	I/O/Input		Serial data output (CH1).	
PB7/SO1	I/O/Output			
PC0/KR0 to PC7/KR7	I/O/Input	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Capable of driving 12mA sync current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Serves as key return inputs when operating key scan with fluorescent display panel (FDP) segment signal (8 pins).	
PE0/ $\overline{INT0/EC}$	Input/Input/Input	(Port E) 8-bit port. Lower 6 bits are for inputs; upper 2 bits are for outputs. (8 pins)	Inputs for external interruption request. (4 pins)	External event inputs for timer/counter.
PE1/INT1	Input/Input			Non-maskable interruption request input.
PE2/INT2	Input/Input		Remote control reception circuit input.	
PE3/INT3/ NMI	Input/Input/Input		Carrier output of remote control transmission circuit.	
PE4/RMC	Input/Input		Output for the timer/counter rectangular waves, and 32kHz oscillation dividing frequency.	
PE5	Input			
PE6/RMCO	Output/Output			
PE7/TO/ADJ	Output/Output/ Output			
PF0/SCL0 PF1/SCL1	Output/I/O	(Port F) 4-bit output port, operating as N-ch open drain output for large current (12mA). (4 pins)	Transfer clock I/Os for I <sup>2</sup> C bus interface.	
PF2/SDA0 PF3/SDA1	Output/I/O		Transfer data I/Os for I <sup>2</sup> C bus interface.	

Pin code	I/O	Functions	
PG0 to PG3	I/O	(Port G) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (4 pins)	
PD0/S0 to PD7/S7	Output/Output	(Port D) 8-bit output ports. (8 pins)	FDP segment signal outputs. (8 pins)
S8 to S11	Output	FDP segment signal outputs. (4 pins)	
T8/S12 to T15/S19	Output/Output	Outputs for FDP timing signals/segment signals. (8 pins)	
T0 to T7	Output	FDP timing signal outputs.	
V <sub>FDP</sub>		FDP voltage supply when incorporated resistor is set by mask option.	
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL	Output		
TEX	Input	Crystal connectors for 32kHz timer/counter clock oscillation. Set 32kHz crystal oscillator between TEX and TX. For usage as event input, attach clock source to TEX, and open TX.	
TX	Output		
$\overline{\text{RST}}$	Input	Low-level active, system reset.	
NC		NC. Under normal operation, connect to V <sub>DD</sub> .	
AV <sub>DD</sub>		Positive power supply for A/D converter.	
AV <sub>REF</sub>	Input	Reference voltage input for A/D converter.	
AV <sub>SS</sub>		A/D converter GND.	
V <sub>DD</sub>		Positive power supply.	
V <sub>SS</sub>		GND.	

I/O Circuit Format for Pins

Pin	Circuit format	When reset
<p>PA0/AN0 to PA7/AN7</p> <p>8 pins</p>	<p>Port A</p> <p>Pull-up resistor "0" when reset</p> <p>Port A data</p> <p>Port A direction "0" when reset</p> <p>Data bus ←</p> <p>RD (Port A)</p> <p>Port A input selection "0" when reset</p> <p>Input multiplexer</p> <p>A/D converter</p> <p>IP Input protection circuit</p> <p>* Pull-up transistor approx. 100kΩ</p>	<p>Hi-Z</p>
<p>PB1/<math>\overline{CS0}</math> PB3/SI0 PB6/SI1</p> <p>3 pins</p>	<p>Port B</p> <p>Pull-up resistor "0" when reset</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus ←</p> <p>RD (Port B)</p> <p>CS0 SI0 SI1</p> <p>Schmitt input</p> <p>* Pull-up transistor approx. 100kΩ</p> <p>Not Schmitt input for SI0 and SI1.</p>	<p>Hi-Z</p>
<p>PB2/<math>\overline{SCK0}</math> PB5/<math>\overline{SCK1}</math></p> <p>2 pins</p>	<p>Port B</p> <p>Pull-up resistor "0" when reset</p> <p><math>\overline{SCK}</math> OUT Output enable</p> <p>Port B output selection "0" when reset</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus ←</p> <p>RD (Port B)</p> <p>Schmitt input</p> <p>* Pull-up transistor approx. 100kΩ</p> <p><math>\overline{SCK}</math> in</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
PB4/SO0 PB7/SO1  2 pins	<p>Port B</p> <p>* Pull-up transistor approx. 100kΩ</p>	Hi-Z
PC0/KR0 to PC7/KR7  8 pins	<p>Port C</p> <p>*1 Large current 12mA *2 Pull-up transistor approx. 100kΩ</p>	Hi-Z
PE0/ $\overline{EC}$ /INT0 PE1/INT1 PE2/INT2 PE3/INT3/ $\overline{NMI}$ PE4/RMC 5 pins	<p>Port E</p>	Hi-Z
PE5 1 pin	<p>Port E</p>	Hi-Z
PE6/RMCO 1 pin	<p>Port E</p>	High level

Pin	Circuit format	When reset
<p>PE7/TO/ADJ</p> <p>1 pin</p>	<p>Port E</p> <p>Internal reset signal</p> <p>Port E data</p> <p>00 01 ADJ16K*1 10 ADJ2K*1 11</p> <p>MPX</p> <p>Port E output selection (upper)</p> <p>Port E output selection (lower)</p> <p>"00" when reset</p> <p>TO output enable</p> <p>*1 ADJ signal is a frequency dividing output for 32kHz oscillation frequency adjustment. ADJ2 can be used for buzzer output.</p> <p>*2 Pull-up transistor approx. 150kΩ.</p>	<p>High level (with approx. 150kΩ resistor when reset)</p>
<p>PF0/SCL0 PF1/SCL1 PF2/SDA0 PF3/SDA1</p> <p>4 pins</p>	<p>Port F</p> <p>SCL, SDA</p> <p>I2C output enable ("0" when reset)</p> <p>Port F data "1" when reset</p> <p>Schmitt input</p> <p>SCL, SDA (I2C circuit)</p> <p>Large current 12mA</p> <p>BUS SW</p> <p>To internal I2C pin (to SCL1 for SCL0)</p>	<p>Hi-Z</p>
<p>Port B</p> <p>Port G</p> <p>PB0 PG0 to PG3</p> <p>5 pins</p>	<p>Pull-up resistor "0" when reset</p> <p>Port B data or Port G data</p> <p>Port B direction or Port G direction "0" when reset</p> <p>Data bus</p> <p>RD (Port B or Port G)</p> <p>* Pull-up transistor approx. 100kΩ</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PD0/S0 to PD7/S7</p> <p>8 pins</p>	<p>Port D</p>	<p>Hi-Z or Low level (when PD resistor is connected)</p>
<p>S8 to S11 T15/S12 to T8/S19 T0 to T7</p> <p>20 pins</p>		<p>Hi-Z or Low level (when PD resistor is connected)</p>
<p>EXTAL XTAL</p> <p>2 pins</p>	<ul style="list-style-type: none"> <li>• Diagram shows circuit composition during oscillation.</li> <li>• Feedback resistor is removed during stop, and XTAL becomes High.</li> </ul>	<p>Oscillation</p>
<p>TEX TX</p> <p>2 pins</p>	<ul style="list-style-type: none"> <li>• Diagram shows circuit composition during oscillation.</li> <li>• When the operation of the oscillation circuit is stopped by the software, the feedback resistor is removed, and TEX becomes Low level and TX becomes High level.</li> </ul>	<p>Oscillation</p>
<p><math>\overline{\text{RST}}</math></p> <p>1 pin</p>		<p>Low level</p>

## Absolute Maximum Ratings

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V <sub>DD</sub>	-0.3 to +7.0	V	
Input voltage	V <sub>IN</sub>	-0.3 to +7.0* <sup>1</sup>	V	
Output voltage	V <sub>OUT</sub>	-0.3 to +7.0* <sup>1</sup>	V	
Display output voltage	V <sub>OD</sub>	V <sub>DD</sub> - 40 to V <sub>DD</sub> + 0.3	V	As P channel transistor is open drain, V <sub>DD</sub> is reference.
High level output current	I <sub>OH</sub>	-5	mA	All pins excluding outputs* <sup>2</sup> (value per pin)
	I <sub>ODH1</sub>	-15	mA	Display outputs S0 to S11 (value per pin)
	I <sub>ODH2</sub>	-35	mA	Display outputs T0 to T7, and T8/S19 to T15/S12 (value per pin)
High level total output current	ΣI <sub>OH</sub>	-40	mA	Total for all pins excluding display outputs
	ΣI <sub>ODH</sub>	-100	mA	Total for all display outputs
Low level output current	I <sub>OL</sub>	15	mA	Port (value per pin)
	I <sub>OLC</sub>	20	mA	Large current Port (value per pin)* <sup>3</sup>
Low level total output current	ΣI <sub>OL</sub>	100	mA	Total for all output pins
Operating temperature	T <sub>opr</sub>	-20 to +75	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	
Allowable power dissipation	P <sub>D</sub>	600	mW	

\*1) V<sub>IN</sub> and V<sub>OUT</sub> must not exceed V<sub>DD</sub> + 0.3V.

\*2) Specifies output current of general-purpose I/O ports.

\*3) The large current drive transistor is the N-CH transistor of Port C (PC) and Port F (PF).

**Note)** Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

## Recommended Operating Conditions

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V <sub>DD</sub>	4.5	5.5	V	Guaranteed operation range for high-speed mode (1/2, 1/4 frequency dividing clock)
		3.5	5.5	V	Guaranteed operation range for low-speed mode (1/16 frequency dividing clock) or SLEEP mode
		2.7	5.5	V	Guaranteed operation range with TEX clock
		2.5	5.5	V	Guaranteed data hold range during STOP
High level input voltage	V <sub>IH</sub>	0.7V <sub>DD</sub>	V <sub>DD</sub>	V	*1
	V <sub>IHS</sub>	0.8V <sub>DD</sub>	V <sub>DD</sub>	V	Hysteresis input*2
	V <sub>IHEX</sub>	V <sub>DD</sub> - 0.4	V <sub>DD</sub> + 0.3	V	EXTAL *3
Low level input voltage	V <sub>IL</sub>	0	0.3V <sub>DD</sub>	V	*1
	V <sub>ILS</sub>	0	0.2V <sub>DD</sub>	V	Hysteresis input*2
	V <sub>ILEX</sub>	-0.3	0.4	V	EXTAL *3
Operating temperature	Topr	-20	+75	°C	

\*1) Value for each pin of normal input port (PA, PB0, PB3, PB4, PB6, PB7, PC, PE5, PG).

\*2) Value of the following pins:  $\overline{\text{RST}}$ ,  $\overline{\text{CS0}}$ ,  $\overline{\text{SCK0}}$ ,  $\overline{\text{SCK1}}$ ,  $\overline{\text{EC/INT0}}$ , INT1, INT2, INT3/ $\overline{\text{NMI}}$ , RMC, SCL0, SCL1, SDA0, SDA1.

\*3) Specifies only during external clock input.

Electrical Characteristics

DC Characteristics

(Ta = -20 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output current	VOH	PA, PB, PC, PE6, PE7, PG	VDD = 4.5V, IOH = -0.5mA	4.0			V
			VDD = 4.5V, IOH = -1.2mA	3.5			V
Low level output current	VOL	PA, PB, PC, PE6, PE7, PG	VDD = 4.5V, IOL = 1.8mA			0.4	V
			VDD = 4.5V, IOL = 3.6mA			0.6	V
		PC, PF	VDD = 4.5V, IOL = 12.0mA			1.5	V
		PF (SCL0, SCL1, SDA0, SDA1)	VDD = 4.5V, IOL = 3.0mA			0.4	V
			VDD = 4.5V, IOL = 4.0mA			0.6	V
Input current	IiHE	EXTAL	VDD = 5.5V, VIH = 5.5V	0.5		40	μA
	IiLE		VDD = 5.5V, VIL = 0.4V	-0.5		-40	μA
	IiHT	TEX	VDD = 5.5V, VIL = 5.5V	0.1		10	μA
	IiLT		VDD = 5.5V, VIL = 0.4V	-0.1		-10	μA
	IiLR	RST*1	VDD = 5.5V, VIL = 0.4V	-1.5		-400	μA
	IiL	PA to PC*2, PG*2	VDD = 4.5V, VIL = 4.0V	-3.3		-50	μA
Display output current	IOH	S0 to S11		-8			mA
		S12/T15 to S19/T8, T0 to T7	VDD = 4.5V VOH = VDD - 2.5V	-20			mA
Open drain output leakage current (P-CH Tr off state)	ILOL	S0 to S11, S12/T15 to S19/T8, T0 to T7	VDD = 5.5V VOL = VDD - 35V VFDP = VDD - 35V			-20	μA
Pull-down resistance*3	RL	S0 to S11, S12/T15 to S19/T8, T0 to T7	VDD = 5V VOD - VFDP = 30V	60	100	270	kΩ
I/O leakage current	IIZ	PA to PC*2, PG*2, RST*1	VDD = 5.5V VI = 0, 5.5V			±10	μA
Open drain output leakage current (N-ch Tr off state)	ILOH	PF	VDD = 5.5V, VOH = 5.5V			10	μA
I <sup>2</sup> C bus switch connection impedance (Output Tr off state)	RBS	SCL0: SCL1 SDA0: SDA1	VDD = 4.5V VSCL0 = VSCL1 = 2.25V VSDA0 = VSDA1 = 2.25V			120	Ω

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Power supply current*4	I <sub>DD1</sub>	V <sub>DD</sub>	High speed mode operation (1/2 frequency dividing clock)		31	50	mA
			V <sub>DD</sub> = 5.5V, 10MHz crystal oscillation (C <sub>1</sub> = C <sub>2</sub> = 15pF)				
	I <sub>DD2</sub>		V <sub>DD</sub> = 3V, 32kHz crystal oscillation (C <sub>1</sub> = C <sub>2</sub> = 47pF)		40	100	μA
	I <sub>DDS1</sub>		SLEEP mode		2.5	10	mA
			V <sub>DD</sub> = 5.5V, 16MHz crystal oscillation (C <sub>1</sub> = C <sub>2</sub> = 15pF)				
	I <sub>DDS2</sub>		V <sub>DD</sub> = 3V, 32kHz crystal oscillation (C <sub>1</sub> = C <sub>2</sub> = 47pF)		8	30	μA
I <sub>DDS3</sub>	STOP mode V <sub>DD</sub> = 5.5V, termination of 16MHz and 32kHz crystal oscillation				10	μA	
Input capacity	C <sub>IN</sub>	PA to PC, PE0 to PE5, PF, PG, EXTAL, XTAL, TEX, TX, $\overline{\text{RST}}$	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

- \*1)  $\overline{\text{RST}}$  specifies the input current when pull-up resistance has been selected; leakage current when no resistance has been selected.
- \*2) PA to PC and PG specify the input current when pull-up resistance has been selected, leakage current when no resistance has been selected.
- \*3) When incorporated pull-down resistance has been selected through mask option.
- \*4) When all pins are open.

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	1		16	MHz
System clock input pulse width	tXL tXH	EXTAL	Fig. 1, Fig. 2 External clock drive	28			ns
System clock input rise time, fall time	tCR tCF	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	tEH tEL	EC	Fig. 3	4tsys*			ns
Event count input clock rise time, fall time	tER tEF	EC	Fig. 3			20	ms
System clock frequency	fc	TEX TX	VDD = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count input pulse width	tTL tTH	TEX	Fig. 3	10			μs
Event count input rise time, fall time	tTR tTF	TEX	Fig. 3			20	ms

\* tsys indicates the three values below according to the upper two bits (CPU clock selected) of the control clock register (address: 00FEH).

tsys (ns) = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Fig. 1. Clock timing

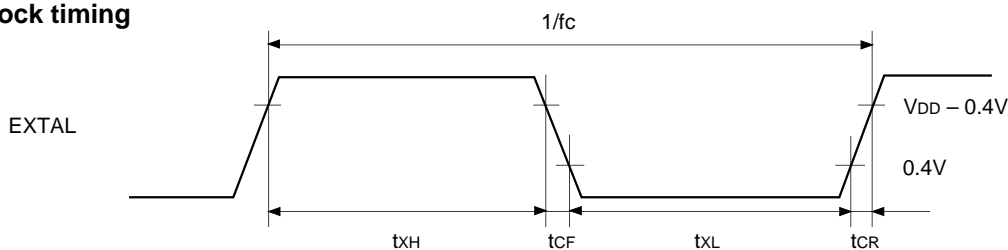


Fig. 2. Clock applied conditions

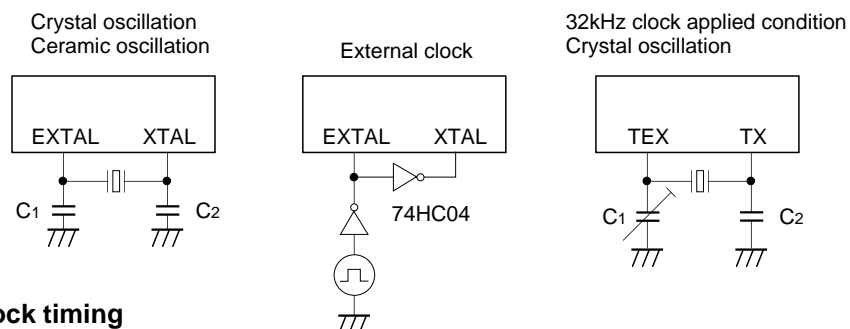
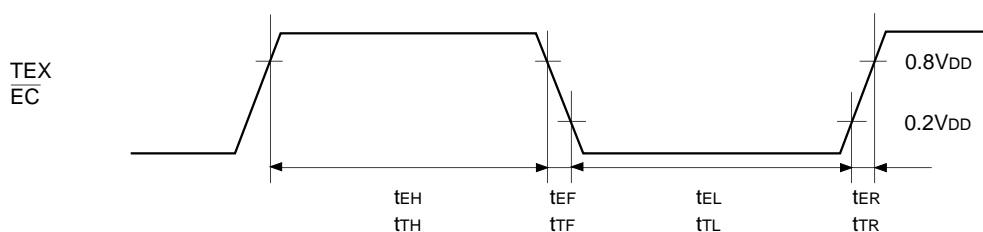


Fig. 3. Event count clock timing



(2) Serial transfer (CH0)

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	t <sub>DCSK</sub>	$\overline{SCK0}$	Chip select transfer mode ( $\overline{SCK}$ = output mode)		1.5t <sub>sys</sub> + 200	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ float delay time	t <sub>DCSKF</sub>	$\overline{SCK0}$	Chip select transfer mode ( $\overline{SCK}$ = output mode)		1.5t <sub>sys</sub> + 200	ns
$\overline{CS} \downarrow \rightarrow SO$ delay time	t <sub>DCSO</sub>	SO0	Chip select transfer mode		1.5t <sub>sys</sub> + 200	ns
$\overline{CS} \uparrow \rightarrow SO$ float delay time	t <sub>DCSOF</sub>	SO0	Chip select transfer mode		1.5t <sub>sys</sub> + 200	ns
$\overline{CS}$ High level width	t <sub>WHCS</sub>	$\overline{CS0}$	Chip select transfer mode	t <sub>sys</sub> + 200		ns
$\overline{SCK}$ cycle time	t <sub>KCY</sub>	$\overline{SCK0}$	Input mode	2t <sub>sys</sub> + 200		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ High, Low level width	t <sub>KH</sub> t <sub>KL</sub>	$\overline{SCK0}$	Input mode	t <sub>sys</sub> + 100		ns
			Output mode	8000/fc - 100		ns
SI input setup time (for $\overline{SCK} \uparrow$ )	t <sub>SIK</sub>	SI0	$\overline{SCK}$ input mode	-t <sub>sys</sub> + 100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (for $\overline{SCK} \uparrow$ )	t <sub>KSI</sub>	SI0	$\overline{SCK}$ input mode	2t <sub>sys</sub> + 100		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK} \downarrow \rightarrow SO$ delay time	t <sub>KSO</sub>	SO0	$\overline{SCK}$ input mode		2t <sub>sys</sub> + 200	ns
			$\overline{SCK}$ output mode		100	ns

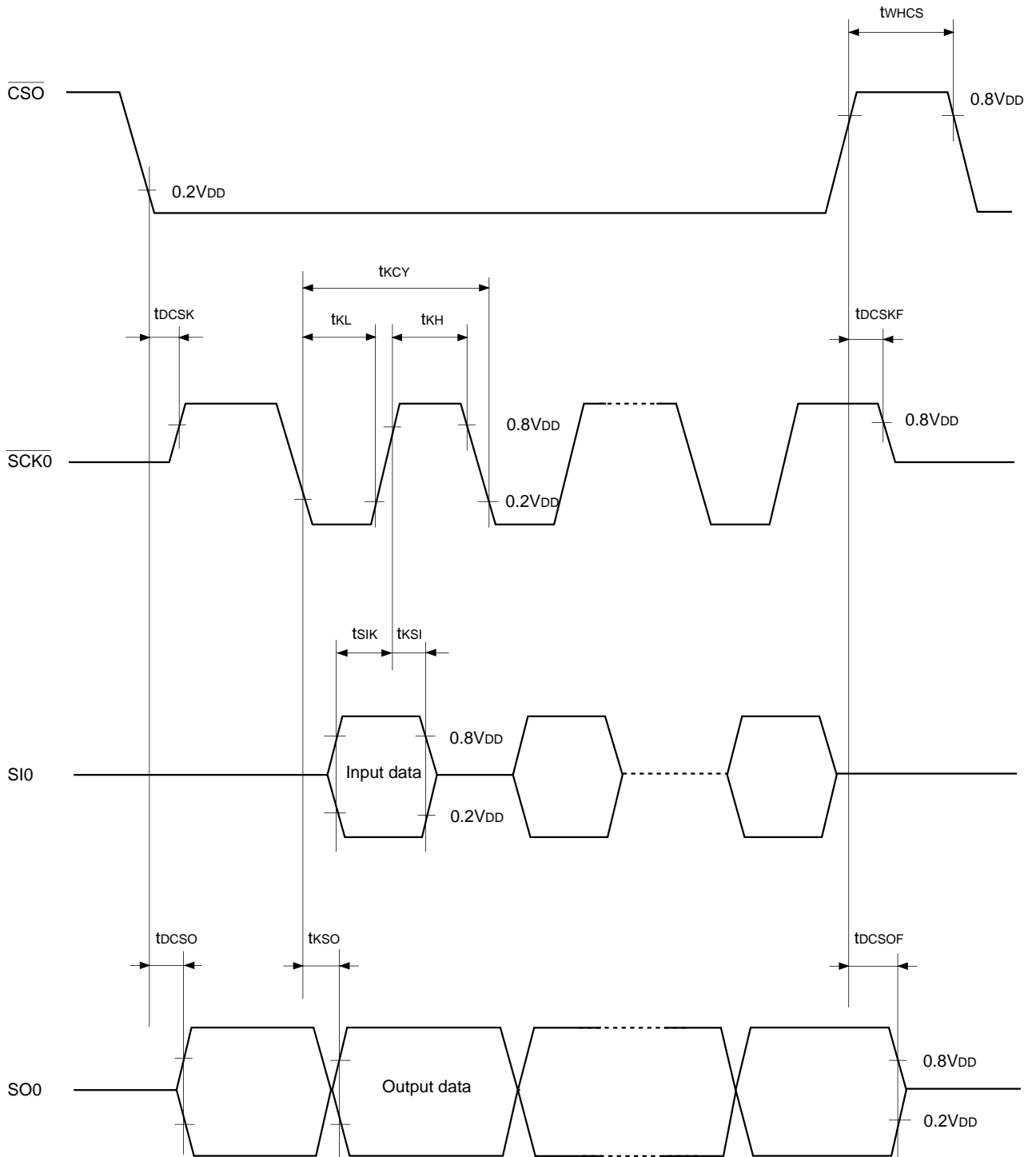
**Note 1)** t<sub>sys</sub> indicates the three values below according to the upper two bits (CPU clock selected) of the control clock register (address: 00FEH).

t<sub>sys</sub> (ns) = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

**Note 2)**  $\overline{CS}$ ,  $\overline{SCK}$ , SI and SO correspond to each pin of  $\overline{CS0}$ ,  $\overline{SCK0}$ , SI0 and SO0.

**Note 3)** The load condition for the  $\overline{SCK}$  output mode, SO output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer CH0 timing (CH0)



**Serial transfer (CH1) (SIO mode)**

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

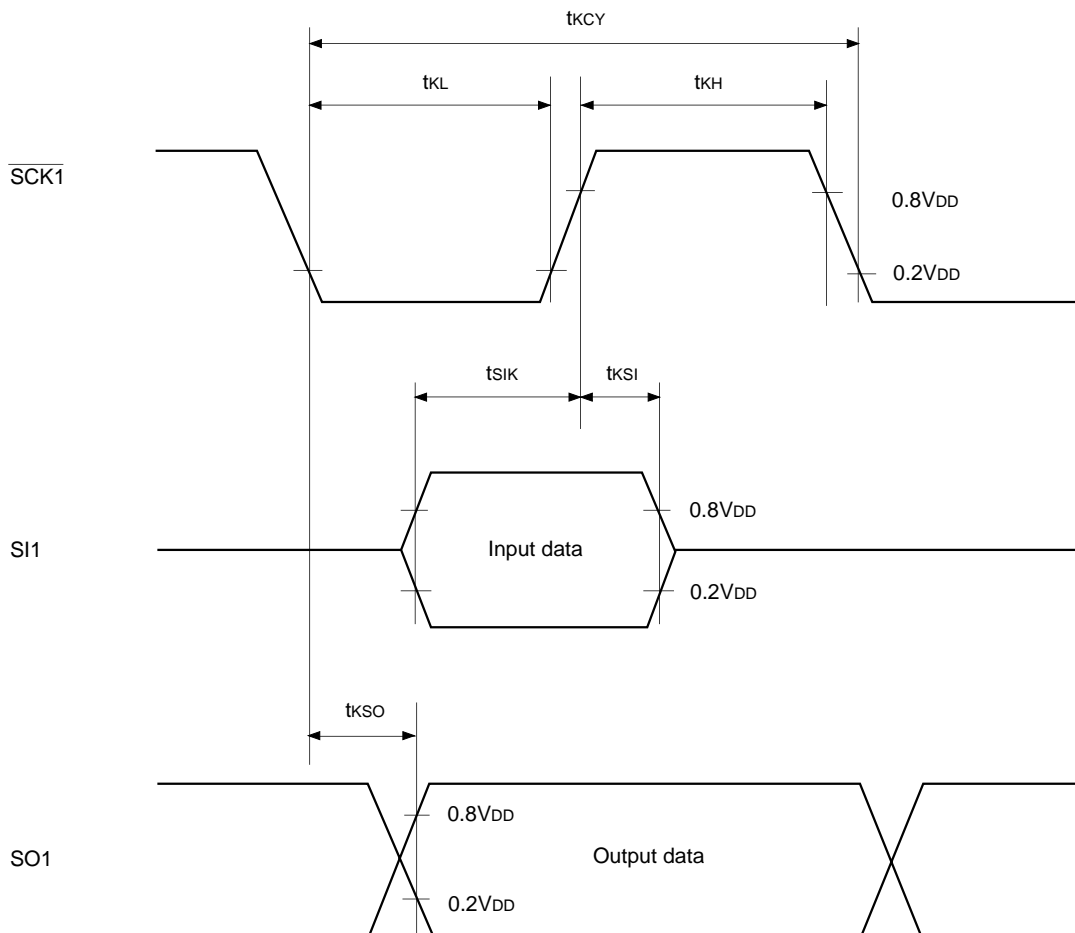
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	$t_{\text{KCY}}$	$\overline{\text{SCK1}}$	Input mode	$2t_{\text{sys}} + 200$		ns
			Ouput mode	$16000/f_c$		ns
$\overline{\text{SCK1}}$ High, Low level width	$t_{\text{KH}}$ $t_{\text{KL}}$	$\overline{\text{SCK1}}$	Input mode	$t_{\text{sys}} + 100$		ns
			Ouput mode	$8000/f_c - 50$		ns
SI1 input setup time (for $\overline{\text{SCK1}} \uparrow$ )	$t_{\text{SIK}}$	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ ouput mode	200		ns
SI1 input hold time (for $\overline{\text{SCK1}} \uparrow$ )	$t_{\text{KSI}}$	SI1	$\overline{\text{SCK1}}$ input mode	$t_{\text{sys}} + 200$		ns
			$\overline{\text{SCK1}}$ ouput mode	100		ns
$\overline{\text{SCK1}} \downarrow \rightarrow \text{SO1}$ delay time	$t_{\text{KSO}}$	SO1	$\overline{\text{SCK1}}$ input mode		$t_{\text{sys}} + 200$	ns
			$\overline{\text{SCK1}}$ ouput mode		100	ns

**Note 1)**  $t_{\text{sys}}$  indicates the three values below according to the upper two bits (CPU clock selected) of the control clock register (address: 00FEH).

$t_{\text{sys}}$  (ns) =  $2000/f_c$  (upper two bits = "00"),  $4000/f_c$  (upper two bits = "01"),  $16000/f_c$  (upper two bits = "11")

**Note 2)** The load condition for the  $\overline{\text{SCK1}}$  output mode, SO1 output delay time is  $50\text{pF} + 1\text{TTL}$ .

**Fig. 5. Serial transfer CH1 timing (SIO mode)**



**Serial transfer (CH1) (Special mode)**

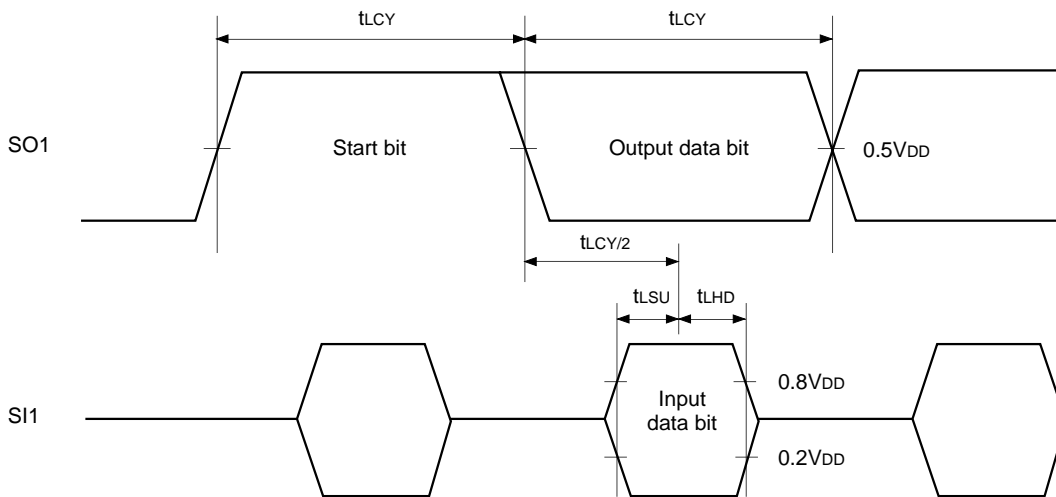
( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
SO1 cycle time	$t_{LCY}^*$	SO1 SI1			104		$\mu\text{s}$
SI1 data setup time	$t_{LSU}$	SI1		2			$\mu\text{s}$
SI1 data hold time	$t_{LHD}$	SI1		2			$\mu\text{s}$

\*  $t_{LCY}$  is specified only when the lower two bits (SO1 clock selected) of the serial mode register (CH1) (SIOM1: address 01E2H) is set to 104 $\mu\text{s}$ .

**Note)** The load condition for SO1 is 50pF + 1TTL.

**Fig. 6. Serial transfer CH1 timing (Special mode)**

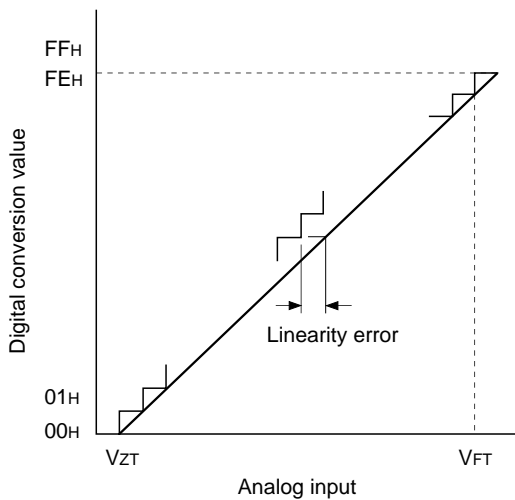


**(3) A/D converter characteristics**

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $AV_{REF} = 4.0$  to  $AV_{DD}$ ,  $V_{SS} = AV_{SS} = 0\text{V}$  reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			$T_a = 25^\circ\text{C}$ $V_{DD} = AV_{DD} = AV_{REF} = 5.0\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$			$\pm 3$	LSB
Zero transition voltage	$V_{ZT}^{*1}$			-10	10	70	mV
Full-scale transition voltage	$V_{FT}^{*2}$			4910	4970	5030	mV
Conversion time	$t_{CONV}$			$160/f_{ADC}^{*3}$			$\mu\text{s}$
Sampling time	$t_{SAMP}$			$12/f_{ADC}^{*3}$			$\mu\text{s}$
Reference input voltage	$V_{REF}$	$AV_{REF}$	$V_{DD} = AV_{DD} = 4.5$ to $5.5\text{V}$	$AV_{DD} - 0.5$		$AV_{DD}$	V
Analog input voltage	$V_{IAN}$	$AN0$ to $AN7$		0		$AV_{REF}$	V
$AV_{REF}$ current	$I_{REF}$	$AV_{REF}$	Operation mode		0.6	1.0	mA
	$I_{REFS}$		SLEEP mode STOP mode 32kHz operation mode			10	$\mu\text{A}$

**Fig. 7. Definition of A/D converter terms**



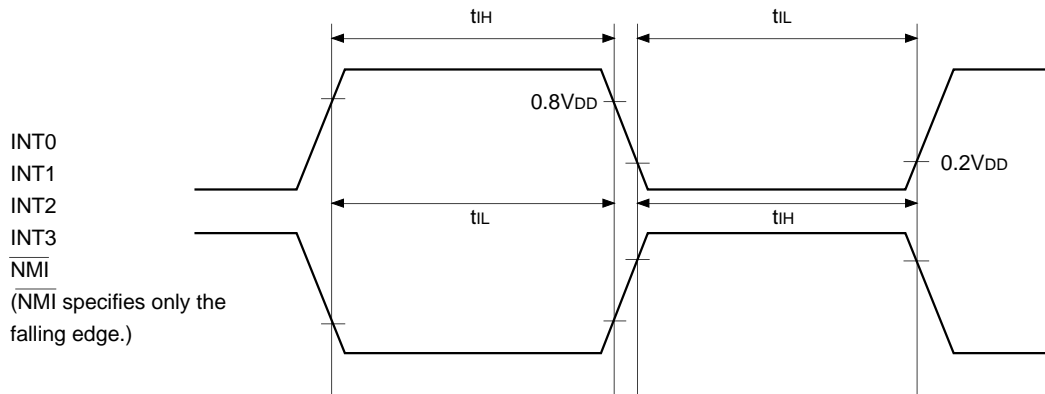
- \*1)  $V_{ZT}$ : Value at which the digital conversion value changes from 00H to 01H and vice versa.
- \*2)  $V_{FT}$ : Value at which the digital conversion value changes from FEH to FFH and vice versa.
- \*3)  $f_{ADC}$  indicates the below values due to the contents of bit 6 (CKS) of the A/D control register (address: 00F9H) and bits 7 (PCK1) and 6 (PCK0) of the clock control register (address: 00FEH).

PCK1, PCK0 \ CKS	0 ( $\phi/2$ selection)	1 ( $\phi$ selection)
	00 ( $\phi = f_{EX}/2$ )	$f_{ADC} = f_c/2$
01 ( $\phi = f_{EX}/4$ )	$f_{ADC} = f_c/4$	$f_{ADC} = f_c/2$
11 ( $\phi = f_{EX}/16$ )	$f_{ADC} = f_c/16$	$f_{ADC} = f_c/8$

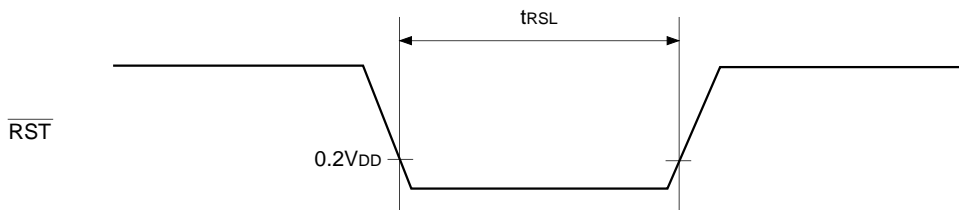
**(4) Interruption, reset input** (Ta = -20 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption High, Low level width	t <sub>IH</sub> t <sub>IL</sub>	INT0 INT1 INT2 INT3 <u>NMI</u>		1		μs
Reset input Low level width	t <sub>RSL</sub>	<u>RST</u>		32/fc		μs

**Fig. 8. Interruption input timing**



**Fig. 9. RST input timing**



(5) I<sup>2</sup>C bus timing

(T<sub>a</sub> = -20 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
SCL clock frequency	f <sub>SCL</sub>	SCL		0	100	kHz
Bus-free time before starting transfer	t <sub>BUF</sub>	SDA, SCL		4.7		μs
Hold time for starting transfer	t <sub>HD; STA</sub>	SDA, SCL		4.0		μs
Clock Low level width	t <sub>LOW</sub>	SCL		4.7		μs
Clock High level width	t <sub>HIGH</sub>	SCL		4.0		μs
Setup time for repetitive transfers	t <sub>SU; STA</sub>	SDA, SCL		4.7		μs
Data hold time	t <sub>HD; DAT</sub>	SDA, SCL		0*		μs
Data setup time	t <sub>SU; DAT</sub>	SDA, SCL		250		ns
SDA, SCL rise time	t <sub>R</sub>	SDA, SCL			1	μs
SDA, SCL fall time	t <sub>F</sub>	SDA, SCL			300	ns
Setup time for transfer completion	t <sub>SU; STO</sub>	SDA, SCL		4.7		μs

\* The data hold time must exceed 300ns because the SCL rise time (300ns max.) is not taken into consideration.

Fig.10. I<sup>2</sup>C bus transfer timing

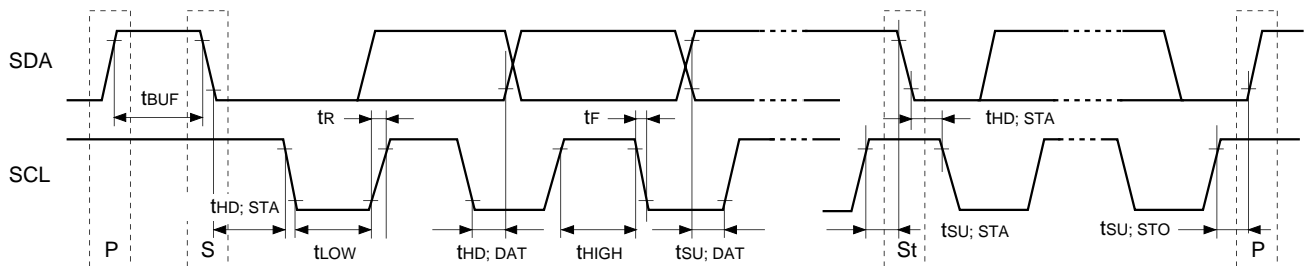
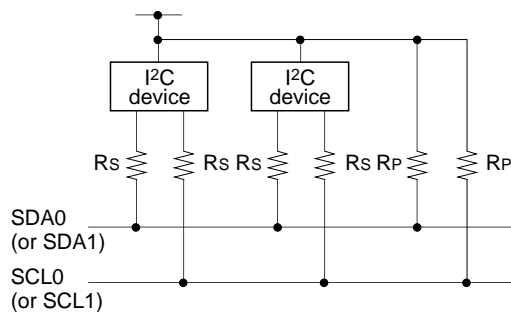


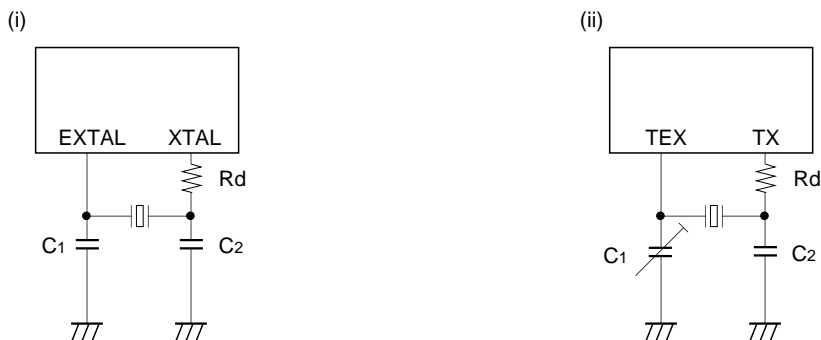
Fig.11. Recommended circuit example for I<sup>2</sup>C device



- Pull-up resistors (R<sub>P</sub>) must be connected to SDA0 (or SDA1) and SCL0 (or SCL1).
- Serial resistance (R<sub>s</sub> = 300Ω or less) of SDA0 (or SDA1) and SCL0 (SCL1) reduces spike noise caused by CRT flash-over.

Appendix

Fig. 12. Recommended oscillation circuit

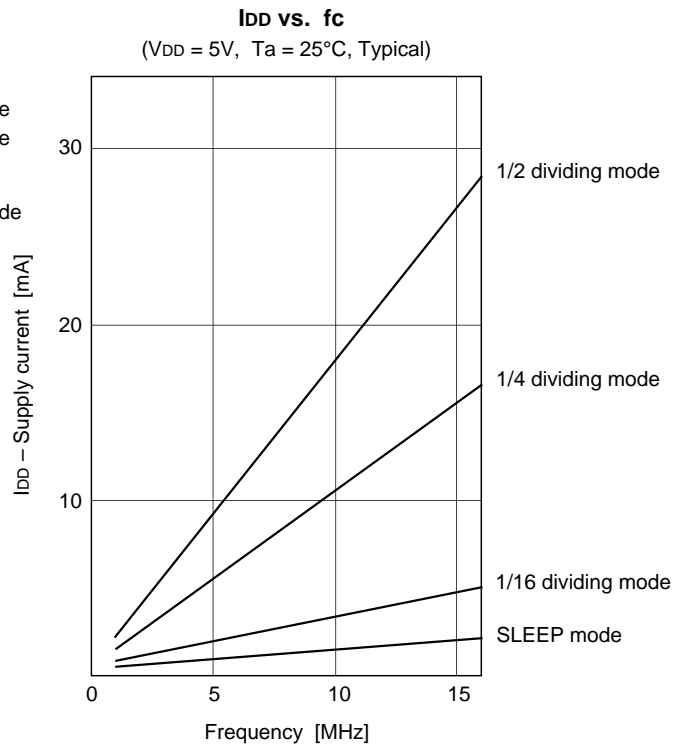
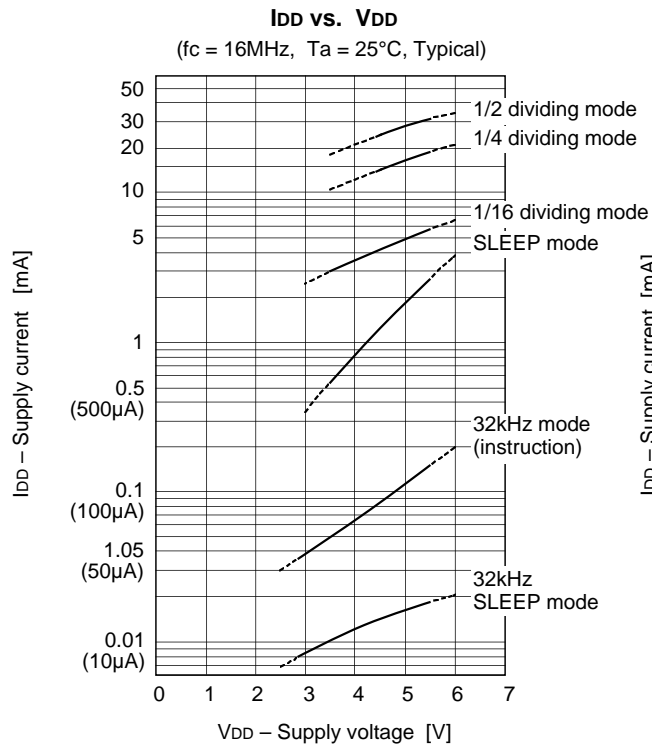


Manufacturer	Model	fc (MHz)	C <sub>1</sub> (pF)	C <sub>2</sub> (pF)	R <sub>d</sub> (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00	5	5		
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16 (12)	16 (12)	0	(i)
		10.00	16 (12)	16 (12)		
		12.00	12	12		
		16.00	12	12		
	P3	32.768kHz	30	18	470k	(ii)

Mask Option Table

Item	Content	
Reset pin pull-up resistance	Non-existent	Existent
High voltage drive output port pull-down resistance	Non-existent	Existent (Selectable for each pin)

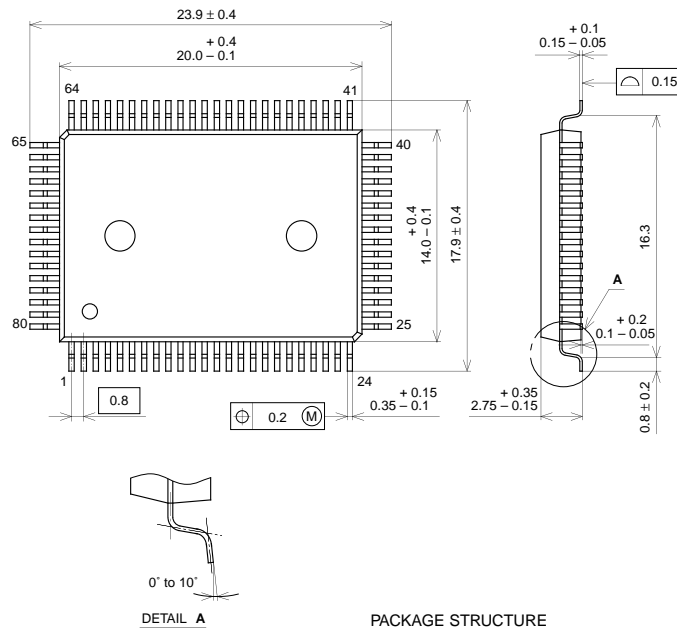
Characteristics Curve



Package Outline

Unit : mm

80PIN QFP (PLASTIC)

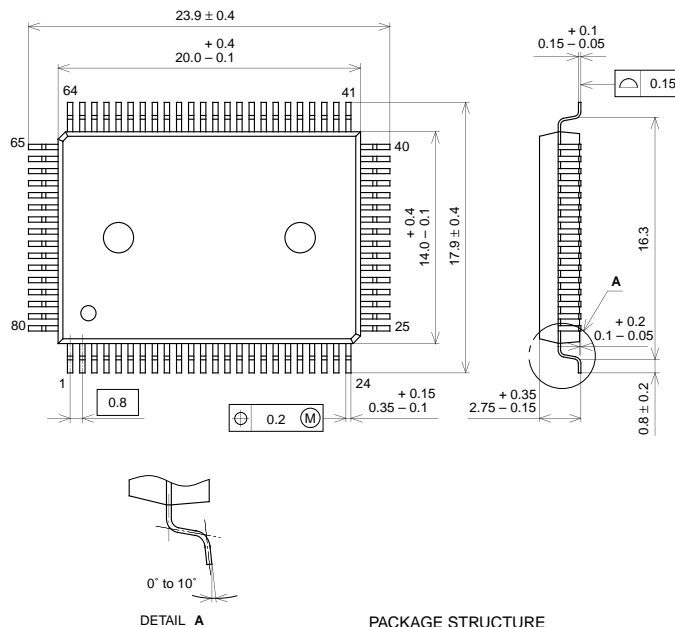


SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g

80PIN QFP (PLASTIC)



SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18μm



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