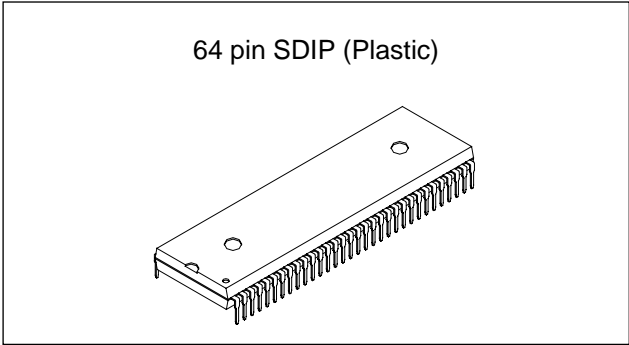


**CMOS 8-bit Single Chip Microcomputer**

**Description**

The CXP82712/82716 microcomputer is composed of a 8-bit CPU, ROM, RAM, and I/O ports. These chips feature many other high-performance circuits in a single-chip CMOS design, including an A/D converter, serial interface, timer/counter, time base timer, fluorescent display controller/driver, remote control receiver, PWM output circuit and 32kHz timer/counter.

This device also includes sleep/stop functions which can be used to achieve low power consumption.



**Structure**

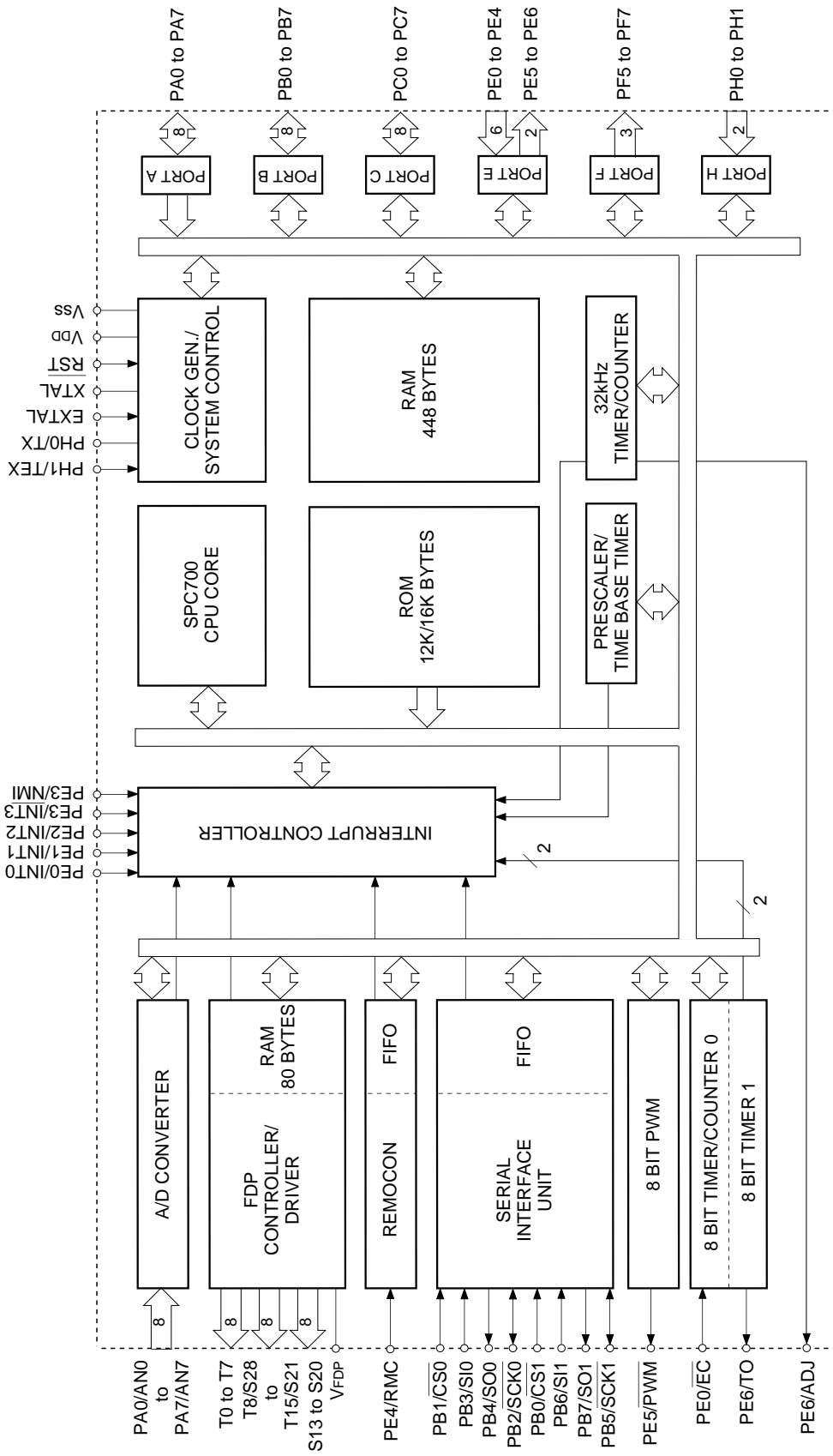
Silicon gate CMOS IC

**Features**

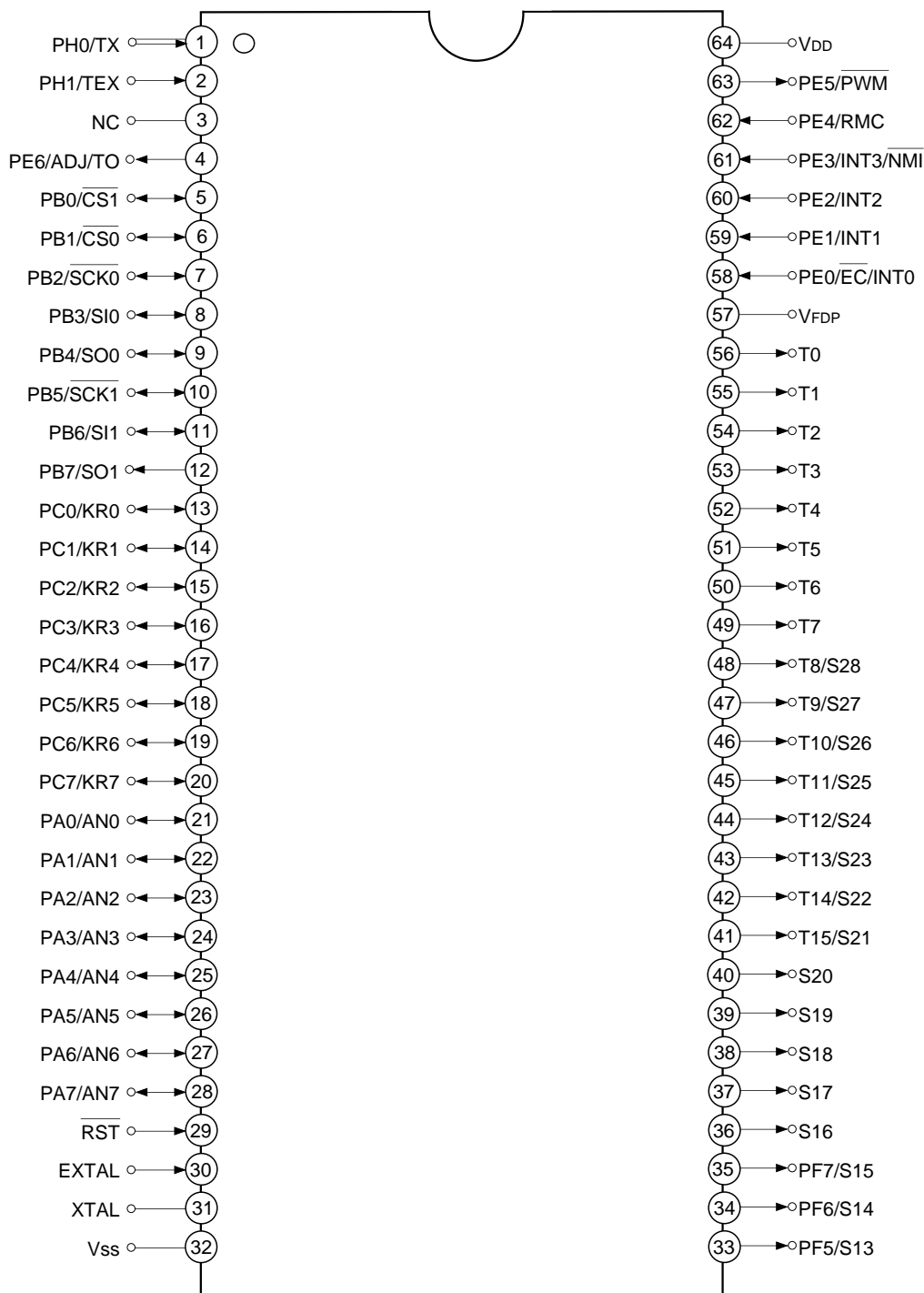
- Instruction set which supports a wide array of data types
  - 213 types of instructions which include 16-bit calculations, multiplication and division arithmetic, and boolean bit operations.
- Minimum instruction cycle 400ns for 10MHz, 122µs for 32kHz operation
- On-chip ROM 12K bytes (CXP82712)  
16K bytes (CXP82716)
- On-chip RAM 448 bytes (Including fluorescent display data area)
- Peripheral functions
  - A/D converter 8-bit, 8-channel, successive approximation system  
(conversion rate 32µs/10MHz)
  - Serial interface On-chip 8-bit, 8-stage FIFO (1 to 8 bytes auto transfer),  
1 circuit 2-channel
  - Timers 8-bit timer  
8-bit timer/counter  
19-bit time base timer  
32kHz timer/counter
  - Fluorescent display controller/driver 24 high voltage tolerance output ports  
Maximum of 144 segments display available  
1 to 16 digits dynamic display  
Dimmer function  
High voltage tolerance output (40V)  
On-chip pull-down resistor (Mask option)  
Hardware key scan function (Maximum of 8 × 8 key matrix available)
- Remote control receiver circuit On-chip 6-stage FIFO 8-bit pulse measurement counter
- PWM output 8-bit, 1-channel
- Interruption 13 factors, 13 vectors, multi-interruption possible
- Standby mode Sleep/stop
- Package 64-pin plastic SDIP
- Piggyback/evaluator CXP82700 64-pin ceramic SDIP

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Block Diagram



Pin Assignment (Top View)



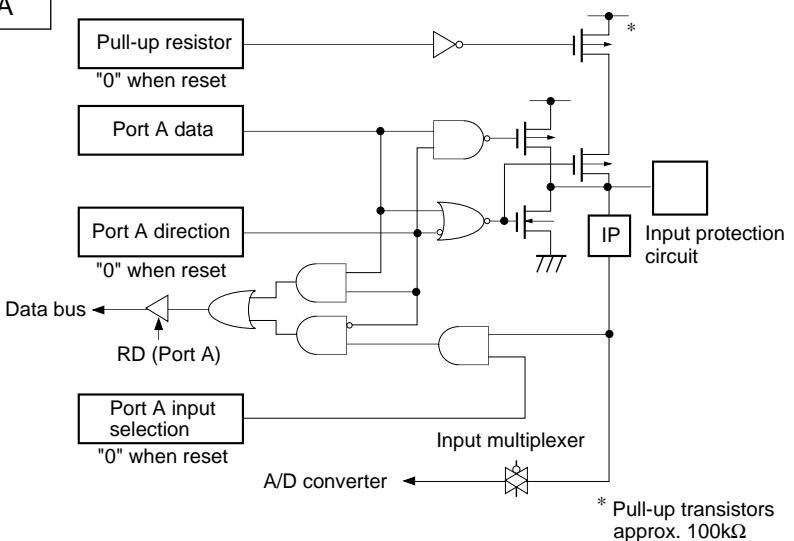
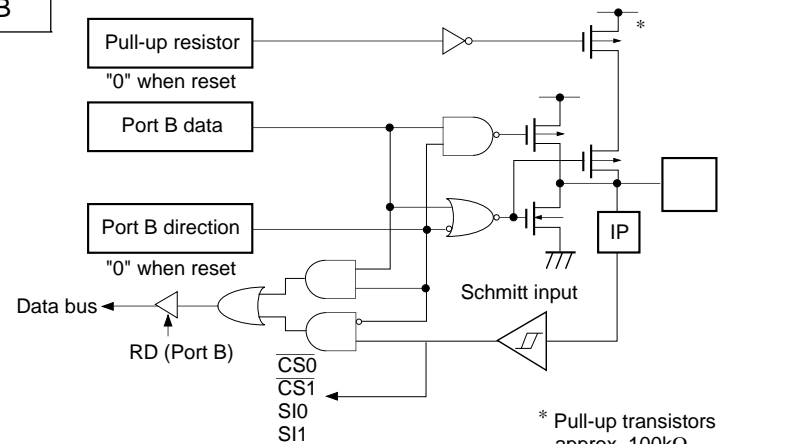
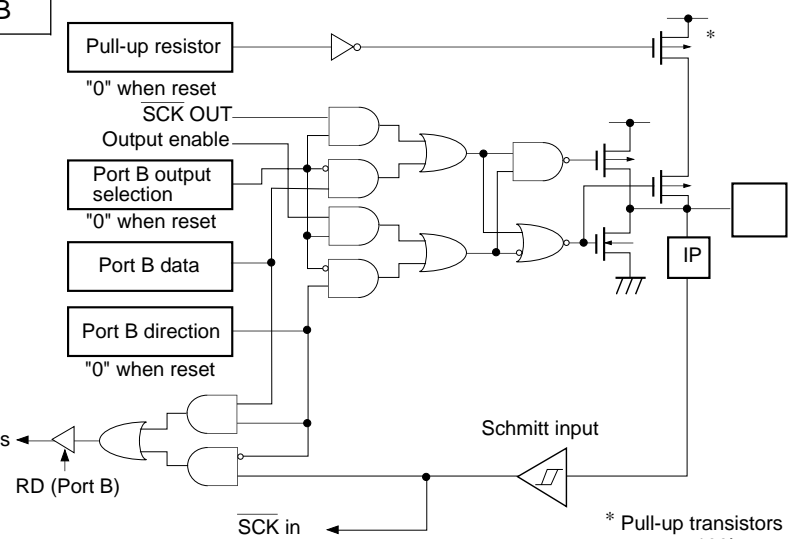
- Note)**
1. NC (Pin 3) is always connected to V<sub>DD</sub>.
  2. PH0/TX (Pin 1) is input port during port selection;  
oscillation output during oscillation selection

Pin Description

Symbol	I/O	Functions	
PA0/AN0 to PA7/AN7	I/O/Analog Input	(Port A) 8-bit I/O port. I/O can be set in a bit unit. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (8 pins)
PB0/ $\overline{\text{CS1}}$	I/O/Input	(Port B) 8-bit I/O port. I/O can be set in a bit unit. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Chip select input for serial interface (CH1).
PB1/ $\overline{\text{CS0}}$	I/O/Input		Chip select input for serial interface (CH0).
PB2/ $\overline{\text{SCK0}}$	I/O/I/O		Serial clock I/O (CH0).
PB3/SI0	I/O/Input		Serial data input (CH0).
PB4/SO0	I/O/Output		Serial data output (CH0).
PB5/ $\overline{\text{SCK1}}$	I/O/I/O		Serial clock I/O (CH1).
PB6/SI1	I/O/Input		Serial data input (CH1).
PB7/SO1	I/O/Output		Serial data output (CH1).
PC0/KR0 to PC7/KR7	I/O/Input	(Port C) 8-bit I/O port. I/O can be set in a bit unit. Capable of driving 12mA sink current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Key return input for FDP segment signal which performs key scanning.
PE0/INT0/ $\overline{\text{EC0}}$	Input/Input/ Input	(Port E) Lower 5 bits are for inputs; upper 2 bits are for outputs. (7 pins)	External interrupt requests. (4 pins)
PE1/INT1	Input/Input		
PE2/INT2	Input/Input		External event input to timer/counter. (1 pin)
PE3/INT3/ $\overline{\text{NMI}}$	Input/Input/ Input		Non-maskable interruption request input.
PE4/RMC	Input/Input		Input for remote control receiver circuit.
PE5/ $\overline{\text{PWM}}$	Output/Output		8-bit PWM output.
PE6/ADJ/TO	Output		Output for timer/counter rectangular waveform and 32kHz oscillation frequency division.

Symbol	I/O	Functions	
PF5/S13 to PF7/S15	Output/Output	(Port F) 3-bit output port. (3 pins)	Segment signal output for FDP.
S16 to S20	Output	Segment signal output for FDP.	
T8/S28 to T15/S21	Output/Output	Dual purpose output for FDP timing and segment signals.	
T0 to T7	Output	Timing signal output for FDP.	
V <sub>FDP</sub>		Provides voltage for FDP when on-chip resistor is selected under mask option.	
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL	Output		
PH1/TEX	Input/Input	(Port H) 2-bit input port. (2 pins)	Crystal connectors for 32kHz timer/counter clock oscillation circuit. Connect a 32kHz crystal oscillator between TEX and TX. For usage as event input, connect clock oscillation source to TEX, and leave TX open.
PH0/TX	Input/Output		
$\overline{\text{RST}}$	Input	System reset pin of active "L" level. $\overline{\text{RST}}$ is input pin.	
NC		NC. Under normal operating conditions, connect to V <sub>DD</sub> .	
V <sub>DD</sub>		Vcc supply.	
V <sub>SS</sub>		GND	

I/O Circuit Format for Pins

Pin	Circuit format	When reset
<p>PA0/AN0 to PA7/AN7</p> <p>8 pins</p>	<p>Port A</p>  <p>Pull-up resistor "0" when reset</p> <p>Port A data</p> <p>Port A direction "0" when reset</p> <p>Data bus</p> <p>RD (Port A)</p> <p>Port A input selection "0" when reset</p> <p>Input multiplexer</p> <p>A/D converter</p> <p>* Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>
<p>PB0/<math>\overline{\text{CS1}}</math> PB1/<math>\overline{\text{CS0}}</math> PB3/<math>\overline{\text{SI0}}</math> PB6/<math>\overline{\text{SI1}}</math></p> <p>4 pins</p>	<p>Port B</p>  <p>Pull-up resistor "0" when reset</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus</p> <p>RD (Port B)</p> <p>Schmitt input</p> <p><math>\overline{\text{CS0}}</math> <math>\overline{\text{CS1}}</math> <math>\overline{\text{SI0}}</math> <math>\overline{\text{SI1}}</math></p> <p>* Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>
<p>PB2/<math>\overline{\text{SCK0}}</math> PB5/<math>\overline{\text{SCK1}}</math></p> <p>2 pins</p>	<p>Port B</p>  <p>Pull-up resistor "0" when reset</p> <p>SCK OUT</p> <p>Output enable</p> <p>Port B output selection "0" when reset</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus</p> <p>RD (Port B)</p> <p>Schmitt input</p> <p>SCK in</p> <p>* Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PB4/SO0 PB7/SO1</p> <p>2 pins</p>	<p>Port B</p> <p>* Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>
<p>PC0/KR0 to PC7/KR7</p> <p>8 pins</p>	<p>Port C</p> <p>*1 Large current drive of 12mA possible *2 Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>
<p>PE0/<math>\overline{EC}</math>/INT0 PE1/INT1 PE2/INT2 PE3/INT3/<math>\overline{NMI}</math> PE4/RMC</p> <p>5 pins</p>	<p>Port E</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PE5/PWM</p> <p>1 pin</p>	<p>Port E</p>	<p>High level</p>
<p>PE6/TO/ADJ</p> <p>1 pin</p>	<p>Port H</p> <p>* ADJ signals are frequency division outputs for 32kHz oscillation frequency adjustment. ADJ2K provides usage as buzzer output.</p>	<p>High level (High level with 150kΩ resistor when reset)</p>
<p>PF5/S13 to PF7/S15</p> <p>3 pins</p>	<p>Port F</p> <p>* High voltage tolerance transistor</p> <p>* Mask option</p> <p>Pull-down resistor</p> <p>VFD</p>	<p>Hi-Z or Low level (When PD resistor is connected)</p>



## Absolute Maximum Ratings

(V<sub>SS</sub> = 0V)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V <sub>DD</sub>	-0.3 to +7.0	V	
Input voltage	V <sub>IN</sub>	-0.3 to +7.0* <sup>1</sup>	V	
Output voltage	V <sub>OUT</sub>	-0.3 to +7.0* <sup>1</sup>	V	
Display output voltage	V <sub>OD</sub>	V <sub>DD</sub> - 40 to V <sub>DD</sub> + 0.3	V	As P channel transistor is open drain, V <sub>DD</sub> voltage is determined as standard.
High level output current	I <sub>OH</sub>	-5	mA	Other than display output pins* <sup>2</sup> : per pin
	I <sub>ODH1</sub>	-15	mA	Display output S13 to S20: per pin
	I <sub>ODH2</sub>	-35	mA	Display output T0 to T7, T8/S28 to T15/S21: per pin
High level total output current	∑I <sub>OH</sub>	-40	mA	Total of pins other than display output pins
	∑I <sub>ODH</sub>	-100	mA	Total of display output pins
Low level output current	I <sub>OL</sub>	15	mA	Port 1 pin
	I <sub>OLC</sub>	20	mA	Large current port* <sup>3</sup> : per pin
Low level total output current	∑I <sub>OL</sub>	100	mA	Entire pin total
Operating temperature	T <sub>opr</sub>	-20 to +75	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	
Allowable power dissipation	P <sub>D</sub>	1000	mW	

\*<sup>1</sup> V<sub>IN</sub> and V<sub>OUT</sub> must not exceed V<sub>DD</sub> + 0.3V.

\*<sup>2</sup> Specifies output current of general-purpose I/O ports.

\*<sup>3</sup> The large current drive transistor is an N-ch transistor of Port C (PC).

**Note)** If the absolute maximum ratings are exceeded, the LSI could reach permanent breakdown. Also, observing recommended operating conditions is desirable; otherwise, the LSI's reliability could be affected.

## Recommended Operating Conditions

(V<sub>SS</sub> = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V <sub>DD</sub>	4.5	5.5	V	High speed mode (1/2, 1/4 dividing clock) guaranteed operation range
		3.5	5.5	V	Low speed mode (1/16 dividing clock) guaranteed operation range
		2.7	5.5	V	Guaranteed operation range with TEX clock
		2.5	5.5	V	Guaranteed data hold operation range during stop
High level input voltage	V <sub>IH</sub>	0.7V <sub>DD</sub>	V <sub>DD</sub>	V	*1
	V <sub>IHS</sub>	0.8V <sub>DD</sub>	V <sub>DD</sub>	V	Hysteresis input*2
	V <sub>IHEX</sub>	V <sub>DD</sub> - 0.4	V <sub>DD</sub> + 0.3	V	EXTAL pin*3
Low level input voltage	V <sub>IL</sub>	0	0.3V <sub>DD</sub>	V	*1
	V <sub>ILS</sub>	0	0.2V <sub>DD</sub>	V	Hysteresis input*2
	V <sub>ILEX</sub>	-0.3	0.4	V	EXTAL pin*3
Operating temperature	Topr	-20	+75	°C	

\*1 All regular input port (PA, PB4, PB7, PC, PH).

\*2 For pins  $\overline{\text{RST}}$ ,  $\overline{\text{CS0}}$ ,  $\overline{\text{CS1}}$ ,  $\overline{\text{SCK0}}$ ,  $\overline{\text{SI0}}$ ,  $\overline{\text{SI1}}$ ,  $\overline{\text{SCK1}}$ ,  $\overline{\text{EC/INT0}}$ , INT1, INT2, INT3/ $\overline{\text{NMI}}$ , RMC.

\*3 Specifies only for external clock input.

**Electrical Characteristics**

**DC Characteristics**

(Ta = -20 to +75°C, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit	
High level output voltage	VOH	PA, PB, PC, PE5, PE6	VDD = 4.5V, IOH = -0.5mA	4.0			V	
			VDD = 4.5V, IOH = -1.2mA	3.5			V	
Low level output voltage	VOL		VDD = 4.5V, IOL = 1.8mA			0.4	V	
			VDD = 4.5V, IOL = 3.6mA			0.6	V	
		PC	VDD = 4.5V, IOL = 12.0mA			1.5	V	
		Input current	EXTAL	IiHE	VDD = 5.5V, VIH = 5.5V	0.5		40
IiLE	VDD = 5.5V, VIL = 0.4V			-0.5		-40	μA	
		TEX	IiHT	VDD = 5.5V, VIL = 5.5V	0.1		10	μA
			IiLT	VDD = 5.5V, VIL = 0.4V	-0.1		-10	μA
		RST*1	IiLR	VDD = 5.5V, VIL = 0.4V	-1.5		-400	μA
			PA to PC*2	IiH	VDD = 4.5V, VIH = 4.0V	3.3		
IiL	VDD = 5.5V, VIL = 0.4V				50	μA		
Display output current	IOH	S13 to S20		-8			mA	
		S21/T15 to S28/T8 T0 to T7	VDD = 4.5V VOH = VDD - 2.5V	-20			mA	
Open drain output leak current (P-CH Tr off state)	ILOL	S13 to S20 S21/T15 to S28/T8 T0 to T7	VDD = 5.5V VOL = VDD - 35V VFDP = VDD - 35V			-20	μA	
Pull-down resistor*3	RL	S13 to S20 S21/T15 to S28/T8 T0 to T7	VDD = 5V VFDP = VDD - 35V	60	100	270	kΩ	
Input/Output leak current	IIZ	PA to PC*2, PE0 to PE4 RST*2	VDD = 5.5V VI = 0, 5.5V			±10	μA	
Supply current*4	IDD1	VDD	High-speed mode operation (1/2 frequency dividing clock)		20	40	mA	
			VDD = 5.5V, 10MHz crystal oscillation (C1 = C2 = 15pF)					
	IDD2		VDD = 3V, 32kHz crystal oscillation (C1 = C2 = 47pF)		35	100	μA	
	IDDS1		Sleep mode		1.2	8	mA	
			VDD = 5.5V, 10MHz crystal oscillation (C1 = C2 = 15pF)					
IDDS2	VDD = 3V, 32kHz crystal oscillation (C1 = C2 = 47pF)		9	30	μA			
IDDS3	Stop mode VDD = 5.5V, 10MHz termination of 10MHz and 32kHz crystal oscillation.				10	μA		

Item	Symbol	Pin	Codition	Min.	Typ.	Max.	Unit
Input capacitance	C <sub>IN</sub>	Pins other than S13 to S28, T0 to T7, PE5, PE6, V <sub>DD</sub> , V <sub>SS</sub> , V <sub>FDP</sub>	1MHz clock 0V for pins other than the measured pins		10	20	pF

\*1  $\overline{\text{RST}}$  specifies the input current when pull-up resistor has been selected; leakage current when no resistor has been selected.

\*2 Pins PA to PC specify the input current when pull-up resistor has been selected; leakage current when no resistor has been selected.

\*3 Applies when the on-chip pull-down resistor is selected under the mask option.

\*4 All output pins are left open.

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	1		10	MHz
System clock input pulse width	t <sub>XL</sub> , t <sub>XH</sub>	EXTAL	Fig. 1, Fig. 2 External clock drive	37.5			ns
System clock input rise and fall time	t <sub>CR</sub> , t <sub>CF</sub>	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	t <sub>EH</sub> , t <sub>EL</sub>	$\overline{EC}$	Fig. 3	t <sub>sys</sub> + 50*			ns
Event count input clock rise and fall time	t <sub>ER</sub> , t <sub>EF</sub>	$\overline{EC}$	Fig. 3			20	ms
System clock frequency	fc	TEX TX	V <sub>DD</sub> = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count input clock input pulse width	t <sub>TL</sub> , t <sub>TH</sub>	TEX	Fig. 3	10			μs
Event count input clock rise and fall time	t <sub>TR</sub> , t <sub>TF</sub>	TEX	Fig. 3			20	ms

\* t<sub>sys</sub> indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: 00FEH).

t<sub>sys</sub> [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

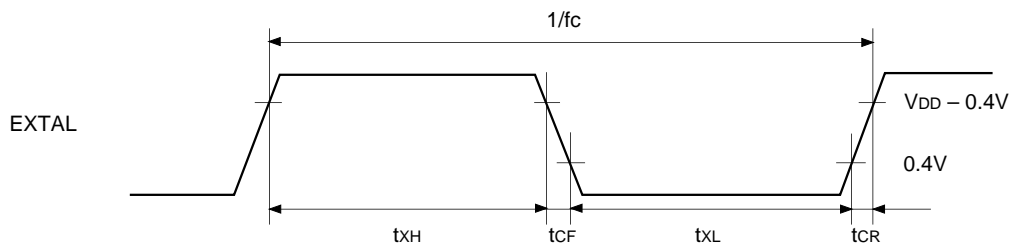


Fig. 1. Clock timing

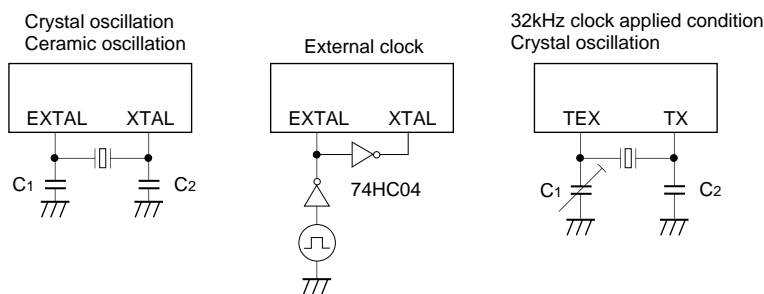


Fig. 2. Clock applied conditions

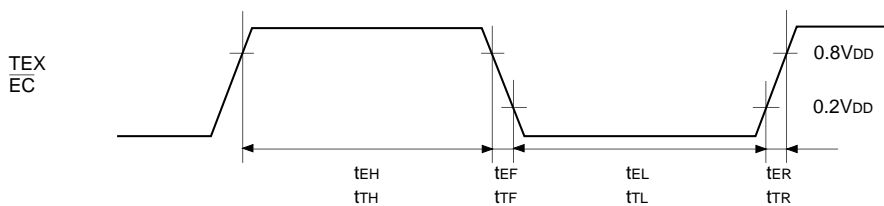


Fig. 3. Event count clock timing

(2) Serial transfer

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ ( $\overline{CS1} \downarrow \rightarrow \overline{SCK1}$ ) delay time	$t_{DCSK}$	$\overline{SCK0}$ ( $\overline{SCK1}$ )	Chip select transfer mode ( $\overline{SCK0}$ ( $\overline{SCK1}$ ) = output mode)		$1.5t_{sys} + 200$	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ ( $\overline{CS1} \uparrow \rightarrow \overline{SCK1}$ ) float delay time	$t_{DCSKF}$	$\overline{SCK0}$ ( $\overline{SCK1}$ )	Chip select transfer mode ( $\overline{SCK0}$ ( $\overline{SCK1}$ ) = output mode)		$1.5t_{sys} + 200$	ns
$\overline{CS0} \downarrow \rightarrow SO0$ ( $\overline{CS1} \downarrow \rightarrow SO1$ ) delay time	$t_{DCSO}$	SO0 (SO1)	Chip select transfer mode		$1.5t_{sys} + 200$	ns
$\overline{CS0} \uparrow \rightarrow SO0$ ( $\overline{CS1} \uparrow \rightarrow SO1$ ) float delay time	$t_{DCSOF}$	SO0 (SO1)	Chip select transfer mode		$1.5t_{sys} + 200$	ns
$\overline{CS0}$ ( $\overline{CS1}$ ) high level width	$t_{WHCS}$	$\overline{CS0}$ ( $\overline{CS1}$ )	Chip select transfer mode	$t_{sys} + 200$		ns
$\overline{SCK0}$ ( $\overline{SCK1}$ ) cycle time	$t_{KCY}$	$\overline{SCK0}$ ( $\overline{SCK1}$ )	Input mode	$2t_{sys} + 200$		ns
			Output mode	$16000/fc$		ns
$\overline{SCK0}$ ( $\overline{SCK1}$ ) high and low level widths	$t_{KH}$ $t_{KL}$	$\overline{SCK0}$ ( $\overline{SCK1}$ )	Input mode	$t_{sys} + 100$		ns
			Output mode	$8000/fc - 50$		ns
SI0 (SI1) input setup time (for $\overline{SCK0} \uparrow$ ( $\overline{SCK1} \uparrow$ ))	$t_{SIK}$	SI0 (SI1)	$\overline{SCK0}$ ( $\overline{SCK1}$ ) input mode	100		ns
			$\overline{SCK0}$ ( $\overline{SCK1}$ ) output mode	200		ns
SI0 (SI1) input hold time (for $\overline{SCK0} \uparrow$ ( $\overline{SCK1} \uparrow$ ))	$t_{KSI}$	SI0 (SI1)	$\overline{SCK0}$ ( $\overline{SCK1}$ ) input mode	$t_{sys} + 200$		ns
			$\overline{SCK0}$ ( $\overline{SCK1}$ ) output mode	100		ns
$\overline{SCK0} \downarrow \rightarrow SO0$ ( $\overline{SCK1} \downarrow \rightarrow SO1$ ) delay time	$t_{KSO}$	SO0 (SO1)	$\overline{SCK0}$ ( $\overline{SCK1}$ ) input mode		$t_{sys} + 200$	ns
			$\overline{SCK0}$ ( $\overline{SCK1}$ ) output mode		100	ns

**Note 1)**  $t_{sys}$  indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: 00FEH).

$t_{sys}$  [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

**Note 2)** The load condition for the  $\overline{SCK0}$  ( $\overline{SCK1}$ ) output mode, SO0 (SO1) output delay time is 50pF + 1TTL.

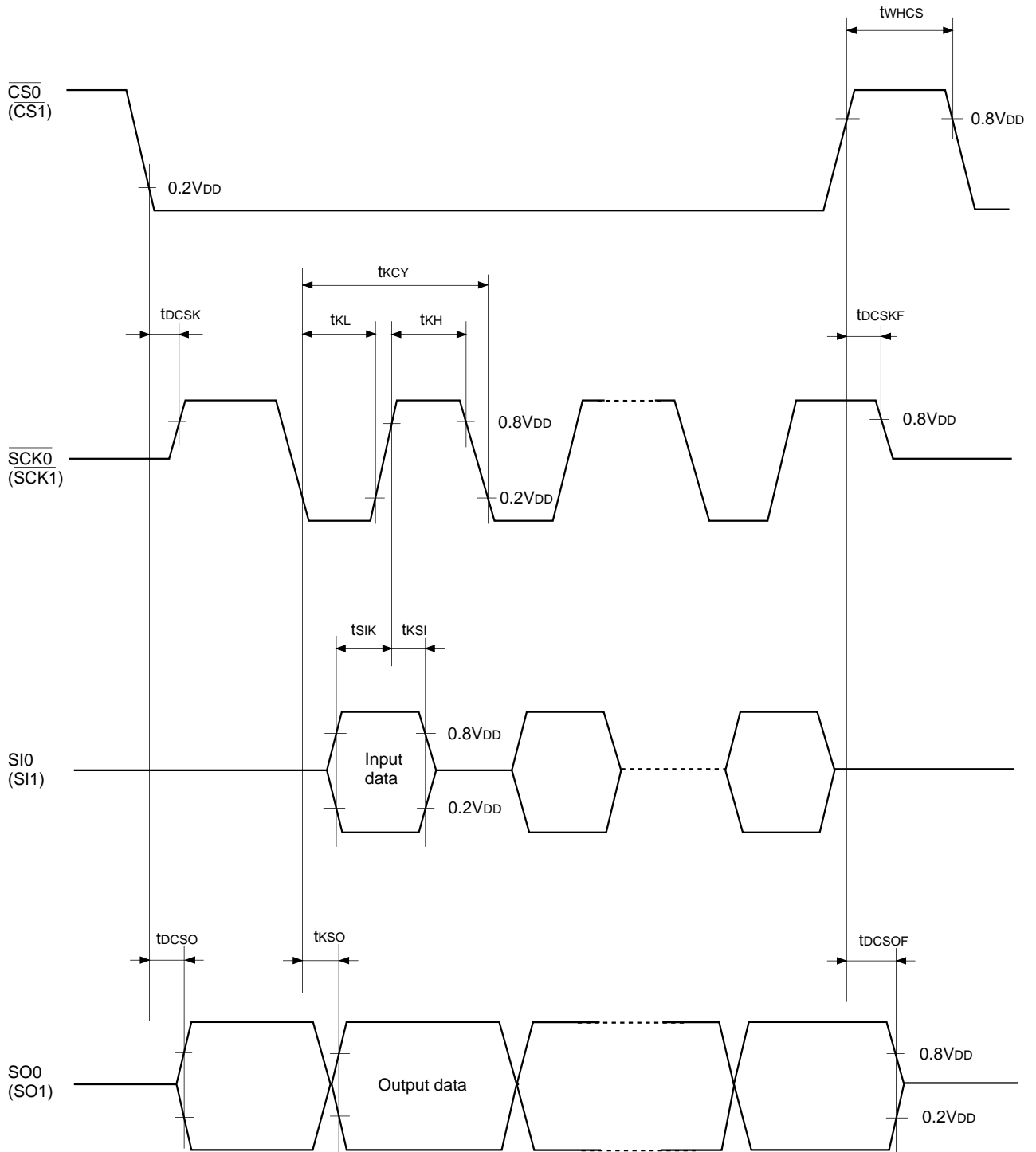
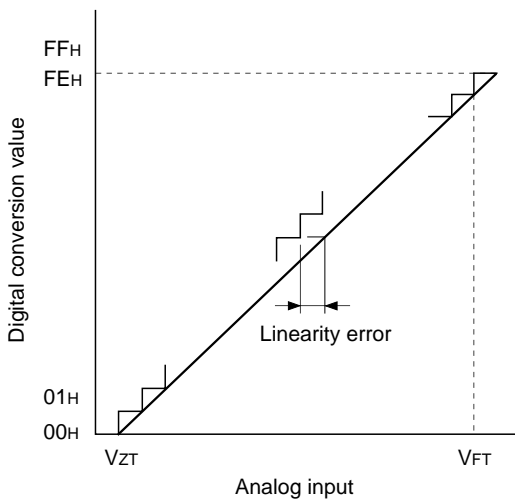


Fig. 4. Serial transfer timing

**(3) A/D converter characteristics** ( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $AV_{REF} = 4.0$  to  $AV_{DD}$ ,  $V_{SS} = AV_{SS} = 0\text{V}$ )

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			$T_a = 25^\circ\text{C}$ $V_{DD} = 5.0\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$			$\pm 3$	LSB
Zero transition voltage	$V_{ZT}^{*1}$			-10	70	150	mV
Full-scale transition voltage	$V_{FT}^{*2}$			4930	5050	5120	mV
Conversion time	$t_{CONV}$			$160/f_{ADC}^{*3}$			$\mu\text{s}$
Sampling time	$t_{SAMP}$			$12/f_{ADC}^{*3}$			$\mu\text{s}$
Analog input voltage	$V_{IAN}$	AN0 to AN7		0		$V_{DD}$	V



- \*1  $V_{ZT}$ : Value at which the digital conversion value changes from 00H to 01H and vice versa.
- \*2  $V_{FT}$ : Value at which the digital conversion value changes from FEH to FFH and vice versa.
- \*3  $f_{ADC}$  indicates the below values due to the Bit6 (CKS) of A/D control register (address: 00F9H) and the Bit7 (PCK1) and Bit6 (PCK0) of clock control register (address: 00FEH)

**Fig. 5. Definition of A/D converter terms**

PCK1, 0	CSK	
	0 ( $\phi/2$ selection)	1 ( $\phi$ selection)
00 ( $\phi = f_{EX}/2$ )	$f_{ADC} = f_c/2$	$f_{ADC} = f_c$
01 ( $\phi = f_{EX}/4$ )	$f_{ADC} = f_c/4$	$f_{ADC} = f_c/2$
11 ( $\phi = f_{EX}/16$ )	$f_{ADC} = f_c/16$	$f_{ADC} = f_c/8$

(4) Interruption, reset input

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	$t_{IH}$ $t_{IL}$	INT0 INT1 INT2 INT3 $\overline{\text{NMI}}$		1		$\mu\text{s}$
Reset input low level width	$t_{RSL}$	$\overline{\text{RST}}$		$32/f_c$		$\mu\text{s}$

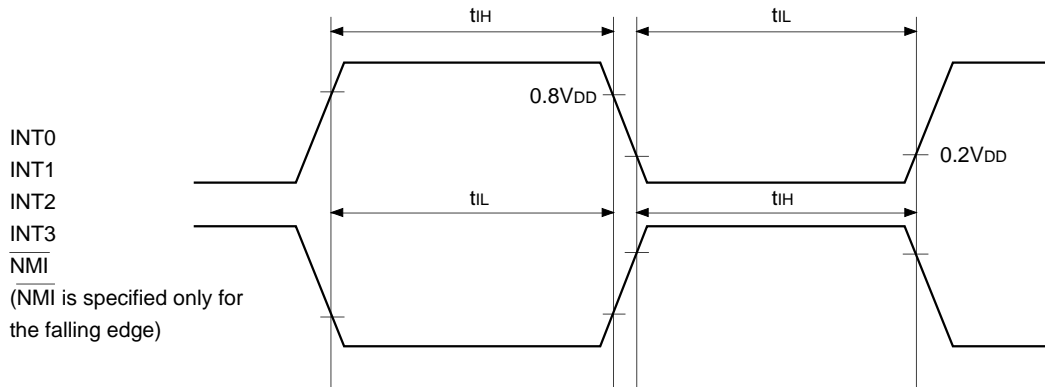


Fig 6. Interruption input timing

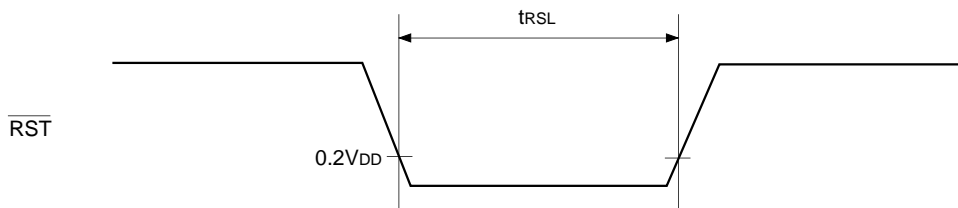


Fig. 7.  $\overline{\text{RST}}$  input timing

Appendix

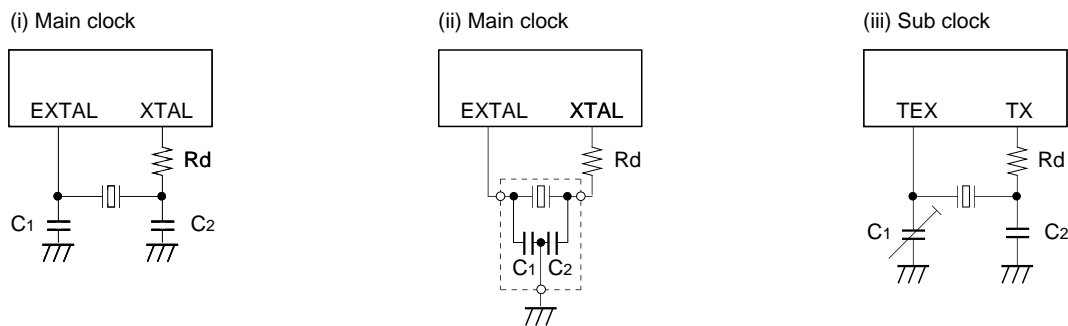


Fig. 8. Recommended oscillation circuit

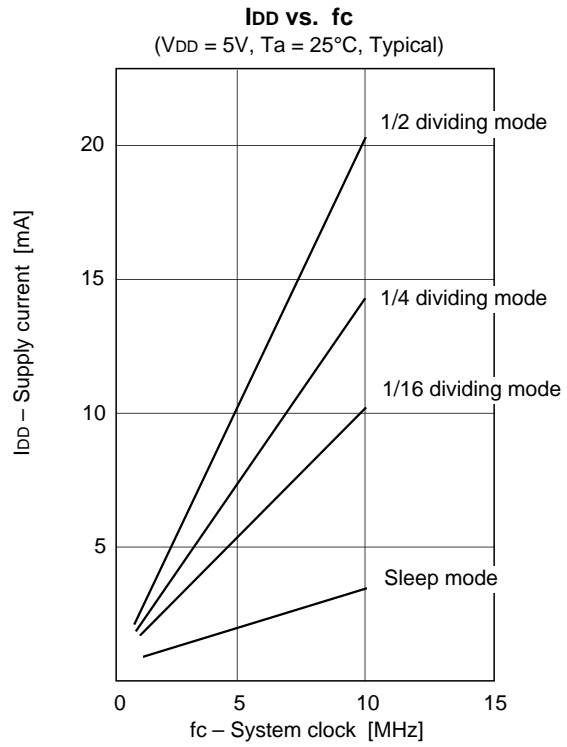
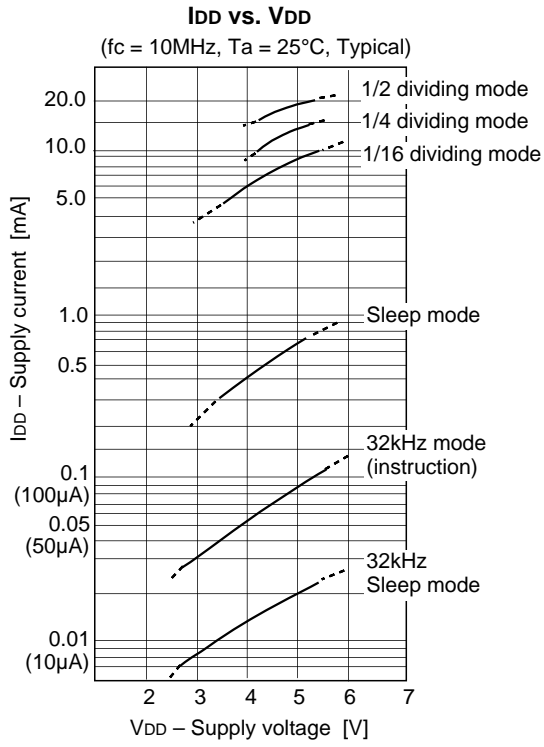
Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd ( $\Omega$ )	Circuit example
MURATA MFG CO., LTD.	CSA4.19MG	4.19	30	30	0	(i)
	CSA8.00MTZ	8.00				
	CSA10.0MTZ	10.00				
	CST4.19MGW*	4.19				(ii)
	CST8.00MTW*	8.00				
	CST10.0MTW*	10.00				
RIVER ELETEC CORPORATION	HC-49/U03	4.19	12	12	0	(i)
		8.00				
		10.00				
KINSEKI LTD.	HC-49/U (-S)	4.19	27	27	0	
		8.00				
		10.00				
	P3	32.768kHz	50	22	1M	(iii)

Those marked with an asterisk (\*) signify types with built-in ground capacitance (C1, C2).

Mask Option Table

Item	Content	
Reset pin pull-up resistor	Non-existent	Existent
High tension proof pull-down resistor	Non-existent	Existent (selected every pin)

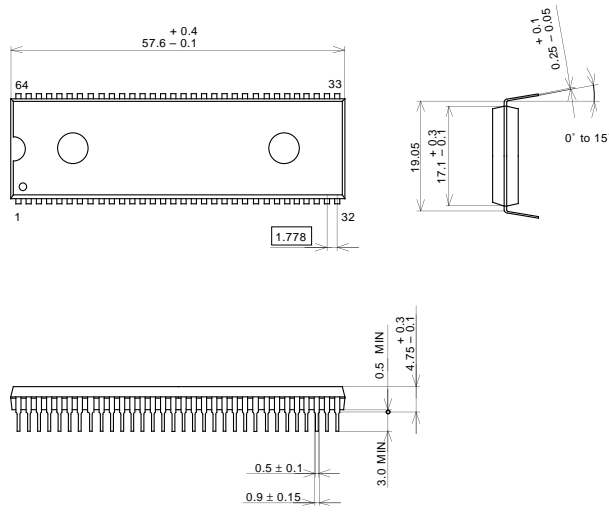
Characteristics Curves



Package Outline

Unit: mm

64PIN SDIP (PLASTIC)

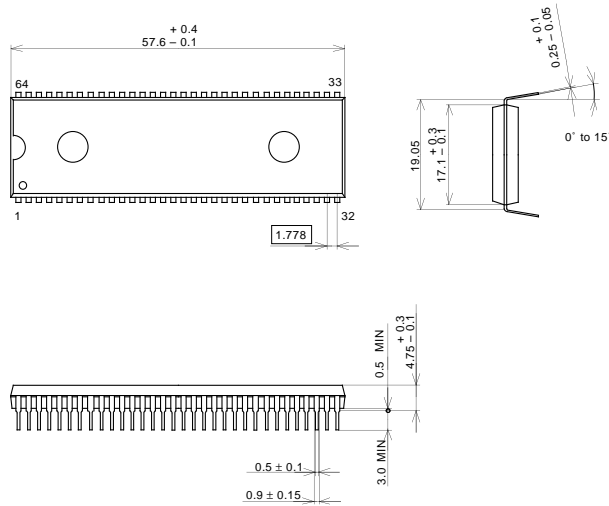


SONY CODE	SDIP-64P-01
EIAJ CODE	P-SDIP64-17.1x57.6-1.778
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	8.6g

64PIN SDIP (PLASTIC)



SONY CODE	SDIP-64P-01
EIAJ CODE	P-SDIP64-17.1x57.6-1.778
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	8.6g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18µm



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