

CMOS 8-bit Single Chip Microcomputer

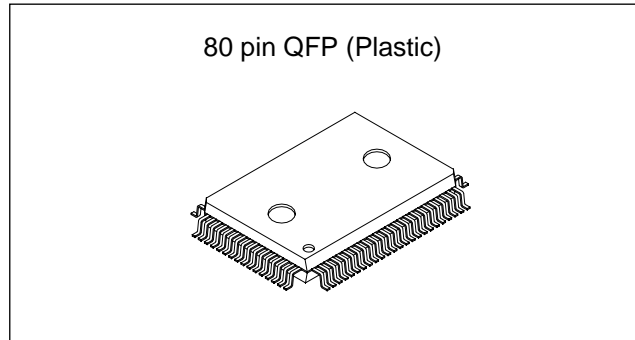
Description

The CXP825P40 is a highly integrated CMOS 8-bit single chip microcomputer which is mainly composed of an 8-bit CPU, PROM, RAM, and I/O ports. This microcomputer features many other high-performance circuits in a single chip CMOS design, including an A/D converter, serial interface, timer/counter, time-base timer, capture timer/counter, fluorescent display tube controller/driver, remote control receiver. Also, the CXP825P40 provides the power-on reset function as well as the sleep/stop function which assures reduced power consumption.

Being a PROM-incorporated version of the CXP82540 which has on-chip mask ROM, the CXP825P40 permits program writing. Therefore, it is ideally suited for use in system development stage evaluation and job lot production.

Features

- Instruction set which supports a wide array of data types 213 types
 - 16-bit arithmetic instruction/multiplication and division instructions/boolean bit operation instruction
- Minimum instruction cycle During operation 400ns/10MHz
- Incorporated PROM capacity 40K bytes
- Incorporated RAM capacity 1120 bytes (Including the fluorescent display data area)
- Peripheral functions
 - A/D converter 8-bit, 8-channel, successive comparison type (conversion time: 32 μ s at 10MHz)
 - Serial interface 1-channel data interface with an 8-bit, 8-stage FIFO (1 to 8 bytes automatic transfer)
 - Timers 1 channel, 8-bit clock synchronized interface
 - 8-bit timer
 - 8-bit timer/counter
 - 19-bit time-base timer
 - 16-bit capture timer/counter
 - Fluorescent display tube controller/driver
 - Display of up to 336 segments
 - 1 to 16 digits dynamic display
 - Dimmer function
 - High voltage tolerance output (40V)
 - Built-in pull-down resistor
 - Remote control receiver
 - Built-in noise suppressor circuit
 - Built-in 8-bit pulse counter and 6-stage FIFO
- Interrupts 14 factors, 15 vectors, multiple interrupt processing
- Standby mode Sleep/stop
- Package 80-pin plastic QFP

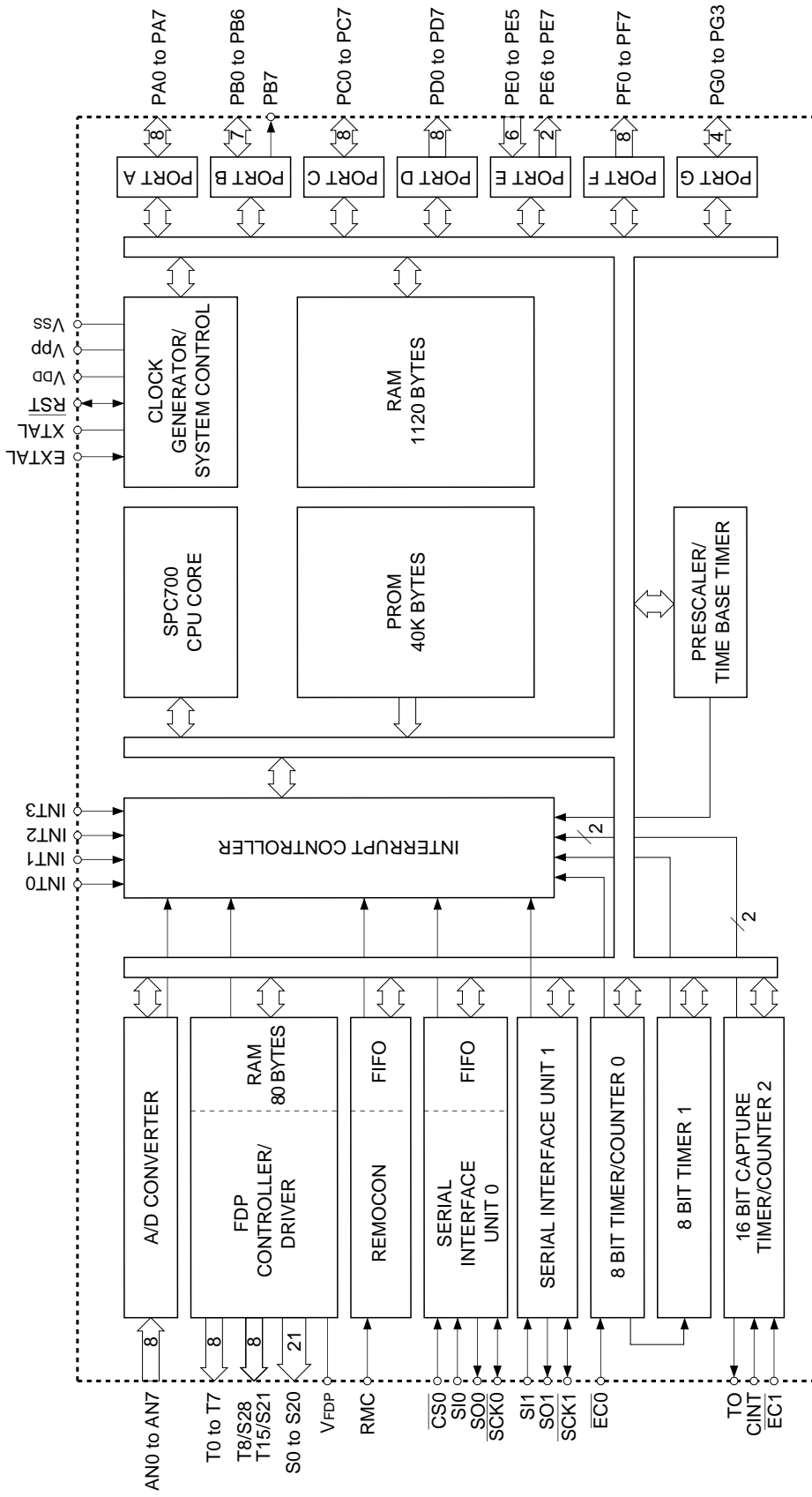


Structure

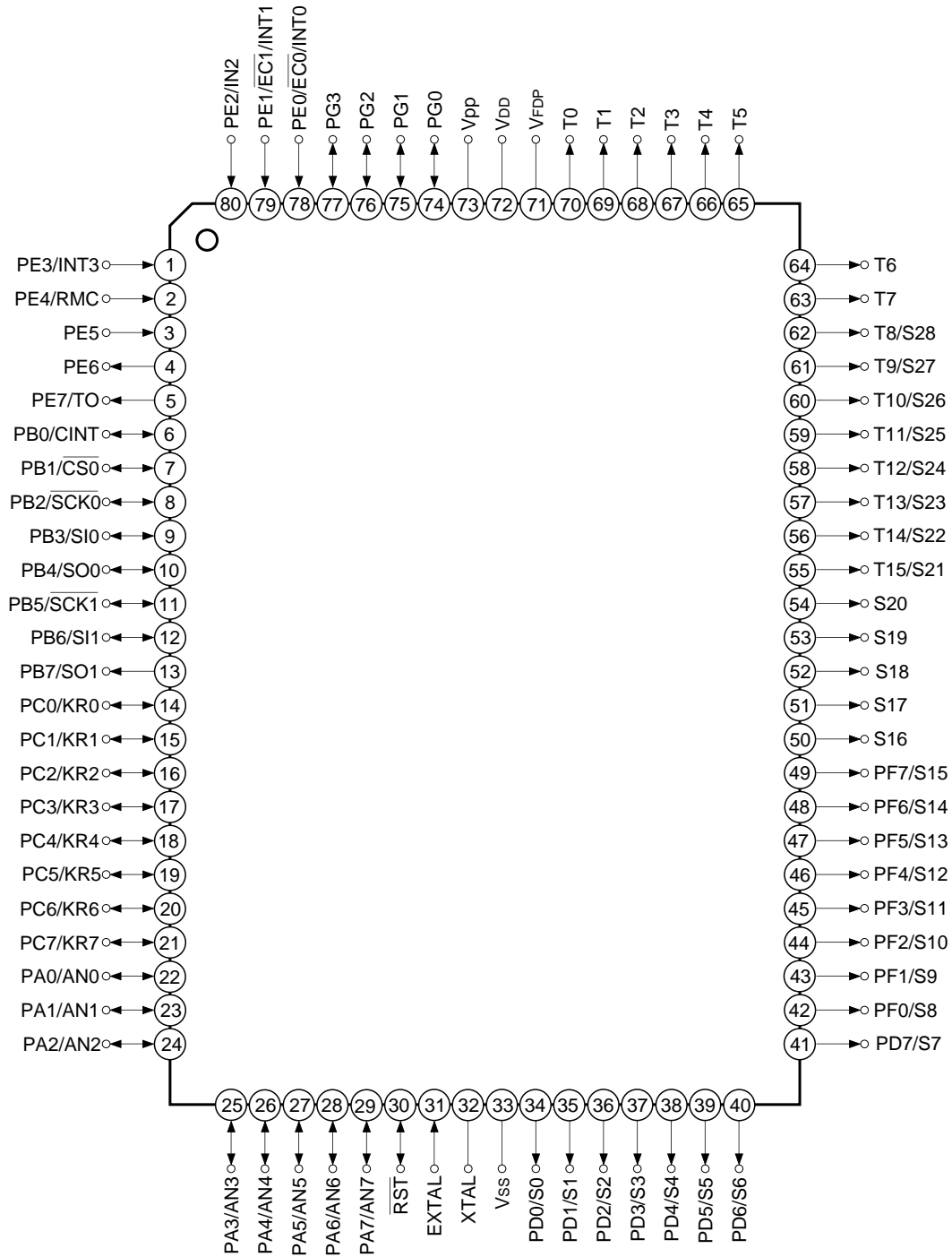
Silicon gate CMOS IC

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Block Diagram



Pin Assignment (Top View)



Note) Vpp (Pin 73) is always connected to VDD.

Pin Description

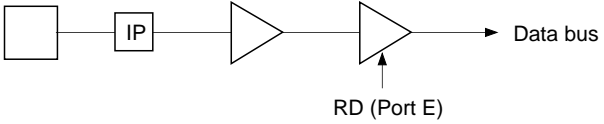
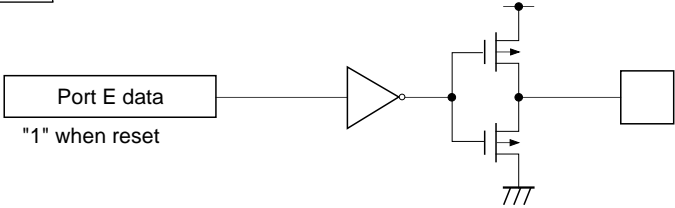
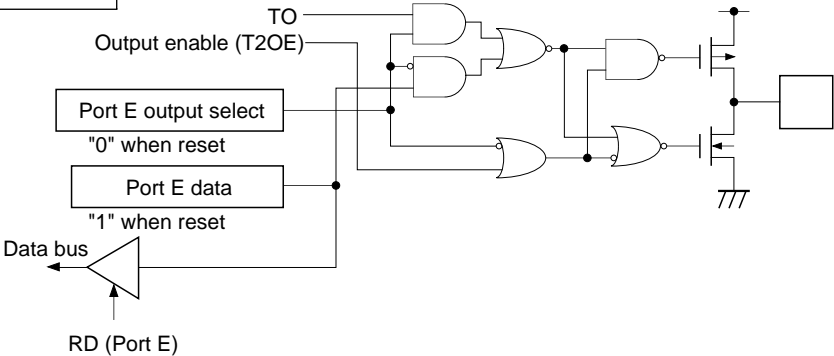
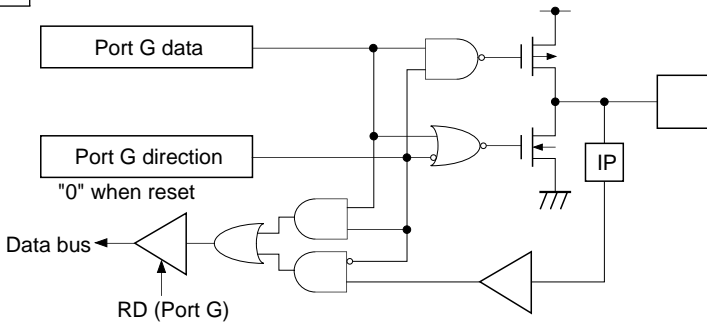
Symbol	I/O	Description	
PA0/AN0 to PA7/AN7	I/O/Analog input	(Port A) 8-bit I/O port; single bit addressable. (8 pins)	Analog input to A/D converter. (8 pins)
PB0/CINT	I/O/Input	(Port B) Single bit addressable from amongst lower 7 bits; highest bit (PB7) dedicated to output. (8 pins)	External capture input for 16-bit timer/counter.
PB1/ $\overline{\text{CS0}}$	I/O/Input		Chip select input for serial interface (CH0).
PB2/ $\overline{\text{SCK0}}$	I/O/I/O		Serial clock (CH0) I/O.
PB3/SI0	I/O/Input		Serial data (CH0) input.
PB4/SO0	I/O/Output		Serial data (CH0) output.
PB5/ $\overline{\text{SCK1}}$	I/O/I/O		Serial clock (CH1) I/O.
PB6/SI1	I/O/Input		Serial data (CH1) input.
PB7/SO1	Output/Output		Serial data (CH1) output.
PC0/KR0 to PC7/KR7	I/O/Input	(Port C) 8-bit I/O port; single bit addressable. Can provide 12mA sink current. (8 pins)	Key return input for FDP segment signal which performs key scanning.
PE0/INT0/ $\overline{\text{EC0}}$	Input/Input/Input	(Port E) 8-bit port with lower 6 bits dedicated to input and upper 2 bits dedicated to output. (8 pins)	Input for external interrupt requests. (4 pins)
PE1/INT1/ $\overline{\text{EC1}}$	Input/Input/Input		
PE2/INT2	Input/Input		Input for remote control receiver circuit.
PE3/INT3	Input/Input		
PE4/RMC	Input/Input		
PE5	Input		
PE6	Output		Output pin for 16-bit timer/counter rectangular waveform.
PE7/TO	Output/Output		
PG0 to PG3	I/O	(Port G) 4-bit I/O port; single bit addressable. (4 pins)	
PF0/S8 to PF7/S15	Output/Output	(Port F) 8-bit dedicated output port. (8 pins)	Segment signal output for FDP.
S16 to S20	Output	Segment signal output for FDP.	
T8/S28 to T15/S21	Output/Output	Dual purpose output for FDP timing and segment signals.	
T0 to T7	Output	Timing signal output for FDP.	
PD0/S0 to PD7/S7	Output/Output	(Port D) 8-bit dedicated output port. (8 pins)	Segment signal output for FDP.

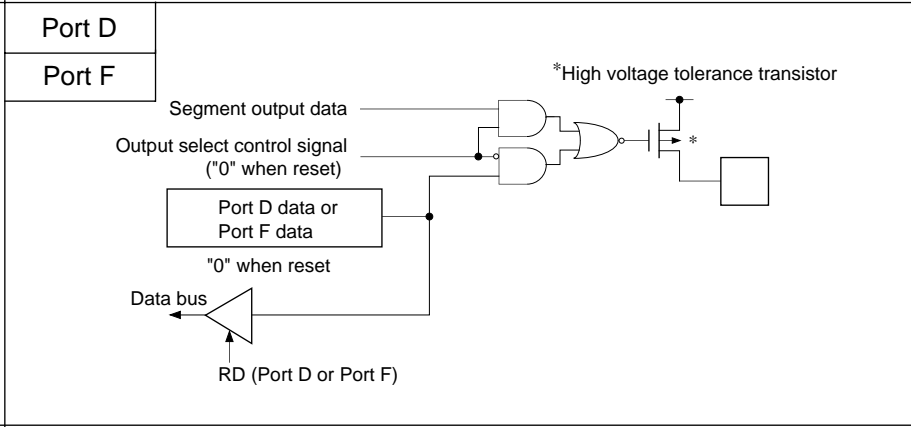
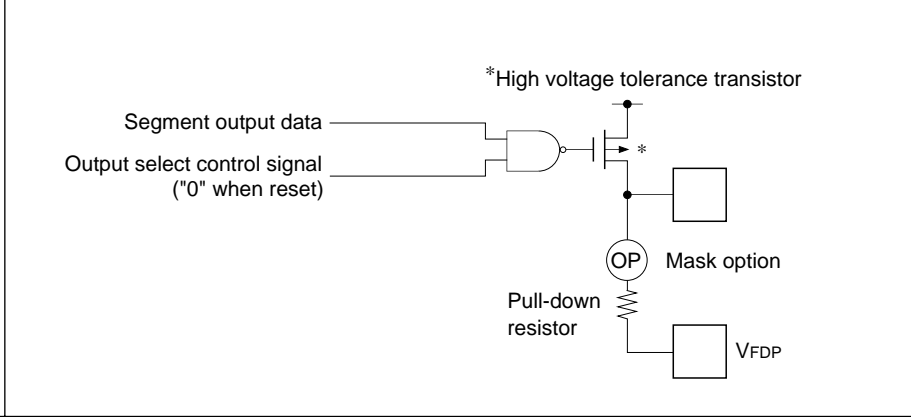
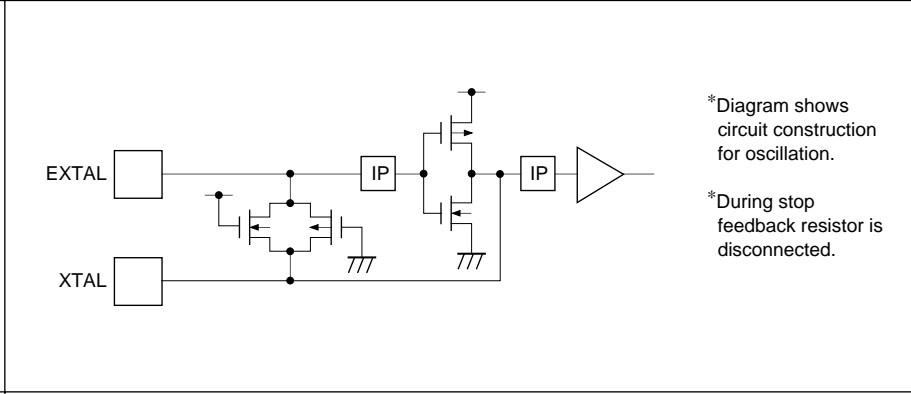
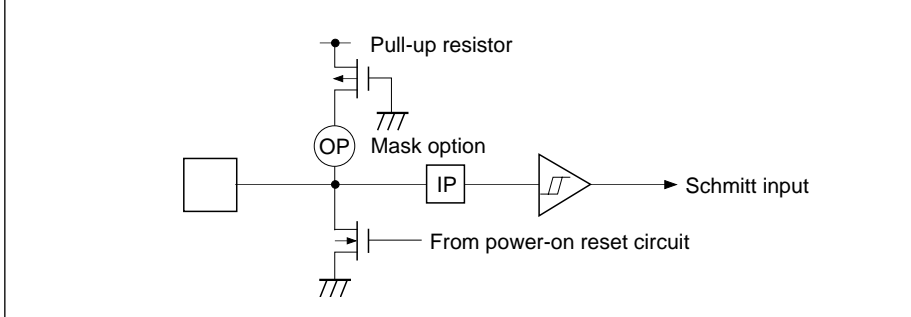
Symbol	I/O	Description
V _{FDP}		Provides voltage for FDP.
EXTAL	Input	Connection for system clock oscillation crystal. When using an external clock, input normal signal to the EXTAL pin and reverse phase signal to the XTAL pin.
XTAL	Output	
$\overline{\text{RST}}$	I/O	System reset, active "L". The $\overline{\text{RST}}$ pin is an input/output pin which outputs a "L" level when the power is turned on and the on-chip power-on reset circuit.
V _{pp}		Positive power supply for the programmable on-chip PROM; connect to V _{DD} for normal operation.
V _{DD}		Positive power supply pin.
V _{SS}		GND

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
<p>PA0/AN0 to PA7/AN7</p> <p>8 pins</p>	<p>Port A</p> <p>Port A data</p> <p>Port A direction "0" when reset</p> <p>Data bus</p> <p>RD (Port A)</p> <p>Port A input select "0" when reset</p> <p>Input multiplexer</p> <p>A/D converter</p> <p>IP</p> <p>Input protection circuit</p>	<p>Hi-Z</p>
<p>PB0/CINT PB1/CS0 PB3/SI0 PB6/SI1</p> <p>4 pins</p>	<p>Port B</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus</p> <p>RD (Port B)</p> <p>Schmitt input</p> <p>CINT CS0 SI0 SI1</p> <p>IP</p> <p>Input protection circuit</p>	<p>Hi-Z</p>
<p>PB2/SCK0 PB5/SCK1</p> <p>2 pins</p>	<p>Port B</p> <p>SCK OUT Output enable</p> <p>Port B output select "0" when reset</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus</p> <p>RD (Port B)</p> <p>Schmitt input</p> <p>SCK in</p> <p>IP</p> <p>Input protection circuit</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PB4/SO0</p> <p>1 pin</p>	<p>Port B</p>	<p>Hi-Z</p>
<p>PB7/SO1</p> <p>1 pin</p>	<p>Port B</p>	<p>High level</p>
<p>PC0/KR0 to PC7/KR7</p> <p>8 pins</p>	<p>Port C</p>	<p>Hi-Z</p>
<p>PE0/EC0/INT0 PE1/EC1/INT1 PE2/INT2 PE3/INT3 PE4/RMC</p> <p>5 pins</p>	<p>Port E</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PE5</p> <p>1 pin</p>	<p>Port E</p> 	<p>Hi-Z</p>
<p>PE6</p> <p>1 pin</p>	<p>Port E</p> 	<p>High level</p>
<p>PE7/TO</p> <p>1 pin</p>	<p>Port E</p> 	<p>High level</p>
<p>PG0 to PG3</p> <p>4 pins</p>	<p>Port G</p> 	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PD0/S0 to PD7/S7</p> <p>PF0/S8 to PF7/S15</p> <p>16 pins</p>		<p>Hi-Z</p>
<p>S16 to S20</p> <p>T15/S21 to T8/S28</p> <p>T0 to T7</p> <p>21 pins</p>		<p>Low level</p>
<p>EXTAL</p> <p>XTAL</p> <p>2 pins</p>	 <p>*Diagram shows circuit construction for oscillation.</p> <p>*During stop feedback resistor is disconnected.</p>	<p>Oscillation</p>
<p>$\overline{\text{RST}}$</p> <p>1 pin</p>		<p>Low level</p>

Absolute Maximum Ratings

(V_{SS} = 0V)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	-0.3 to +7.0	V	
Input voltage	V _{IN}	-0.3 to +7.0* ¹	V	
Output voltage	V _{OUT}	-0.3 to +7.0* ¹	V	
Display output voltage	V _{OD}	V _{DD} - 40 to V _{DD} + 0.3	V	As P channel transistor is open drain, V _{DD} voltage is determined as standard.
High level output current	I _{OH}	-5	mA	Other than display output pins* ² : per pin
	I _{ODH1}	-15	mA	Display outputs S0 to S20: per pin
	I _{ODH2}	-35	mA	Display outputs T0 to T7, T8/S28 to T15/S21: per pin
High level total output current	∑I _{OH}	-40	mA	Total of pins other than display output pins
	∑I _{ODH}	-100	mA	Total of display output pins
Low level output current	I _{OL}	15	mA	Port 1 pin
	I _{OLC}	20	mA	Large current port pin * ³ : per pin
Low level total output current	∑I _{OL}	100	mA	Entire pin total
Operating temperature	T _{opr}	-10 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	600	mW	

*¹ V_{IN} and V_{OUT} cannot exceed V_{DD} + 0.3V.

*² Rating for output current of general input/output port.

*³ The large current drive transistor is an N-channel transistor of Port C.

Note) If the absolute maximum ratings are exceeded, the LSI could reach permanent breakdown. Also, observing recommended operating conditions is desirable; otherwise, the LSI's reliability could be affected.

Recommended Operating Conditions

(V_{SS} = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	4.5	5.5	V	High-speed mode (1/2, 1/4 clock) guaranteed operation range
		3.5	5.5		Low-speed mode(1/16clock) guaranteed operation range
		2.5	5.5		Guaranteed data hold operation range during stop
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*1
	V _{IHS}	0.8V _{DD}	V _{DD}	V	Hysteresis input*2
	V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL pin*3
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	*1
	V _{ILS}	0	0.2V _{DD}	V	Hysteresis input
	V _{ILEX}	-0.3	0.4	V	EXTAL pin*3
Operating temperature	T _{opr}	-10	+75	°C	

*1 All regular input ports (PA, PB3, PB4, PB6, PC, PE5, PG).

*2 For pins $\overline{\text{RST}}$, $\overline{\text{CINT}}$, $\overline{\text{CS0}}$, $\overline{\text{SCK0}}$, $\overline{\text{SCK1}}$, $\overline{\text{EC0/INT0}}$, $\overline{\text{EC1/INT1}}$, INT2, INT3, RMC.

*3 Rating only for external clock input.

Electrical Characteristics

DC Characteristics

(Ta = -10 to +75°C, Vss = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V _{OH}	PA, PB, PC, PE6, PE7, PG, RST (for V _{OL} only)	V _{DD} = 4.5V, I _{OH} = -0.5mA	4.0			V
			V _{DD} = 4.5V, I _{OH} = -1.2mA	3.5			V
Low level output voltage	V _{OL}	PA, PB, PC, PE6, PE7, PG, RST (for V _{OL} only)	V _{DD} = 4.5V, I _{OL} = 1.8mA			0.4	V
			V _{DD} = 4.5V, I _{OL} = 3.6mA			0.6	V
		PC	V _{DD} = 4.5V, I _{OL} = 12.0mA			1.5	V
Input current	I _{IHE}	EXTAL	V _{DD} = 5.5V, V _{IH} = 5.5V	0.5		40	μA
	I _{I LE}		V _{DD} = 5.5V, V _{IL} = 0.4V	-0.5		-40	μA
	I _{I LR}		$\overline{\text{RST}}$	V _{DD} = 5.5V, V _{IL} = 0.4V	-1.5		-400
Display output current	I _{OH}	S0 to S20	V _{DD} = 4.5V	-8			mA
		S21/T15 to S28/T8 T0 to T7	V _{OH} = V _{DD} - 2.5V	-20			mA
Open drain output leak current (P-CH Tr off state)	I _{LOL}	S0 to S20 S21/T15 to S28/T8 T0 to T7	V _{DD} = 5.5V V _{OL} = V _{DD} - 35V V _{FDP} = V _{DD} - 35V			-20	μA
Pull-down resistor	R _L	S0 to S20 S21/T15 to S28/T8 T0 to T7	V _{DD} = 5V V _{OD} - V _{FDP} = 30V	60	100	270	kΩ
Input/output leak current	I _{Iz}	PA to PC, PE, PG	V _{DD} = 5.5V V _I = 0, 5.5V			±10	μA
Supply current*1	I _{DD1}	V _{DD}	V _{DD} = 5.5V High-speed mode (1/2 clock) operation 10MHz crystal oscillator (C ₁ = C ₂ = 15pF)		25	40	mA
	I _{DDSL}		Sleep mode		3	8	mA
	I _{DDST}		Stop mode			30	μA
Input capacitance	C _{IN}	For pins other than S0 to S28, T0 to T7, PB7, PE6, PE7, V _{DD} , V _{SS} , V _{FDP}	1MHz clock 0V for pins other than the measured pins.		10	20	pF

*1 All output pins are left open.

AC Characteristics

(1) Clock timing

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
System clock frequency	f_c	XTAL EXTAL	Fig. 1, Fig. 2	1	10	MHz
System clock input pulse width	t_{XL} , t_{XH}	EXTAL	Fig. 1, Fig. 2 External clock driver	45		ns
System clock input rising and falling times	t_{CR} , t_{CF}	EXTAL	Fig. 1, Fig. 2 External clock driver		200	ns
Event count input clock pulse width	t_{EH} , t_{EL}	$\overline{\text{EC0}}$, EC1	Fig. 3	$t_{\text{sys}} + 50^*$		ns
Event count input clock rising and falling times	t_{ER} , t_{EF}	$\overline{\text{EC0}}$, EC1	Fig. 3		20	ms

* t_{sys} is determined by the upper two bits of the clock control register (Address: 00FEH; CPU clock selected) resulting in one of the 3 following values:

$t_{\text{sys}} [\text{ns}] = 2000/f_c$ (Upper 2 bits = "00"), $4000/f_c$ (Upper 2 bits = "01"), $16000/f_c$ (Upper 2 bits = "11")

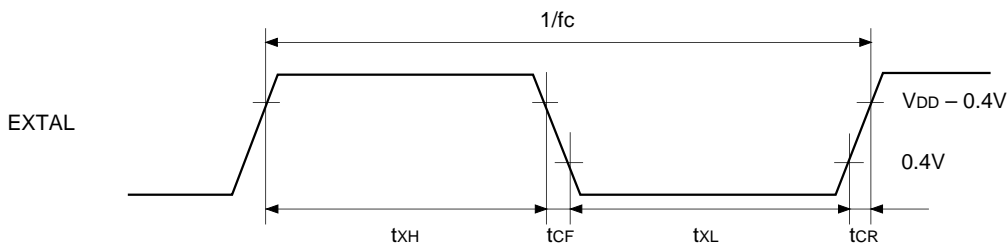


Fig. 1. Clock timing

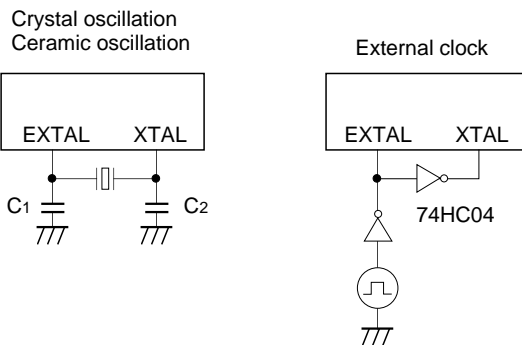


Fig. 2. Clock applying condition

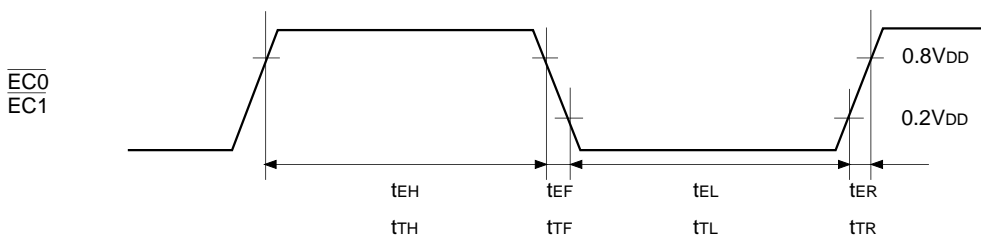


Fig. 3. Event count clock timing

(2) Serial transfer (CH0)

(Ta = -10 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{CS0}} \downarrow \rightarrow \overline{\text{SCK0}}$ delay time	t _{DCSK}	$\overline{\text{SCK0}}$	Chip select transfer mode (SCK0 = output mode)		t _{sys} + 200	ns
$\overline{\text{CS0}} \uparrow \rightarrow \overline{\text{SCK0}}$ float delay time	t _{DCSKF}	$\overline{\text{SCK0}}$	Chip select transfer mode (SCK0 = output mode)		t _{sys} + 200	ns
$\overline{\text{CS0}} \downarrow \rightarrow \text{SO0}$ delay time	t _{DCSO}	SO0	Chip select transfer mode		t _{sys} + 200	ns
$\overline{\text{CS0}} \uparrow \rightarrow \text{SO0}$ float delay time	t _{DCSOF}	SO0	Chip select transfer mode		t _{sys} + 200	ns
$\overline{\text{CS0}}$ high level width	t _{WHCS}	$\overline{\text{CS0}}$	Chip select transfer mode	t _{sys} + 200		ns
$\overline{\text{SCK0}}$ cycle time	t _{KCY}	$\overline{\text{SCK0}}$	Input mode	2t _{sys} + 200		ns
			Output mode	16000/fc		ns
$\overline{\text{SCK0}}$ high and low level width	t _{KH} t _{KL}	$\overline{\text{SCK0}}$	Input mode	t _{sys} + 100		ns
			Output mode	8000/fc - 50		ns
SI0 input setup time (against $\overline{\text{SCK0}} \uparrow$)	t _{SIK}	SI0	$\overline{\text{SCK0}}$ input mode	100		ns
			$\overline{\text{SCK0}}$ output mode	200		ns
SI0 input hold time (against $\overline{\text{SCK0}} \uparrow$)	t _{KSI}	SI0	$\overline{\text{SCK0}}$ input mode	t _{sys} + 200		ns
			$\overline{\text{SCK0}}$ output mode	100		ns
$\overline{\text{SCK0}} \downarrow \rightarrow \text{SO0}$ delay time	t _{KSO}	SO0	$\overline{\text{SCK0}}$ input mode		t _{sys} + 200	ns
			$\overline{\text{SCK0}}$ output mode		100	ns

Note 1) t_{sys} is determined by the upper two bits of the clock control register (Address: 00FE_H; CPU clock selected) resulting in one of the 3 following values:

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) The load of $\overline{\text{SCK0}}$ output mode and SO0 output delay time is 50pF + 1TTL.

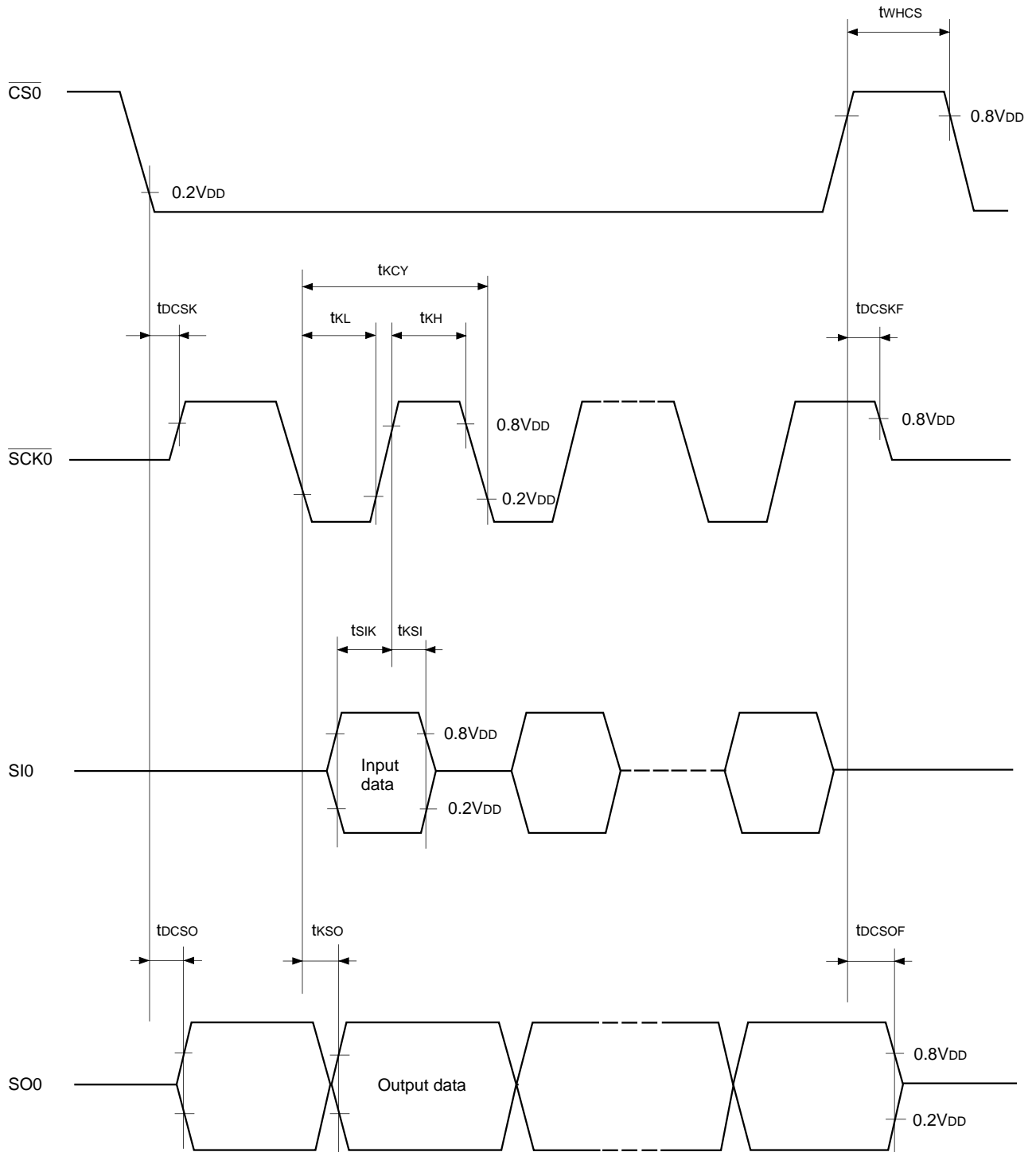


Fig. 4. Serial transfer CH0 timing

Serial transfer (CH1)

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY}	$\overline{\text{SCK1}}$	Input mode	1000		ns
			Output mode	$16000/f_c$		ns
$\overline{\text{SCK1}}$ high and low level width	t_{KH} t_{KL}	$\overline{\text{SCK1}}$	Input mode	400		ns
			Output mode	$8000/f_c - 50$		ns
SI1 input setup time (against $\overline{\text{SCK1}} \uparrow$)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (against $\overline{\text{SCK1}} \uparrow$)	t_{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	200		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}} \downarrow \rightarrow \text{SO1}$ delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		200	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

Note) The load of $\overline{\text{SCK1}}$ output mode and SO1 output delay time is $50\text{pF} + 1\text{TTL}$.

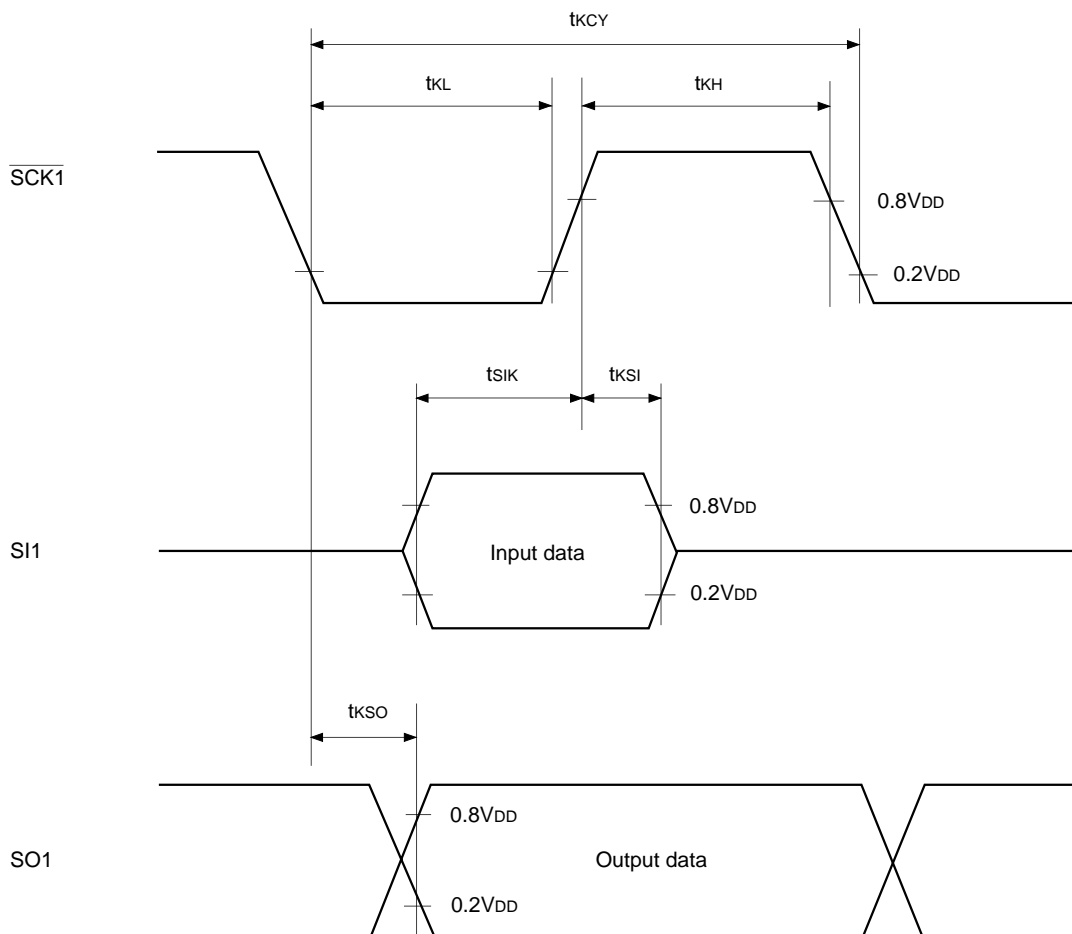
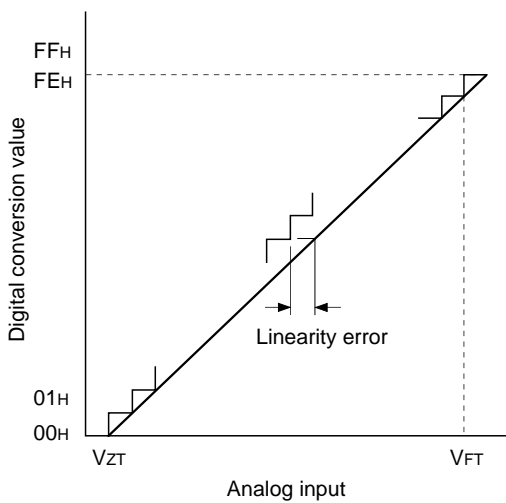


Fig. 5. Serial transfer CH1 timing

(3) A/D converter characteristics

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			A/D converter operation only $T_a = 25^\circ\text{C}$ $V_{DD} = 5.0\text{V}$ $V_{SS} = 0\text{V}$			± 3	LSB
Zero transition voltage	V_{ZT}^{*1}			-10	70	150	mV
Full-scale transition voltage	V_{FT}^{*2}			4930	5050	5120	mV
Conversion time	t_{CONV}			$160/f_{ADC}^{*3}$			μs
Sampling time	t_{SAMP}			$12/f_{ADC}^{*3}$			μs
Analog input voltage	V_{IAN}	AN0 to AN7		0		V_{DD}	V



- *1 V_{ZT} : Digital Value converted between 00H and 01H.
- *2 V_{FT} : Digital Value converted between FEH and FFH.
- *3 f_{ADC} : ADC operation clock selection (MSC: Bit 0 of address 01FFH) and assumes following values:
 $f_{ADC} = f_c/2$ when PS2 is selected.
 $f_{ADC} = f_c$ when PS1 is selected.

Fig. 6. Definition of A/D converter terms

(4) Interrupts, reset inputs (Ta = -10 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interrupt low and high level widths	t _{IH} t _{IL}	INT0 INT1 INT2 INT3		1		μs
Reset input low level width	t _{RSL}	RST		8/fc		μs

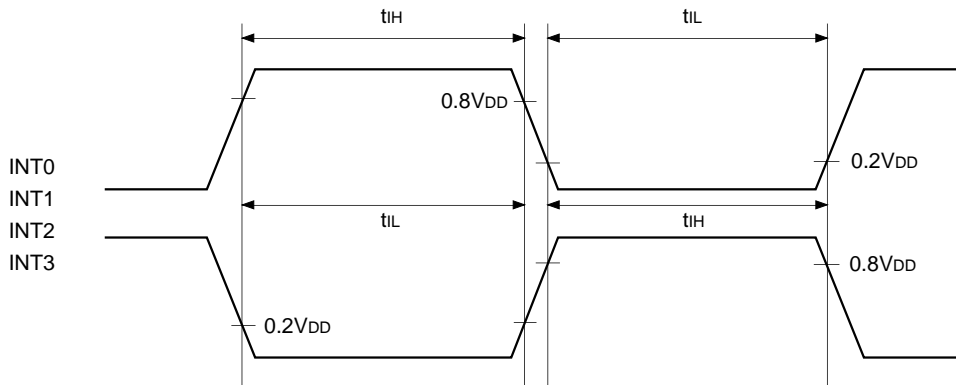


Fig. 7. Interrupt input timing

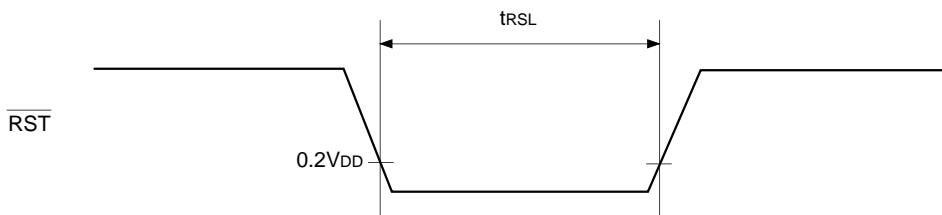


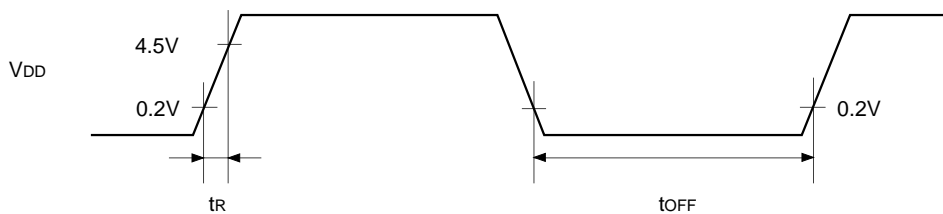
Fig. 8. RST input timing

(5) Power-on reset

Power-on reset* (Ta = -10 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rising time	t _R	VDD	Power-on reset	0.05	50	ms
Power supply cut-off time	t _{OFF}		Repetitive power-on reset	1		ms

* Specifies only when power-on reset function is selected.



The power supply should be rise smoothly.

Fig. 9. Power-on reset

Supplement

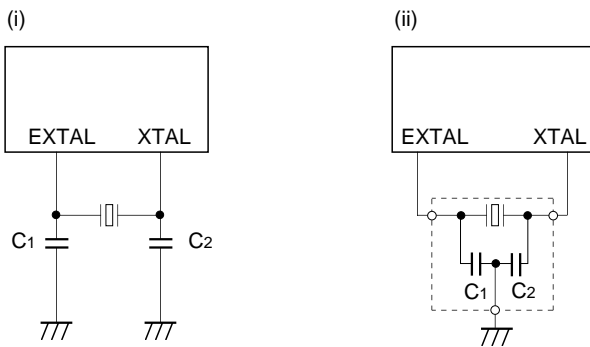


Fig. 10. Recommended oscillation circuit

Manufacturer	Model	fc (MHz)	C ₁ (pF)	C ₂ (pF)	Circuit Example
MURATA MFG CO., LTD	CSA4.19MG	4.19	30	30	(i)
	CSA8.00MTZ	8.00			
	CSA10.0MTZ	10.00			
	CST4.19MGW*	4.19			(ii)
	CST8.00MTW*	8.00			
	CST10.0MTW*	10.00			
RIVER ELETEC CORPORATION	HC-49/U03	4.19	15	15	(i)
		8.00			
		10.00			
KINSEKI LTD.	HC-49/U (-S)	4.19	27	27	
		8.00			
		10.00			

* Indicates types with on-chip grounding capacitors (C₁ and C₂).

Product List

Optional item	Mask	CXP825P40Q-1-□□□
Package	80 pin plastic QFP	80 pin plastic QFP
ROM capacity	32K byte/40K bytes	PROM 40K bytes
Reset pin pull-up resistor	Existent/Non existent	Existent
Power-on reset circuit	Existent/Non existent	Existent
High voltage tolerance pin pull-down resistor	Existent/Non existent	Non Existent (S0/PD0 to S15/PF7) Existent (T0 to S16)

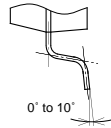
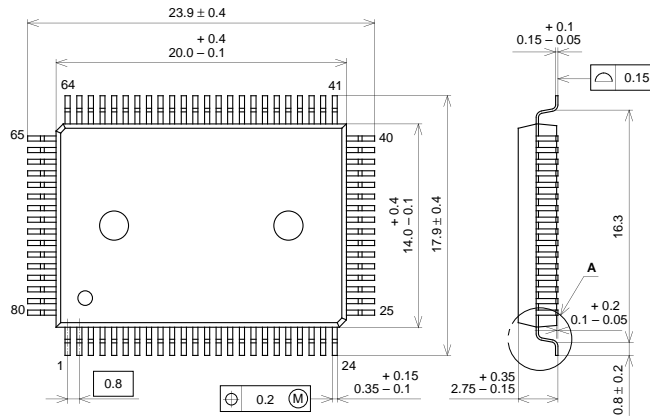
Note on Operation

V_{pp} (Pin 73) is always connected to V_{DD}.

Package Outline

Unit: mm

80PIN QFP (PLASTIC)



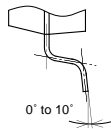
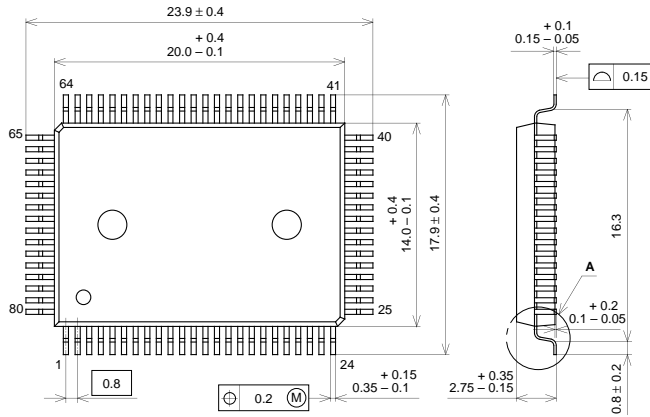
DETAIL A

PACKAGE STRUCTURE

SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g

80PIN QFP (PLASTIC)



DETAIL A

PACKAGE STRUCTURE

SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	42 ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm



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