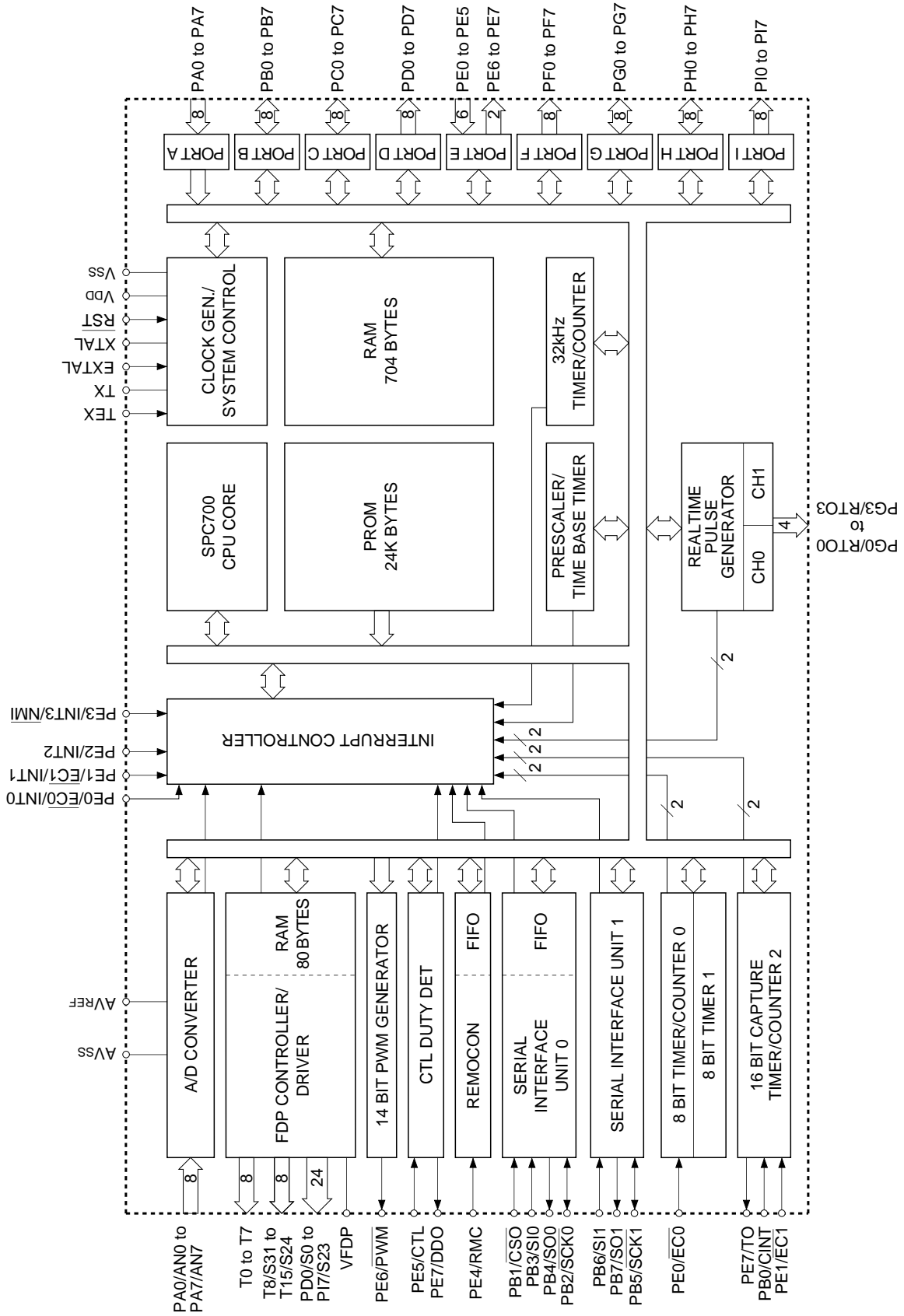
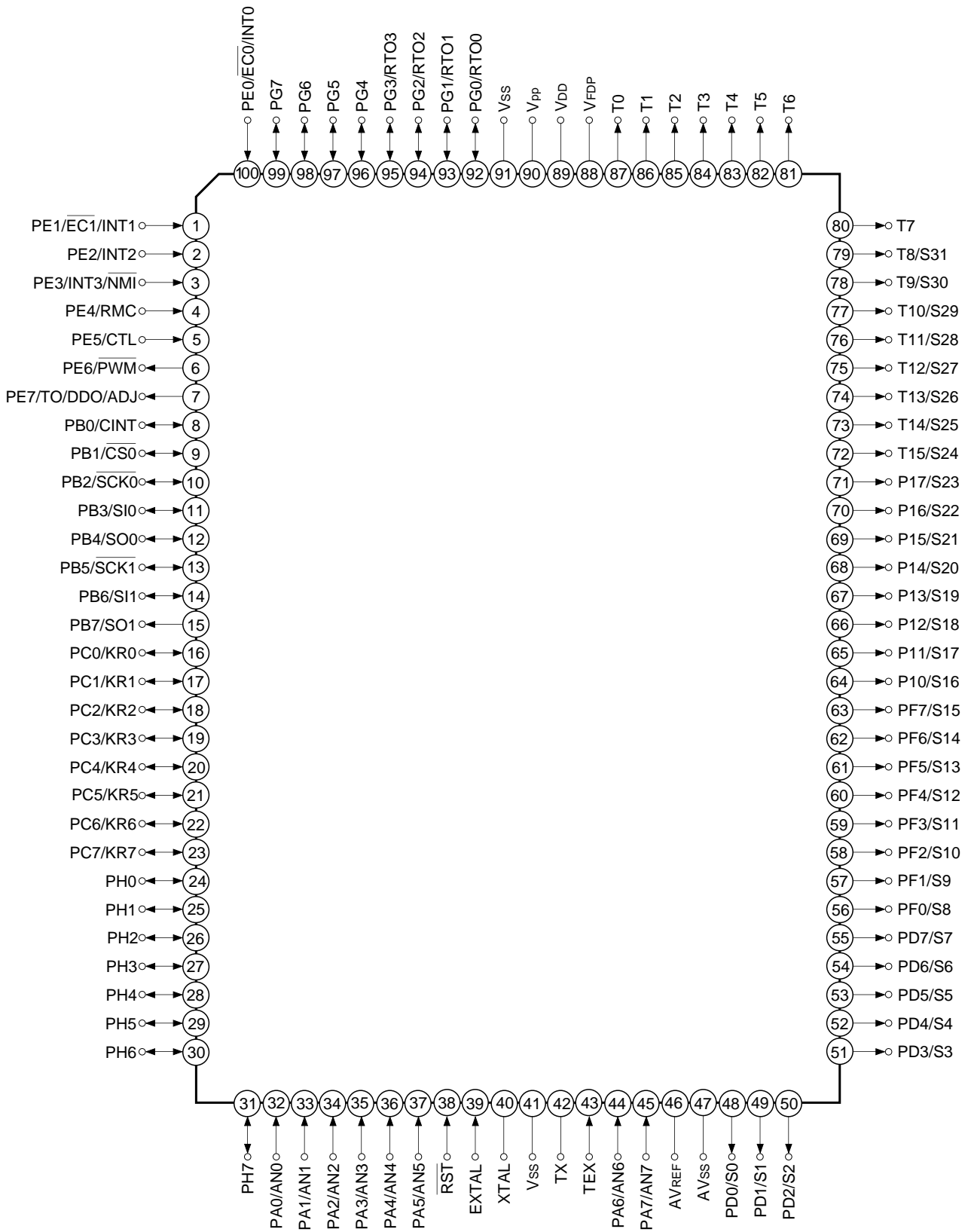


Block Diagram



Pin Assignment (Top View)



Note) V_{pp} (Pin 90) must be connected to V_{DD}.

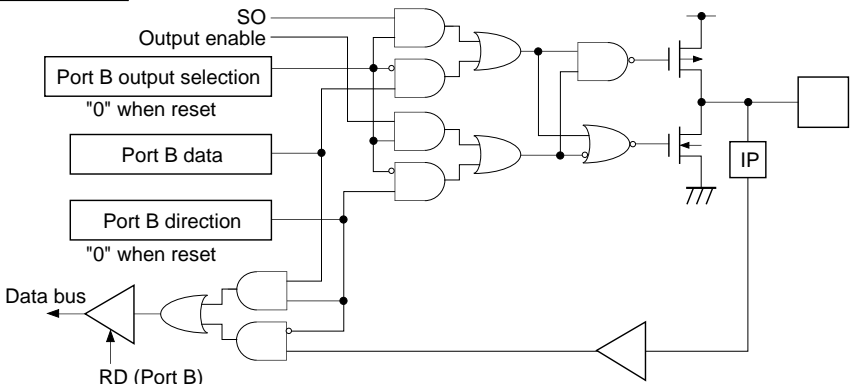
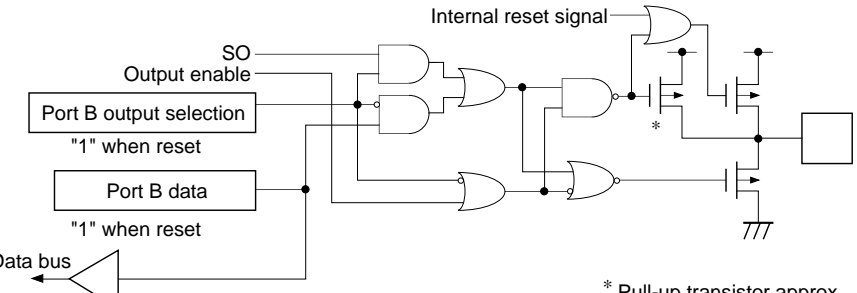
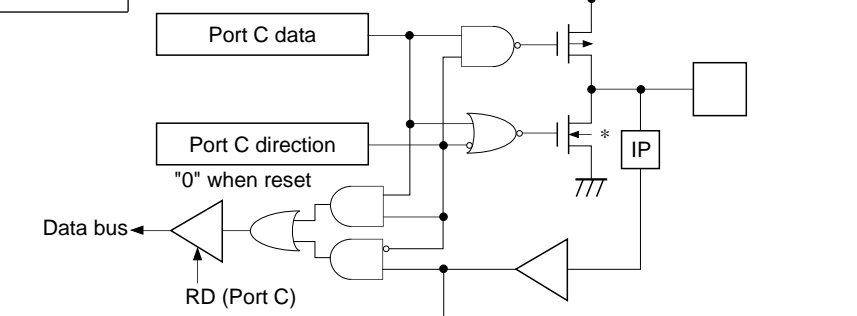
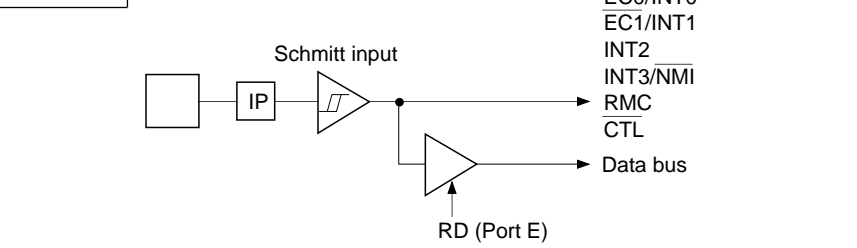
Pin Description

Symbol	I/O	Functions		
PA0/AN0 to PA7/AN7	I/O/ Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bit . (8 pins)	Analog inputs to A/D converter. (8 pins)	
PB0/CINT	I/O/Input	(Port B) 8-bit I/O port. I/O for lower 7bits can be set in a unit of single bits. Uppermost bit (PB7) is for output only. (8 pins)	Capture input to 16-bit timer/counter.	
PB1/ $\overline{\text{CS0}}$	I/O/Input		Chip select input for serial interface (CH0).	
PB2/ $\overline{\text{SCK0}}$	I/O/I/O		Serial clock I/O (CH0).	
PB3/SI0	I/O/Input		Serial data input (CH0).	
PB4/SO0	I/O/Output		Serial data output (CH0).	
PB5/ $\overline{\text{SCK1}}$	I/O/I/O		Serial clock I/O (CH1).	
PB6/SI1	I/O/Input		Serial data input (CH1).	
PB7/SO1	Output/Output		Serial data output (CH1).	
PC0/KR0 to PC7/KR7	I/O/Input	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Capable of driving 12mA sync current.	Serves as key return inputs when operating key scan with FDP segment signal.	
PD0/S0 to PD7/S7	Output/Output	(Port D) 8-bit output port. (8 pins)	FDP segment signal outputs.	
PE0/INT0/ $\overline{\text{EC0}}$	Input/Input/Input	(Port E) 8-bit port. Lower 6 bits are for inputs; upper 2 bits are for outputs. (8 pins)	Inputs for external interruption request. (4 pins)	External event inputs for timer/counter. (2 pins)
PE1/INT1/ $\overline{\text{EC1}}$	Input/Input/Input			Remote control reception circuit input.
PE2/INT2	Input/Input			
PE3/INT3/ $\overline{\text{NMI}}$	Input/Input/Input			
PE4/RMC	Input/Input			
PE5/CTL	Input/Input			
PE6/ $\overline{\text{PWM}}$	Output/Output		14-bit PWM output.	
PE7/TO/DDO/ ADJ	Output/Output/ Output/Output	Output for the 16-bit timer/counter rectangular waves, CTU duty detection, and 32kHz oscillation frequency demultiplication.		
PF0/S8 to PF7/S15	Output/Output	(Port F) 8-bit output port. (8 pins)	FDP segment signal outputs.	
PG0/PTO0 to PG3/RTO3	I/O/Output	(Port G) 8-bit I/O port. I/O can be set in a unit of single bits. Data for the lower 4 bits are gated with the contents of RTO or OR-gate output.	Outputs for real-time pulse generator (RTG). Functions as high-precision, real-time pulse output port. (4 pins)	
PG4 to PG7	I/O	(8 pins)		

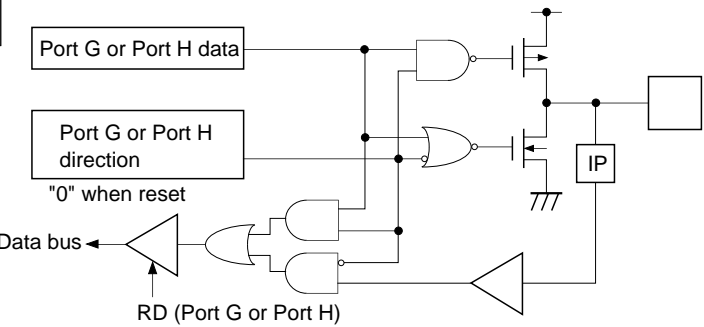
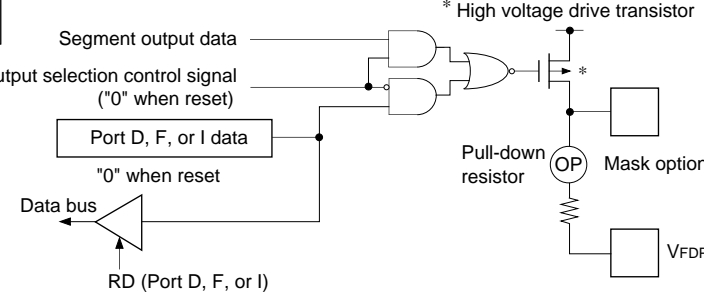
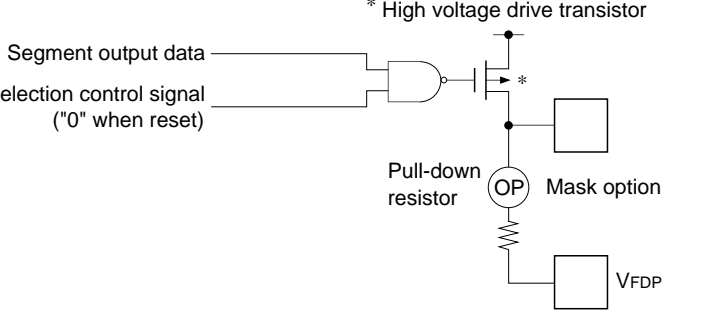
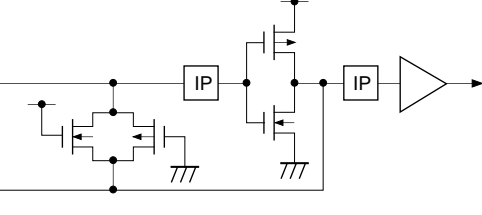
Symbol	I/O	Functions	
PH0 to PH7	I/O	(Port H) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	
PI0/S16 to PI7/S23	Output/Output	(Port I) 8-bit output ports. (8 bits)	FDP segment signal outputs.
T8/S31 to T15/S24	Output/Output	Outputs for FDP timing (digit) signals/sagment signals.	
T0 to T7	Output	FDP timing signal outputs.	
V _{FDP}		FDP voltage supply when incorporated resistor is set by mask option.	
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL	Output		
TEX	Input	Crystal connectors for 32kHz timer/counter clock oscillation. Set 32kHz crystal oscillator between TEX and TX. For usage as event input, attach clock source to TEX, and open TX.	
TX	Output		
$\overline{\text{RST}}$	Input	Low-level active, system reset.	
AV _{REF}	Input	Reference voltage input for A/D converter.	
AV _{SS}		A/D converter GND.	
V _{DD}		V _{cc} supply.	
V _{pp}		V _{cc} supply for incorporated PROM writing. Connect to V _{DD} during normal operation.	
V _{SS}		GND.	

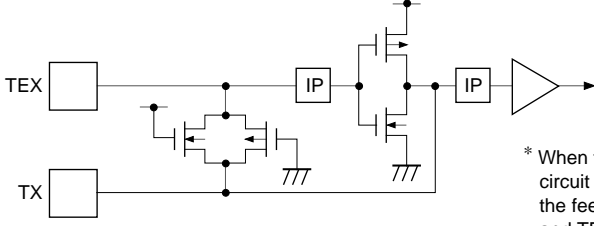
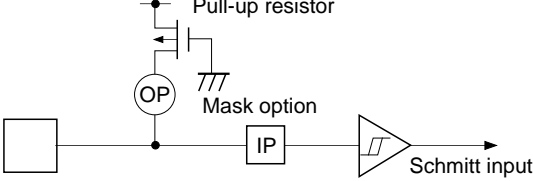
Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
<p>PA0/AN0 to PA7/AN7</p> <p>8 pins</p>	<p>Port A</p> <p>Port A data</p> <p>Port A direction "0" when reset</p> <p>Data bus</p> <p>RD (Port A)</p> <p>Port A input selection "0" when reset</p> <p>Input multiplexer</p> <p>A/D converter</p> <p>IP Input protection circuit</p>	<p>Hi-Z</p>
<p>PB0/CINT PB1/CS0 PB3/SI0 PB6/SI1</p> <p>4 pins</p>	<p>Port B</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus</p> <p>RD (Port B)</p> <p>Schmitt input</p> <p>CINT CS0 SI0 SI1</p> <p>IP</p>	<p>Hi-Z</p>
<p>PB2/SCK0 PB5/SCK1</p> <p>2 pins</p>	<p>Port B</p> <p>SCK out Output enable</p> <p>Port B output selection "0" when reset</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus</p> <p>RD (Port B)</p> <p>Schmitt input</p> <p>SCK in</p> <p>IP</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PB4/SO0</p> <p>1 pin</p>	<p>Port B</p> 	<p>Hi-Z</p>
<p>PB7/SO1</p> <p>1 pin</p>	<p>Port B</p>  <p>* Pull-up transistor approx. 200kΩ</p>	<p>High level</p>
<p>PC0/KR0 to PC7/KR7</p> <p>8 pins</p>	<p>Port C</p>  <p>* High current drive of 12mA possible</p>	<p>Hi-Z</p>
<p>PE0/$\overline{\text{EC0}}$/INT0 PE1/$\overline{\text{EC1}}$/INT1 PE2/INT2 PE3/INT3/$\overline{\text{NMI}}$ PE4/RMC PE5/CTL</p> <p>6 pins</p>	<p>Port E</p> 	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PE6/PWM</p> <p>1 pin</p>	<p>Port E</p>	<p>High level</p>
<p>PE7/TO/ DDO/ADJ</p> <p>1 pin</p>	<p>Port E</p>	<p>High level</p>
<p>PG0/RTO0 to PG3/RTO3</p> <p>4 pins</p>	<p>Port G</p>	<p>Hi-Z</p>

Pin	Circuit format		When reset
PG4 to PG7 PH0 to PH7 12 pins	Port G Port H		Hi-Z
PD0/S0 to PD7/S7 PF0/S8 to PF7/S15 PI0/S16 to PI7/S23 24 pins	Port D Port F Port I		Hi-Z or Low level (when PD resistance is added)
T15/S24 to T8/S31 T0 to T7 16 pins			Hi-Z or Low level (when PD resistance is added)
EXTAL XTAL 2 pins	EXTAL XTAL	 <p data-bbox="1045 1534 1260 1680"> * Diagram shows circuit composition during oscillation. * Feedback resistor is removed during stop. </p>	Oscillation

Pin	Circuit format	When reset
<p>TEX TX</p> <p>2 pins</p>	 <p>* Diagram shows circuit composition during oscillation.</p> <p>* When the operation of the oscillation circuit is stopped by the software, the feedback resistor is removed, and TEX and TX become "Low" level and "High" level respectively.</p>	<p>Oscillation</p>
<p>$\overline{\text{RST}}$</p> <p>1 pin</p>	 <p>Pull-up resistor</p> <p>OP</p> <p>Mask option</p> <p>IP</p> <p>Schmitt input</p>	<p>Low level</p>

Absolute Maximum Ratings

(V_{SS} = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	-0.3 to +7.0	V	
	V _{pp}	-0.3 to +13.0	V	Incorporated PROM
	AV _{SS}	-0.3 to +0.3	V	
Input voltage	V _{IN}	-0.3 to +7.0* ¹	V	
Output voltage	V _{OUT}	-0.3 to +7.0* ¹	V	
Display output voltage	V _{OD}	V _{DD} - 40 to V _{DD} + 0.3	V	As P channel transistor is open drain, V _{DD} is reference.
High level output current	I _{OH}	-5	mA	All pins excluding display outputs* ² (value per pin)
	I _{ODH1}	-15	mA	Display outputs S0 to S23 (value per pin)
	I _{ODH2}	-35	mA	Display outputs T0 to T7, and T8/S31 to T15/S24 (value per pin)
High level total output current	∑I _{OH}	-40	mA	Total for all pins excluding display outputs
	∑I _{ODH}	-100	mA	Total for all display outputs
Low level output current	I _{OL}	15	mA	Port 1
	I _{OLC}	20	mA	High current Port 1 * ³
Low level total output current	∑I _{OL}	100	mA	Total for all output pins
Operating temperature	T _{opr}	-10 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	600	mW	

*¹ V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*² Specifies output current of general-purpose I/O ports.

*³ The high current drive transistor is the N-CH transistor of Port C (PC).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	4.5	5.5	V	High-speed mode Guaranteed operation range
		3.5	5.5		Low-speed mode Guaranteed operation range
		2.7	5.5		Guaranteed operation range with TEX clock
		2.5	5.5		Guaranteed data hold range during STOP
	V _{pp}	V _{pp} = V _{DD}		V	*4
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*1
	V _{IHS}	0.8V _{DD}	V _{DD}	V	Hysteresis input*2
	V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL*3
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	*1
	V _{ILS}	0	0.2V _{DD}	V	Hysteresis input*2
	V _{ILEX}	-0.3	0.4	V	EXTAL*3
Operating temperature	Topr	-10	+75	°C	

*1 Value for each pin of normal input ports (PA, PB3, PB4, PB6, PC, PG, PH).

*2 Value of the following pins: $\overline{\text{RST}}$, CINT, $\overline{\text{CS0}}$, $\overline{\text{SCK0}}$, $\overline{\text{SCK1}}$, $\overline{\text{EC0/INT0}}$, $\overline{\text{EC1/INT1}}$, INT2, INT3/ $\overline{\text{MTI}}$, RMC, CTL.

*3 Specifies only during external clock input.

*4 V_{pp} and V_{DD} should be set to the same voltage.

Electrical Characteristics

DC Characteristics

(Ta = -10 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V _{OH}	PA, PB, PC, PE6, PE7, PG, PH	V _{DD} = 4.5V, I _{OH} = -0.5mA	4.0			V
			V _{DD} = 4.5V, I _{OH} = -1.2mA	3.5			V
Low level output voltage	V _{OL}		V _{DD} = 4.5V, I _{OL} = 1.8mA			0.4	V
			V _{DD} = 4.5V, I _{OL} = 3.6mA			0.6	V
Input current	I _{IHE}	EXTAL	V _{DD} = 5.5V, V _{IH} = 5.5V	0.5		40	μA
			V _{DD} = 5.5V, V _{IL} = 0.4V	-0.5		-40	μA
	I _{IHT}	TEX	V _{DD} = 5.5V, V _{IH} = 5.5V	0.1		10	μA
			V _{DD} = 5.5V, V _{IL} = 0.4V	-0.1		-10	μA
	I _{ILR}	RST	V _{DD} = 5.5V, V _{IL} = 0.4V	-1.5		-400	μA
Display output current	I _{OH}	S0 to S23	V _{DD} = 4.5V, V _{OH} = V _{DD} - 2.5V	-8			mA
		S24/T15 to S31/T8 T0 to T7		-20			mA
Open drain output leakage current (P-CH Tr in off state)	I _{IOL}	S24/T15 to S31/T8 T0 to T7	V _{DD} = 5.5V V _{OL} = V _{DD} - 35V V _{FDP} = V _{DD} - 35V			-20	μA
Pull-down resistance	R _L	S24/T15 to S31/T8 T0 to T7	V _{DD} = 5V V _{FDP} = V _{DD} - 35V	60	100	270	kΩ
I/O leakage current	I _{Iz}	PA to PC, PE, PG, PH	V _{DD} = 5.5V V _I = 0, 5.5V			±10	μA
Power supply current*	I _{DD1}	V _{DD}	High-speed mode operation (1/2 frequency demultiplier clock) V _{DD} = 5.5V, 10MHz crystal oscillation (C ₁ = C ₂ = 15pF)		20	40	mA
			V _{DD} = 3V, 32kHz crystal oscillation (C ₁ = C ₂ = 47pF)		400	1000	μA
	I _{DDS1}		Sleep mode V _{DD} = 5.5V, 10MHz crystal oscillation (C ₁ = C ₂ = 15pF)		1.2	8	mA
			V _{DD} = 3V, 32kHz crystal oscillation (C ₁ = C ₂ = 47pF)		9	30	μA
	I _{DDS3}		Stop mode V _{DD} = 5.5V, Termination of 10MHz and 32kHz crystal oscillation				30
Input capacity	C _{IN}	Pins other than S0 to S31, T0 to T7, PB7, PE6, AV _{REF} , AV _{SS} , V _{FDP} , V _{DD} , V _{SS}	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

* When all pins are open.

AC Characteristics

(1) Clock timing

(Ta = -10 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	1		10	MHz
System clock input pulse width	t _{XL} t _{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	37.5			ns
System clock input rise time, fall time	t _{CR} t _{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	t _{EH} t _{EL}	$\overline{EC0}$, EC1	Fig. 3	t _{sys} + 50*1			ns
Event count input clock rise time, fall time	t _{ER} t _{EF}	$\overline{EC0}$, EC1	Fig. 3			20	ms
System clock frequency	fc	TEX TX	VDD = 2.7 to 5.5V Fig. 2 (32kHz clock application condition)		32.768		kHz
Event count input pulse width	t _{TL} t _{TH}	TEX	Fig. 3	10			μs
Event count input rise time, fall time	t _{TR} t _{TF}	TEX	Fig. 3			20	ms

*1 t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: 00FEH).

t_{sys} [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Fig. 1. Clock timing

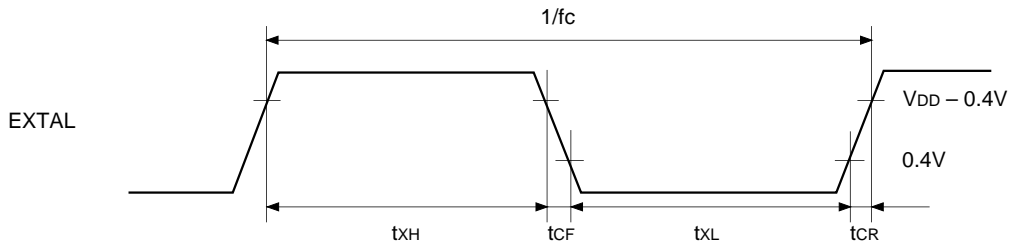


Fig. 2. Clock applied conditions

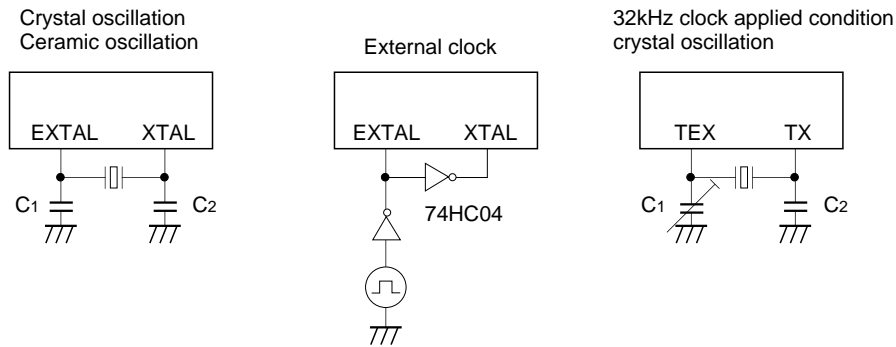
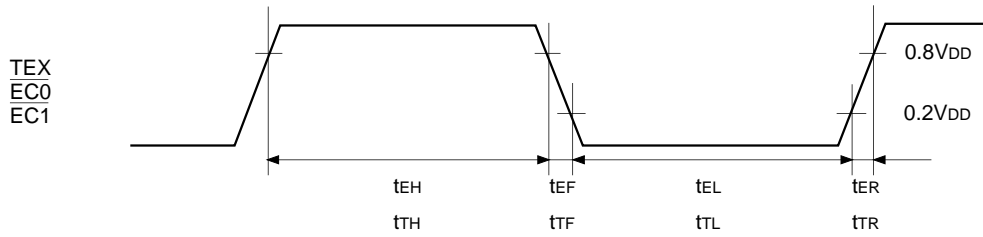


Fig. 3. Event count clock timing



(2) Serial transfer (CH0)

(Ta = -10 to +75°C, VDD = 4.5 to 5.5V, VSS=0V reference)

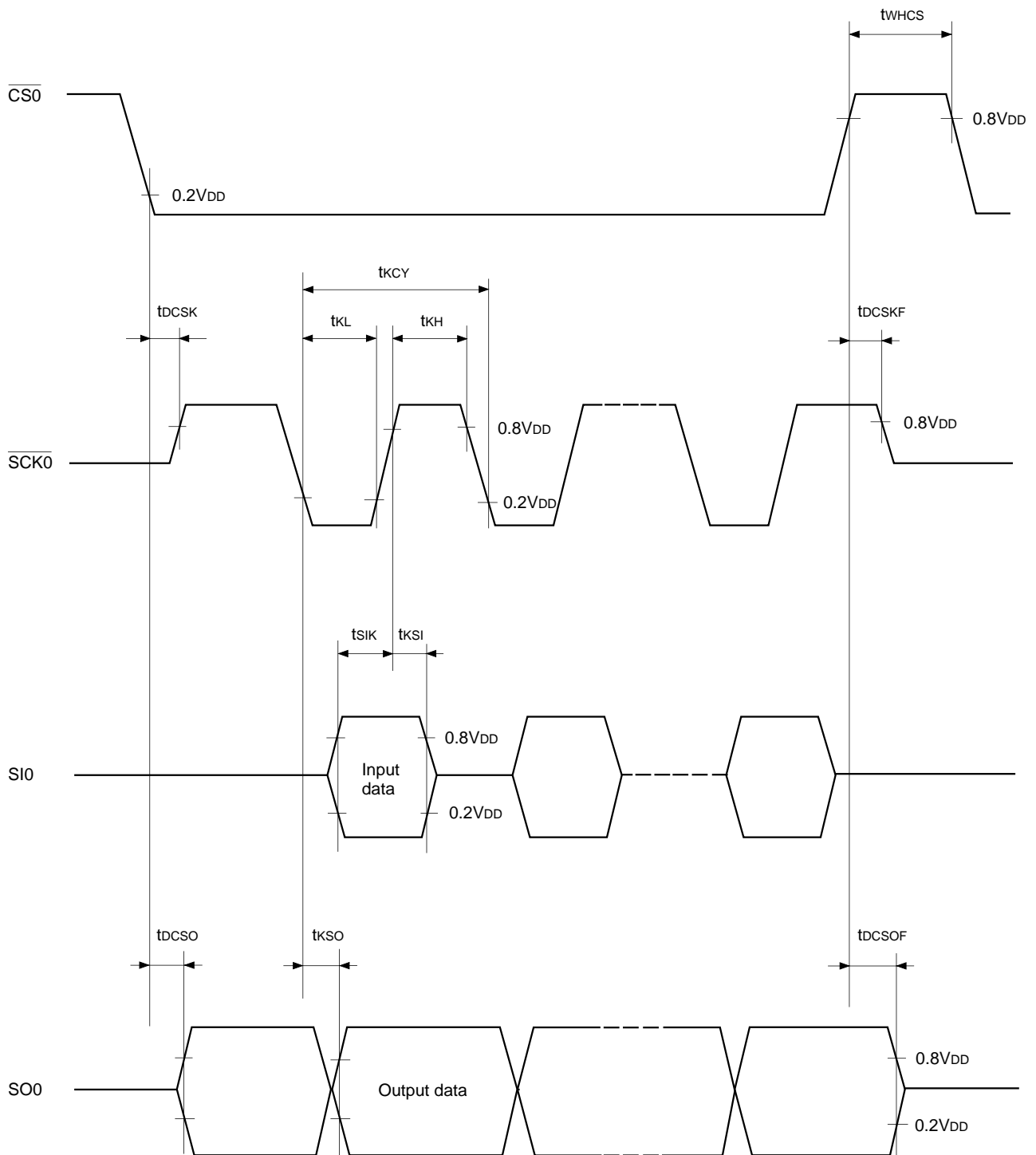
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ delay time	t _{DCSK}	$\overline{SCK0}$	Chip select transfer mode (SCK0 = output mode)		t _{sys} + 200	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ float delay time	t _{DCSKF}	$\overline{SCK0}$	Chip select transfer mode (SCK0 = output mode)		t _{sys} + 200	ns
$\overline{CS0} \downarrow \rightarrow SO0$ delay time	t _{DCSO}	SO0	Chip select transfer mode		t _{sys} + 200	ns
$\overline{CS0} \uparrow \rightarrow SO0$ float delay time	t _{DCSOF}	SO0	Chip select transfer mode		t _{sys} + 200	ns
$\overline{CS0}$ High level width	t _{WHCS}	$\overline{CS0}$	Chip select transfer mode	t _{sys} + 200		ns
$\overline{SCK0}$ cycle time	t _{KCY}	$\overline{SCK0}$	Input mode	2t _{sys} + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ High, Low level width	t _{KH} t _{KL}	$\overline{SCK0}$	Input mode	t _{sys} + 100		ns
			Output mode	8000/fc - 50		ns
SI0 input set-up time (for $\overline{SCK0} \uparrow$)	t _{SIK}	SI0	$\overline{SCK0}$ input mode	100		ns
			$\overline{SCK0}$ output mode	200		ns
SI0 input hold time (for $\overline{SCK0} \uparrow$)	t _{KSI}	SI0	$\overline{SCK0}$ input mode	t _{sys} + 200		ns
			$\overline{SCK0}$ output mode	100		ns
$\overline{SCK0} \downarrow \rightarrow SO0$ delay time	t _{KSO}	SO0	$\overline{SCK0}$ input mode		t _{sys} + 200	ns
			$\overline{SCK0}$ output mode		100	ns

Note 1) t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: 00FEH).

t_{sys} [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Note 2) The load condition for the $\overline{SCK0}$ output mode, SO0 output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer CH0 timing



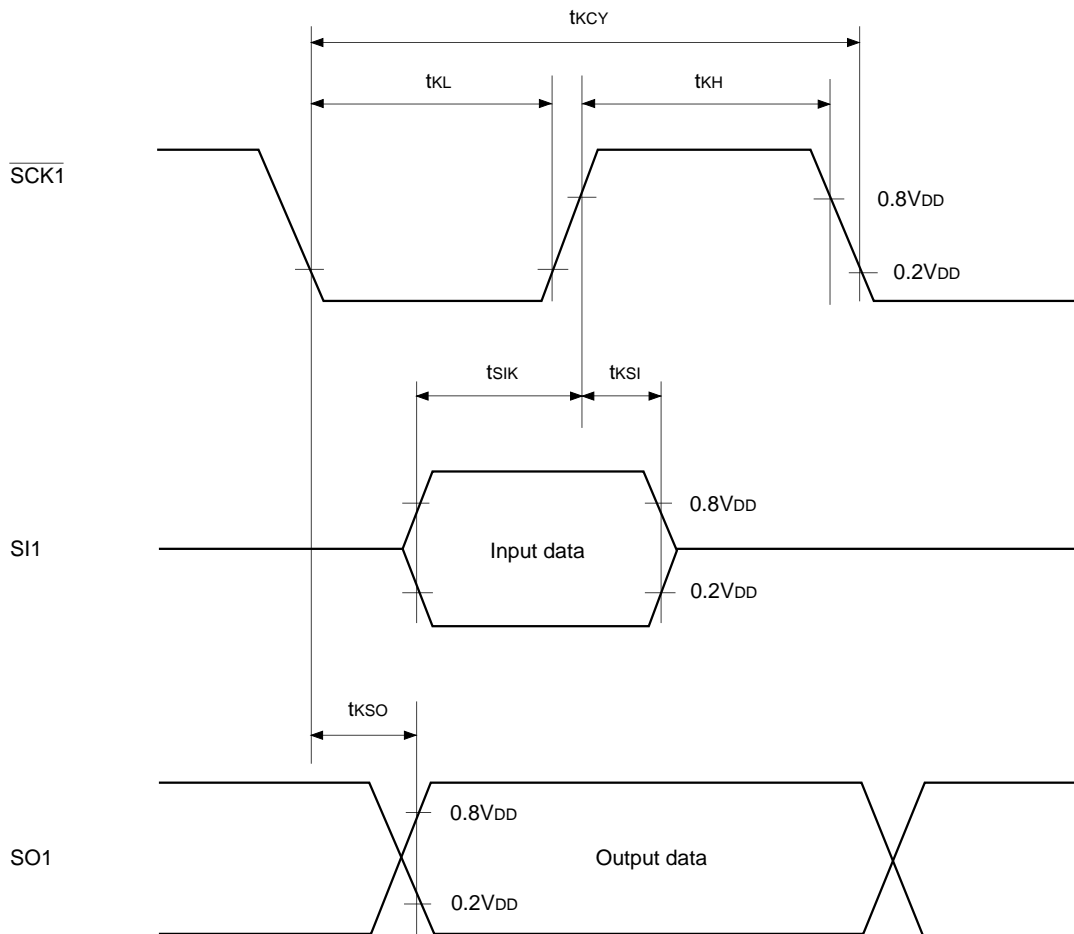
Serial transfer (CH1)

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY}	$\overline{\text{SCK1}}$	Input mode	1000		ns
			Output mode	$16000/f_c$		ns
$\overline{\text{SCK1}}$ High, Low level width	t_{KH} t_{KL}	$\overline{\text{SCK1}}$	Input mode	400		ns
			Output mode	$8000/f_c - 50$		ns
SI1 input set-up time (for $\overline{\text{SCK1}} \uparrow$)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (for $\overline{\text{SCK1}} \uparrow$)	t_{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	200		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}} \downarrow \rightarrow \text{SO1}$ delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		200	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

Note) The load condition for the $\overline{\text{SCK1}}$ output mode, SO1 output delay time is $50\text{pF} + 1\text{TTL}$.

Fig. 5. Serial transfer CH1 timing

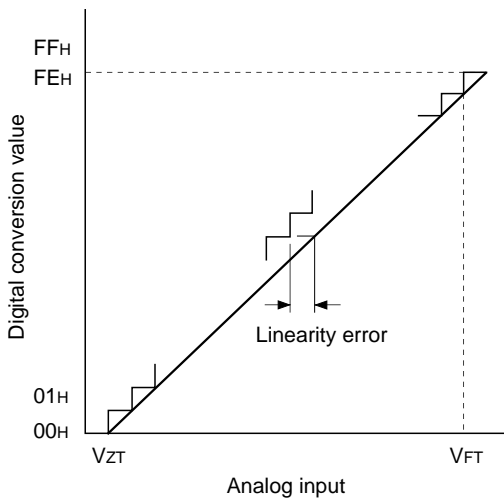


(3) A/D converter characteristics

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $AV_{REF} = 4.0$ to AV_{DD} , $V_{SS} = AV_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error						± 3	LSB
Zero transition voltage	V_{ZT}^{*1}		$T_a = 25^\circ\text{C}$ $V_{DD} = AV_{DD} = 5.0\text{V}$ $V_{DD} = AV_{SS} = 0\text{V}$	-10	70	150	mV
Full-scale transition voltage	V_{FT}^{*2}			4930	5050	5120	mV
Conversion time	t_{CONV}			$160/f_{ADC}^{*3}$			μs
Sampling time	t_{SAMP}			$12/f_{ADC}^{*3}$			μs
Reference input voltage	V_{REF}	AV_{REF}		$V_{DD} - 0.5$		V_{DD}	V
Analog input voltage	V_{IAN}	$AN0$ to $AN7$		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operation mode		0.6	1.0	mA
	I_{REFS}		Sleep mode Stop mode 32kHz operation mode			10	μA

Fig. 6. Definitions of A/D converter terms



- *1 V_{ZT} : Value at which the digital conversion value changes from 00H to 01H and vice versa.
- *2 V_{FT} : Value at which the digital conversion value changes from FEH to FFH and vice versa.
- *3 f_{ADC} indicates the below values due to ADC operation clock selection (ADCS: Bit 6 of address 00F9H).
 During PS2 selection, $f_{ADC} = f_c/2$
 During PS1 selection, $f_{ADC} = f_c$

(4) Interruption, reset input (Ta = -10 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption High, Low level width	t _{IH} t _{IL}	INT0 INT1 INT2 $\overline{\text{NMI/INT3}}$		1		μs
Reset input Low level width	t _{RSL}	$\overline{\text{RST}}$		8/fc		μs

Fig. 7. Interruption input timing

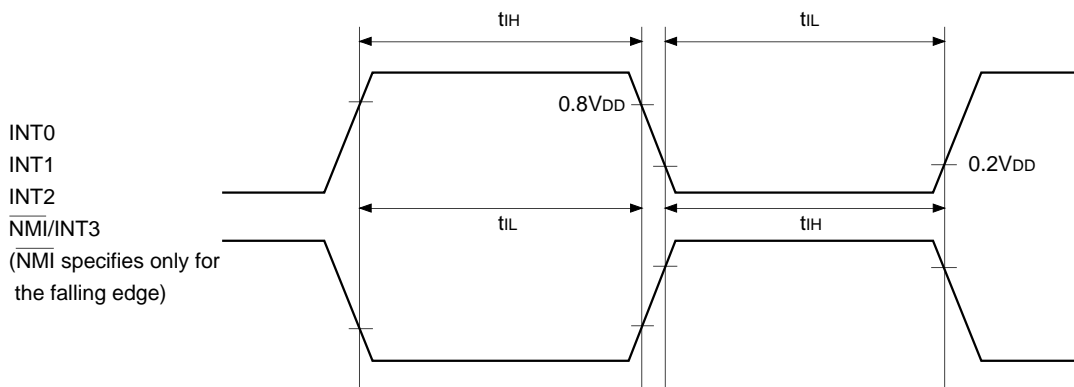
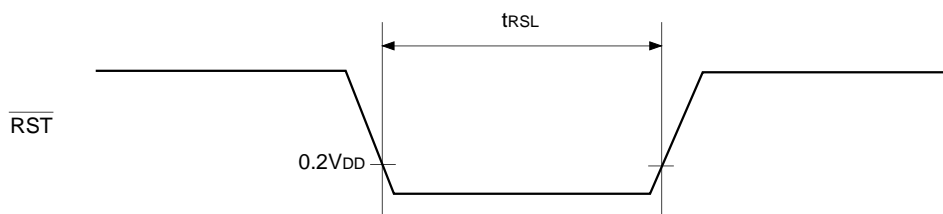


Fig. 8. $\overline{\text{RST}}$ input timing

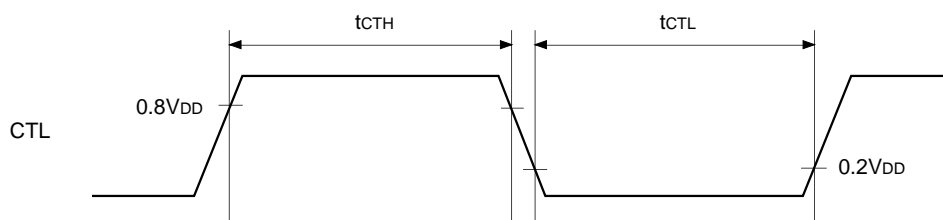


(5) Others

(Ta = -10 to +75°C, VDD = 4.5 to 5.0V, Vss = 0V reference)

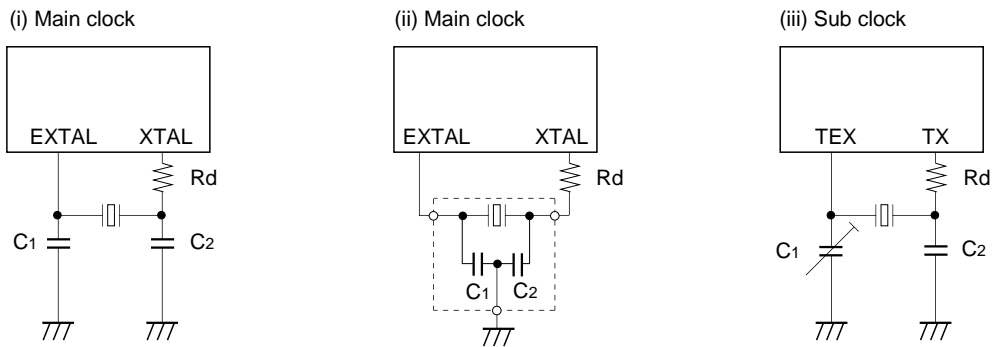
Item	Symbol	Pin	Condition	Min.	Max.	Unit
CLK input High, Low level width	t _{CTH} t _{CTL}	CTL	t _{sys} = 2000/fc	t _{sys} + 200		ns

Fig. 9. Other timing



Appendix

Fig. 10. Recommended oscillation circuit



Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example
MURATA MFG CO., LTD	CSA4.19MG	4.19	30	30	0	(i)
	CSA8.00MTZ	8.00				
	CSA10.0MTZ	10.00				
	CST4.19MGW*	4.19				(ii)
	CST8.00MTW*	8.00				
	CST10.0MTW*	10.00				
RIVER ELETEC CORPORATION	HC-49/U03	4.19	15	15	0	(i)
		8.00				
		10.00				
KINSEKI LTD.	HC-49/U (-S)	4.19	27	27	0	
		8.00				
		10.00				
	P3	32.768kHz	30	39	330k	(iii)

Those marked with an asterisk (*) signify types with built-in ground capacitance (C1, C2).

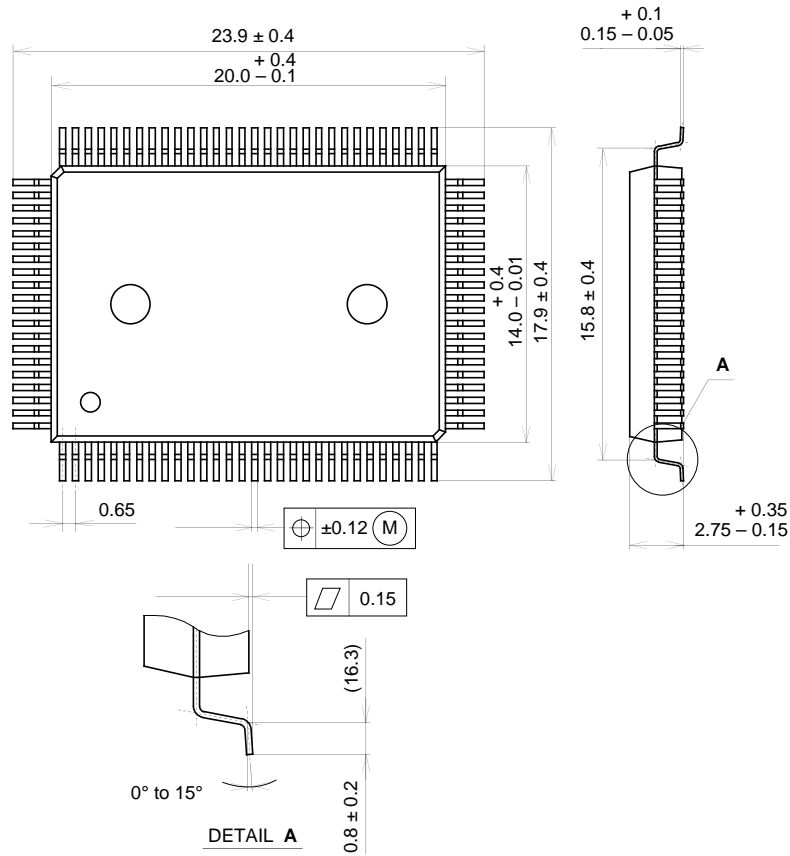
Selection Guide

Optional item	Mask product	CXP822P24Q-1- □□□
Package	100-pin plastic QFP	100-pin plastic QFP
ROM capacitance	20K bytes/24K bytes	PROM 24K bytes
Reset pin pull-up resistor	Existent/Non-existent	Existant
High voltage drive pin pull-up resistor	Existent/Non-existent	Non existent (S0/PD0 to S23/PF7) Existent (T0 to T15/S24)

Package Outline

Unit: mm

100PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-100P-L01
EIAJ CODE	*QFP100-P-1420-A
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.4g



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