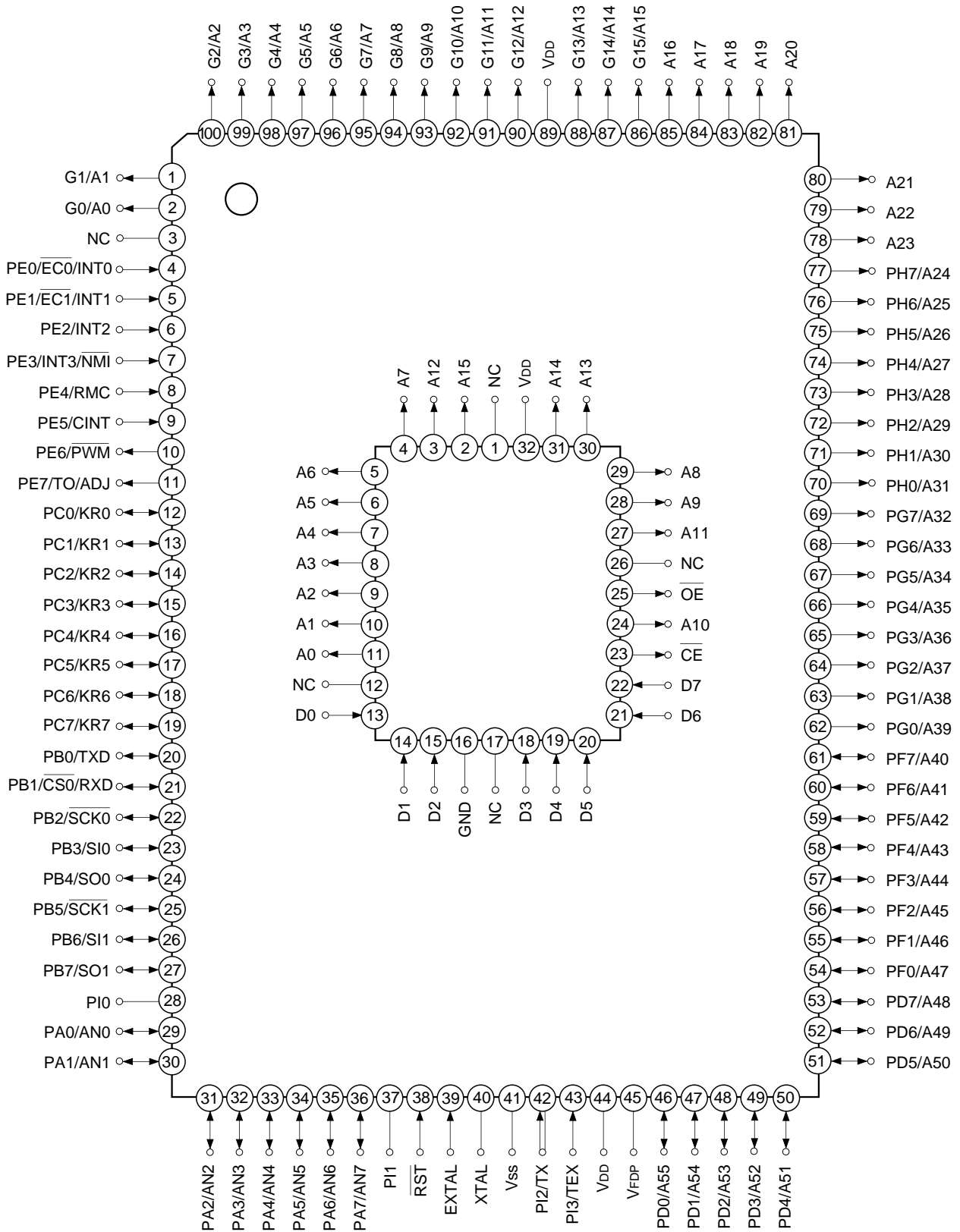
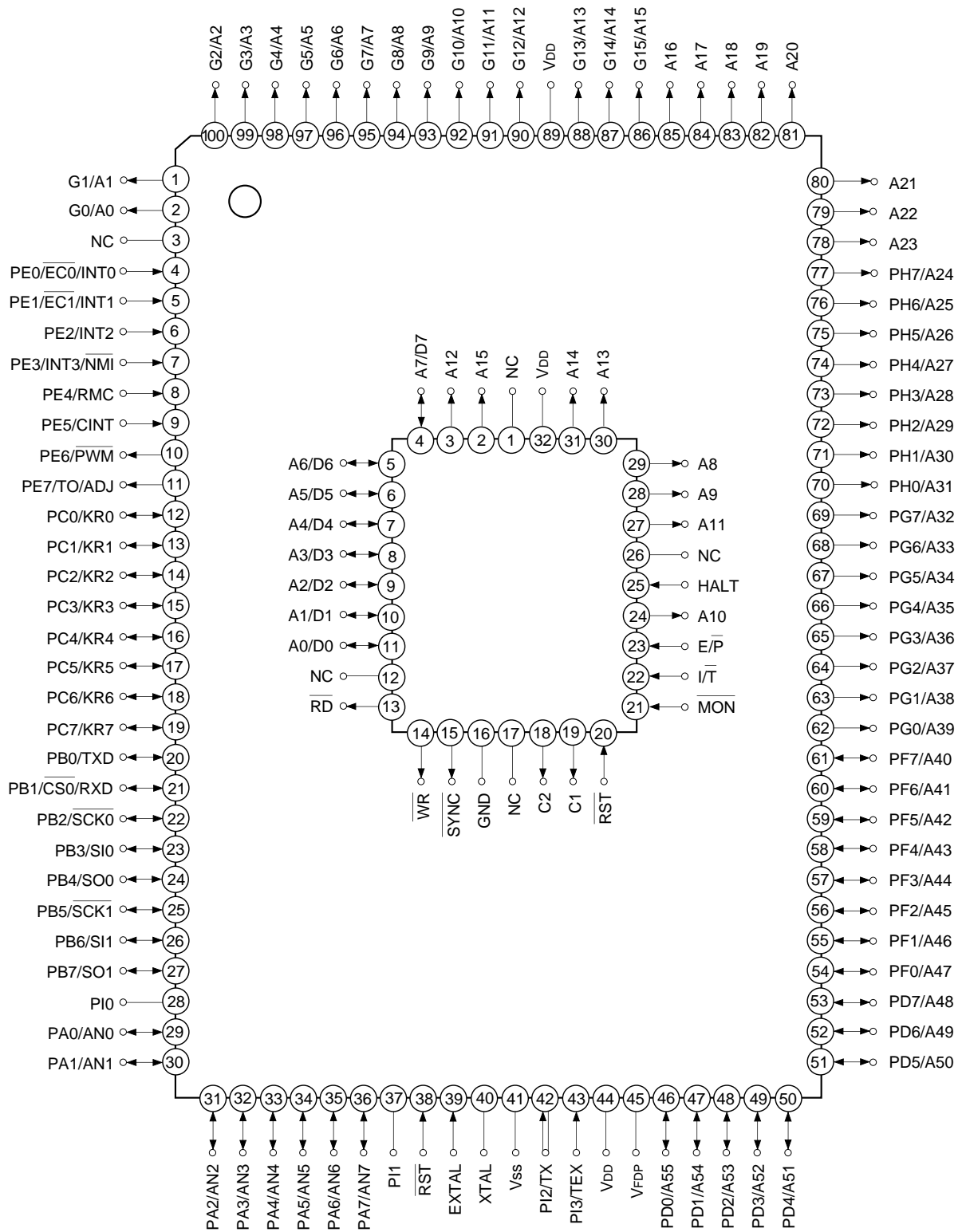


Pin Configuration in Piggyback Mode



- Note)** 1. Do not any connetions toNC (Pin 3).
 2. V_{DD} (Pins 44 and 89) are both connected to V_{DD}.

Pin Configuration in Evaluator Mode

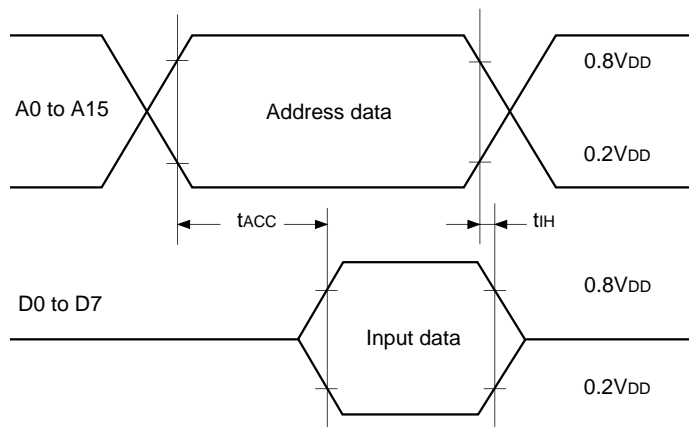


- Note)**
1. Do not any connetions to NC (Pin 3).
 2. VDD (Pins 44 and 89) are both connected to VDD.

EPROM Read Timing

($T_a = -20$ to $+75^\circ\text{C}$, $V_{cc} = 4.5$ to 5.5V , $V_{ss} = 0\text{V}$ reference)

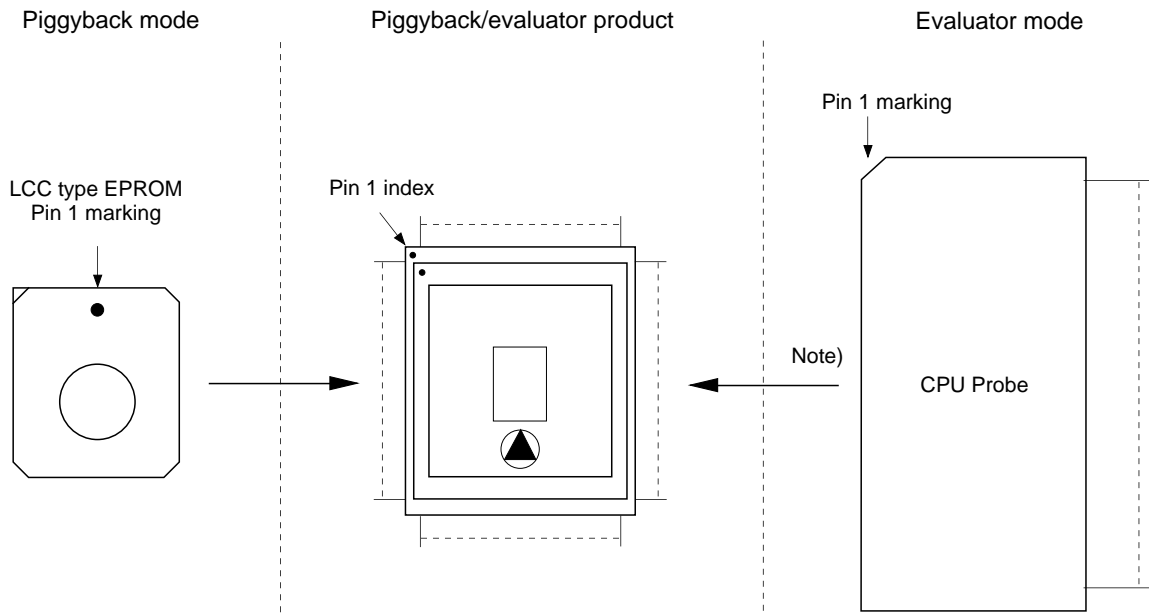
Item	Symbol	Pins	Min.	Max.	Unit
Address → Data input delay time	t_{ACC}	A0 to A15 D0 to D7		120	ns
Address → Data hold time	t_{IH}	A0 to A15 D0 to D7	0		ns



Products List

Option item	Products		
	Mask		Piggyback/evaluator
	CXP82052	CXP82060	CXP82000-U01Q
Package	100-pin plastic QFP		100-pin ceramic PQFP
ROM capacitance	52K bytes	60K bytes	EPROM 60K bytes
Pull-up resistance for reset pin	Existent/Non-existent		Existent
Pull-down resistance for high voltage drive pin	Existent/Non-existent		Existent: G0/A0 to A23 Non-existent: PD0/A55 to PH7/A24

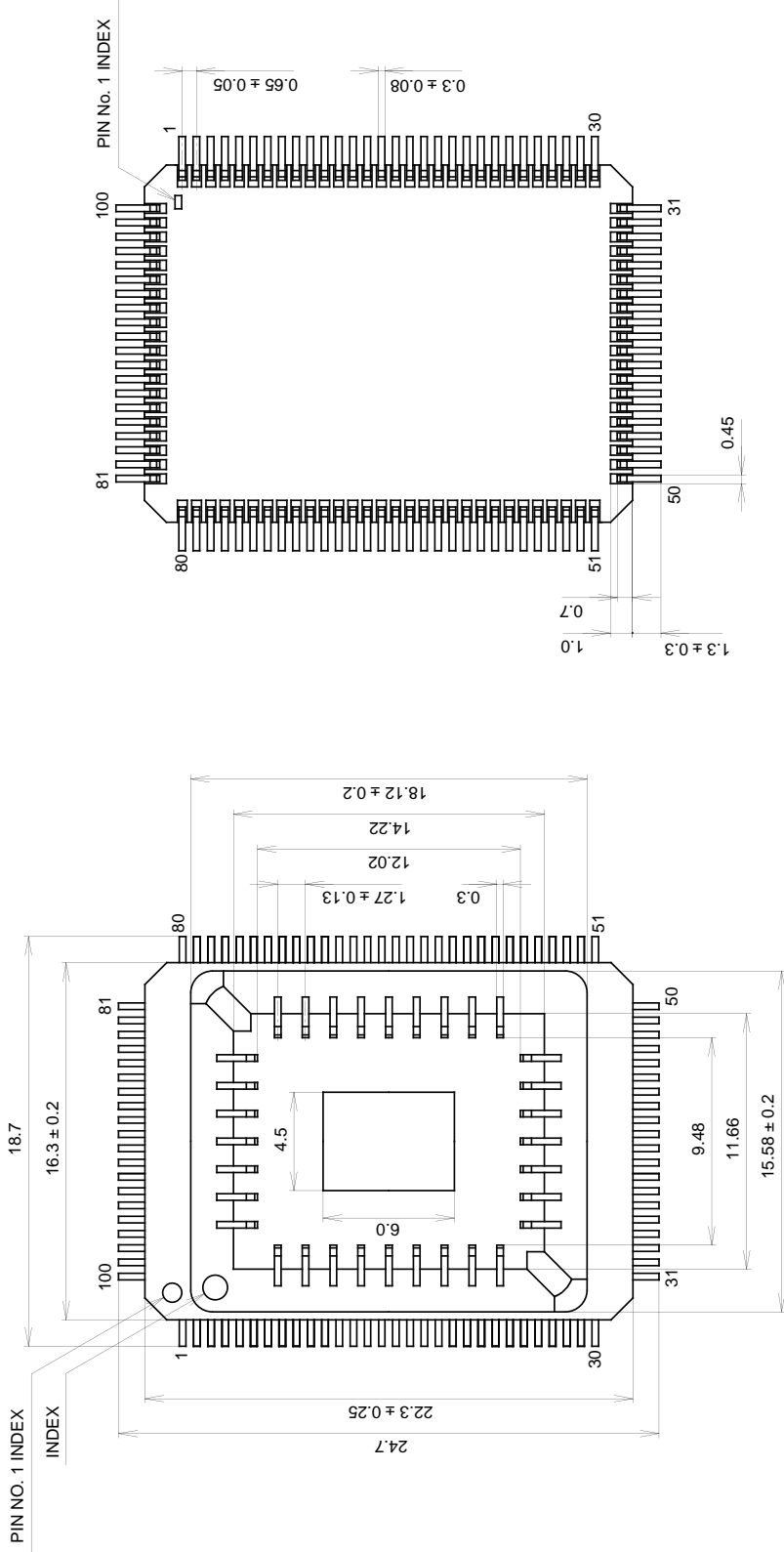
Piggyback mode/evaluator mode can be switched as shown below.



Note) Evaluation cap should be connected to CPU probe.

Package Outline Unit: mm

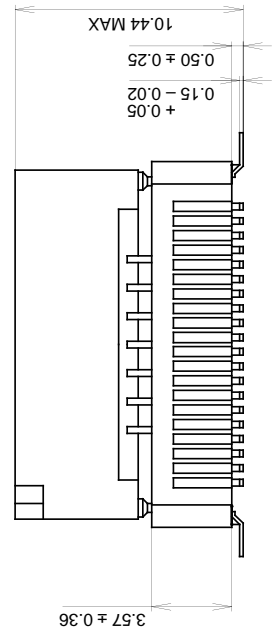
100PIN PQFP (CERAMIC)



PACKAGE STRUCTURE

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	5.7g

SONY CODE	PQFP-100C-L01
EIA/J CODE	AQFP100-C-0000-A
JEDEC CODE	_____





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