

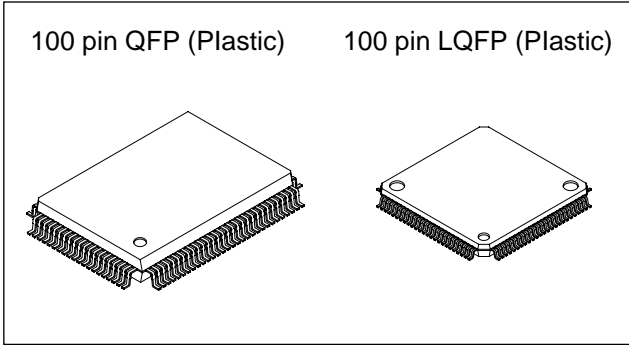
CXP81952M/81960M

CMOS 8-bit Single Chip Microcomputer

Description

The CXP81952M/81960M is a CMOS 8-bit micro-computer which consists of A/D converter, serial interface, timer/counter, time base timer, vector interruption, high precision timing pattern generation circuit, PWM generator, PWM for tuner, 32kHz timer/event counter, remote control reception circuit, and FRC capture unit, as well as basic configurations like 8-bit CPU, ROM, RAM and I/O port. They are integrated into a single chip.

Also the CXP81952M/81960M provides sleep/stop functions which enable to lower power consumption and ultra-low speed instruction mode in 32kHz operation.



Structure

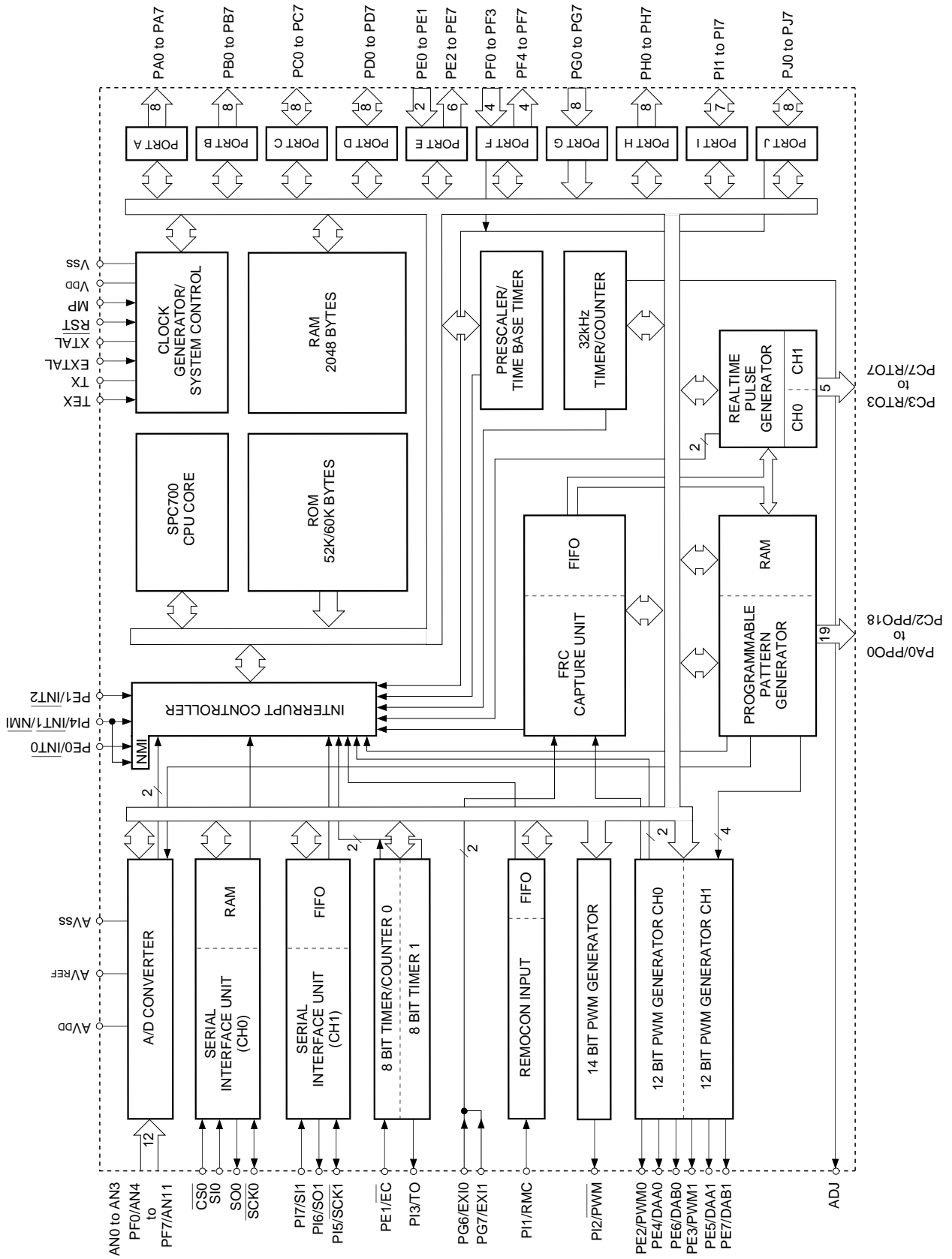
Silicon gate CMOS IC

Features

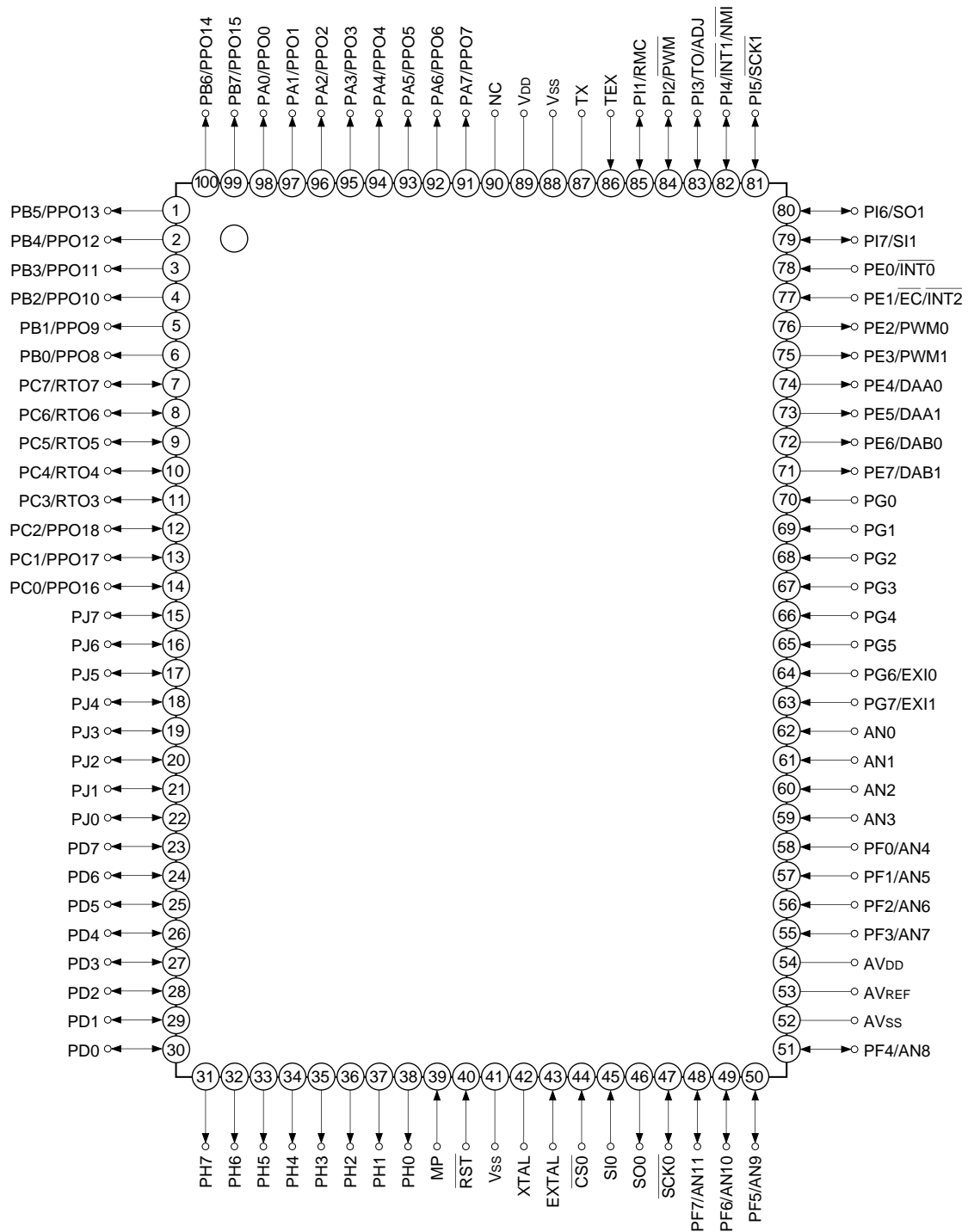
- A wide instruction set (213 instructions) which covers various types of data
 - 16-bit operation/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle
 - 200ns at 20MHz operation (4.5 to 5.5V)
 - 333ns at 12MHz operation (2.7 to 5.5V)
 - 122µs at 32kHz operation
- Incorporated ROM capacity 52K bytes (CXP81952M), 60K bytes (CXP81960M)
- Incorporated RAM capacity 2048 bytes
- Peripheral functions
 - A/D converter 8 bits, 12 channels, successive approximation system (Conversion time of 16µs at 20MHz)
 - Serial Interface Incorporated buffer RAM (1 to 32 bytes auto transfer), 1 channel
Incorporated 8-bit and 8-stage FIFO (1 to 8 bytes auto transfer), 1 channel
 - Timer 8-bit timer, 8-bit timer/counter, 19-bit time base timer, 32kHz timer/counter
 - High precision timing pattern generator PPG: maximum of 19 pins, 32 stages programmable
RTG: 5 pins, 2 channels
 - PWM/DA gate output PWM: 12 bits, 2 channels (Repetitive frequency of 78kHz at 20MHz)
DA gate pulse output: 13 bits, 4 channels
 - FRC capture unit Incorporated 26-bit and 8-stage FIFO
 - PWM output 14 bits, 1 channel
 - Remote control reception circuit 8-bit pulse measurement counter with on-chip 6-stage FIFO
- Interruption 20 factors, 15 vectors, multi-interruption possible
- Standby mode Sleep/stop
- Package 100-pin plastic QFP/LQFP
- Piggyback/evaluator CXP81900M

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Block Diagram



Pin Assignment 1 (Top View) 100-pin QFP package



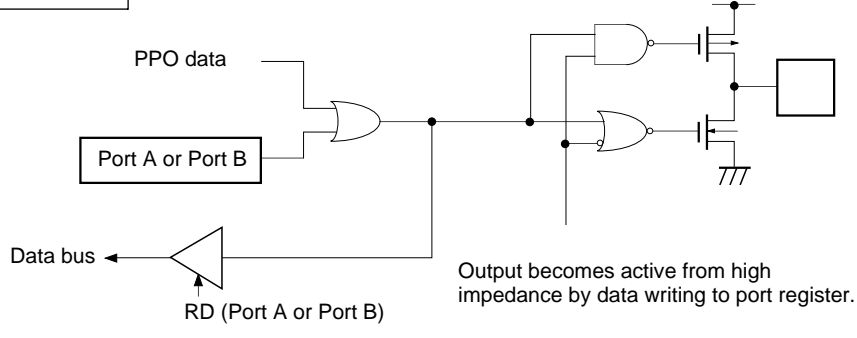
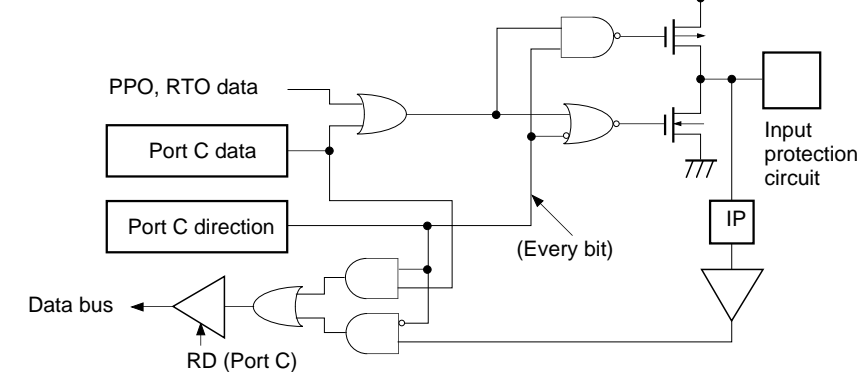
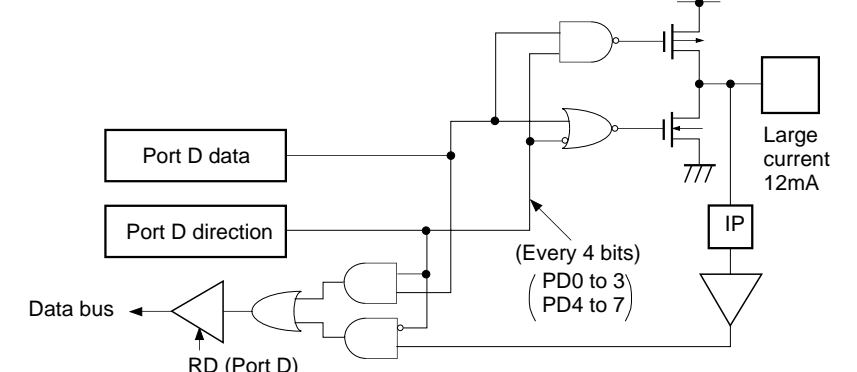
- Note)**
1. NC (Pin 90) is always connected to VDD.
 2. Vss (Pins 41 and 88) are both connected to GND.
 3. MP (Pin 39) is always connected to GND.

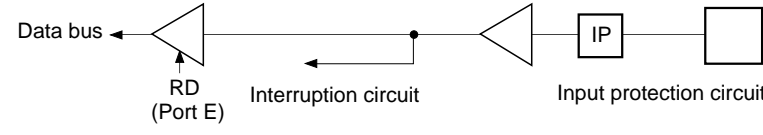
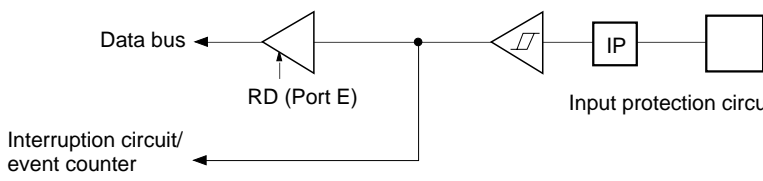
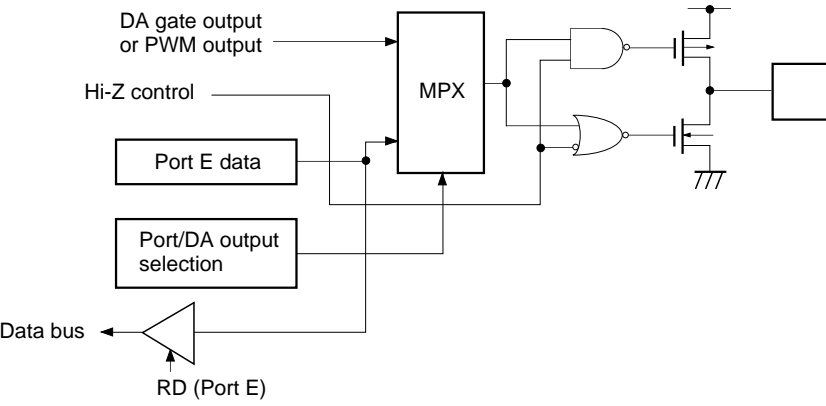
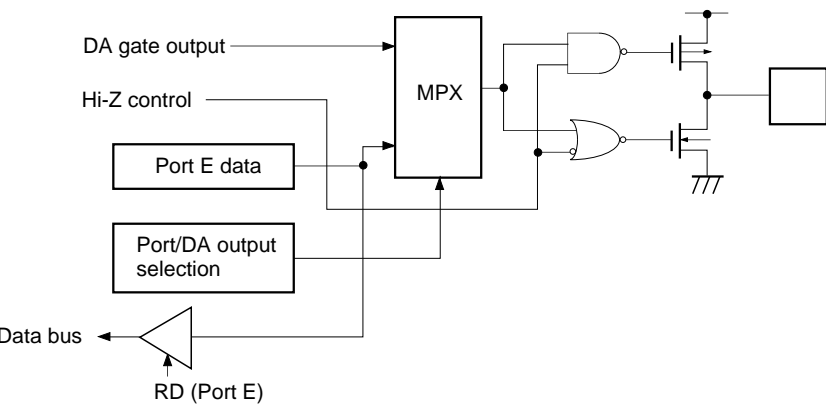
Pin Description

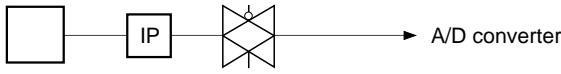
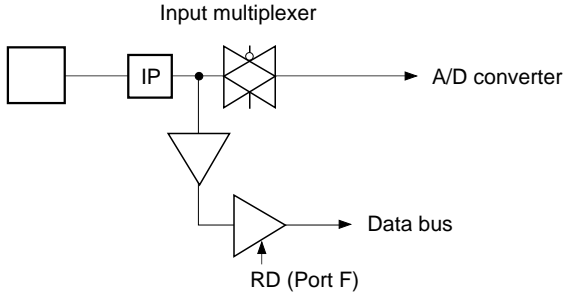
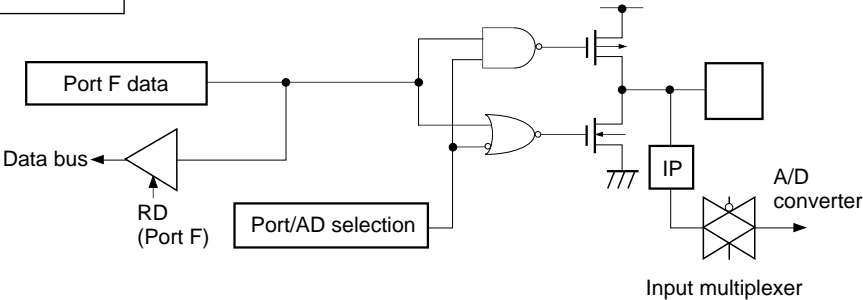
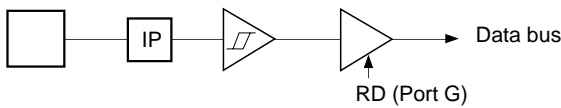
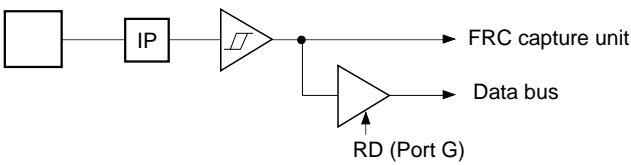
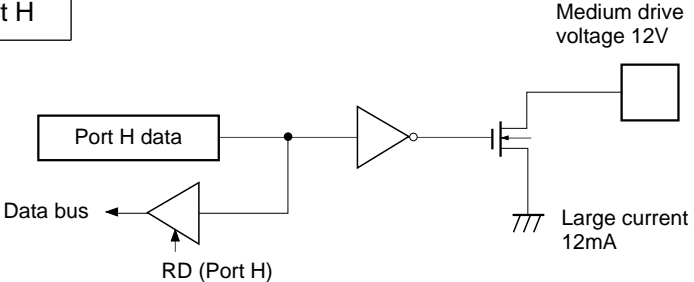
Symbol	I/O	Description		
PA0/PPO0 to PA7/PPO7	Output/ Real-time output	(Port A) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	Programmable pattern generator (PPG) output. Functions as high precision real-time pulse output port. (19 pins)	
PB0/PPO8 to PB7/PPO15	Output/ Real-time output	(Port B) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)		
PC0/PPO16 to PC2/PPO18	I/O/ Real-time output	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Data is gated with PPO or RTO contents by OR-gate and they are output. (8 pins)		
PC3/RTO3 to PC7/RTO7	I/O/ Real-time output		Real-time pulse generator (RTG) output. Functions as high precision real-time pulse output port. (5 pins)	
PD0 to PD7	I/O	(Port D) 8-bit I/O port. I/O can be set in a unit of 4bits. Can drive 12mA sink current. (8 pins)		
PE0/ $\overline{\text{INT0}}$	Input/Input	(Port E) 8-bit port. Lower 2 bits are for input; upper 6 bits are for output. (8 pins)	Input pin to request external interruption. Active at the falling edge.	
PE1/ $\overline{\text{EC}}/\overline{\text{INT2}}$	Input/Input/Input		External event input pin for timer/counter.	Input pin to request external interruption. Active at the falling edge.
PE2/PWM0	Output/Output		PWM output pins. (2 pins)	
PE3/PWM1	Output/Output			
PE4/DAA0	Output/Output			DA gate pulse output pins. (4 pins)
PE5/DAA1	Output/Output			
PE6/DAB0	Output/Output			
PE7/DAB1	Output/Output			
AN0 to AN3	Input	Analog input pins to A/D converter. (12 pins)		
PF0/AN4 to PF3/AN7	Input/Input	(Port F) 8-bit port. Lower 4 bits are for input; upper 4 bits are for output. Lower 4 bits also serve as standby release input pin. (8 pins)		
PF4/AN8 to PF7/AN11	Output/Input			
$\overline{\text{SCK0}}$	I/O	Serial clock (CH0) I/O pin.		
SO0	Output	Serial data (CH0) output pin.		
SI0	Input	Serial data (CH0) input pin.		
$\overline{\text{CS0}}$	Input	Serial chip select (CH0) input pin.		

Symbol	I/O	Description	
PG0 to PG4	Input	(Port G) 8-bit input port. (8 pins)	External input pin to FRC capture unit.
PG5			
PG6/EXI0			
PG7/EXI1			
PH0 to PH7	Output	(Port H) 8-bit output port; N-ch open drain output of medium drive voltage (12V) and large current (12mA). (8 pins)	
PI1/RMC	I/O/Input	(Port I) 7-bit I/O port. I/O port can be set in a unit of single bits. (7 pins)	Remote control reception circuit input pin.
PI2/PWM	I/O/Output		14-bit PWM output pin.
PI3/TO/ADJ	I/O/Output/Output		Timer/counter, 32kHz oscillation adjustment output pin.
PI4/INT1/ NMI	I/O/Input/Input		Input pin to request external interruption and non-maskable interruption. Active at the falling edge.
PI5/SCK1	I/O/I/O		Serial clock (CH1) I/O pin.
PI6/SO1	I/O/Output		Serial data (CH1) output pin.
PI7/SI1	I/O/Input		Serial data (CH1) input pin.
PJ0 to PJ7	I/O		(Port J) 8-bit I/O port. I/O and standby release input can be set in a unit of single bits.
EXTAL	Input	Connects a crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and input opposite phase clock to XTAL pin.	
XTAL	Output		
TEX	Input	Connects a crystal oscillator for 32kHz timer clock. When used as event counter, input to TEX pin and leave TX pin open. (Feedback resistor is not removed.)	
TX	Output		
RST	Input	System reset pin; active at Low level.	
MP	Input	Microprocessor mode input pin. Always connect to GND.	
AVDD		Positive power supply pin of A/D converter.	
AVREF	Input	Reference voltage input pin of A/D converter.	
AVss		GND pin of A/D converter.	
VDD		Positive power supply pin.	
Vss		GND pin. Connect both Vss pins to GND.	

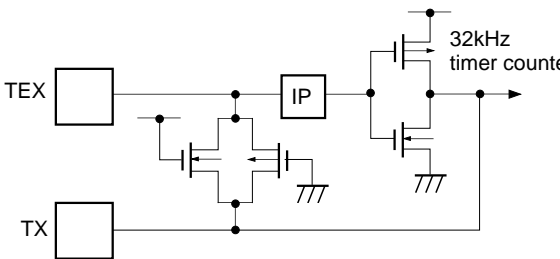
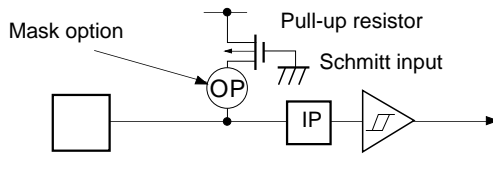
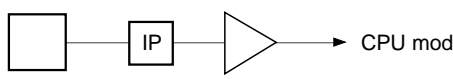
Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
<p>Port A Port B</p> <p>PA0/PPO0 to PA7/PPO7 PB0/PPO8 to PB7/PPO15</p> <p>16 pins</p>	 <p>PPO data</p> <p>Port A or Port B</p> <p>Data bus</p> <p>RD (Port A or Port B)</p> <p>Output becomes active from high impedance by data writing to port register.</p>	<p>Hi-Z</p>
<p>Port C</p> <p>PC0/PPO16 to PC2/PPO18 PC3/RTO3 to PC7/RTO7</p> <p>8 pins</p>	 <p>PPO, RTO data</p> <p>Port C data</p> <p>Port C direction</p> <p>Data bus</p> <p>RD (Port C)</p> <p>(Every bit)</p> <p>Input protection circuit</p> <p>IP</p>	<p>Hi-Z</p>
<p>Port D</p> <p>PD0 to PD7</p> <p>8 pins</p>	 <p>Port D data</p> <p>Port D direction</p> <p>Data bus</p> <p>RD (Port D)</p> <p>(Every 4 bits) (PD0 to 3) (PD4 to 7)</p> <p>Large current 12mA</p> <p>IP</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PE0/$\overline{\text{INT0}}$</p> <p>1 pin</p>	<p>Port E</p>  <p>Data bus</p> <p>RD (Port E)</p> <p>Interruption circuit</p> <p>Input protection circuit</p>	<p>Hi-Z</p>
<p>PE1/$\overline{\text{EC}}/\overline{\text{INT2}}$</p> <p>1 pin</p>	<p>Port E</p>  <p>Data bus</p> <p>RD (Port E)</p> <p>Interruption circuit/ event counter</p> <p>Input protection circuit</p>	<p>Hi-Z</p>
<p>PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1</p> <p>4 pins</p>	<p>Port E</p>  <p>DA gate output or PWM output</p> <p>Hi-Z control</p> <p>Port E data</p> <p>Port/DA output selection</p> <p>Data bus</p> <p>RD (Port E)</p> <p>MPX</p> <p>AND</p> <p>GND</p>	<p>Hi-Z</p>
<p>PE6/DAB0 PE7/DAB1</p> <p>2 pins</p>	<p>Port E</p>  <p>DA gate output</p> <p>Hi-Z control</p> <p>Port E data</p> <p>Port/DA output selection</p> <p>Data bus</p> <p>RD (Port E)</p> <p>MPX</p> <p>AND</p> <p>GND</p>	<p>High level</p>

Pin	Circuit format	When reset
<p>AN0 to AN3</p> <p>4 pins</p>	<p>Input multiplexer</p> 	<p>Hi-Z</p>
<p>PF0/AN4 to PF3/AN7</p> <p>4 pins</p>	<p>Port F</p> <p>Input multiplexer</p> 	<p>Hi-Z</p>
<p>PF4/AN8 to PF7/AN11</p> <p>4 pins</p>	<p>Port F</p> 	<p>Hi-Z</p>
<p>PG0 to PG5</p> <p>6 pins</p>	<p>Port G</p> <p>Schmitt input</p> 	<p>Hi-Z</p>
<p>PG6/EXI0 to PG7/EXI1</p> <p>2 pins</p>	<p>Port G</p> <p>Schmitt input</p> 	<p>Hi-Z</p>
<p>PH0 to PH7</p> <p>8 pins</p>	<p>Port H</p>  <p>Medium drive voltage 12V</p> <p>Large current 12mA</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PJ0 to PJ7</p> <p>8 pins</p>		<p>Hi-Z</p>
<p>$\overline{\text{CS0}}$ SIO</p> <p>2 pins</p>		<p>Hi-Z</p>
<p>SO0</p> <p>1 pin</p>		<p>Hi-Z</p>
<p>$\overline{\text{SCK0}}$</p> <p>1 pin</p>		<p>Hi-Z</p>
<p>EXTAL XTAL</p> <p>2 pins</p>	<ul style="list-style-type: none"> • Diagram shows the circuit composition during oscillation. • Feedback resistor is removed during stop mode. 	<p>Oscillation</p>

Pin	Circuit format	When reset
<p>TEX TX</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Diagram shows the circuit composition during oscillation. • Feedback resistor is removed during 32kHz oscillation circuit stop by software. At this time TEX pin outputs Low level and TX pin outputs High level. 	<p>Oscillation</p>
<p>$\overline{\text{RST}}$</p> <p>1 pin</p>	 <p>Mask option</p> <p>Pull-up resistor</p> <p>Schmitt input</p> <p>IP</p>	<p>Low level</p>
<p>MP</p> <p>1 pin</p>	 <p>IP</p> <p>CPU mode</p>	<p>Hi-Z</p>

Absolute Maximum Ratings

(V_{SS} = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	-0.3 to +7.0	V	
	AV _{DD}	AV _{SS} to +7.0* ¹	V	
	AV _{SS}	-0.3 to +0.3	V	
Input voltage	V _{IN}	-0.3 to +7.0* ²	V	
Output voltage	V _{OUT}	-0.3 to +7.0* ²	V	
Medium drive output voltage	V _{OUTP}	-0.3 to +15.0	V	PH pin
High level output current	I _{OH}	-5	mA	
High level total output current	∑I _{OH}	-50	mA	Total of output pins
Low level output current	I _{OL}	15	mA	Pins excluding large current outputs (value per pin)
	I _{OLC}	20	mA	Large current output pin (value per pin* ³)
Low level total output current	∑I _{OL}	130	mA	Total of output pins
Operating temperature	T _{opr}	-20 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	600	mW	QFP
		380		LQFP

*1 AV_{DD} and V_{DD} should be set to the same voltage.

*2 V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*3 The large current operation transistors are the N-CH transistors of the PD and PH ports.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	4.5	5.5	V	fc = 20MHz or less Guaranteed operation range for high-speed mode (1/2 frequency dividing clock)
		2.7	5.5	V	fc = 12MHz or less
		2.7	5.5	V	Guaranteed operation range for low-speed mode (1/16 frequency dividing clock)
		2.5	5.5	V	Guaranteed operation range by TEX clock
		2.0	5.5	V	Guaranteed data hold range for stop mode
Analog supply voltage	AV _{DD}	2.7	5.5	V	*1
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*2
	V _{IHS}	0.8V _{DD}	V _{DD}	V	CMOS Schmitt input*3 and PE0/ $\overline{\text{INT0}}$
			5.5	V	CMOS Schmitt input*6
	V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL*4, *7 and TEX*5, *7
			V _{DD} + 0.2	V	EXTAL*4, *8 and TEX*5, *8
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	*2, *7
		0	0.2V _{DD}	V	*2, *8
	V _{ILS}	0	0.2V _{DD}	V	CMOS Schmitt input*3 and PE0/ $\overline{\text{INT0}}$
	V _{ILEX}	-0.3	0.4	V	EXTAL*4, *7 and TEX*5, *7
			0.2	V	EXTAL*4, *8 and TEX*5, *8
Operating temperature	T _{opr}	-20	+75	°C	

*1 AV_{DD} and V_{DD} should be set to the same voltage.

*2 Normal input ports (PC, PD, PF0 to PF3, PG, PI and PJ), MP

*3 $\overline{\text{SCK0}}$, $\overline{\text{RST}}$, PE1/ $\overline{\text{EC/INT2}}$, PI1/ $\overline{\text{RMC}}$, PI4/ $\overline{\text{INT1/NMI}}$, PI5/ $\overline{\text{SCK1}}$ and PI7/SI1

*4 Specifies only when the external clock is input.

*5 Specifies only when the external event count clock is input.

*6 $\overline{\text{CS0}}$, SI0 and PG

*7 In case of 4.5 to 5.5V supply voltage (V_{DD}).

*8 In case of 2.7 to 3.3V supply voltage (V_{DD}).

Electrical Characteristics

DC Characteristics ($V_{DD} = 4.5$ to $5.5V$)

($T_a = -20$ to $+75^\circ C$, $V_{SS} = 0V$ reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE2 to PE7, PF4 to PF7,	$V_{DD} = 4.5V, I_{OH} = -0.5mA$	4.0			V
			$V_{DD} = 4.5V, I_{OH} = -1.2mA$	3.5			V
Low level output voltage	V_{OL}	PH (V_{OL} only) PI1 to PI7	$V_{DD} = 4.5V, I_{OL} = 1.8mA$			0.4	V
			$V_{DD} = 4.5V, I_{OL} = 3.6mA$			0.6	V
		PD, PH	$V_{DD} = 4.5V, I_{OL} = 12.0mA$			1.5	V
Input current	I_{IHE}	EXTAL	$V_{DD} = 5.5V, V_{IH} = 5.5V$	0.5		40	μA
	I_{ILE}		$V_{DD} = 5.5V, V_{IL} = 0.4V$	-0.5		-40	μA
	I_{IHT}	TEX	$V_{DD} = 5.5V, V_{IH} = 5.5V$	0.1		10	μA
	I_{ILT}		$V_{DD} = 5.5V, V_{IL} = 0.4V$	-0.1		-10	μA
	I_{ILR}		\overline{RST}^{*1}	$V_{DD} = 5.5V, V_{IL} = 0.4V$	-1.5		-400
I/O leakage current	I_{IZ}	PA to PG, PI, PJ, MP AN0 to AN3, CS0, SI0, SO0 SCK0, \overline{RST}^{*1}	$V_{DD} = 5.5V, V_I = 0, 5.5V$			± 10	μA
Open drain output leakage current (in N-CH Tr OFF state)	I_{LOH}	PH	$V_{DD} = 5.5V, V_{OH} = 12V$			50	μA
Supply current*2	I_{DD1}	V_{DD}	High speed mode (1/2 frequency dividing clock) operation $V_{DD} = 5.5V, 20MHz$ crystal oscillation ($C_1 = C_2 = 15pF$)		39	60	mA
	I_{DDS1}		$V_{DD} = 3V, 32kHz$ crystal oscillation ($C_1 = C_2 = 47pF$)		39	100	μA
	I_{DD2}		Sleep mode $V_{DD} = 5.5V, 20MHz$ crystal oscillation ($C_1 = C_2 = 15pF$)		2.1	10	mA
	I_{DDS2}		$V_{DD} = 3V, 32kHz$ crystal oscillation ($C_1 = C_2 = 47pF$)		7	30	μA
	I_{DDS3}		Stop mode $V_{DD} = 5.5V, \text{termination of } 20MHz \text{ and } 32kHz \text{ oscillation}$				10
Input capacity	C_{IN}	Other than $V_{DD}, V_{SS}, AV_{DD}, \text{ and } AV_{SS}$	Clock 1MHz 0V other than the measured pins		10	20	pF

*1 For \overline{RST} pin, specifies the input current when the pull-up resistor is selected, and specifies leakage current when non-resistor is selected.

*2 When all output pins are open.

DC Characteristics (V_{DD} = 2.7 to 3.3V)

(T_a = -20 to +75°C, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V _{OH}	PA to PD, PE2 to PE7, PF4 to PF7,	V _{DD} = 2.7V, I _{OH} = -0.12mA	2.5			V
			V _{DD} = 2.7V, I _{OH} = -0.45mA	2.1			V
Low level output voltage	V _{OL}	PH (V _{OL} only) PI1 to PI7	V _{DD} = 2.7V, I _{OL} = 1.0mA			0.25	V
			V _{DD} = 2.7V, I _{OL} = 1.4mA			0.4	V
		PJ, SO0, SCK0	V _{DD} = 2.7V, I _{OL} = 4.5mA			0.9	V
Input current	I _{IHE}	EXTAL	V _{DD} = 3.3V, V _{IH} = 3.3V	0.3		20	μA
	I _{ILE}		V _{DD} = 3.3V, V _{IL} = 0.3V	-0.3		-20	μA
	I _{IHT}	TEX	V _{DD} = 3.3V, V _{IH} = 3.3V	0.1		10	μA
	I _{ILT}		V _{DD} = 3.3V, V _{IL} = 0.3V	-0.1		-10	μA
	I _{ILR}		R _{ST} *1	-0.9		-200	μA
I/O leakage current	I _{Iz}	PA to PG, PI, PJ, MP AN0 to AN3, CS0, SI0, SO0 SCK0, R _{ST} *1	V _{DD} = 3.3V, V _I = 0, 3.3V			±10	μA
Open drain output leakage current	I _{LOH}	PH	V _{DD} = 3.3V, V _{OH} = 12V			50	μA
Supply current*2	I _{DD1}	V _{DD}	12MHz crystal oscillation (C ₁ = C ₂ = 15pF) V _{DD} = 3.0V ± 0.3V*3		13	25	mA
	I _{DDS1}		Sleep mode V _{DD} = 3.0V ± 0.3V		0.7	2.0	mA
	I _{DDS3}		Stop mode (EXTAL and TEX pins oscillation stop) V _{DD} = 3.0V ± 0.3V			10	μA
Input capacity	C _{IN}	Other than V _{DD} , V _{SS} , AV _{DD} , and AV _{SS}	Clock 1MHz 0V other than the measured pins		10	20	pF

*1 For R_{ST} pin, specifies the input current when the pull-up resistor is selected, and specifies leakage current when non-resistor is selected.

*2 When all output pins are open.

*3 When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FE_H) to "00" and operating in high-speed mode (1/2 dividing clock).

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, VDD = 2.7 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2 VDD = 4.5 to 5.5V	1	20	MHz
System clock input pulse width	tXL, tXH	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive) VDD = 4.5 to 5.5V	23	37.5	ns
System clock input rise and fall times	tCR, tCF	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive)		200	ns
Event count clock input pulse width	tEH, tEL	\overline{EC}	Fig. 3	tsys × 4*1		ns
Event count clock input rise and fall times	tER, tEF	\overline{EC}	Fig. 3		20	ns
System clock frequency	fc	TEX TX	Fig. 2 VDD = 2.5 to 5.5V (32kHz clock applied condition)	32.768		kHz
Event count clock input pulse width	tTL, tTH	TEX	Fig. 3	10		μs
Event count clock input rise and fall times	tTR, tTF	TEX	Fig. 3		20	ms

*1 tsys indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Fig. 1. Clock timing

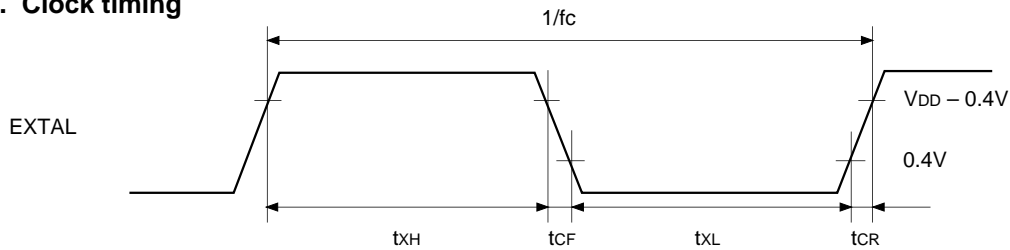


Fig. 2. Clock applied condition

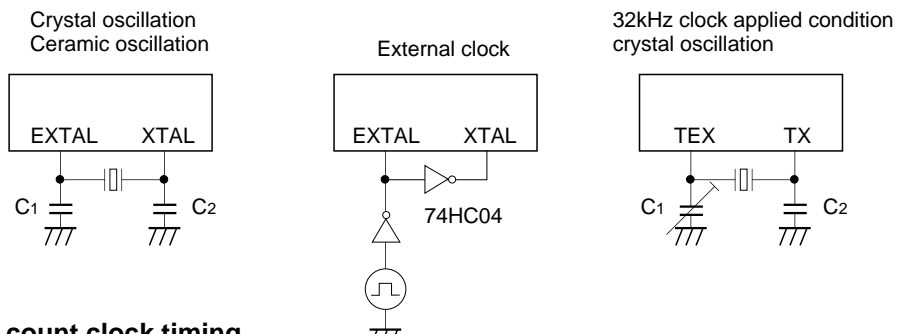
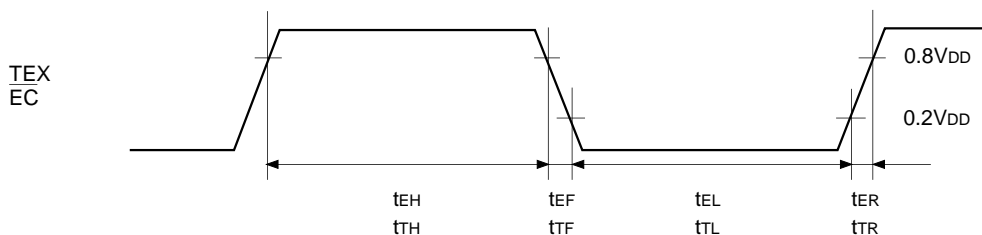


Fig. 3. Event count clock timing



(2) Serial transfer (CH0)

(Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	t _{DCSK}	$\overline{SCK0}$	Chip select transfer mode (SCK = output mode)		t _{sys} + 200	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ floating delay time	t _{DCSKF}	$\overline{SCK0}$	Chip select transfer mode (SCK = output mode)		t _{sys} + 200	ns
$\overline{CS} \downarrow \rightarrow SO$ delay time	t _{DCSO}	SO0	Chip select transfer mode		t _{sys} + 200	ns
$\overline{CS} \downarrow \rightarrow SO$ floating delay time	t _{DCSOF}	SO0	Chip select transfer mode		t _{sys} + 200	ns
\overline{CS} High level width	t _{WHCS}	$\overline{CS0}$	Chip select transfer mode	t _{sys} + 200		ns
\overline{SCK} cycle time	t _{KCY}	$\overline{SCK0}$	Input mode	2t _{sys} + 200		ns
			Output mode	16000/fc		ns
\overline{SCK} High and Low level widths	t _{KH} t _{KL}	$\overline{SCK0}$	Input mode	t _{sys} + 100		ns
			Output mode	8000/fc - 100		ns
SI input setup time (for $\overline{SCK} \uparrow$)	t _{SIK}	SI0	\overline{SCK} input mode	-t _{sys} + 100		ns
			\overline{SCK} output mode	200		ns
SI input hold time (for $\overline{SCK} \uparrow$)	t _{KSI}	SI0	\overline{SCK} input mode	2t _{sys} + 100		ns
			\overline{SCK} output mode	100		ns
$\overline{SCK} \downarrow \rightarrow SO$ delay time	t _{KSO}	SO0	\overline{SCK} input mode		2t _{sys} + 200	ns
			\overline{SCK} output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) \overline{CS} , \overline{SCK} , SI and SO represents $\overline{CS0}$, $\overline{SCK0}$, SI0 and SO0, respectively.

Note 3) The load of \overline{SCK} output mode and SO output delay time is 50pF + 1TTL.

Serial transfer (CH0)

(Ta = -20 to +75°C, V_{DD} = 2.7 to 3.3V, V_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	t _{D_{CSK}}	$\overline{SCK0}$	Chip select transfer mode (\overline{SCK} = output mode)		t _{sys} + 250	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ floating delay time	t _{D_{CSKF}}	$\overline{SCK0}$	Chip select transfer mode (\overline{SCK} = output mode)		t _{sys} + 200	ns
$\overline{CS} \downarrow \rightarrow SO$ delay time	t _{D_{CSO}}	SO0	Chip select transfer mode		t _{sys} + 250	ns
$\overline{CS} \downarrow \rightarrow SO$ floating delay time	t _{D_{CSOF}}	SO0	Chip select transfer mode		t _{sys} + 200	ns
\overline{CS} High level width	t _{WH_{CS}}	$\overline{CS0}$	Chip select transfer mode	t _{sys} + 200		ns
\overline{SCK} cycle time	t _{K_{CY}}	$\overline{SCK0}$	Input mode	2t _{sys} + 200		ns
			Output mode	16000/fc		ns
\overline{SCK} High and Low level widths	t _{K_H} t _{K_L}	$\overline{SCK0}$	Input mode	t _{sys} + 100		ns
			Output mode	8000/fc - 150		ns
SI input setup time (for $\overline{SCK} \uparrow$)	t _{SIK}	SI0	\overline{SCK} input mode	-t _{sys} + 100		ns
			\overline{SCK} output mode	200		ns
SI input hold time (for $\overline{SCK} \uparrow$)	t _{K_{SI}}	SI0	\overline{SCK} input mode	2t _{sys} + 100		ns
			\overline{SCK} output mode	100		ns
$\overline{SCK} \downarrow \rightarrow SO$ delay time	t _{K_{SO}}	SO0	\overline{SCK} input mode		2t _{sys} + 250	ns
			\overline{SCK} output mode		125	ns

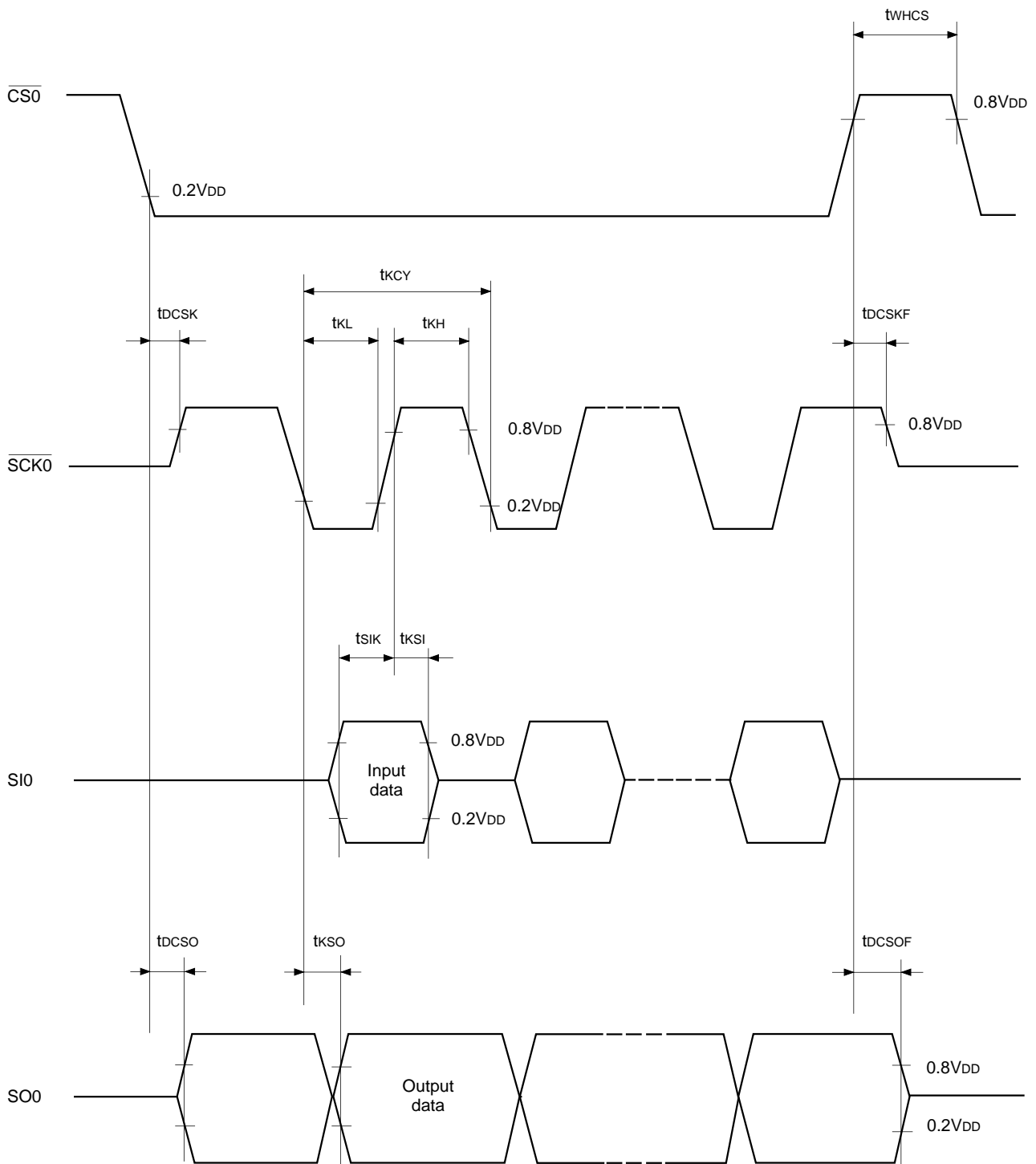
Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) \overline{CS} , \overline{SCK} , SI and SO represents $\overline{CS0}$, $\overline{SCK0}$, SI0 and SO0, respectively.

Note 3) The load of \overline{SCK} output mode and SO output delay time is 50pF.

Fig. 4. Serial transfer timing (CH0)



Serial transfer (CH1)

(Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t _{KCY}	$\overline{\text{SCK1}}$	Input mode	2t _{sys} + 200		ns
			Output mode	8000/fc		ns
$\overline{\text{SCK1}}$ High and Low level widths	t _{KH} t _{KL}	$\overline{\text{SCK1}}$	Input mode	t _{sys} + 100		ns
			Output mode	4000/fc - 100		ns
SI1 input setup time (for $\overline{\text{SCK1}}$ ↑)	t _{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (for $\overline{\text{SCK1}}$ ↑)	t _{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	t _{sys} + 200		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}}$ ↓ → SO1 delay time	t _{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		t _{sys} + 200	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

$$t_{\text{sys}} [\text{ns}] = 2000/\text{fc} \text{ (Upper 2 bits = "00")}, 4000/\text{fc} \text{ (Upper 2 bits = "01")}, 16000/\text{fc} \text{ (Upper 2 bits = "11")}$$

Note 2) The load of $\overline{\text{SCK1}}$ output mode and SO1 output delay time is 50pF + 1TTL.

Serial transfer (CH1)

(Ta = -20 to +75°C, V_{DD} = 2.7 to 3.3V, V_{SS} = 0V reference)

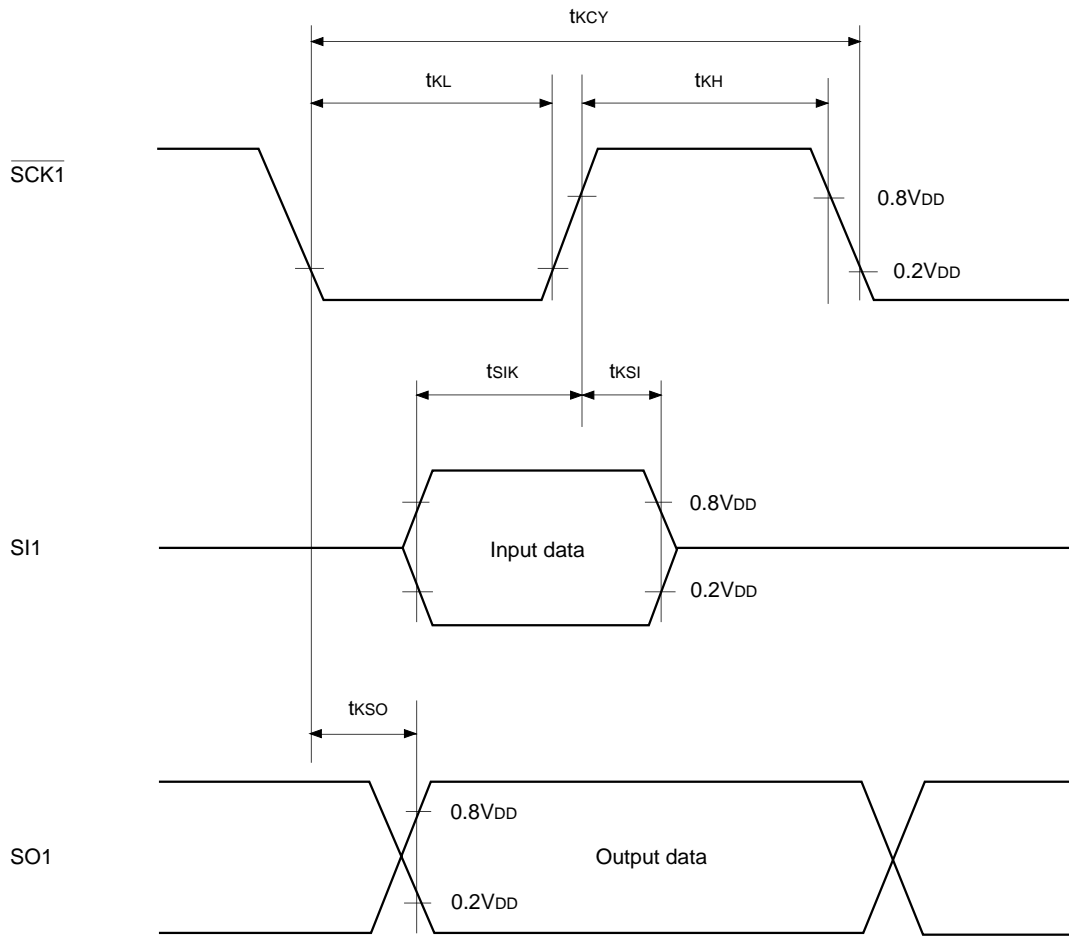
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t _{KCY}	$\overline{\text{SCK1}}$	Input mode	2t _{sys} + 200		ns
			Output mode	8000/fc		ns
$\overline{\text{SCK1}}$ High and Low level widths	t _{KH} t _{KL}	$\overline{\text{SCK1}}$	Input mode	t _{sys} + 100		ns
			Output mode	4000/fc - 150		ns
SI1 input setup time (for $\overline{\text{SCK1}}$ ↑)	t _{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (for $\overline{\text{SCK1}}$ ↑)	t _{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	t _{sys} + 200		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}}$ ↓ → SO1 delay time	t _{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		t _{sys} + 250	ns
			$\overline{\text{SCK1}}$ output mode		125	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

$$t_{\text{sys}} [\text{ns}] = 2000/\text{fc} \text{ (Upper 2 bits = "00")}, 4000/\text{fc} \text{ (Upper 2 bits = "01")}, 16000/\text{fc} \text{ (Upper 2 bits = "11")}$$

Note 2) The load of $\overline{\text{SCK1}}$ output mode and SO1 output delay time is 50pF.

Fig. 5. Serial transfer CH1 timing



(4) A/D converter characteristics

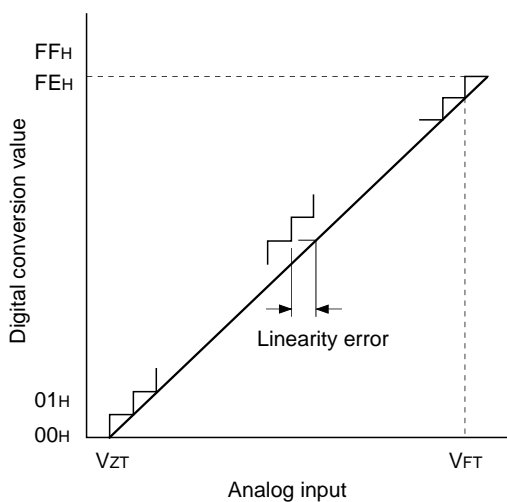
($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = AV_{DD} = 4.5$ to 5.5V , $AV_{REF} = 4.0$ to AV_{DD} , $V_{SS} = AV_{SS} = 0\text{V}$ reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			$T_a = 25^\circ\text{C}$ $V_{DD} = AV_{DD} = AV_{REF} = 5.0\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$			± 1	LSB
Absolute error						± 2	LSB
Conversion time	t_{CONV}			$160/f_{ADC}^{*1}$			μs
Sampling time	t_{SAMP}			$12/f_{ADC}^{*1}$			μs
Reference input voltage	V_{REF}	AV_{REF}	$V_{DD} = AV_{DD} = 4.5$ to 5.5V	$AV_{DD} - 0.5$		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN11		0			V
AV_{REF} current	I_{REF}	AV_{REF}	Operating mode		0.6	1.0	mA
	I_{REFS}		Sleep mode Stop mode 32kHz operating mode			10	μA

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = AV_{DD} = 2.7$ to 3.3V , $AV_{REF} = 2.7$ to AV_{DD} , $V_{SS} = AV_{SS} = 0\text{V}$ reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			$T_a = 25^\circ\text{C}$ $V_{DD} = AV_{DD} = AV_{REF} = 3.0\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$			± 1	LSB
Absolute error						± 2	LSB
Conversion time	t_{CONV}			$160/f_{ADC}^{*1}$			μs
Sampling time	t_{SAMP}			$12/f_{ADC}^{*1}$			μs
Reference input voltage	V_{REF}	AV_{REF}	$V_{DD} = AV_{DD} = 2.7$ to 3.3V	$AV_{DD} - 0.3$		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN11		0			V
AV_{REF} current	I_{REF}	AV_{REF}	Operating mode		0.3	0.7	mA
	I_{REFS}		Sleep mode Stop mode 32kHz operating mode			10	μA

Fig. 6. Definitions of A/D converter terms



*1 The value of f_{ADC} is as follows by selecting ADC operation clock (MSC: Address 01FFH bit 0).
When PS2 is selected, $f_{ADC} = f_c/2$
When PS1 is selected, $f_{ADC} = f_c$

(4) Interruption, reset input (Ta = -20 to +75°C, VDD = 2.7 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
External interruption High and Low level widths	t _{IH} t _{IL}	$\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$ $\overline{\text{NMI}}$ PJ0 to PJ7		1		μs
Reset input Low level width	t _{RSL}	$\overline{\text{RST}}$		32/fc		μs

Fig. 7. Interruption input timing

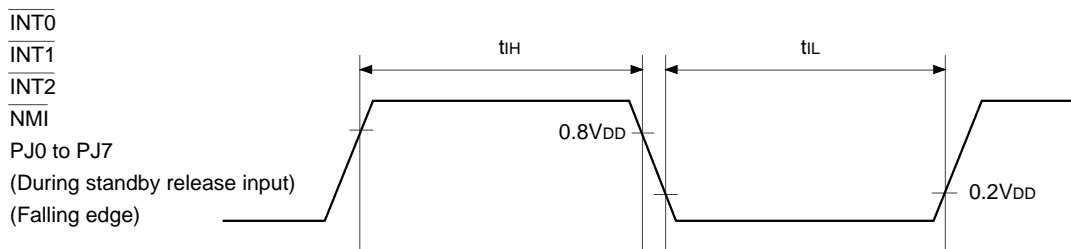
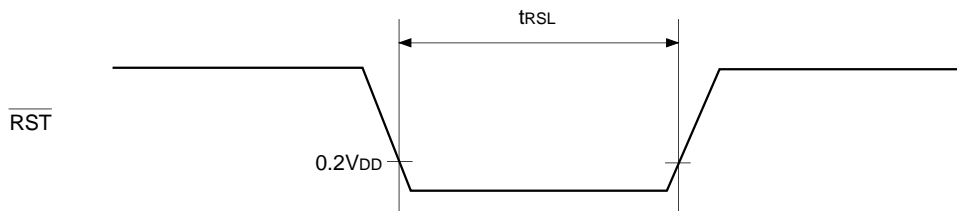


Fig. 8. Reset input timing



(5) Others

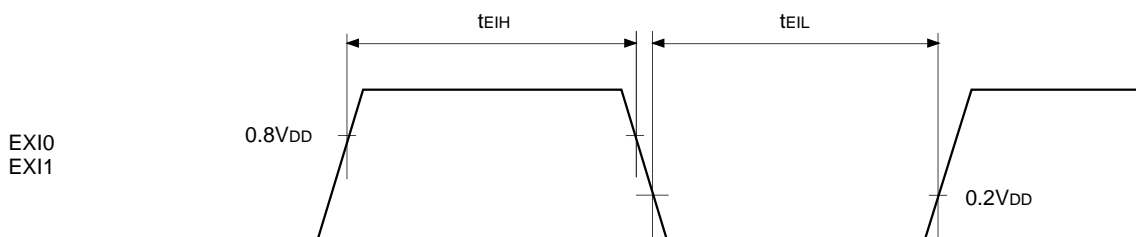
(Ta = -20 to +75°C, VDD = 2.7 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
EXI input High and Low level widths	t _{EIH} t _{EIL}	EXI0 EXI1	t _{sys} = 2000/fc	t _{FRC} × 8 + 200 + t _{sys}		ns

Note) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

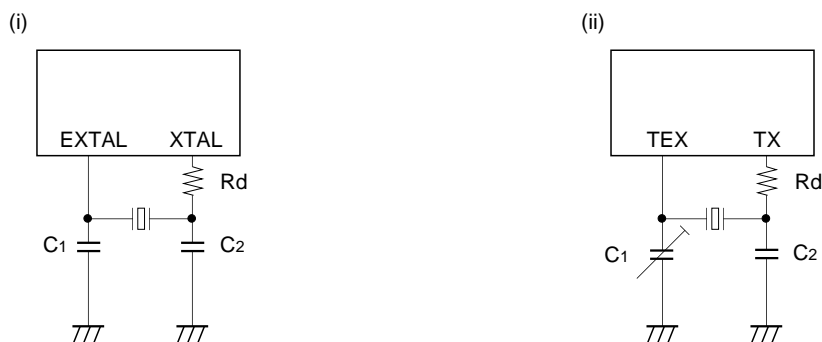
t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")
t_{FRC} = 1000/fc [ns]

Fig. 9. Other timings



Appendix

Fig. 10. Recommended oscillation circuit



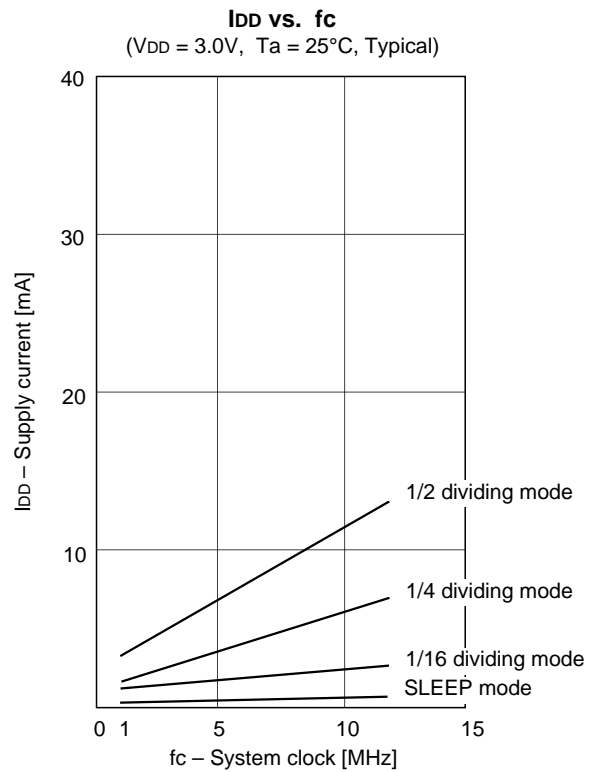
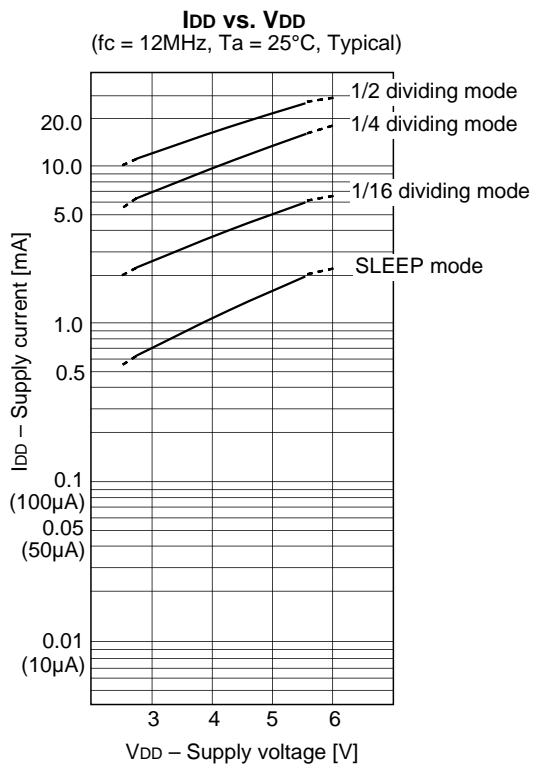
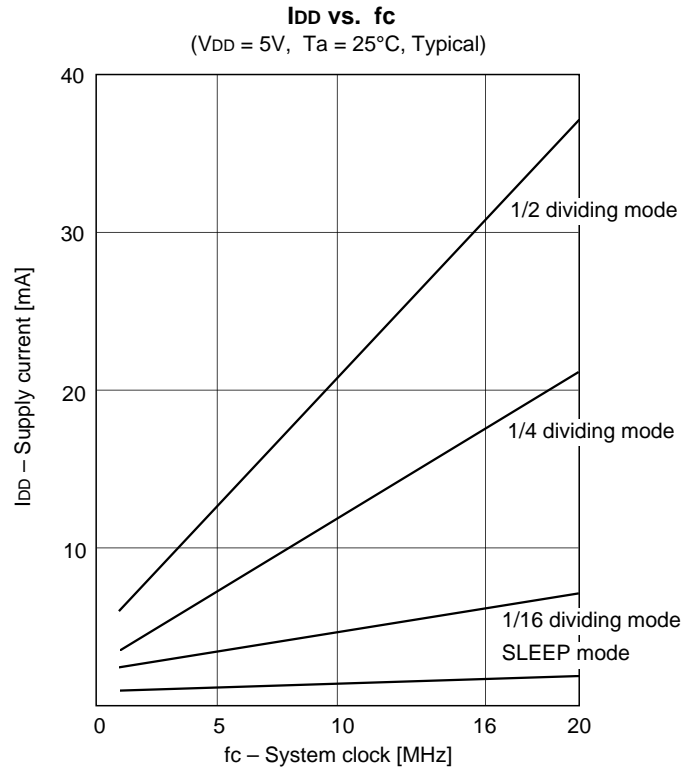
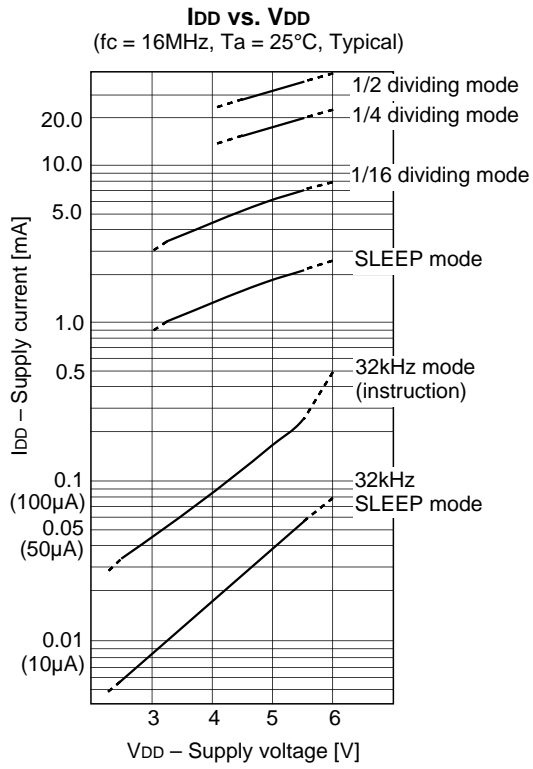
Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00	5	5		
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16 (12)	16 (12)	0	(i)
		10.00	16 (12)	16 (12)		
		12.00	12	12		
		16.00	12	12		
	P3	32.768kHz	30	18	470K	(ii)
NIHON DENPA KOGYO CO., LTD	AT-51	20.00	2*1	2*1	0*1	(i)

*1 Typical

Mask option table

Item	Content	
Reset pin pull-up resistor	Non-existent	Existent

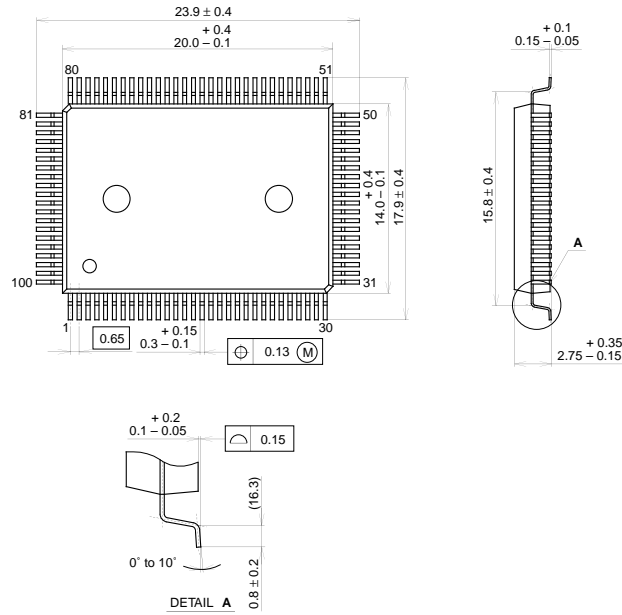
Characteristics Curve



Package Outline

Unit: mm

100PIN QFP (PLASTIC)

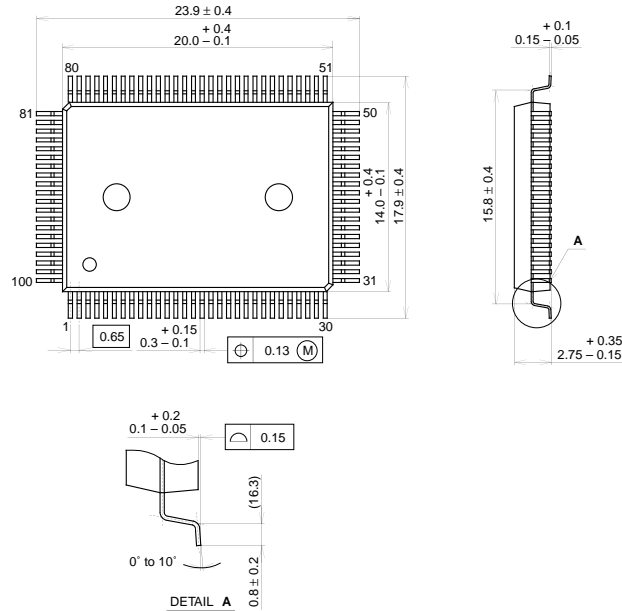


SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

100PIN QFP (PLASTIC)



SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

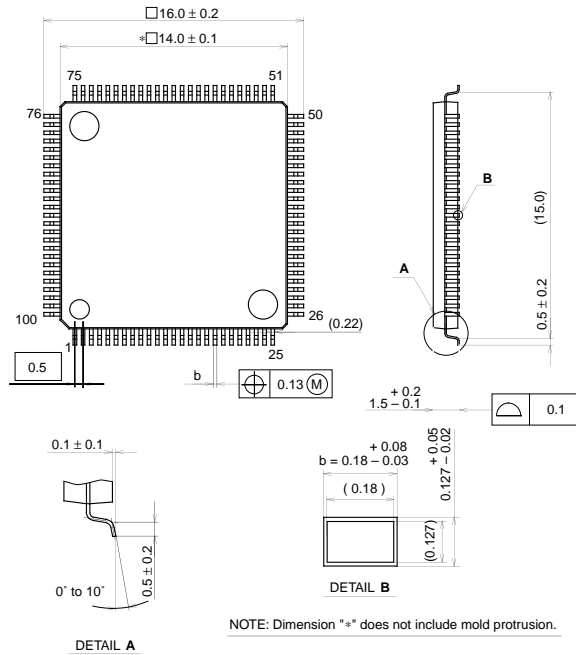
LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18µm

Package Outline

Unit: mm

100PIN LQFP (PLASTIC)

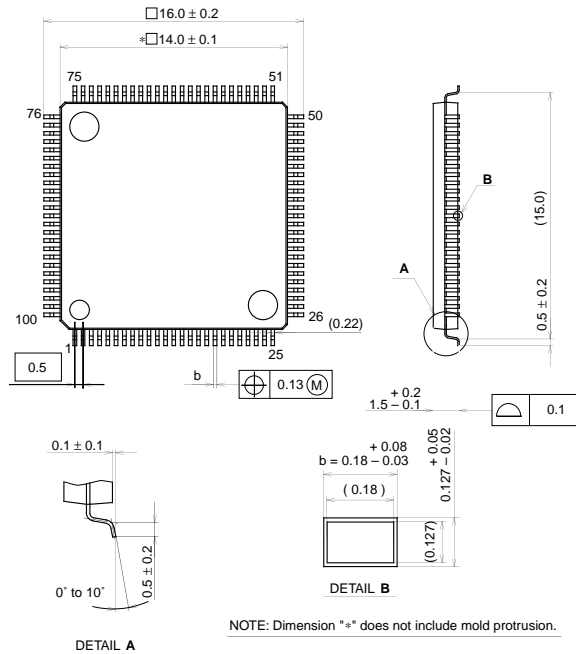


PACKAGE STRUCTURE

SONY CODE	LQFP-100P-L01
EIAJ CODE	P-LQFP100-14x14-0.5
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.7g

100PIN LQFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	LQFP-100P-L01
EIAJ CODE	P-LQFP100-14x14-0.5
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.7g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18 μ m



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