

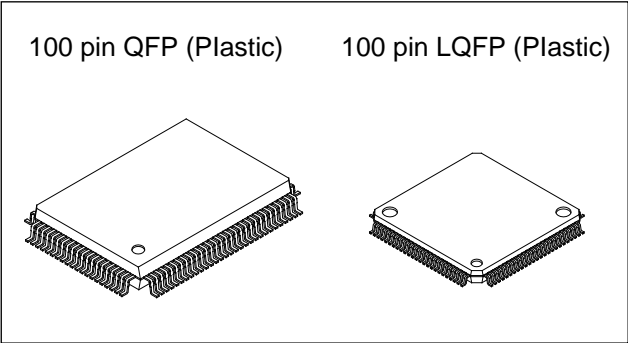
CXP81720B/81724B

CMOS 8-bit Single Chip Microcomputer

Description

The CXP81720B/81724B is a CMOS 8-bit micro-computer which consists of A/D converter, serial interface, timer/counter, time-base timer, high-precision timing pattern generation circuit, PWM output, 32kHz timer/counter, remote control reception circuit, as well as basic configurations like 8-bit CPU, ROM, RAM and I/O port. They are integrated into a single chip.

Also CXP81720B/81724B provides sleep/stop functions which enables to lower power consumption.

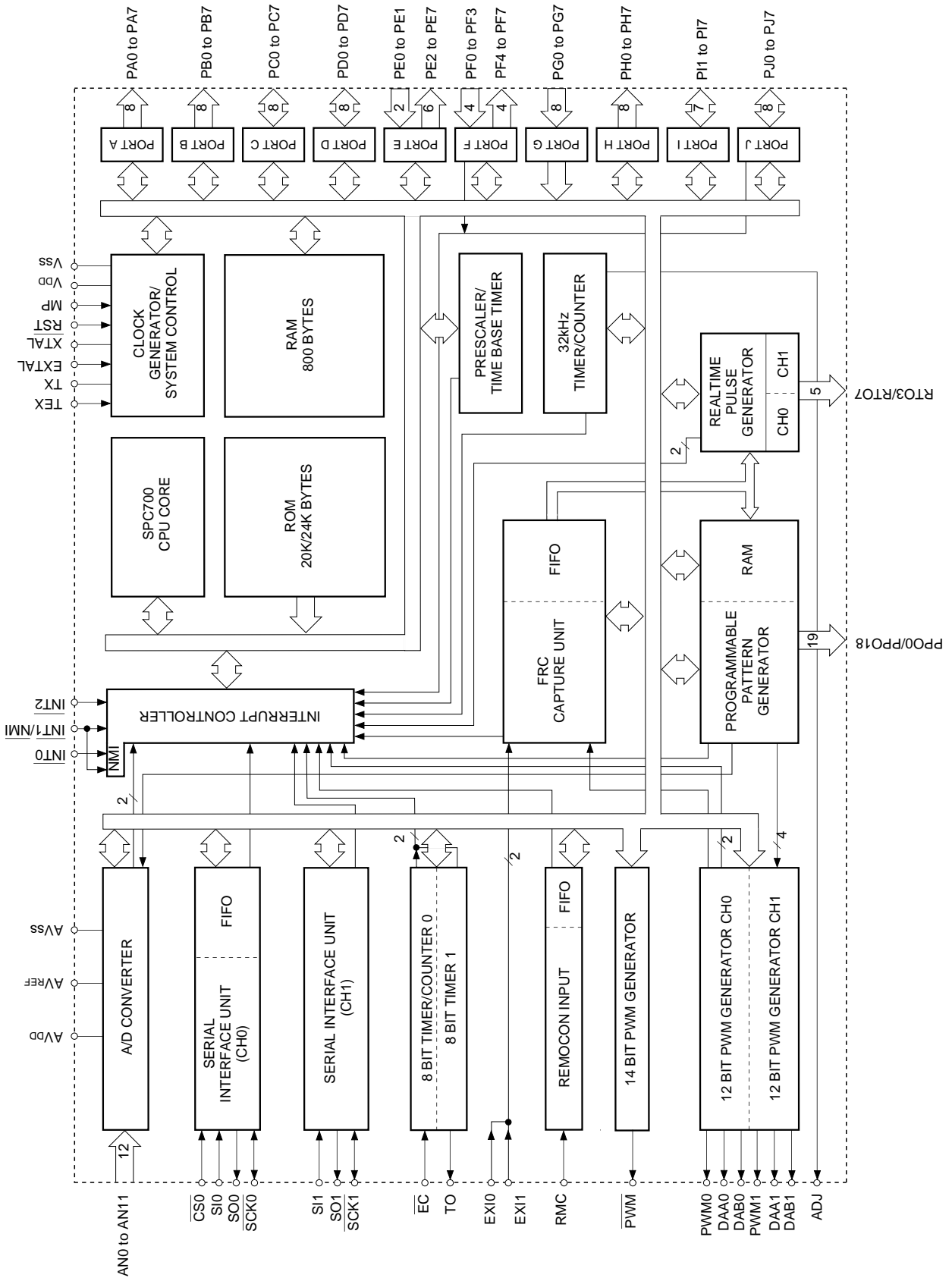


Structure
Silicon gate CMOS IC

Features

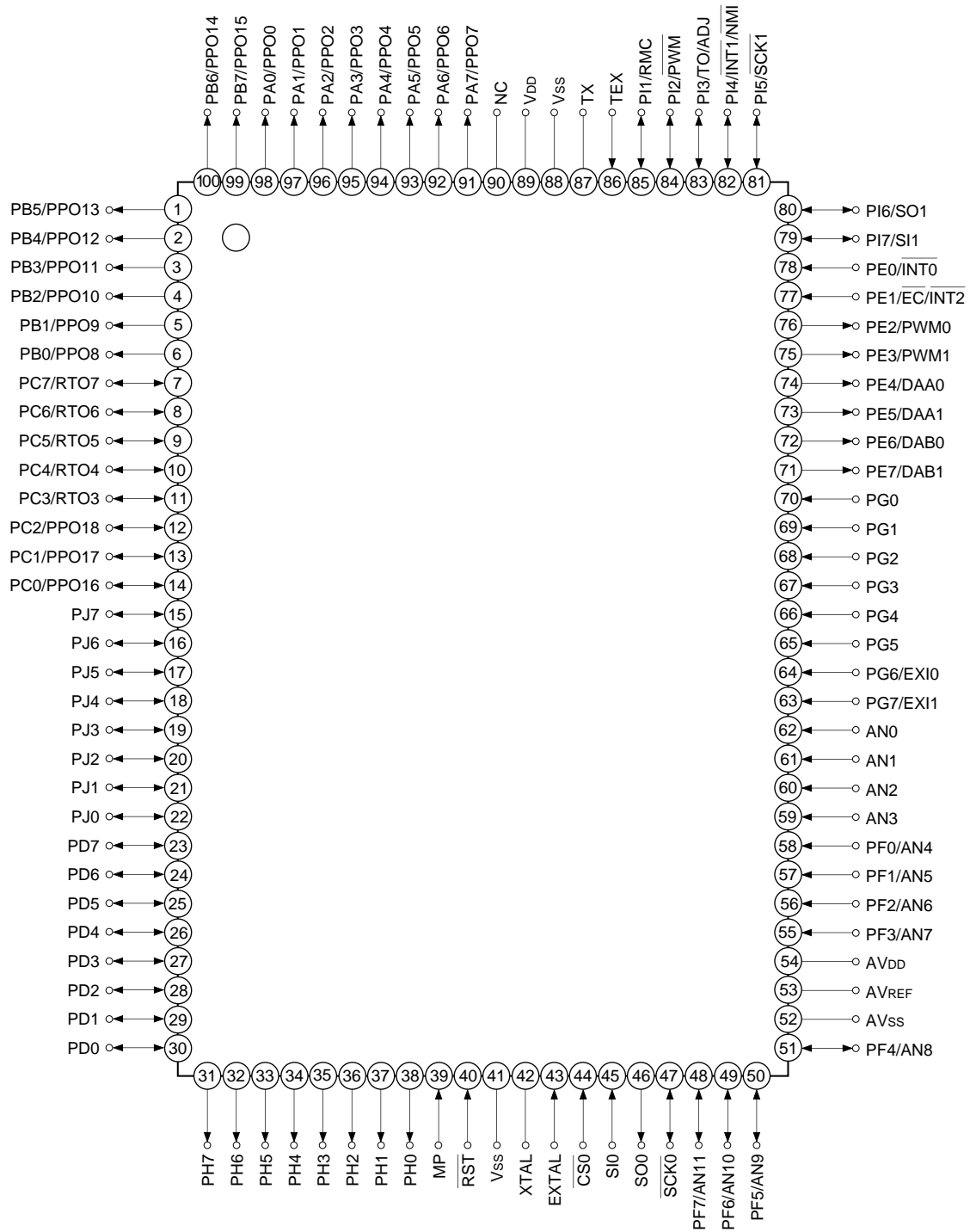
- A wide instruction set (213 instructions) which covers various types of data
 - 16-bit arithmetic/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle
 - 250ns at 16MHz operation (4.5 to 5.5V)
 - 122µs at 32kHz operation (2.7 to 5.5V)
- Incorporated ROM capacity
 - 20K bytes (CXP81720B)
 - 24K bytes (CXP81724B)
- Incorporated RAM capacity
 - 800 bytes
- Peripheral functions
 - A/D converter
 - 8 bits, 12 channels, successive approximation method (Conversion time of 20.0µs at 16MHz)
 - Serial interface
 - Incorporated 8-bit and 8-stage FIFO, 1 channel (Auto transfer for 1 to 8 bytes)
 - 8-bit clock sync type, 1 channel
 - Timer
 - 8-bit timer, 8-bit timer/counter, 19-bit time-base timer
 - 32kHz timer/counter
 - High-precision timing pattern generator
 - PPG: maximum of 19 pins, 32 stages programmable
 - RTG: 5 pins, 2 channels
 - PWM/DA gate output
 - PWM: 12 bits, 2 channels (Repetitive frequency 62kHz/16MHz)
 - DA gate pulse output: 12 bits, 4 channels
 - FRC capture unit
 - Incorporated 26-bit and 8-stage FIFO
 - PWM output
 - 14 bits, 1 channel
 - Remote control reception circuit
 - 8-bit pulse measuring counter, 6-stage FIFO
- Interruption
 - 20 factors, 15 vectors, multi-interruption possible
- Standby mode
 - Sleep/stop
- Package
 - 100-pin plastic QFP/LQFP
- Piggyback/evaluator
 - CXP81800

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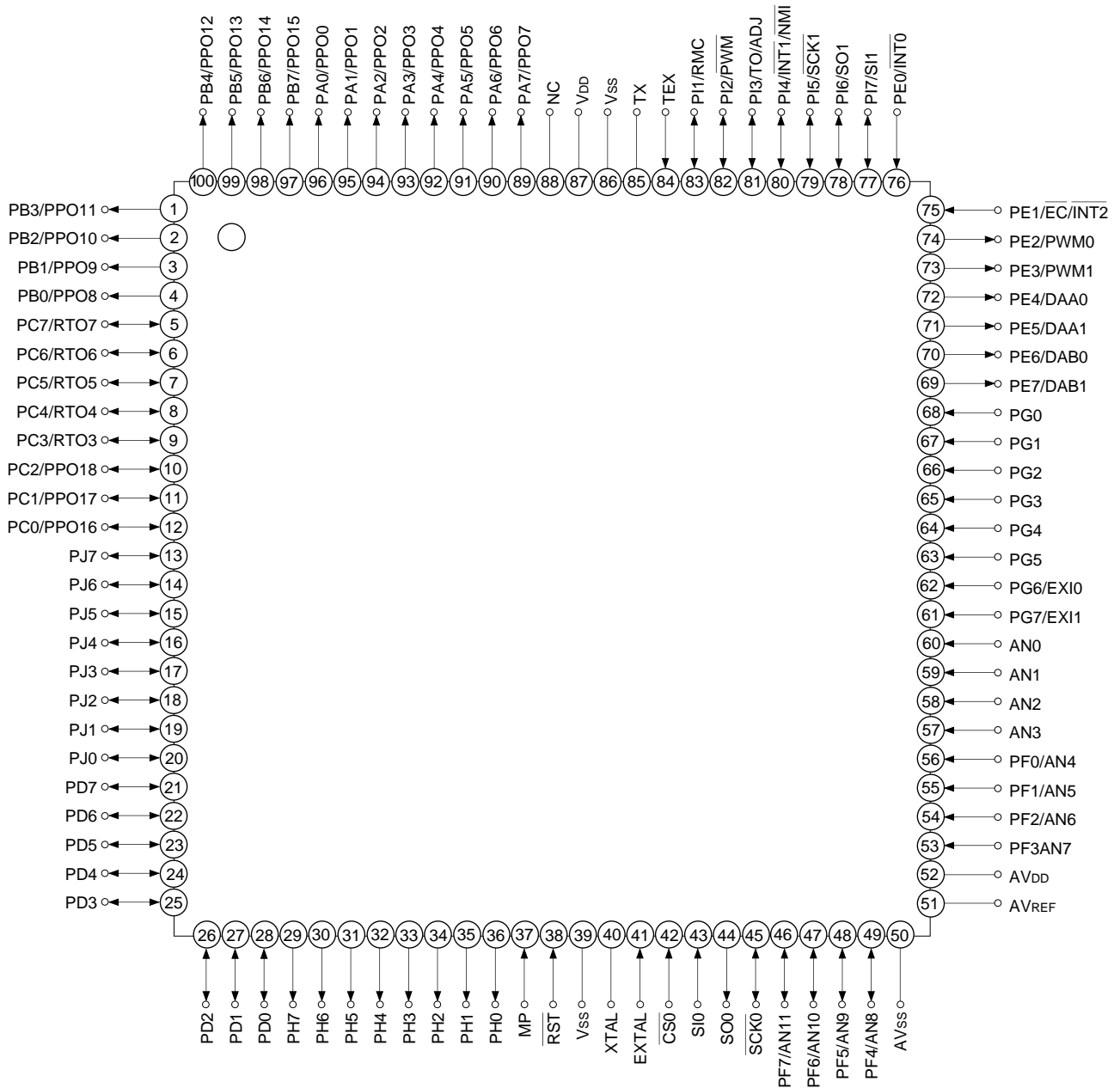
Block Diagram

Pin Assignment (Top View) 100-pin QFP package



- Note)** 1. NC (Pin 90) is always connected to V_{DD}.
 2. V_{SS} (Pins 41 and 88) are both connected to GND.

Pin Assignment (Top View) 100-pin LQFP package



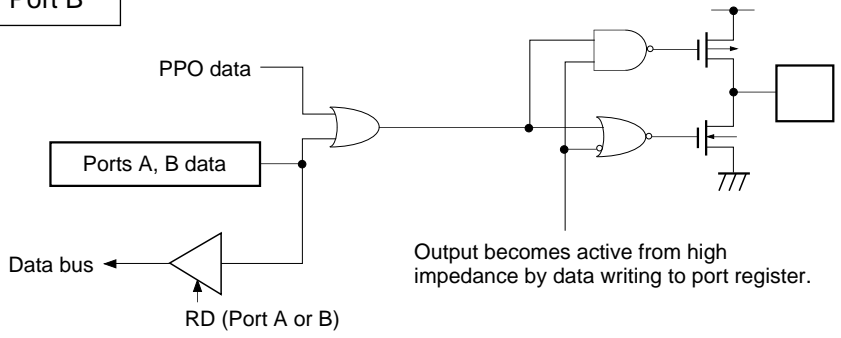
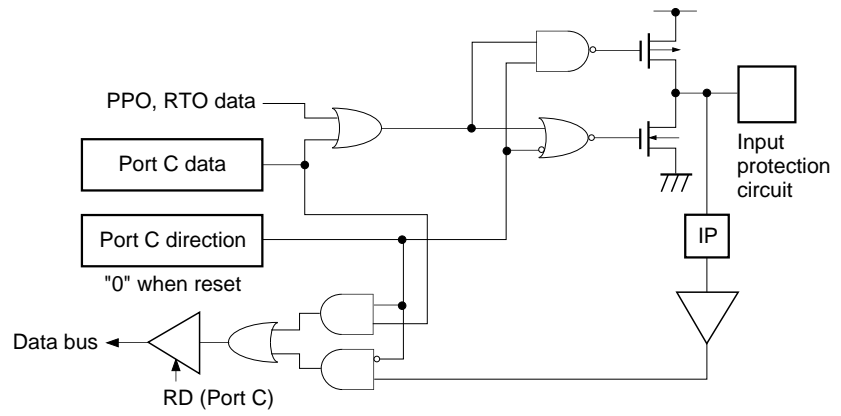
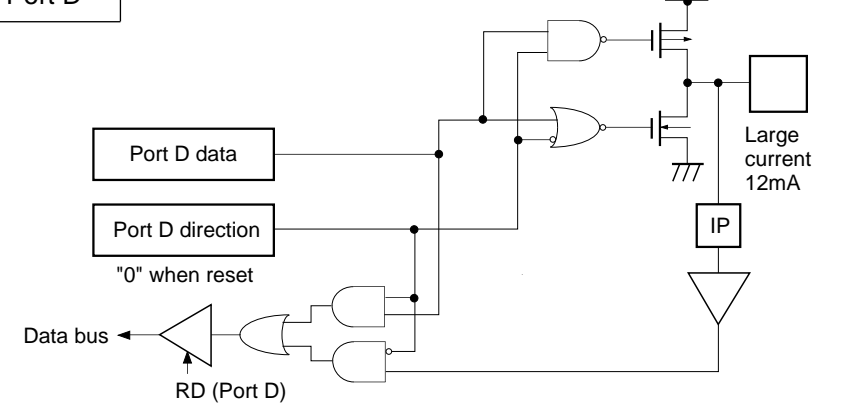
- Note**
1. NC (Pin 88) is always connected to VDD.
 2. Vss (Pins 39 and 86) are both connected to GND.

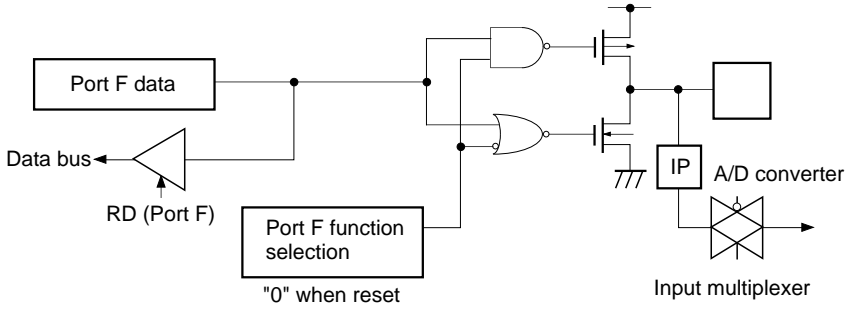
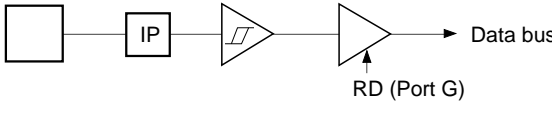
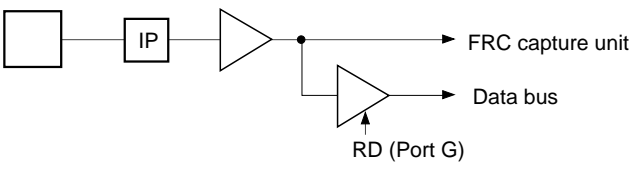
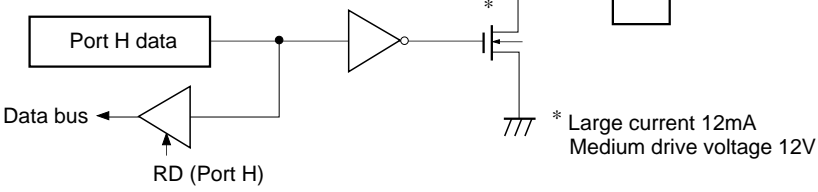
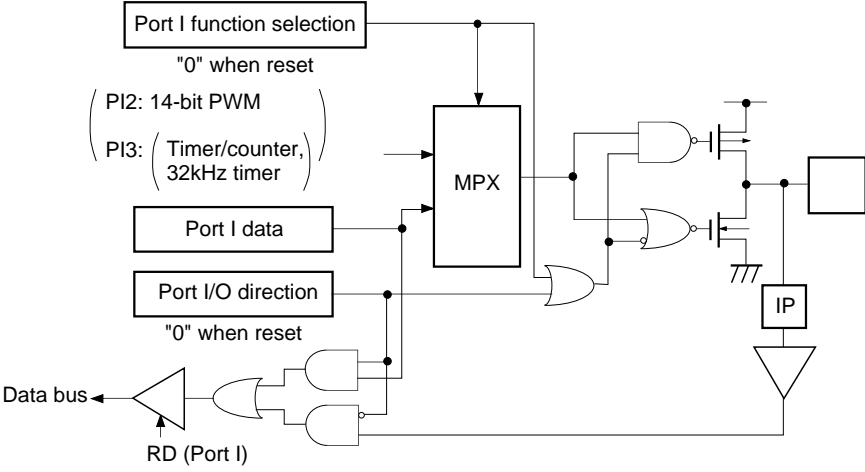
Pin Description

Symbol	I/O	Description		
PA0/PPO0 to PA7/PPO7	Output/ Real time output	(Port A) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	Programmable pattern generator (PPG) output. Functions as high-precision real-time pulse output port. (19 pins)	
PB0/PPO8 to PB7/PPO15	Output/ Real time output	(Port B) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)		
PC0/PPO16 to PC2/PPO18	I/O/ Real time output	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Data is gated with PPO or RTO contents by OR-gate and they are output. (8 pins)		
PC3/RTO3 to PC7/RTO7	I/O/ Real time output		Real-time pulse generator (RTG) output. Functions as high-precision real-time pulse output port. (5 pins)	
PD0 to PD7	I/O	(Port D) 8-bit I/O port. I/O can be set in a unit of 4 bits. Can drive 12mA sink current. (8 pins)		
PE0/ $\overline{\text{INT0}}$	Input/input	(Port E) 8-bit port. Lower 2 bits are for input; upper 6 bits are for output. (8 pins)	Input to request external interruption. Active at the falling edge.	
PE1/ $\overline{\text{EC}}/\overline{\text{INT2}}$	Input/input/input		External event input for timer/counter.	Input to request external interruption. Active at the falling edge.
PE2/PWM0	Output/output		PWM outputs. (2 pins)	
PE3/PWM1	Output/output			
PE4/DAA0	Output/output			DA gate pulse outputs. (4 pins)
PE5/DAA1	Output/output			
PE6/DAB0	Output/output			
PE7/DAB1	Output/output			
AN0 to AN3	Input	Analog inputs to A/D converter. (12 pins)		
PF0/AN4 to PF3/AN7	Input/input	(Port F) 8-bit port. Lower 4 bits are for input; upper 4 bits are for output.		
PF4/AN8 to PF7/AN11	Output/input	Lower 4 bits also serve as standby release input pin. (8 pins)		
$\overline{\text{SCK0}}$	I/O	Serial clock I/O (CH0).		
SO0	Output	Serial data output (CH0).		
SI0	Input	Serial data input (CH0).		
$\overline{\text{CS0}}$	Input	Serial chip select input (CH0).		

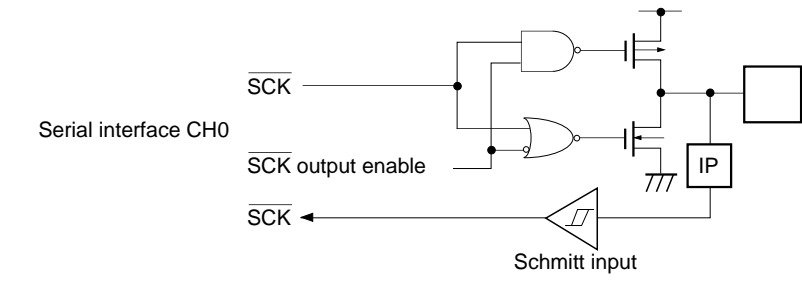
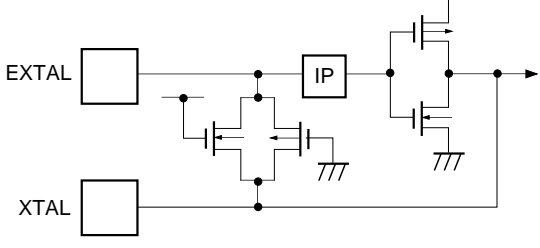
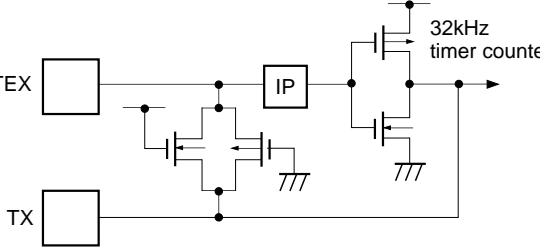
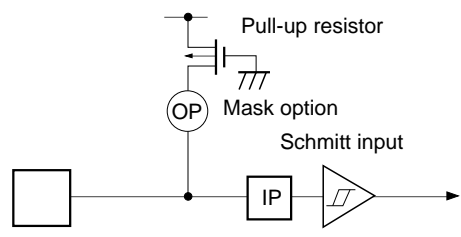
Symbol	I/O	Description	
PG0 to PG5	Input	(Port G)	
PG6/EXI0	Input/input	8-bit input port. (8 pins)	External input to FRC capture unit. (2 pins)
PG7/EXI1	Input/input		
PH0 to PH7	Output	(Port H) N-ch open drain output of medium drive voltage (12V) and large current (12mA). (8 pins)	
PI1/RMC	I/O/input	(Port I) 7-bit I/O port. I/O port can be set in a unit of single bits. (7 pins)	Remote control reception circuit input.
PI2/PWM	I/O/output		14-bit PWM output.
PI3/TO/ADJ	I/O/output/output		Timer/counter, 32kHz oscillation adjustment output.
PI4/INT1/ NMI	I/O/input/input		Input to request external interruption and non maskable interruption. Active at the falling edge.
PI5/SCK1	I/O/I/O		Serial clock I/O (CH1).
PI6/SO1	I/O/output		Serial data output (CH1).
PI7/SI1	I/O/input		Serial data input (CH1).
PJ0 to PJ7	I/O	(Port J) 8-bit I/O port. I/O and standby release input function can be set in a unit of single bits.	
EXTAL	Input	Connects a crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and input opposite phase clock to XTAL pin.	
XTAL	Output		
TEX	Input	Connects a crystal oscillator for 32kHz timer/counter clock. When used as event counter, input to TEX pin and leave TX pin open.	
TX	Output		
RST	Input	System reset; active at Low level.	
MP	Input	Test mode pin. Always connect to GND.	
AVDD		Positive power supply of A/D converter.	
AVREF	Input	Reference voltage input of A/D converter.	
AVSS		GND of A/D converter.	
VDD		Positive power supply.	
VSS		GND. Connect both Vss pins to GND.	

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
<p>Port A Port B</p> <p>PA0/PPO0 to PA7/PPO7 PB0/PPO8 to PB7/PPO15</p> <p>16 pins</p>		<p>Hi-Z</p>
<p>Port C</p> <p>PC0/PPO16 to PC2/PPO18 PC3/RTO3 to PC7/RTO7</p> <p>8 pins</p>		<p>Hi-Z</p>
<p>Port D</p> <p>PD0 to PD7</p> <p>8 pins</p>		<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PF4/AN8 to PF7/AN11</p> <p>4 pins</p>	<p>Port F</p>  <p>Port F data</p> <p>Data bus</p> <p>RD (Port F)</p> <p>Port F function selection "0" when reset</p> <p>Input multiplexer</p> <p>IP</p> <p>A/D converter</p>	<p>Hi-Z</p>
<p>PG0 to PG5</p> <p>6 pins</p>	<p>Port G</p>  <p>Schmitt input</p> <p>Data bus</p> <p>RD (Port G)</p> <p>Note) For PG4 and PG5, CMOS Schmitt input or TTL Schmitt input can be selected with the mask option.</p>	<p>Hi-Z</p>
<p>PG6/EXI0 PG7/EXI1</p> <p>2 pins</p>	<p>Port G</p>  <p>FRC capture unit</p> <p>Data bus</p> <p>RD (Port G)</p>	<p>Hi-Z</p>
<p>PH0 to PH7</p> <p>8 pins</p>	<p>Port H</p>  <p>Port H data</p> <p>Data bus</p> <p>RD (Port H)</p> <p>* Large current 12mA Medium drive voltage 12V</p>	<p>Hi-Z</p>
<p>PI2/PWM PI3/TO/ADJ</p> <p>2 pins</p>	<p>Port I</p>  <p>Port I function selection "0" when reset (PI2: 14-bit PWM PI3: (Timer/counter, 32kHz timer))</p> <p>Port I data</p> <p>Port I/O direction "0" when reset</p> <p>MPX</p> <p>Data bus</p> <p>RD (Port I)</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PI1/RMC PI4/INT1/NMI PI7/SI1</p> <p>3 pins</p>	<p>Port I</p> <p>Port I data</p> <p>Port I direction "0" when reset</p> <p>Data bus</p> <p>RD (Port I)</p> <p>Schmitt input</p> <p>IP</p> <p>(PI1: Remote control circuit PI4: Interruption circuit PI7: Serial interface CH1)</p>	<p>Hi-Z</p>
<p>PI5/SCK1 PI6/SO1</p> <p>2 pins</p>	<p>Port I</p> <p>Port I function selection</p> <p>Serial interface CH1</p> <p>Port I data</p> <p>Port I direction "0" when reset</p> <p>Data bus</p> <p>RD (Port I)</p> <p>MPX</p> <p>MPX</p> <p>Serial interface CH1</p> <p>IP</p> <p>PI6 is not Schmitt input</p>	<p>Hi-Z</p>
<p>PJ0 to PJ7</p> <p>8 pins</p>	<p>Port J</p> <p>Port J data</p> <p>Port J direction "0" when reset</p> <p>Data bus</p> <p>RD (Port J)</p> <p>Edge detection</p> <p>Standby release</p> <p>IP</p>	<p>Hi-Z</p>
<p>CS0 SI0</p> <p>2 pins</p>	<p>Schmitt input</p> <p>CS SI</p> <p>Serial interface CH0</p>	<p>Hi-Z</p>
<p>SO0</p> <p>1 pin</p>	<p>Serial interface CH0</p> <p>SO</p> <p>SO output enable</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>$\overline{\text{SCK0}}$</p> <p>1 pin</p>	<p>Serial interface CH0</p>  <p>SCK</p> <p>SCK output enable</p> <p>SCK</p> <p>Schmitt input</p>	<p>Hi-Z</p>
<p>EXTAL XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Diagram shows the circuit composition during oscillation. • Feedback resistor is removed during stop mode. XTAL becomes High level. 	<p>Oscillation</p>
<p>TEX TX</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Diagram shows the circuit composition during oscillation. • Feedback resistor is removed during oscillation circuit stop by software. At this time TEX pin outputs Low level and TX pin outputs High level. 	<p>Oscillation</p>
<p>$\overline{\text{RST}}$</p> <p>1 pin</p>	 <p>Pull-up resistor</p> <p>Mask option</p> <p>Schmitt input</p>	<p>L level</p>

Absolute Maximum Ratings

(V_{SS} = 0V)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	−0.3 to +7.0	V	
	AV _{DD}	AV _{SS} to +7.0* ¹	V	
	AV _{SS}	−0.3 to +0.3	V	
Input voltage	V _{IN}	−0.3 to +7.0* ²	V	
Output voltage	V _{OUT}	−0.3 to +7.0* ²	V	
Medium drive output voltage	V _{OUTP}	−0.3 to +15.0	V	Port H pin
High level output current	I _{OH}	−5	mA	
High level total output current	∑I _{OH}	−50	mA	Total of all output pins
Low level output current	I _{OL}	15	mA	Ports excluding large current outputs
	I _{OLC}	20	mA	Large current outputs* ³
Low level total output current	∑I _{OL}	130	mA	Total of all output pins
Operating temperature	T _{opr}	−20 to +75	°C	
Storage temperature	T _{stg}	−55 to +150	°C	
Allowable power dissipation	P _D	600	mW	QFP package type
		380		LQFP package type

*¹ AV_{DD} and V_{DD} should be set to the same voltage.

*² V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*³ The large current drive transistors are the N-CH transistors of the PD and PH ports.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS}=0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	4.5	5.5	V	Guaranteed operation range for 1/2 and 1/4 frequency dividing clocks
		3.5	5.5		Guaranteed operation range for 1/16 frequency dividing clock and sleep mode
		2.7	5.5		Guaranteed operation range by TEX clock
		2.5	5.5		Guaranteed data hold range during stop mode
Analog voltage	AV _{DD}	4.5	5.5	V	*1
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*2
	V _{IHS}	0.8V _{DD}	V _{DD}	V	CMOS Schmitt input*3
	V _{IHTS}	2.2	V _{DD}	V	TTL Schmitt input*4
	V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL pin*5 TEX pin*6
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	*2
	V _{ILS}	0	0.2V _{DD}	V	CMOS Schmitt input*3
	V _{ILTS}	0	0.8	V	TTL Schmitt input*4
	V _{ILEX}	-0.3	0.4	V	EXTAL pin*5 TEX pin*6
Operating temperature	Topr	-20	+75	°C	

*1 AV_{DD} and V_{DD} should be set to the same voltage.

*2 Normal input port (PC, PD, PE0, PE1, PF0 to PF3, PG, PI and PJ pins), MP pin.

*3 $\overline{CS0}$, SI0, $\overline{SCK0}$, \overline{RST} , $\overline{INT0}$, $\overline{EC/INT2}$, PG (For PG4 and PG5, when CMOS Schmitt input is selected with mask option), RMC, $\overline{INT1/NMI}$, $\overline{SCK1}$ and SI1 pins.

*4 PG4 and PG5 pins (When TTL Schmitt input is selected with mask option)

*5 Specifies only when the external clock is input.

*6 Specifies only when the event count clock is input.

Electrical Characteristics

DC Characteristics ($V_{DD} = 4.5$ to $5.5V$)

($T_a = -20$ to $+75^\circ C$, $V_{SS} = 0V$)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit	
High level output voltage	V_{OH}	PA to PD, PE2 to PE7, PF4 to PF7, PH (VOL only)	$V_{DD} = 4.5V, I_{OH} = -0.5mA$	4.0			V	
			$V_{DD} = 4.5V, I_{OH} = -1.2mA$	3.5			V	
Low level output voltage	V_{OL}	PI1 to PI7 PJ, SO0, SCK0	$V_{DD} = 4.5V, I_{OL} = 1.8mA$			0.4	V	
			$V_{DD} = 4.5V, I_{OL} = 3.6mA$			0.6	V	
		PD, PH	$V_{DD} = 4.5V, I_{OL} = 12.0mA$			1.5	V	
Input current	I_{IHE}	EXTAL	$V_{DD} = 5.5V, V_{IH} = 5.5V$	0.5		40	μA	
	I_{ILE}		$V_{DD} = 5.5V, V_{IL} = 0.4V$	-0.5		-40	μA	
	I_{IHT}	TEX	$V_{DD} = 5.5V, V_{IH} = 5.5V$	0.1		10	μA	
	I_{ILT}		$V_{DD} = 5.5V, V_{IL} = 0.4V$	-0.1		-10	μA	
	I_{ILR}		\overline{RST}^{*1}	$V_{DD} = 5.5V, V_{IL} = 0.4V$	-1.5		-400	μA
I/O leakage current	I_{IZ}	PA to PG, PI, PJ, MP, AN0 to AN3, CS0, SI0, SO0, SCK0, \overline{RST}^{*1}	$V_{DD} = 5.5V, V_I = 0, 5.5V$			± 10	μA	
Open drain output leakage current (in N-ch Tr OFF state)	I_{LOH}	PH	$V_{DD} = 5.5V, V_{OH} = 12V$			50	μA	
Supply current*2	I_{DD1}	V_{DD}	1/2 frequency dividing clock operation $V_{DD} = 5.5V, 16MHz$ crystal oscillation ($C_1 = C_2 = 15pF$)		22	45	mA	
	I_{DDS1}		$V_{DD} = 3V, 32kHz$ crystal oscillation and termination of 16MHz crystal oscillation ($C_1 = C_2 = 47pF$)		35	100	μA	
	I_{DD2}		Sleep mode $V_{DD} = 5.5V, 16MHz$ crystal oscillation ($C_1 = C_2 = 15pF$)		1.1	8	mA	
	I_{DDS2}		$V_{DD} = 3V, 32kHz$ crystal oscillation, termination of 16MHz crystal oscillation ($C_1 = C_2 = 47pF$)		9	30	μA	
	I_{DDS3}		Stop mode $V_{DD} = 5.5V$, termination of 16MHz and 32kHz crystal oscillation				10	μA
	Input capacity		C_{IN}	Other than V_{DD}, V_{SS}, AV_{DD} , and AV_{SS}	Clock 1MHz 0V for no-measured pins		10	20

*1 \overline{RST} pin specifies the input current when the pull-up resistor is selected, and specifies leakage current when non-resistor is selected.

*2 When entire output pins are open.

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	1	16	MHz
System clock input pulse width	t _{XL} , t _{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	28		ns
System clock input rise and fall times	t _{CR} , t _{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive		200	ns
Event count input clock pulse width	t _{EH} , t _{EL}	\overline{EC}	Fig. 3	4t _{sys} *1		ns
Event count input clock rise and fall times	t _{ER} , t _{EF}	\overline{EC}	Fig. 3		20	ns
System clock frequency	fc	TEX TX	Fig. 2 V _{DD} = 2.7 to 5.5V (32kHz clock applied condition)	32.768		kHz
Event count input clock pulse width	t _{TL} , t _{TH}	TEX	Fig. 3	10		μs
Event count input clock rise and fall times	t _{TR} , t _{TF}	TEX	Fig. 3		20	ms

*1 t_{sys} indicates three values according to the contents of the clock control register (CLC: 00FE_h) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Fig. 1. Clock timing

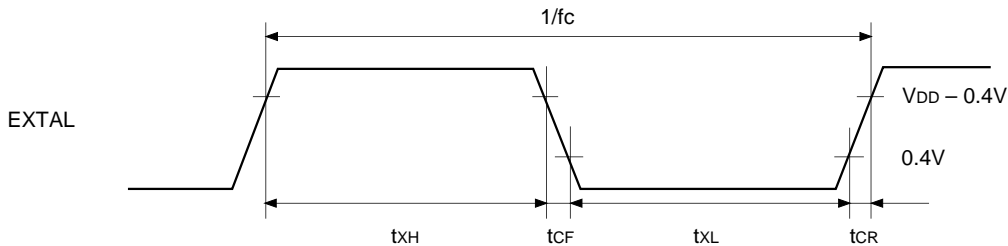


Fig. 2. Clock applied condition

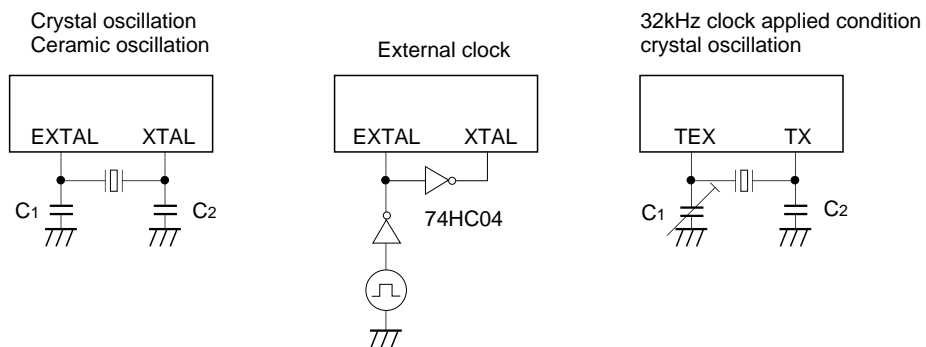
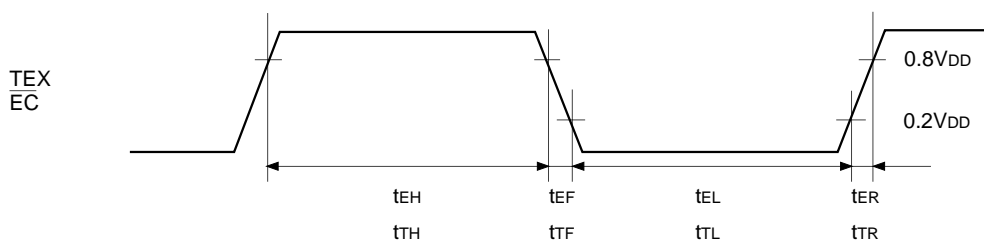


Fig. 3. Event count clock timing



(2) Serial transfer (CH0)

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

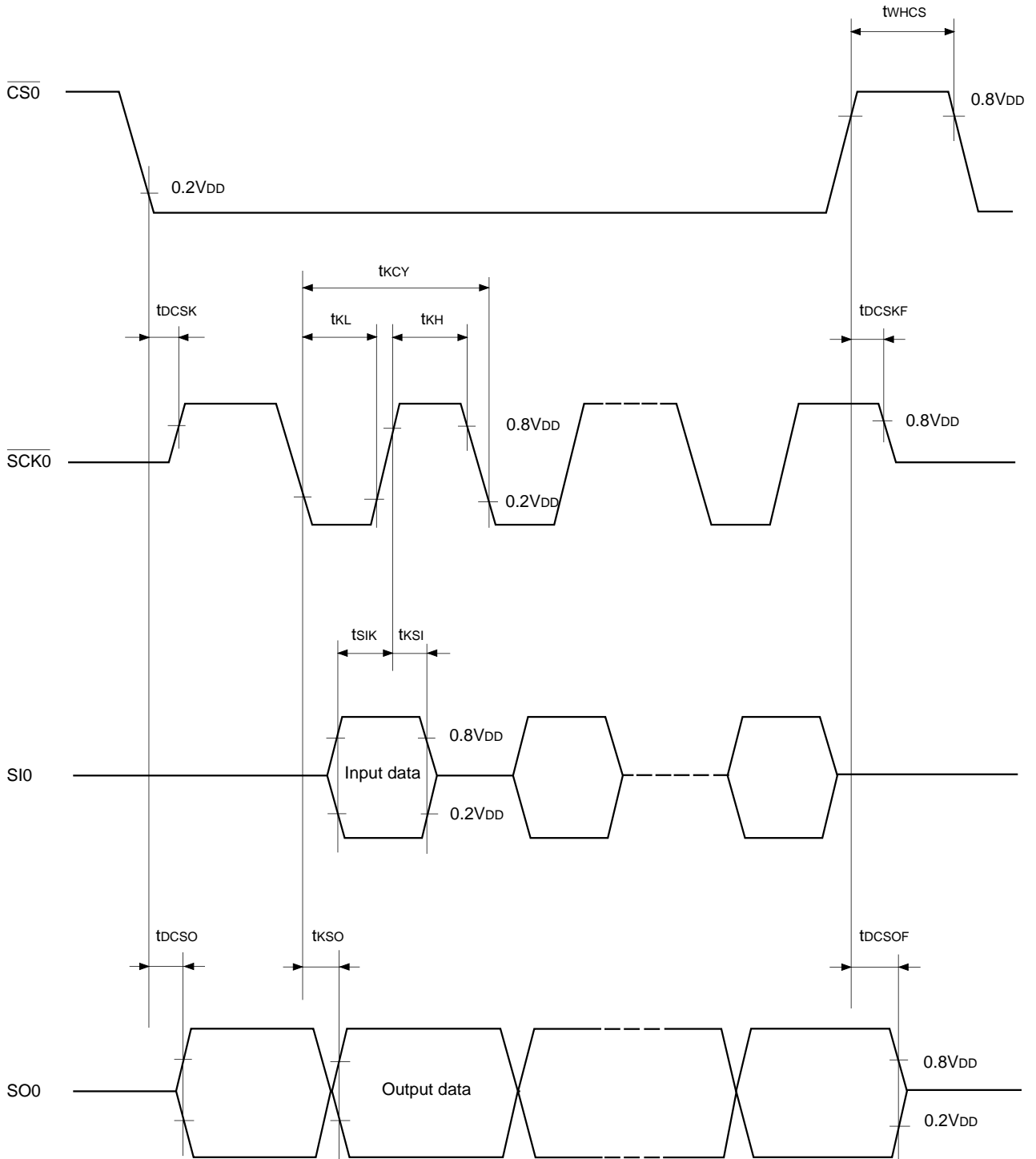
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ delay time	t _{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		t _{sys} + 200	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ float delay time	t _{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		t _{sys} + 200	ns
$\overline{CS0} \downarrow \rightarrow SO0$ delay time	t _{DCSO}	SO0	Chip select transfer mode		t _{sys} + 200	ns
$\overline{CS0} \uparrow \rightarrow SO0$ float delay time	t _{DCSOF}	SO0	Chip select transfer mode		t _{sys} + 200	ns
$\overline{CS0}$ High level width	t _{WHCS}	$\overline{CS0}$	Chip select transfer mode	t _{sys} + 200		ns
$\overline{SCK0}$ cycle time	t _{KCY}	$\overline{SCK0}$	Input mode	2t _{sys} + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ High and Low level widths	t _{KH} t _{KL}	$\overline{SCK0}$	Input mode	t _{sys} + 100		ns
			Output mode	8000/fc - 50		ns
SI0 input setup time (for $\overline{SCK0} \uparrow$)	t _{SIK}	SI0	$\overline{SCK0}$ input mode	100		ns
			$\overline{SCK0}$ output mode	200		ns
SI0 input hold time (for $\overline{SCK0} \uparrow$)	t _{KSI}	SI0	$\overline{SCK0}$ input mode	t _{sys} + 200		ns
			$\overline{SCK0}$ output mode	100		ns
$\overline{SCK0} \downarrow \rightarrow SO0$ delay time	t _{KSO}	SO0	$\overline{SCK0}$ input mode		t _{sys} + 200	ns
			$\overline{SCK0}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC: 00FEh) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) The load of $\overline{SCK0}$ output mode and SO0 output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer CH0 timing



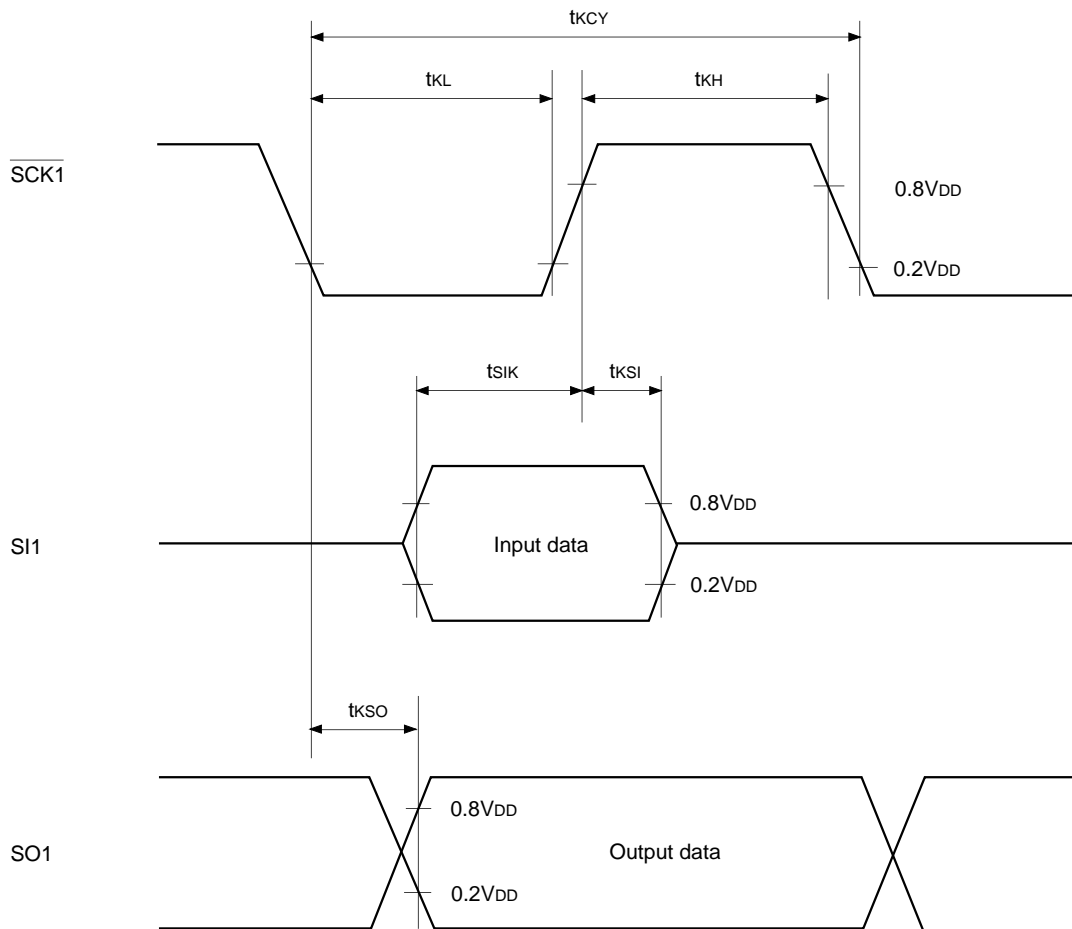
Serial transfer (CH1)

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY}	$\overline{\text{SCK1}}$	Input mode	1000		ns
			Output mode	$16000/f_c$		ns
$\overline{\text{SCK1}}$ High and Low level widths	t_{KH} t_{KL}	$\overline{\text{SCK1}}$	Input mode	400		ns
			Output mode	$8000/f_c - 50$		ns
SI1 input setup time (for $\overline{\text{SCK1}}$ \uparrow)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (for $\overline{\text{SCK1}}$ \uparrow)	t_{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	200		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}}$ $\downarrow \rightarrow$ SO1 delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		200	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

Note) The load of $\overline{\text{SCK1}}$ output mode and SO1 output delay time is $50\text{pF} + 1\text{TTL}$.

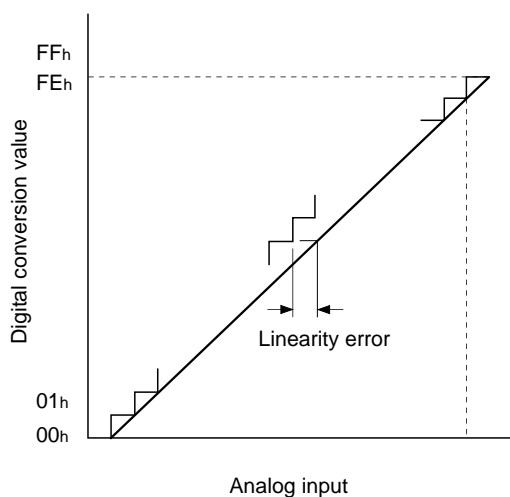
Fig. 5. Serial transfer CH1 timing



(3) A/D converter characteristics ($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = AV_{DD} = 4.5$ to 5.5V , $AV_{REF} = 4.0$ to AV_{DD} , $V_{SS} = AV_{SS} = 0\text{V}$)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			$T_a = 25^\circ\text{C}$ $V_{DD} = AV_{DD} = AV_{REF} = 5.0\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$			± 1	LSB
Absolute error						± 2	LSB
Conversion time	t_{CONV}			$160/f_{ADC}^{*1}$			μs
Sampling time	t_{SAMP}			$12/f_{ADC}^{*1}$			μs
Reference input voltage	V_{REF}	AV_{REF}		$AV_{DD} - 0.5$		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN11		0			V
AV_{REF} current	I_{REF}	AV_{REF}	Operating mode		0.6	1.0	mA
	I_{REFS}		Sleep mode Stop mode 32kHz operating mode			10	μA

Fig. 6. Definitions of A/D converter terms



*1 The value of f_{ADC} is as follows by selecting ADC operation clock (MSC: Address 01FFh bit 0).
 When PS2 is selected, $f_{ADC} = f_c/2$
 When PS1 is selected, $f_{ADC} = f_c$

(4) Interruption, reset input

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption High and Low level widths	t_{IH}	$\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$ NMI PJ0 to PJ7		1		μs
	t_{IL}					
Reset input low level width	t_{RSL}	$\overline{\text{RST}}$		$32/f_c$		μs

Fig. 7. Interruption input timing

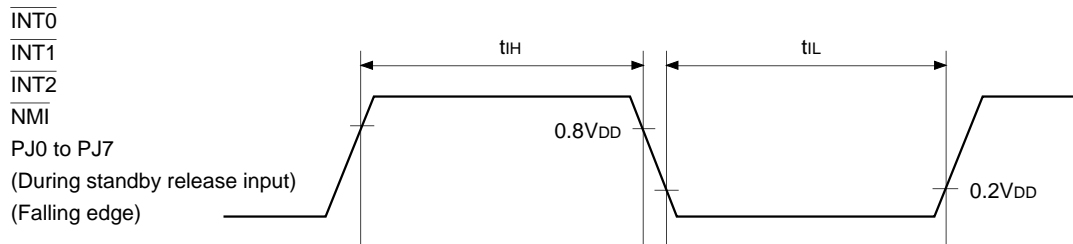
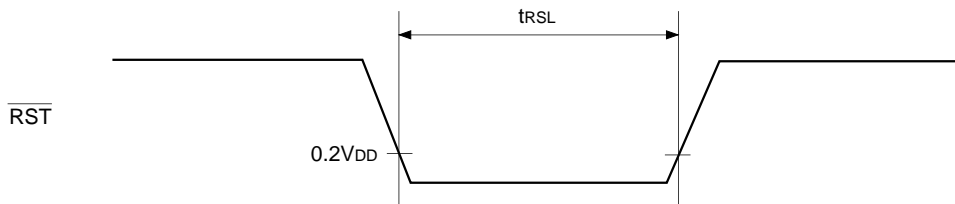


Fig. 8. Reset input timing



(5) Others

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$)

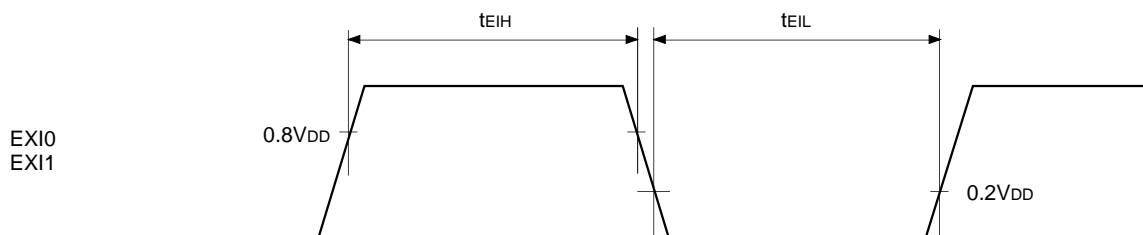
Item	Symbol	Pin	Condition	Min.	Max.	Unit
EXI input High and Low level widths	t_{EIH}	EXI0 EXI1	$t_{\text{sys}} = 2000/f_c$	$t_{\text{sys}} + 200$		ns
	t_{EIL}					

Note) t_{sys} indicates three values according to the contents of the clock control register (CLC: 00FEh) upper 2 bits (CPU clock selection).

$t_{\text{sys}} [\text{ns}] = 2000/f_c$ (Upper 2 bits = "00"), $4000/f_c$ (Upper 2 bits = "01"), $16000/f_c$ (Upper 2 bits = "11")

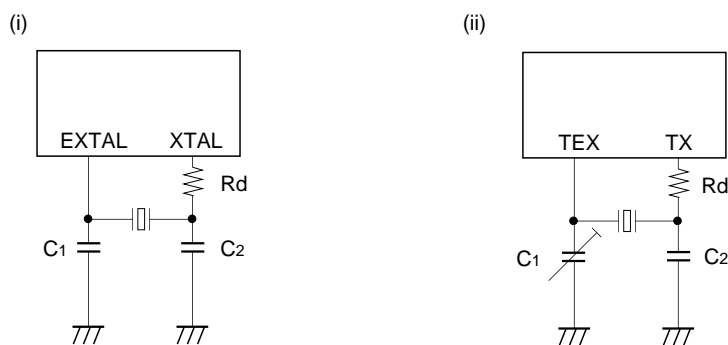
$t_{\text{FRC}} [\text{ns}] = 1000/f_c$

Fig. 9. Other timings



Appendix

Fig. 10. Recommended oscillation circuit



Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00				
		12.00	5	5		
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16	12	0	(i)
		10.00	16	12		
		12.00	12	12		
		16.00	12	12		
	P3	32.768kHz	30	18	470k	(ii)

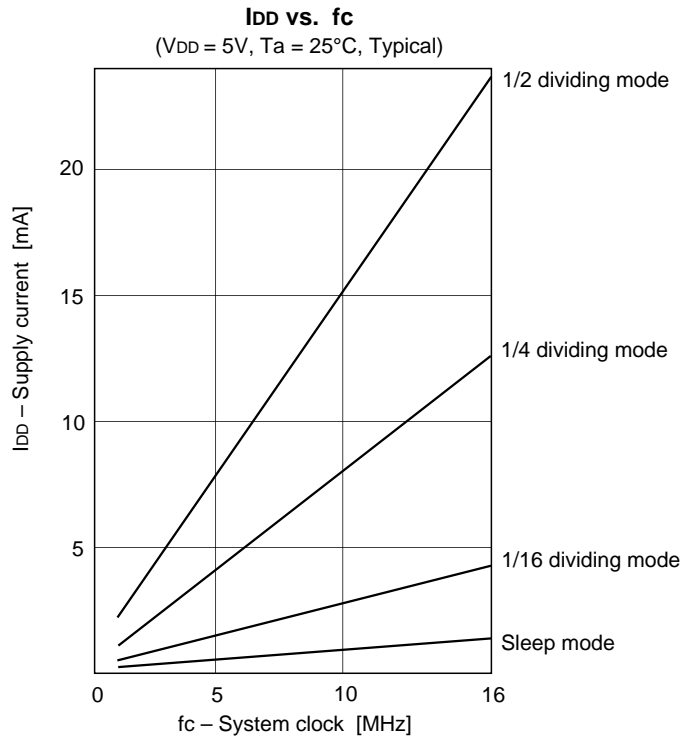
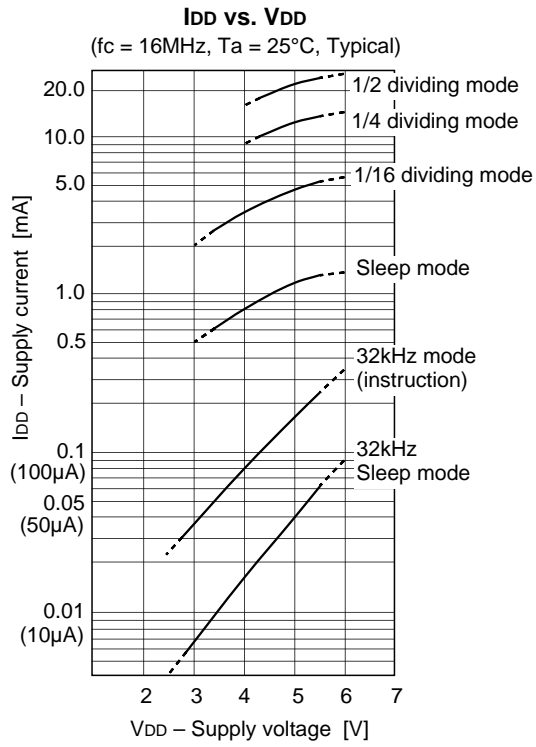
Models with an asterisk (*) have the built-in ground capacitance (C1, C2).

Mask option table

Item	Content	
	Reset pin pull-up resistor	Non-existent
Input circuit format*1	CMOS Schmitt	TTL Schmitt

*1 The input circuit format can be selected each for PG4 pin and PG5 pin.

Characteristics Curve





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