

## CMOS 8-bit Single Chip Microcomputer

### Description

The CXP81100 is a CMOS 8-bit single chip micro-computer of piggyback/evaluator combined type, which is developed for evaluating the function of the CXP81120/81124.

### Features

- A wide instruction set (213 instructions) which cover various types of data
  - 16-bit operation/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle
- Applicable EPROM
- Incorporated RAM capacity
- Peripheral functions
  - A/D converter
  - Serial interface
  - Timer
  - PWM output
- Interruption
- Standby mode
- Package

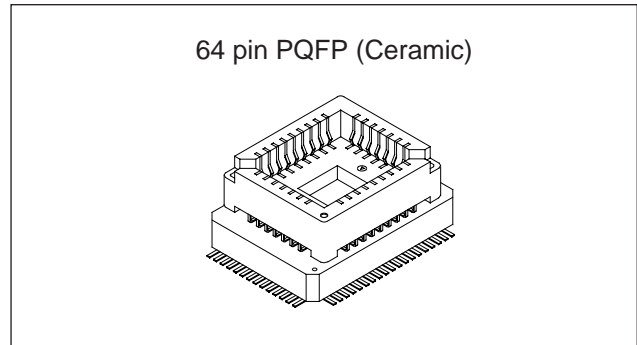
333ns at 12MHz operation (3.0 to 5.5V)  
 250ns at 16MHz operation (4.5 to 5.5V)  
 LCC type 27C128, LCC type 27C256  
 (Maximum 24Kbytes are available.)  
 832bytes

8-bit, 8-channel, successive approximation method  
 (Conversion time of 20 $\mu$ s/16MHz)  
 Incorporated buffer RAM (Auto transfer for 1 to 32bytes),  
 1channel  
 Incorporated 8-bit, 8-stage FIFO  
 (Auto transfer for 1 to 8bytes), 1channel  
 8-bit timer  
 8-bit timer/counter  
 19-bit time base timer  
 12bits, 2channels  
 (repetitive frequency 62.5kHz/16MHz)  
 10 factors, 10 vectors, multi-interruption possible  
 SLEEP/STOP  
 64-pin ceramic PQFP

**Note)** Mask option depends on the type of the CXP81100. Refer to the Products List for details.

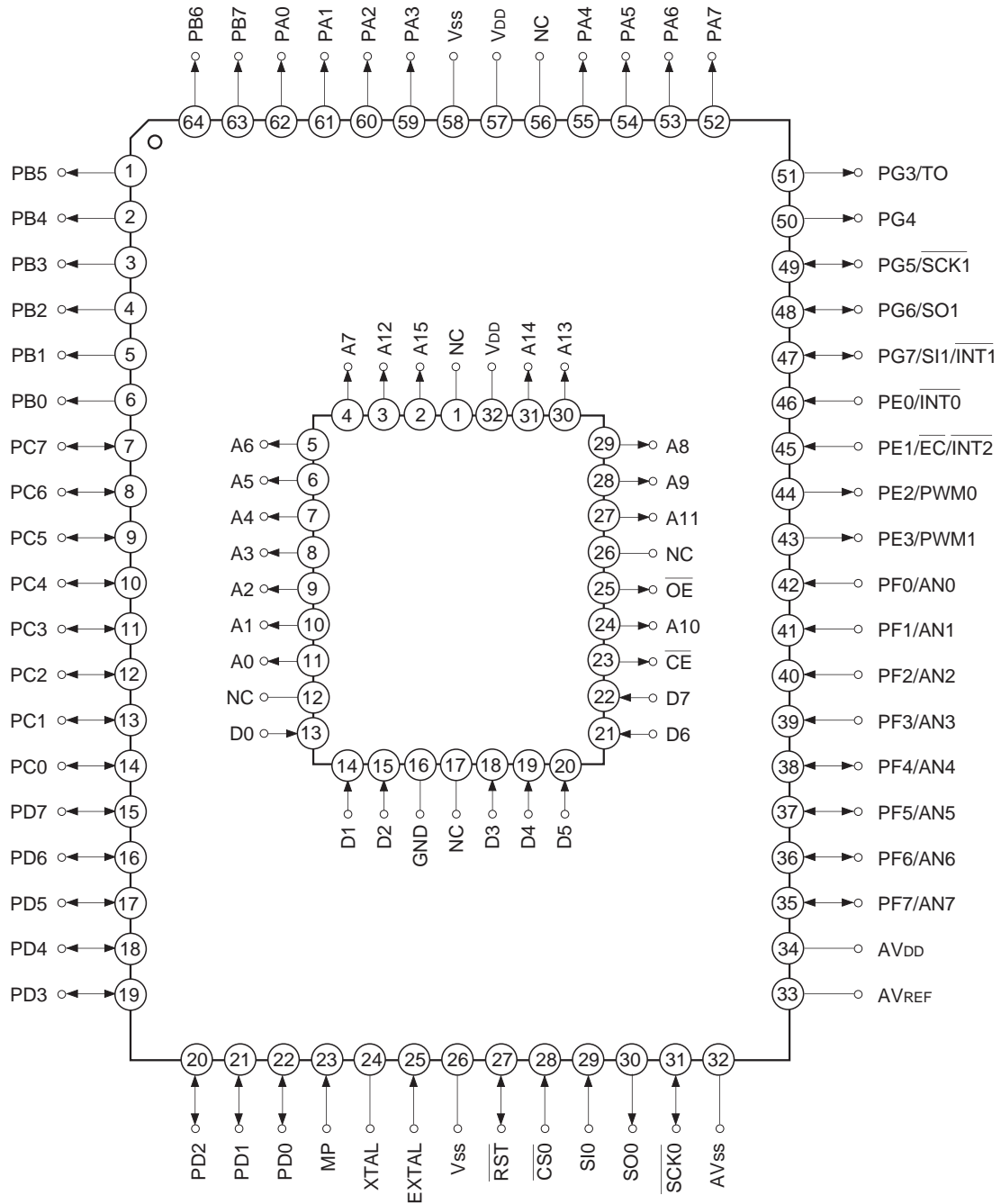
### Structure

Silicon gate CMOS IC



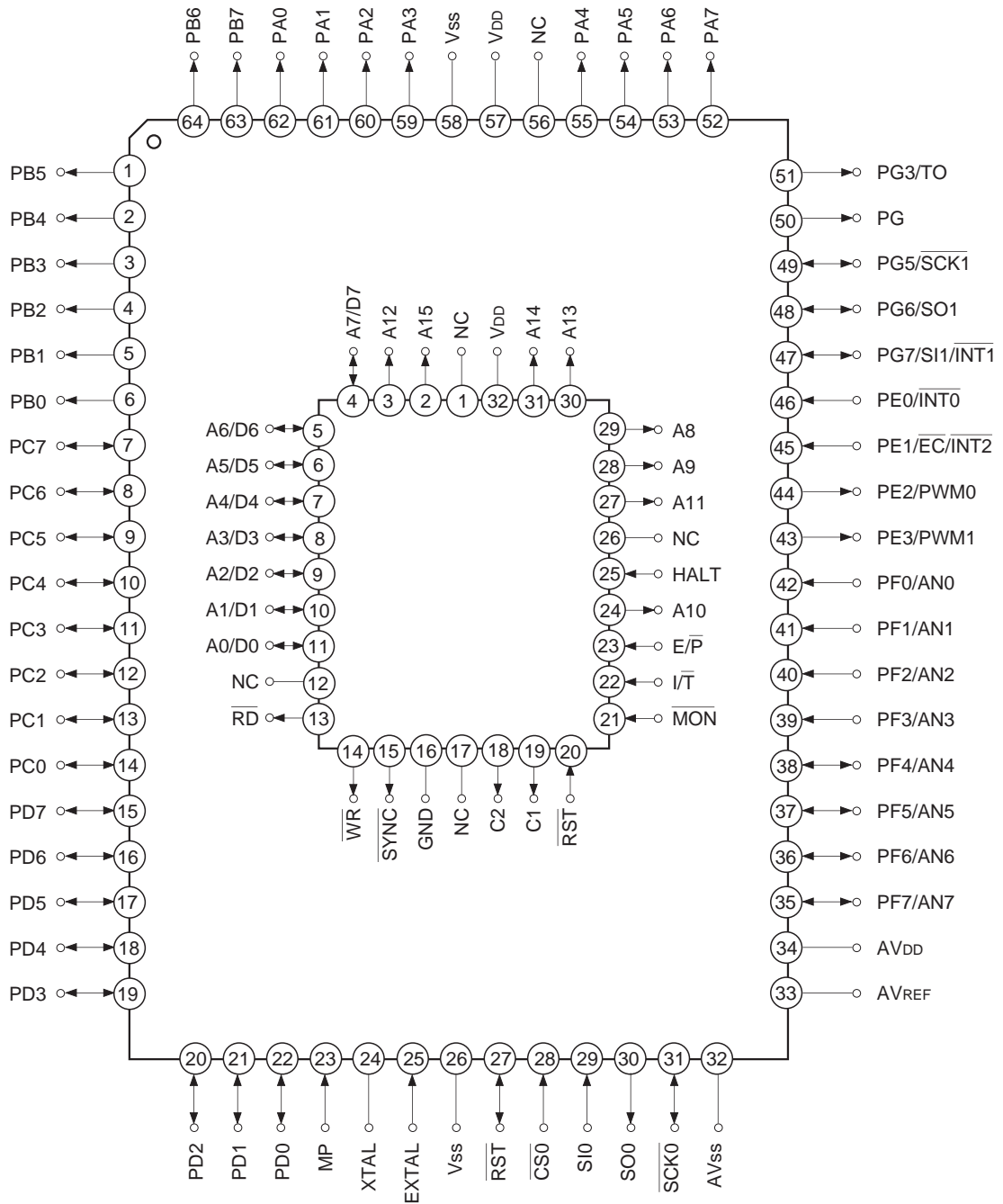
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Pin Assignment in Piggyback Mode



- Note)**
1. NC (Pin 56) is always connected to VDD.
  2. Vss (Pins 26 and 58) are both connected to GND.
  3. MP (Pin 23) is always connected to GND.

Pin Assigment in Evaluator Mode

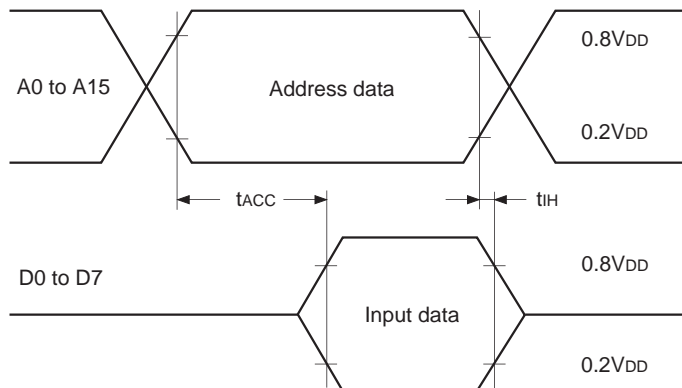


- Note**
1. NC (Pin 56) is always connected to VDD.
  2. Vss (Pins 26 and 58) are both connected to GND.
  3. MP (Pin 23) is always connected to GND.

**EPROM Read Timing** ( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 3.0$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

Item	Symbol	Pin	Min.	Max.	Unit
Address → data input delay time	$t_{ACC}$	A0 to A15 D0 to D7		75*	ns
Address → data hold time	$t_{IH}$	A0 to A15 D0 to D7	0		ns

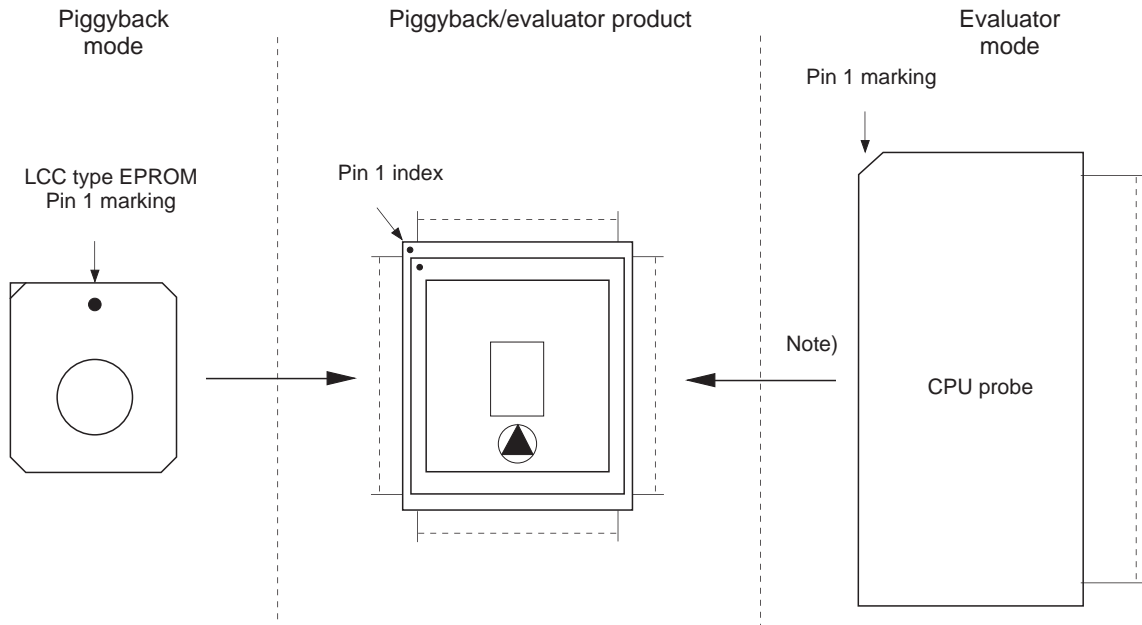
\* At 12MHz operation ( $V_{DD} = 3.0$  to  $5.5\text{V}$ ), At 16MHz operation ( $V_{DD} = 4.5$  to  $5.5\text{V}$ )



**Products List**

Option item	Products		
	Mask product		Piggyback/evaluator product
	CXP81120	CXP81124	CXP81100-U01Q
Package	64-pin plastic LQFP		64-pin ceramic PQFP
ROM capacity	20K bytes	24K bytes	EPROM 24K bytes
Pull-up resistor for reset pin	Existent/Non-existent		Existent
Power on reset circuit	Existent/Non-existent		Existent

Piggyback mode/evaluator mode can be switched as shown below.

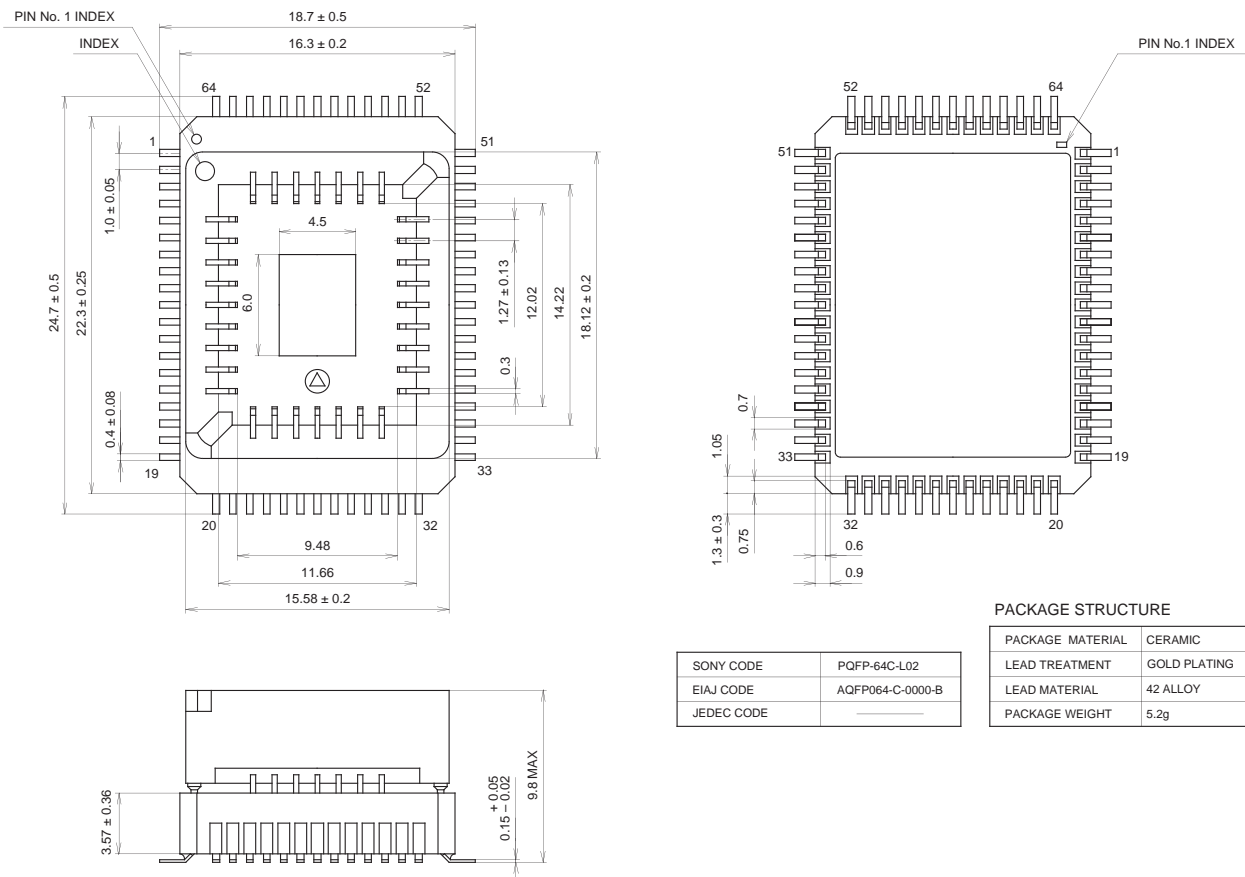


Note) Evaluation cap should be connected to CPU probe.

Package Outline

Unit : mm

64PIN PQFP (CERAMIC)





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