SONY

CXP50P116

CMOS 4-bit Single Chip Microcomputer

Description

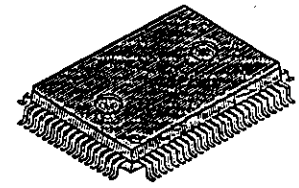
The CXP50P116 features the following variety of functions. A 4-bit CPU, ROM, RAM, I/O port, 8-bit timer, 8-bit timer/counter, 18-bit time base timer, 8-bit serial I/O, vector interrupt and power on reset functions. This CMOS 4-bit microcomputer also integrates a fluorescent display panel controller/driver, PWM output port for D/A conversion, remote control receiving circuit, 3-bit A/D converter, 32kHz timer/event counter, 8-bit reload type timer, supply voltage detection reset and a standby function for low power consumption operation, all in a single chip.

CXP50P116 provides the PROM version of CXP50116 which incorporates a mask ROM. Since program writing is possible, it is suited for evaluation in system development, as well as for limited production.

Features

- Instruction cycle 1.9μs/4.19MHz
  122μs/32kHz
  (Selectable at the program)
- Built-in PROM 16384×8bits
- Built-in RAM 544×4 bit
  (Including the display area)
- General purpose I/O ports 51 ports MAX.
- High current output ports 8 ports
- Biult-in Fluorescent display panel controller/driver
  (Display of up to 256 segments possible)
  —1 to 16 digits dynamic scan display
  (1 to 8 digits at the 24 segments selection)
  —Page mode/Variable mode
  —Dimmer function
  —High voltage resistant output (40V)
  —Selection of built-in pull down resistance possible
  (Mask option)
- Built-in 14-bit PWM output for D/A conversion
- Built-in remote control receiving circuit (Independent from timer/counter)
- Built-in 3-bit A/D converter (1 circuit 8 channels)

80pin QFP (Plastic)



- Built-in 32kHz reload type timer/event counter
- Built-in supply voltage detection reset circuit
- Abundant wake up functions
  WP pin
  4 general purpose ports (Edge detection)
  Remote control receiving circuit
  32kHz timer/counter
- Built-in serial I/O with 8-bit/4-bit variable prescaler
- Built-in timer with 8-bit prescaler, timer/event counter with 8-bit prescaler, 18-bit time base timer and reload type timer with 8-bit prescaler can all be independently controlled.
- Arithmetic and logical operations possible between the entire ROM area, I/O area and the accumulator by means of the memory mapped I/O.
- Reference to the entire ROM area possible using the table look-up instruction.
- 2 kinds of power down modes, sleep and stop
- Built-in power on reset circuit (Mask option)
- 80-pin plastic QFP

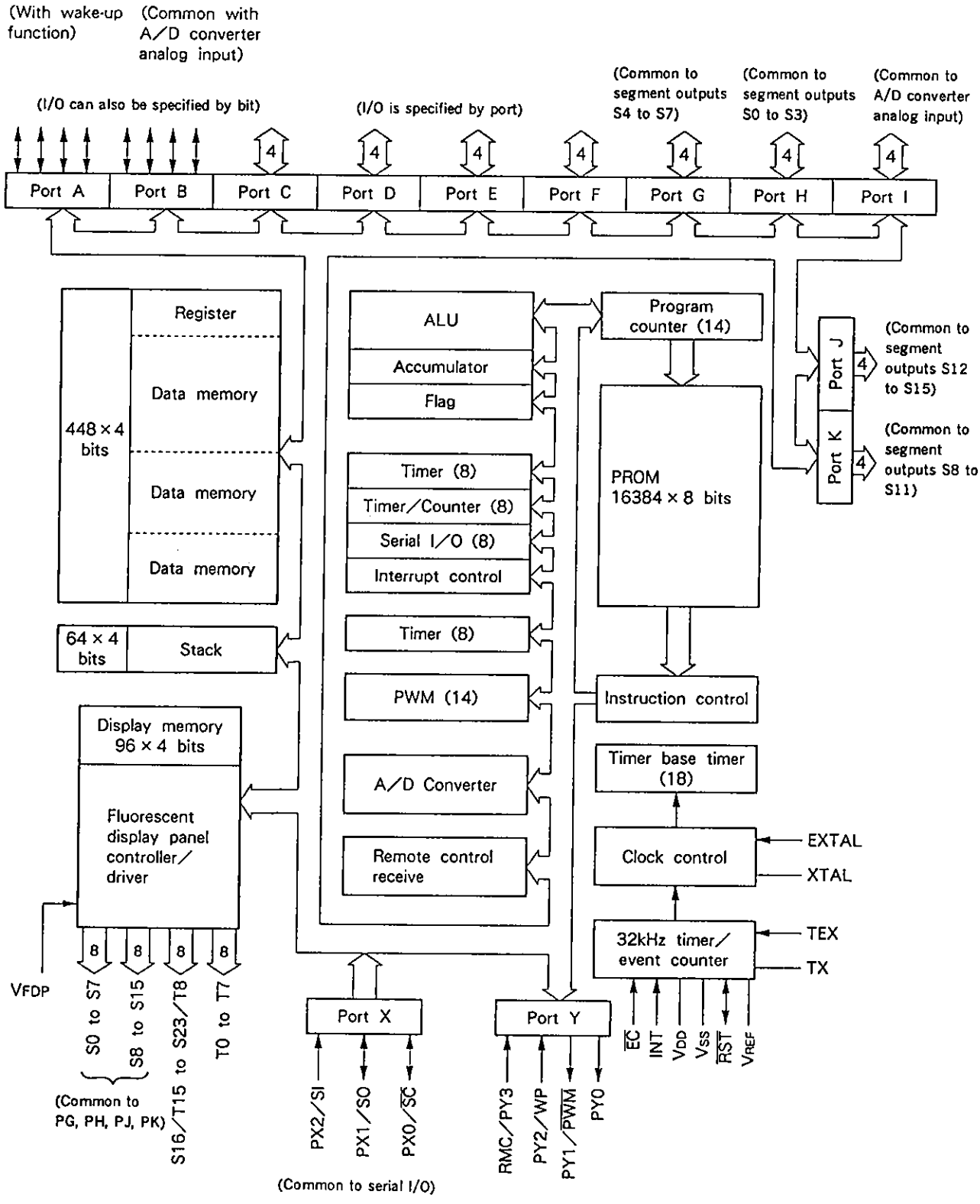
note) mask option is available in type CXP50P116Q-3 for details see CXP50P116Q-3 option table P.16

Structure

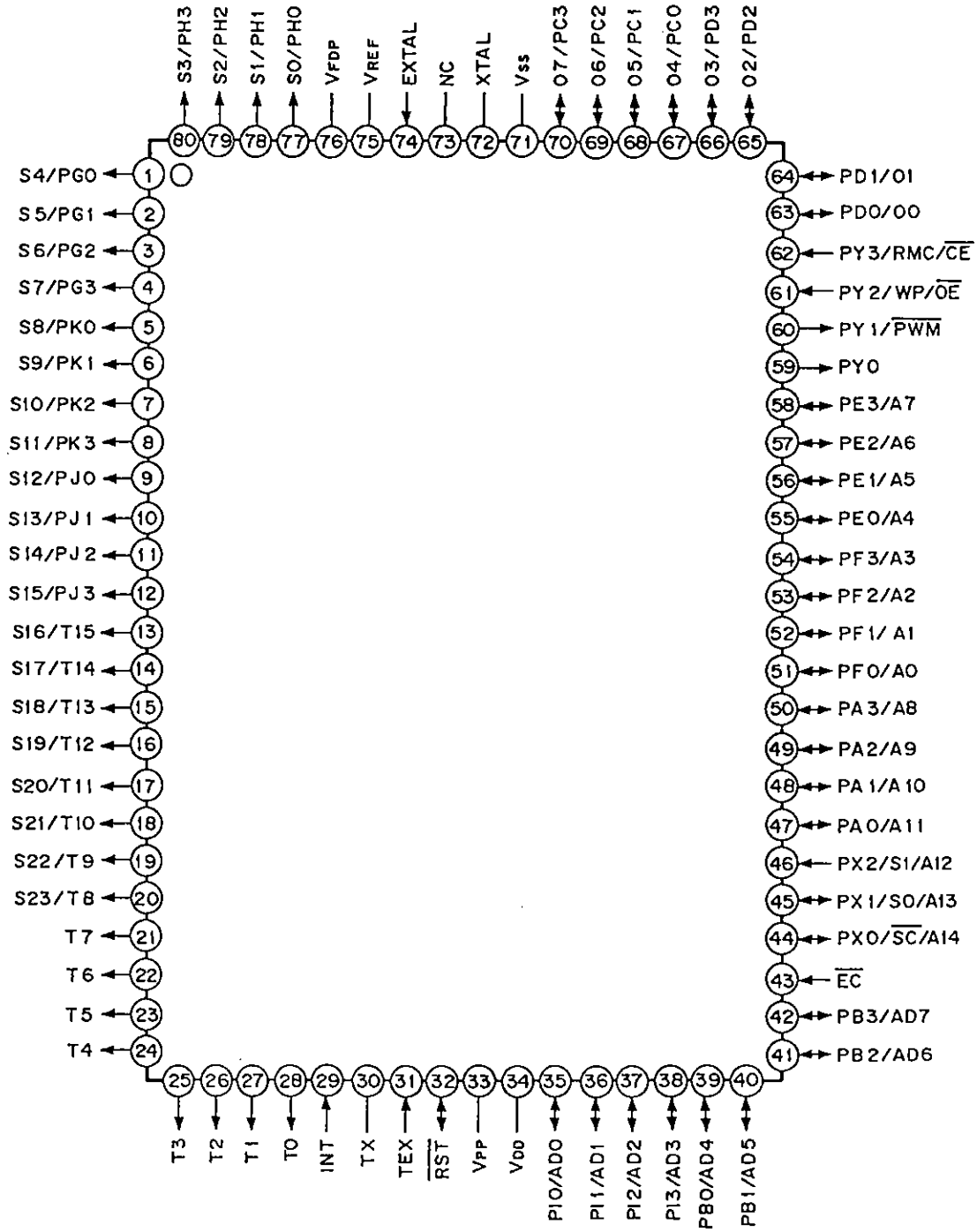
Silicon gate CMOS IC

E90936A16-HP

Block Diagram



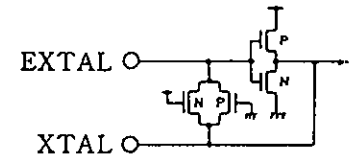
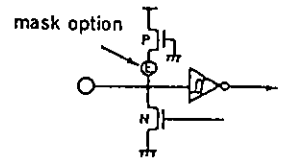
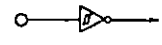
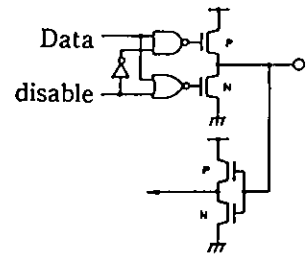
Pin configration (Top View)

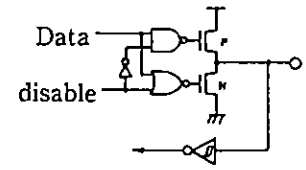
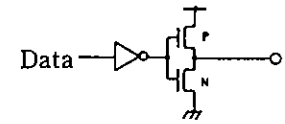
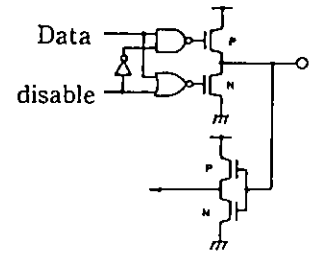


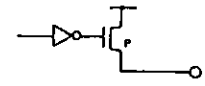
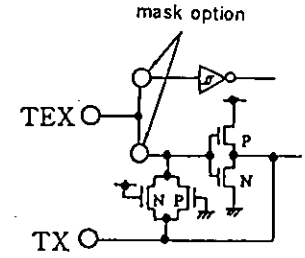
Note)

1. Do not connect anything to Pin 73 (NC).
2. Be sure to connect Vp-p of Pin 33 to V_{DD}.

Pin Description

Symbol	Name	I/O	Description	Equivalent Circuit
V_{DD}	Supply voltage	—	Positive voltage supply pin	
V_{PP}	Write supply voltage	—	Power supply pin for write of built-in PROM. At normal operation connect to V_{DD}	
V_{SS}	Grounding voltage	—	GND pin	
EXTAL	Clock input	I	Clock oscillation circuit input pin. Connect the crystal oscillator or ceramic resonator between the EXTAL and XTAL. To use an external clock input, connect the clock oscillation source to EXTAL pin and keep XTAL pin open	
XTAL	Clock output	—	Clock oscillation circuit output pin	
$\overline{RST}$	Reset	I/O	Output pin of the built-in power on reset circuit. When a reset signal is input from the outside, set 2 or more instruction cycles to "L", (0V).	 Output pull-up resistor (P-ch Tr) N-ch Tr output Schmitt inverter input
INT	External interrput	I	Interrupt input pin. Permits the selection of edge and level modes using a program.	 Schmitt inverter input
$\overline{EC}$	Event counter input	I	Event counter input pin.	
SI/PX2	Serial input Port X	I	Doubles as serial interface (8bits) input pin and as bit "2" (input) of port X. Functions as address input pin during PROM mode.	
SO/PX1	Serial output Port X	I/O	Doubles as serial interface (8bits) output pin and an bit "1" (input) of port X. Functions as address input pin during PROM mode.	 Tri-state output Schmitt input

Symbol	Name	I/O	Description	Equivalent Circuit
$\overline{SC}$/PX0	Serial clock Port X	I/O	Doubles as clock input/output pin for the serial interface and as bit "0" (input) of port X. Functions as address input pin in PROM mode	 Tri-state output Schmitt input
RMC/PY3	Remote control input Port Y	I	Remote control receiver input pin. Input pin for bit "3" of port Y. Functions as $\overline{EC}$ during PROM mode.	
WP/PY2	Wake-up input Port Y	I	Doubles as a wake-up input to release the standby state, and as bit "2" (input) of port Y. Functions as $\overline{OE}$ in PROM mode.	Schmitt inverter input
$\overline{PWM}$/PY1	PWM output Port Y	O	Doubles as a PWM generator (14bits) output and as bit "1" (output) of port Y.	
PY0	Port Y	O	Output pin for bit "0" of port Y.	(When reset: 1) Inverter output
PA0 to PA3	Port A	I/O	4-bit input/output port that can be programmde by bit to serve for input or output. Tri-state output. Functions as address input pin in PROM mode.	 Tri-state output inverter input
PB0/AD4 to PB3/AD7	Analog Voltage input/Port B	I/O	4-bit input/output port with functions equivalent to those of port A. It is also used as A/D converter input.	
PC0 to PC3	Port C	I/O	4-bit input/output port that can be programmed in 4-bit units to serve for input or output. Output format is in tri-state Functions as data I/O pin in PROM mode.	
PD0 to PD3	Port D	I/O	4-bit input/output port with functions equivalent to those of port C. Functions as data I/O pin in PROM mode.	
PE0 to PE3	Port E	I/O	4-bit input/output port with functions equivalent to those of port C. Functions as address input pin in PROM mode.	
PF0 to PF3	Port F	I/O	4-bit input/output port with functions equivalent to those of port C. Functions as address input pin in PROM mode.	

Symbol	Name	I/O	Description	Equivalent Circuit
PI0/AD0 to PI3/AD3	Analog Voltage input/Port I	I/O	4-bit input/output port with functions equivalent to those of port C. It is also used as A/D converter input.	
V_{FDP}	FDP power supply	—	Load current supply pin needed when load resistance is built-in to FDP (Fluoresent display pannel.) output driver.	
T0 to T7	Timing	O	Lower 8-digit output pin of FDP timing signal.	 P-ch open drain output Pull-down resistance (T0 to T15 only)
T8/S23 to T15/S16	Timing/ segment	O	Combination output pin for higher 8-digit of FDP timing signal and the segment signal.	
PG0/S4 to PG3/S7	Port G/ segment	O	Combination pin for the 4-bit output port and FDP segment signal output.	
PH0/S0 to PH3/S3	Port H/ segment	O	The same as port G.	
PJ0/S12 to PJ3/S15	Port J/ segment	O	The same as port G.	
PK0/S8 to PK3/S11	Port K/ segment	O	The same as port G.	
TEX	32kHz T/C clock input	I	Input pin of the 32kHz timer clock generated circuit. Connect 32.768kHz crystal oscillator between TEX and TX. Connect clock oscillation source to TEX pin and keep TX pin open when this circuit is used as event clock input.	
TX	32kHz T/C clock output	—	Output pin of the clock generated circuit.	
V_{REF}	Reference voltage input	—	Reference voltage input for power supply voltage resetting circuit. The zener diode is normally connected.	

Absolute Maximum Ratings Ta = −10 to +75°C, V_{SS} = 0V

Item	Symbol	Rating	Unit	Remarks
Power supply voltage	V_{DD}	−0.3 to +7.0	V	
	V_{PP}	−0.3 to +13.5	V	Version with built-in PROM
Input voltage	V_{IN}	−0.3 to +7.0*1	V	
Output voltage	V_{OUT}	−0.3 to +7.0*1	V	
Display output voltage	V_{OD}	V_{DD}−40 to V_{DD}+0.3	V	As P channel tranisistor is an open drain, V_{DD} voltage is taken as standard.
High level output current	I_{OH}	−5	mA	FOR pins other than display output pins*2: per pin
	I_{ODH1}	−15	mA	Display output S0 to S15: per pin
	I_{ODH2}	−35	mA	Display output T0 to T7, T8/S23 to T15/S16: per pin
High level total output current	ΣI_{OH}	−40	mA	Total of pins other than display output pins
	ΣI_{ODH}	−100	mA	Total of display output pins
Low level output current	I_{OL}	15	mA	Port 1 pin
	I_{OLC}	20	mA	High current port pin*3
Low level total output current	ΣI_{OL}	100	mA	Total for all pins
Operating temperature	T_{str}	−10 to +75	°C	
Storage temperature	T_{stg}	−55 to +150	°C	
Allowable power dissipation	P_D	600	mW	

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operation conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

*1) V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*2) Specifies the output current of the general purpose I/O port PA to PF, PI, SO, $\overline{SC}$, PY0 and PY1.

*3) N-CH transistors of PC and PD ports are high current operation transistors.

Recommended Operating Conditions

V_{SS}=0V

Item	Symbol	Min.	Max.	Unit	Remarks
Power supply voltage	V_{DD}	4.5	5.5	V	Guaranteed range of operation by EXTAL clock
		2.5	5.5	V	Guaranteed range of operation by TEX clock, Guaranteed range of data held during STOP
	V_{PP}	$V_{PP}=V_{DD}$		V	*3
High level input voltage	V_{IH}	$0.7V_{DD}$	V_{DD}	V	
	V_{IHS}	$0.8V_{DD}$	V_{DD}	V	Hysteresis input*1
	V_{IHEX}	$V_{DD}-0.4$	$V_{DD}+0.3$	V	EXTAL pin*2
Low level input voltage	V_{IL}	0	$0.3V_{DD}$	V	
	V_{ILS}	0	$0.2V_{DD}$	V	Hysteresis input*1
	V_{ILEX}	−0.3	0.4	V	EXTAL pin*2
Operating temperature	T_{opr}	−10	+75	°C	

*1) The TEX pin when the counter mode is selected by each of INT, $\overline{EC}$, PX0, PX2, PY2, PY3, $\overline{RST}$ pins and mask option.
*2) Specified only during external clock input.
*3) Set Vpp to the same voltage as V_{DD}

Electrical Characteristics

DC charahteristics

Ta = −10 to +75°C, V_{SS} = 0V

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PF, PI PX0, PX1 PY0, PY1 $\overline{RST}$ (V_{OL} only)	V_{DD}=4.5V, I_{OH}=−0.5mA	4.0			V
			V_{DD}=4.5V, I_{OH}=−1.0mA	3.5			V
Low level output voltage	V_{OL}		V_{DD}=4.5V, I_{OL}=1.8mA			0.4	V
			V_{DD}=4.5V, I_{OL}=3.6mA			0.6	V
		PC, PD	V_{DD}=4.5V, I_{OL}=12mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD}=5.5V, V_{IH}=5.5V	0.5		40	μA
	I_{ILE}		V_{DD}=5.5V, V_{IL}=0.4V	−0.5		−40	μA
	I_{IHT}	TEX*3	V_{DD}=5.5V, V_{IH} 5.5V	0.1		10	μA
	I_{ILT}		V_{DD}=5.5V, V_{IL}=0.4V	−0.1		−10	μA
	I_{ILR}	$\overline{RST}$*2		−1.5		−400	μA
Display output current	I_{OH}	S0 to S15	V_{DD}=4.5V V_{OH}=V_{DD}−2.5V	−7			mA
		S16/T15 to S23/T8, T0 to T7		−18			mA
Open drain output leakage current (P-CH Tr OFF)	R_{LOL}	S0 TO S15, S16/T15 to S23/T8, T0 to T7	V_{DD}=5.5V V_{OL}=V_{DD}−35V			−20	μs
Pull-down resistance*1	R_L	S0 TO S15, S16/T15 to S23/T8, T0 to T7	V_{DD}=5V V_{FDP}=V_{DD}−35V	60	100	270	kΩ
High impedance I/O leakage current	I_{IZ}	PA to PF, PI PX0 to PX2, PY2, PY3, $\overline{EC}$, INT, $\overline{RST}$*2, TEX*3	V_{DD}=5.5V V_I=0, 5.5V			±10	μA
Supply current	I_{DD1}	V_{DD}	ALL output pins open Crystal oscillation (C1=C2=22pF) of V_{DD}=5.5V, 4.19MHz		8	20	mA
	I_{DD2}		Crystal oscillation (C1=C2=18pF) of V_{DD}=3V, 32kHz		0.7	2	mA
	I_{DDSP1}		SLEEP mode V_{DD}=5.5V, 4.19MHz oscillation		5	12	mA
	I_{DDSP2}		V_{DD}=3V, 32kHz oscillation		0.7	2	mA
	I_{DDS1}		STOP mode V_{DD}=3V, 32kHz with T/C		20	120	μA
	I_{DDS2}		V_{DD}=5.5V, 32kHz without T/C (For mask option select counter, Pin is fixed.)			10	μA
Input capacity	C_{IN}	PA to PF, PI, PX, PY2, PY3. EXTAL, TEX, $\overline{EC}$, INT, $\overline{RST}$	Clock 1MHz 0V for pins other than test pins		10	20	pF

*1) When the built-in pull-down resistance is selected by the mask option.
*2) $\overline{RST}$ pin specifies the input current when the pull-up resistance is selected, and specifies leakage current when nonresistance is selected.
*3) The TEX pin specifies the input current when the 32kHz oscillation is selected by the mask option, and specifies leakage current when the counter mode is specified.

AC Characteristics

(1) Clock timing

Ta = −10 to +75°C, V_{DD} = 4.5V to 5.5V, V_{SS} = 0V

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	1		5	MHz
System clock input pulse width	t_{XL} t_{XH}	EXTAL	Fig. 1, Fig. 2 (External clock drive)	90			ns
System clock input rise and fall time	t_{CR} t_{CF}					200	ns
System clock frequency	f_{CS}	TEX*2 TX	V_{DD} = 2.5 to 5.5V Fig. 3		32.768		kHz
Event count clock input pulse width	t_{EL} t_{EH}	$\overline{EC}$	Fig. 4	tsys*1 +0.05			μs
Event count clock input rise and fall time	t_{ER} t_{EF}	$\overline{EC}$	Fig. 4			20	ms
Event count input clock input pulse width	t_{TL} t_{TH}	TEX*3	Fig. 4	10			μs
Event count input clock rise and fall time	t_{TR} t_{TF}	TEX*3	Fig. 4			20	ms

*1) In EXTAL input clock tsys = 8/f_C
In TEX input clock tsys = 4/f_{CS}
*2) Specified when crystal oscillation mode is selected by mask option.
*3) Specified when counter mode is selected by mask option.
Note) When adjusting the frequency accurately, there may by cases where it differs from Fig. 2.

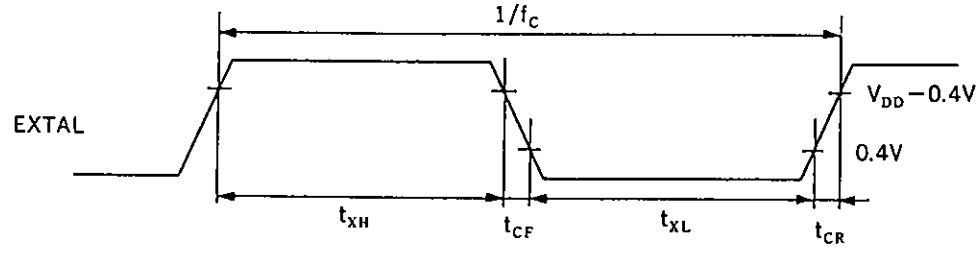


Fig. 1 Clock timing

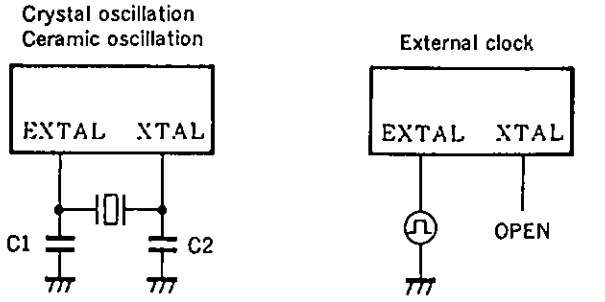


Fig. 2 Clock applying conditions

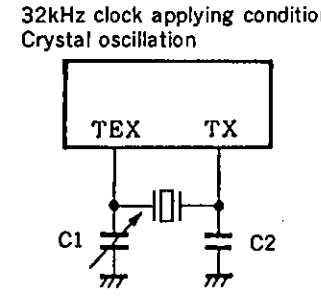


Fig. 3 32kHz Clock applying conditions

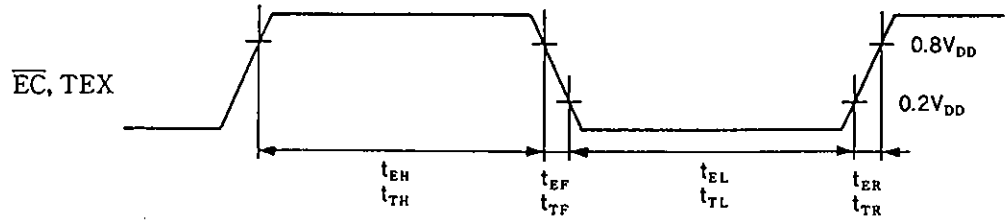


Fig. 4 Event conut clock timing

(2) Serial transfer

Ta=−10 to +75°C, V_{DD}=4.5V to 5.5V, V_{SS}=0V

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Serial transfer clock ($\overline{SC}$) cycle time	t_{KCY}	$\overline{SC}$	Input mode	tsys/4+1.42		μs
			Output mode	t_{SIO}		μs
Serial transfer clock ($\overline{SC}$) high and low level widths	t_{KH} t_{KL}	$\overline{SC}$	Input mode	tsys/8+0.7		μs
			Output mode	$t_{SIO}/2-0.1$		μs
Serial data input setup time (against $\overline{SC}$ ↑)	t_{SIK}	SI	$\overline{SC}$ input mode	0.1		μs
			$\overline{SC}$ output mode	0.2		μs
Serial data input hold time (against $\overline{SC}$ ↑)	t_{KSI}	SI	$\overline{SC}$ input mode	tsys/8+0.5		μs
			$\overline{SC}$ output mode	0.1		μs
Data delay time from $\overline{SC}$ fall	t_{KSO}	SO			tsys/8+0.5	μs

Note 1) In EXTAL input clock tsys=8/f_C
(It cannots be used with TEX input clock)
t_{SIO} turns into either 2tsys, 4tsys, or 16tsys according to the program
2) Load conditions of the data output delay time are 50pF+1TTL

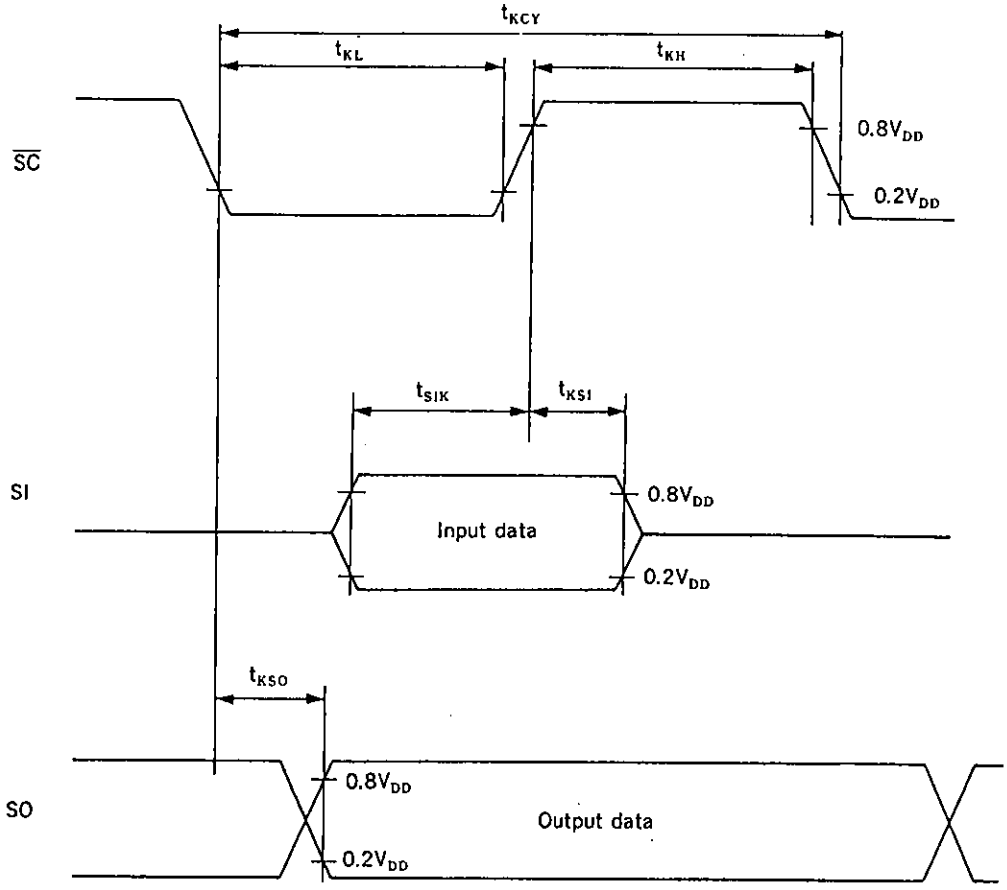


Fig. 5 Serial transfer timing

(3) A/D converter Ta = −10 to +75°C, V_{SS} = 0V

Analog input voltage	Pin	Condition	Digital conversion value
0.0 to 0.33V	AD0 to AD7	V_{DD} = 5V	000
0.82 to 1.29V			001
1.78 to 1.29V			010
2.69 to 3.06V			011
3.56 to 4.06V			100
4.62 to 5.0V			101

Note) The digital conversion value shows the value when FF_H address in the program is read.

(4) Power Supply Voltage Detection Reset Function Ta=−10 to +75°C, V_{SS}=0V

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Operation voltage range of Power supply voltage detection reset function	V_{LPOP}	V_{DD}	Voltage range that allows system operation. (When V_{DD}=4.5V or less 32kHz system operates)	2.5		5.5	V
Power supply voltage drop detection function	V_{POP}	V_{DD}	When V_{REF} pin voltage in at 3.3V Flag set is on when voltage drops System reset is on when voltage rises	3.8	4.0	4.2	V

The graph in Fig. 5 shows the relationship between power supply voltage V_{DD} and reference voltage V_{REF} of the power supply voltage detection reset function.

Note) The graph in Fig. 5 serves as guide to the function operation area obtained using average devices. Individual adjustment is needed when Zener diodes, etc., are connected to V_{REF} pin.

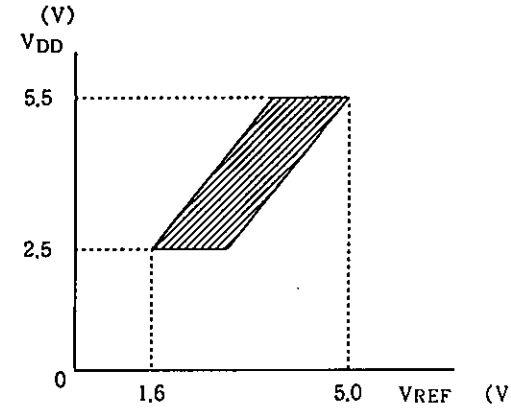


Fig. 6 Power supply voltage detection reset function chart

(5) Others Ta=−10 to +75°C, V_{DD}=4.5 to 5.5V, V_{SS}=0V

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t_{IIH}, t_{IIH}	INT	During edge dotection mode	tsys+0.05		μs
Reset input low level width	t_{RST}	$\overline{RST}$		2tsys*1		μs
Wake-up input high level width	t_{WPH}	WP	STOP mode	500		ns
			SLEEP mode	tsys+0.05		μs
Wake-up input high and low level width	t_{PWH}, t_{PWL}	PA		500		ns

Note) In EXTAL input clock tsys $8/f_C$
In TEX input clock tsys=$4/f_{CS}$

*1) To reset when operating in TEX input clock, hold the low level for more than the oscillation stabilizing time of EXTAL input clock.

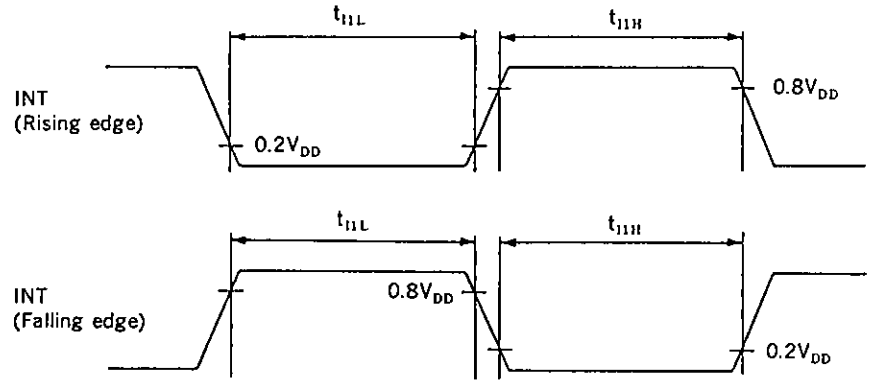


Fig. 7 Interruption input timing

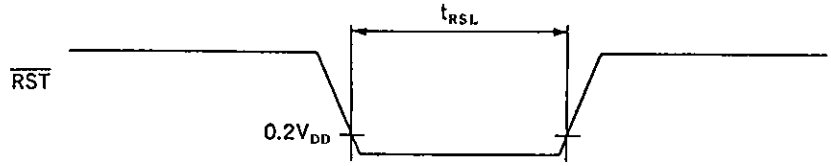


Fig. 8 Reset input timing

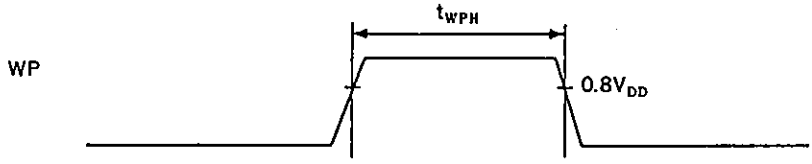


Fig. 9 Wake-up input timing

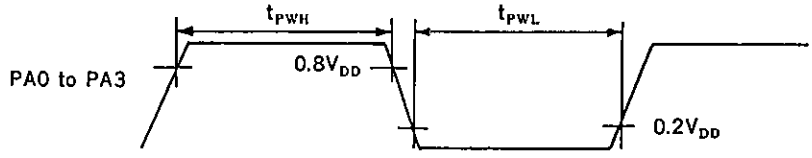


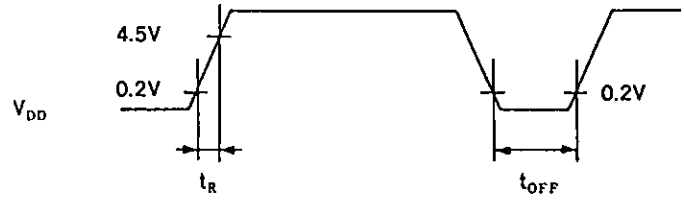
Fig. 10 Wake-up input timing

Power on reset*

Ta = −10 to +75°C, V_{SS} = 0V

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
Power supply rising time	t_R	V_{DD}	Power on reset	0.05	50	ms
Power supply cut-off time	t_{OFF}		Repetitive power on reset	1		ms

* Specified only when power on reset function is selected.



The power supply should rise smoothly.

Fig. 11 Power on reset

Instructions on Usage

To use the crystal oscillator refer to the Additive capacity calculation chart, on Fig. 12 and select the appropriate capacity.

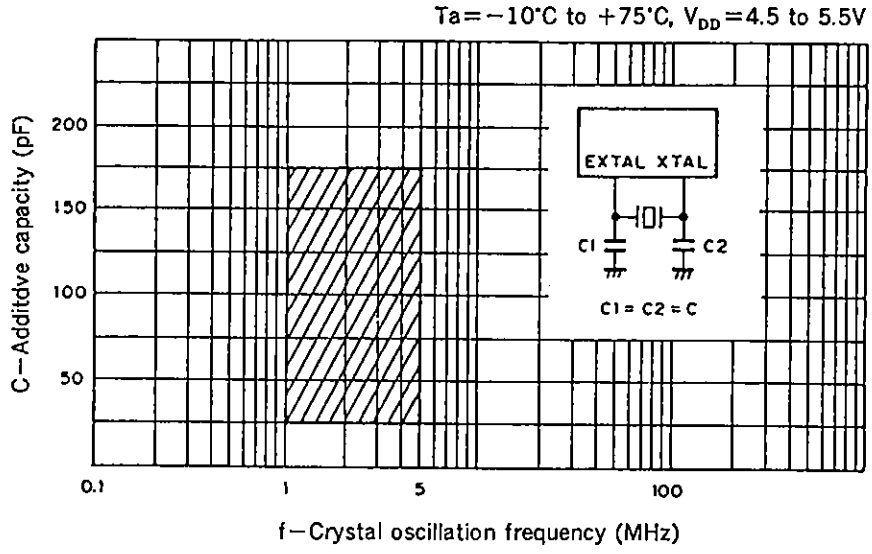


Fig. 12 Crystal oscillation circuit additive capacity calculation chart

Note) The above chart shows a range in which the average quartz resonator has a relatively fast oscillation rising edge stable characteristics. The capacity should be selected to correspond to the appropriate constant for each quartz resonator, should the frequency of the quartz resonator be accurately adjusted.

A circuit where frequency is accurately adjusted is shown on Fig. 13 In this case a 12pF crystal equivalent capacitor (CL) is used.

Here, although C1 and C2 are outside the range shown in the above chart, they can be used.

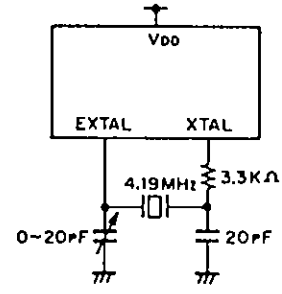


Fig. 13 Frequency aijusting circuit

When using A/D converter as the key input, it is recommended that the circuit structure shown in Fig. 14 be used.

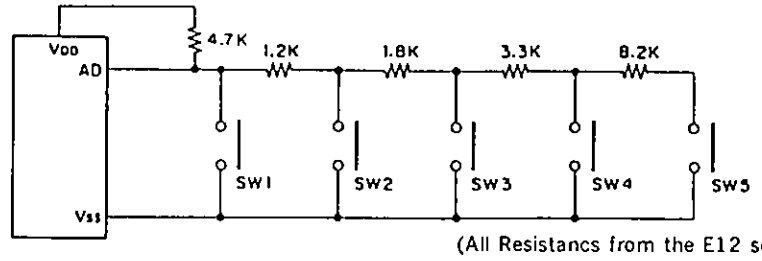


Fig. 14 Recommended example of key circuit by A/D converter

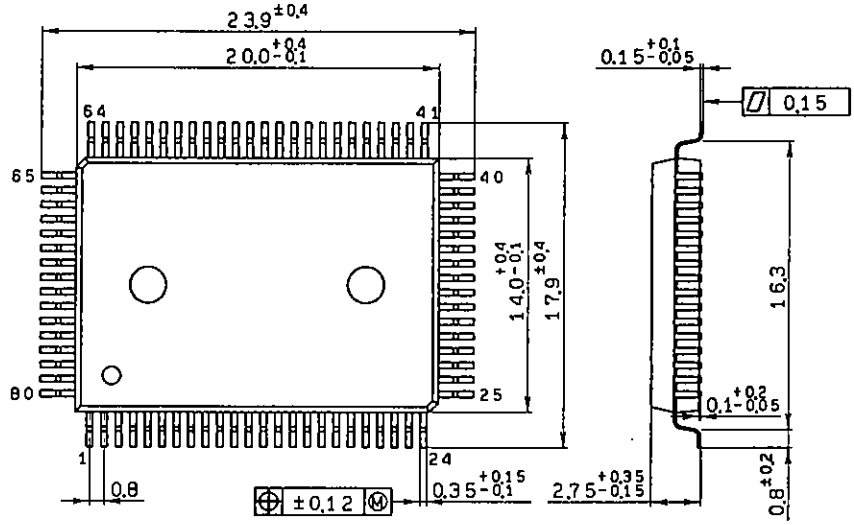
Products List

Optional item	Mass product	CXP50P116Q-3-□□□
Package	80-pin plastic QFP	80-pin plastic QFP
ROM capacity	12K-byte/16K-byte	EPROM 16K-byte
Pull-up resistance of reset pin	Existent/non-existent	Existent
Power on reset circuit	Existent/non-existent	Existent
32KHz timer/counter	Timer/counter	Timer mode
High tension proof pull-down resistance	Existent/non-existent	Non-existent (SO/PHO to S15/PJ3)* Existent (T0 to T15/S16)

* High tension proof pull-down resistance :
Non existent (Common to display/port pins)
Existent (Display output pin)

Package Outline Unit mm

80pin QFP (Plastic) 1.6g



SONY NAME	QFP-80P-L01
EIAJ NAME	*QFP080-P-1420-A
JEDEC CODE	———

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