

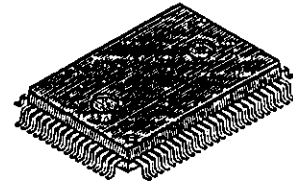
**CMOS 4-bit 1 Chip Microcomputer****Description**

The CXP50120/CXP50124 is a CMOS 4-bit micro-computer which consists of 4-bit CPU, ROM, RAM, I/O port, 8-bit timer, 8-bit timer/counter, 18-bit time base timer, 8-bit serial I/O, vector interruption, power on reset function, fluorescent display tube controller/driver, D/A conversion PWM output port, a remote control receive circuit, 3-bit A/D converters, a 32kHz timer/event counter 8-bit timer and a power supply voltage detection reset function. They are integrated into a single chip with the standby function, etc. which are to be operated at a low power consumption.

**Features**

- Instruction cycle    1.9 $\mu$ s/4.19MHz  
                               122 $\mu$ s/32kHz  
                               (Selectable at programming)
- ROM capacitance  
                               20,480 $\times$ 8 bits (CXP50120)  
                               24,576 $\times$ 8 bits (CXP50124)
- RAM capacitance                               544 $\times$ 4 bits  
   (Display area included)
- 51 general purpose I/O ports
- 8 large current ports (Ports C, D)
- Fluorescent display tube controller/driver  
   (Maximum 256 segments display possible)
   — 1 to 16 digits dynamic scan display  
       (1 to 8 digits at 24 segments)
   — Page mode/variable mode
   — Dimmer function
   — High tension proof output (40V)
   — Pull-down resistance  
       (mask option for each bit)
- 14-bit PWM output for D/A conversion
- Remote control receiving circuit  
   (Be independent of the timer/counter)
- 3-bit A/D converter (8 channels per circuit)
- 32kHz reload timer/event counter

80pin QFP (Plastic)

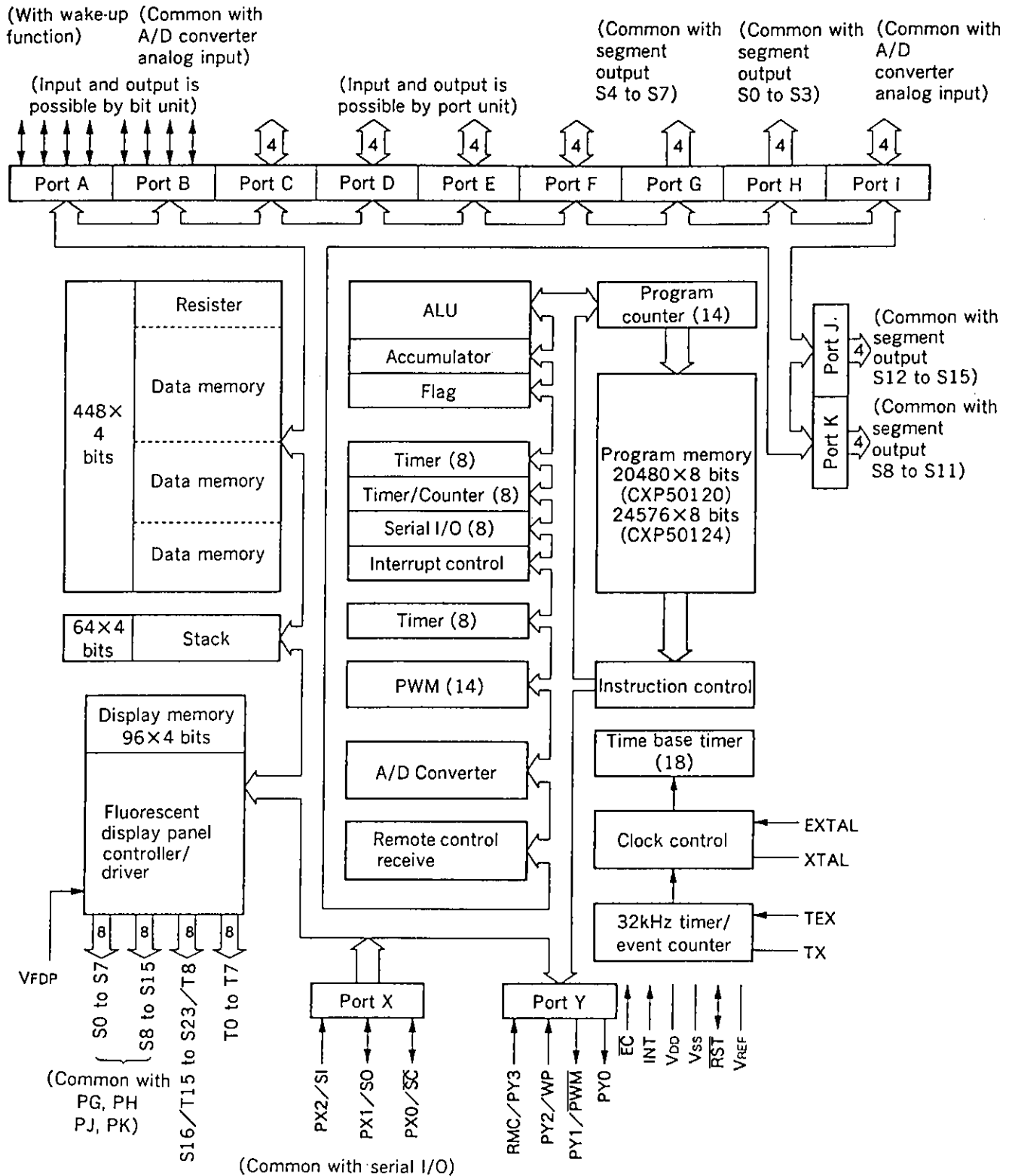


- Power supply voltage detection reset circuit
- Rich wake-up functions  
   WP pin  
   4 general purpose ports (edge detection)  
   32kHz timer/counter  
   Remote control receiving circuit
- 8-bit/4-bit variable prescaler serial I/O
- 8-bit timer with prescaler, 8-bit timer with prescaler/event counter and 18-bit time base timer, 8-bit reload timer with prescaler, independently controlled
- Arithmetic and logical operations possible between the entire ROM area, I/O area and the accumulator by means of memory mapped I/O
- Reference to the entire ROM area is possible with the table look-up instruction
- 2 kinds of power down modes, sleep and stop
- Power on reset circuit (mask option)
- Provided with 80-pin plastic QFP
- Provided with 80-pin piggyback QFP (CXP50100)

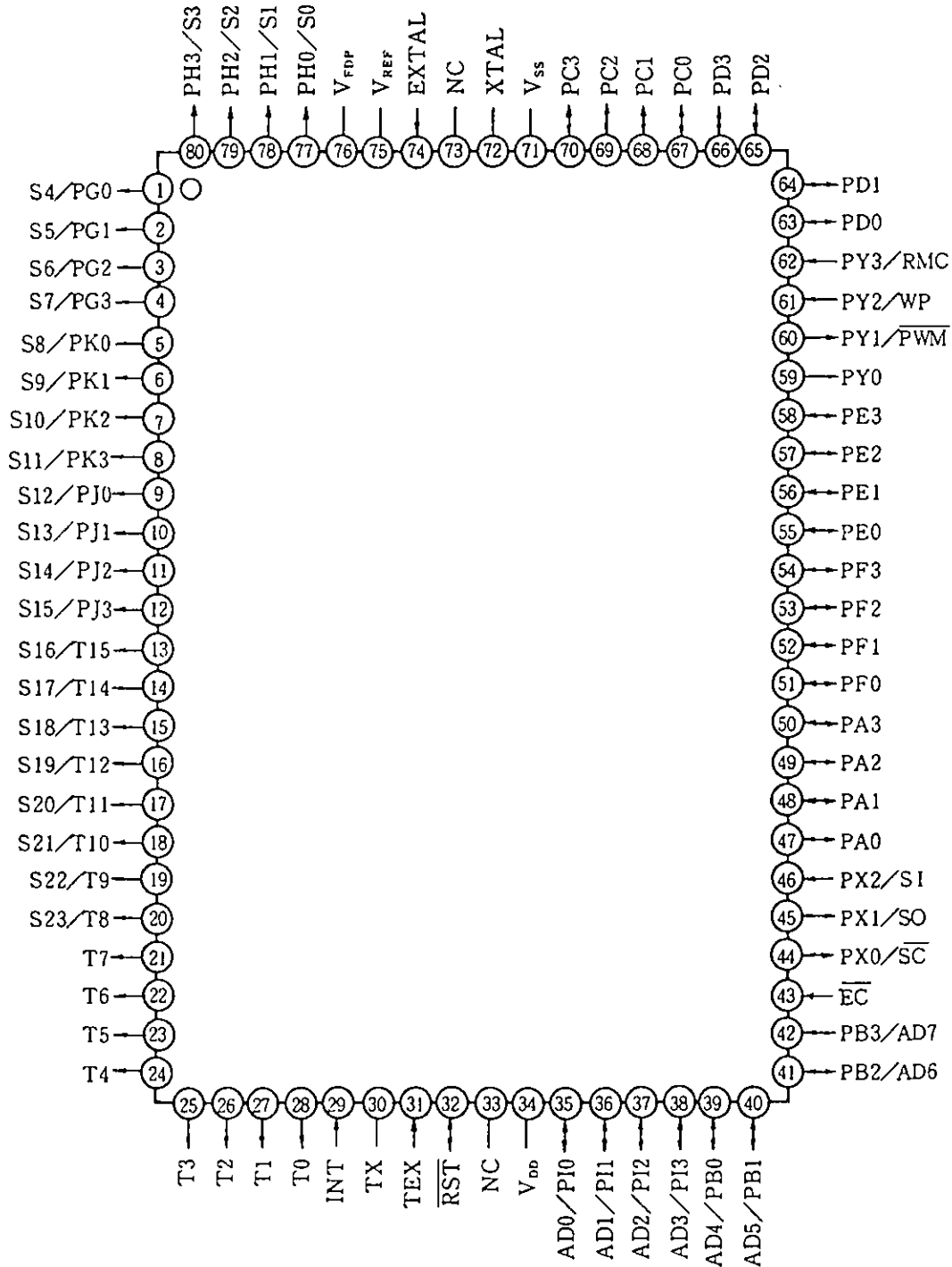
**Structure**

Silicon gate CMOS IC

Block Diagram



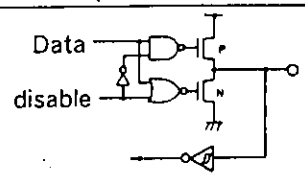
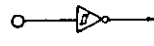
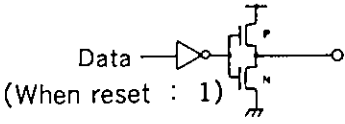
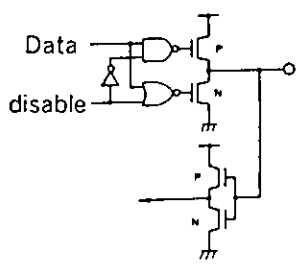
Pin Configuration (Top View)

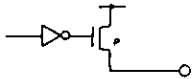
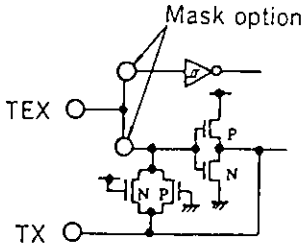


Note) Do not make any connections to NC pins.

Pin Description

| Symbol                  | Name                 | I/O | Description  | Equivalent circuit  |
|-------------------------|----------------------|-----|--|---|
| V <sub>DD</sub>         | Supply voltage       | —   | Positive power supply pin  |   |
| V <sub>SS</sub>         | Grounding voltage    | —   | GND pin  |   |
| EXTAL                   | Clock input          | I   | Clock generation circuit input pin. Connect the crystal oscillator or ceramic resonator between the EXTAL and XTAL. To use an external clock input, connect the clock oscillation source to the EXTAL pin and open the XTAL pin. |   |
| XTAL                    | Clock output         | O   | Output pin of the clock generation circuit   |   |
| $\overline{\text{RST}}$ | Reset                | I/O | Serves as the incorporated power on reset circuit output pin. When inputting a reset signal from the outside, provide 2 instruction cycles or longer of an "L" level (0V).   | <p>Mask option</p> <p>Output pull-up resistor (P-ch Tr)<br/>N-ch Tr output<br/>Schmitt inverter input</p> |
| INT                     | External interrupt   | I   | Serves as interrupt input pin. Permits the selection with a program of the edge and the level modes.   | <p>Schmitt inverter</p>   |
| EC                      | Event count input    | I   | Event counter input pin  |   |
| SI/PX2                  | Serial input Port X  | I   | Doubles as a serial interface (8 bits) input pin and as bit "2" (input) of port X  |   |
| SO/PX1                  | Serial output Port X | I/O | Doubles as a serial interface (8 bits) output pin and as bit "1" (input) of port X   | <p>3-state output or pull-up resistor output possible<br/>Inverter input</p>                              |

| Symbol               | Name                           | I/O | Description   | Equivalent circuit   |
|----------------------|--------------------------------|-----|---|--|
| $\overline{SC}/PX0$  | Serial clock<br>Port X         | I/O | Doubles as clock input/output pin for the serial interface and as bit "0" (input) of port X   |  <p>3-state output or pull-up resistor output possible<br/>Schmitt input</p>    |
| RMC/PY3              | Remote control input<br>Port Y | I   | Doubles as a remote control receiver input pin and as bit "3" (input) of port Y   |  <p>Schmitt inverter</p>  |
| WP/PY2               | Wake-up input<br>Port Y        | I   | Doubles as a wake-up input pin to release the standby state and as bit "2" (input) of port Y.   |  |
| $\overline{PWM}/PY1$ | PWM output<br>Port Y           | O   | Doubles as a PWM generator (14 bits) output and as bit "1" (output) of port Y   |  <p>Inverter output</p>   |
| PY0                  | Port Y                         | O   | Output pin for bit "0" of port Y  |  |
| PA0toPA3             | Port A                         | I/O | This 4-bit input/output port permits its each individual port to be programmed to serve for input or output. Its output format is a 3-state or pull-up resistor output. |  <p>3-state output or pull-up resistor output possible<br/>Inverter input</p> |
| PB0/AD4toPB3/AD7     | Port B/<br>Analog input        | I/O | This 4-bit input/output port has the functions that are equivalent to those of port A. It is also used for A/D converter input.   |  |
| PC0toPC3             | Port C                         | I/O | This 4-bit input/output port permits its each individual port to be programmed to serve for input or output. Its output format is a 3-state or pull-up resistor output. |  |
| PD0toPD3             | Port D                         | I/O | This 4-bit input/output port has the functions that are equivalent to those of port C.  |  |
| PE0toPE3             | Port E                         | I/O | This 4-bit input/output port has the functions that are equivalent to those of port C.  |  |
| PF0toPF3             | Port F                         | I/O | This 4-bit input/output port has the functions that are equivalent to those of port C.  |  |
| PI0/AD0toPI3/AD3     | Port I/<br>Analog input        | I/O | This 4-bit input/output port has the functions that are equivalent to those of port C. It is also used for A/D converter input.   |  |

| Symbol               | Name                       | I/O | Description   | Equivalent circuit   |
|----------------------|----------------------------|-----|---|--|
| $V_{FDP}$            | Power supply for FDP       | —   | Load power supply pin needed when load resistance is built in to output driver for FDP (Fluorescent Display Tube).  |  |
| T0toT7               | Timing                     | 0   | Lower 8-digit output pin of the FDP timing signal   |  <p>P-ch open drain output<br/>Pull-down resistance<br/>(Mask option)</p> |
| T8/S23to<br>T15/S16  | Timing/<br>Segment         | 0   | Combination output pin of higher 8-digit of the FDP timing signal and as the segment signal   |  |
| PG0/S4to<br>PG3/S7   | Port G/<br>Segment         | 0   | Doubles as 4-bit output port and as FDP segment signal output   |  |
| PH0/S0to<br>PH3/S3   | Port H/<br>Segment         | 0   | The same as Port G  |  |
| PJ0/S12to<br>PJ3/S15 | Port J/<br>Segment         | 0   | The same as Port G  |  |
| PK0/S8to<br>PK3/S11  | Port K<br>Segment          | 0   | The same as Port G  |  |
| TEX                  | 32kHz T/C<br>Clock input   | 1   | Input pin of the 32kHz timer clock generation circuit. Connect 32.768kHz crystal oscillator between TEX and TX. To use as event clock input, connect the clock oscillation source to the TEX pin and open the TX pin. |    |
| TX                   | 32kHz T/C<br>Clock output  | 0   | Output pin of the clock generation circuit  |  |
| $V_{REF}$            | Reference voltage<br>input | 1   | Reference voltage input for power supply voltage reset circuit. Connect the zener diode normally.   |  |

Absolute Maximum Ratings ( $T_a = -20^\circ\text{C}$  to  $+75^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ )

| Item                            | Symbol           | Ratings                              | Unit             | Remarks  |
|---------------------------------|------------------|--------------------------------------|------------------|--|
| Power supply voltage            | $V_{DD}$         | $-0.3\text{ to }+7.0$                | V                |  |
| Input voltage                   | $V_{IN}$         | $-0.3\text{ to }+7.0^{*1}$           | V                |  |
| Output voltage                  | $V_{OUT}$        | $-0.3\text{ to }+7.0^{*1}$           | V                |  |
| Display output voltage          | $V_{OD}$         | $V_{DD} - 40\text{ to }V_{DD} + 0.3$ | V                | As P channel transistor is open drain, $V_{DD}$ voltage is determined as standard. |
| High level output current       | $I_{OH}$         | -5                                   | mA               | Other than display output pins*2 : per pin   |
|                                 | $I_{ODH1}$       | -15                                  | mA               | Display output S0 to S15 : per pin   |
|                                 | $I_{ODH2}$       | -35                                  | mA               | Display output T0 to T7, T8/S23 to T15/S16 : per pin                               |
| High level total output current | $\Sigma I_{OH}$  | -40                                  | mA               | Total of other than display output pins  |
|                                 | $\Sigma I_{ODH}$ | -100                                 | mA               | Total of display output pins   |
| Low level output current        | $I_{OL}$         | 15                                   | mA               | Port 1 pin   |
|                                 | $I_{OLC}$        | 20                                   | mA               | High current port : per pin*3  |
| Low level total output current  | $\Sigma I_{OL}$  | 100                                  | mA               | Total of entire pins   |
| Operating temperature           | $T_{opr}$        | $-20\text{ to }+75$                  | $^\circ\text{C}$ |  |
| Storage temperature             | $T_{stg}$        | $-55\text{ to }+150$                 | $^\circ\text{C}$ |  |
| Allowable power dissipation     | $P_D$            | 600                                  | mW               |  |

\*1)  $V_{IN}$  and  $V_{OUT}$  should not exceed  $V_{DD} + 0.3\text{V}$ .

\*2) Specifies the output current of the general purpose I/O port PA to PF, PI, SO,  $\overline{\text{SC}}$ , PY0 and PY1.

\*3) The high current operation transistors are the N-ch transistors of ports PC and PD.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions ( $V_{SS} = 0\text{V}$ )

| Item                     | Symbol            | Min.           | Max.           | Unit             | Remarks   |
|--------------------------|-------------------|----------------|----------------|------------------|---|
| Power supply voltage     | $V_{DD}$          | 4.5            | 5.5            | V                | Guaranteed range of operation by EXTAL clock  |
|                          |                   | 2.5            | 5.5            | v                | Guaranteed range of operation by TEX clock, guaranteed range of data hold during STOP |
| High level input voltage | $V_{IH}$          | $0.7V_{DD}$    | $V_{DD}$       | V                |   |
|                          | $V_{IHS}$         | $0.8V_{DD}$    | $V_{DD}$       | V                | Hysteresis input*1  |
|                          | $V_{IH\text{EX}}$ | $V_{DD} - 0.4$ | $V_{DD} + 0.3$ | V                | EXTAL pin*2   |
| Low level input voltage  | $V_{IL}$          | 0              | $0.3V_{DD}$    | V                |   |
|                          | $V_{ILS}$         | 0              | $0.2V_{DD}$    | V                | Hysteresis input*1  |
|                          | $V_{IL\text{EX}}$ | -0.3           | 0.4            | V                | EXTAL pin*2   |
| Operating temperature    | $T_{opr}$         | -20            | +75            | $^\circ\text{C}$ |   |

\*1) The TEX pin when the counter mode is selected by each of INT,  $\overline{\text{EC}}$ , PX0, PX2, PY2, PY3 and  $\overline{\text{RST}}$  pins and mask option.

\*2) Specified only during external clock input.

Electrical Characteristics

DC characteristics (Ta = -20°C to +75°C, V<sub>SS</sub> = 0V)

| Item   | Symbol  | Pin  | Condition  | Min. | Typ. | Max. | Unit |
|--|---|--|--|------|------|------|------|
| High level output voltage                                | V <sub>OH</sub>   | PA~PF, PI  | V <sub>DD</sub> = 4.5V, I <sub>OH</sub> = -0.5mA                     | 4.0  |      |      | V    |
|  |   | PX0, PX1   | V <sub>DD</sub> = 4.5V, I <sub>OH</sub> = -1.0mA                     | 3.5  |      |      | V    |
| Low level output voltage                                 | V <sub>OL</sub>   | PY0, PY1   | V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 1.8mA                      |      |      | 0.4  | V    |
|  |   | RST(V <sub>OL</sub> only)  | V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 3.6mA                      |      |      | 0.6  | V    |
|  |   | PC, PD   | V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 12mA                       |      |      | 1.5  | V    |
| Input current  | I <sub>IHE</sub>  | EXTAL  | V <sub>DD</sub> = 5.5V, V <sub>IH</sub> = 5.5V                       | 0.5  |      | 40   | μA   |
|  | I <sub>IHE</sub>  |  | V <sub>DD</sub> = 5.5V, V <sub>IL</sub> = 0.4V                       | -0.5 |      | -40  | μA   |
|  | I <sub>IHT</sub>  | TEX* <sup>3</sup>  | V <sub>DD</sub> = 5.5V, V <sub>IH</sub> = 5.5V                       | 0.1  |      | 10   | μA   |
|  | I <sub>ILT</sub>  |  | V <sub>DD</sub> = 5.5V   | -0.1 |      | -10  | μA   |
|  | I <sub>ILR</sub>  | RST* <sup>2</sup>  | V <sub>IL</sub> = 0.4V   | -1.5 |      | -400 | μA   |
| Display output current                                   | I <sub>OH</sub>   | S0toS15  | V <sub>DD</sub> = 4.5V   | -7   |      |      | mA   |
|  |   | S16/T15toS23/T8<br>T0toT7  | V <sub>OH</sub> = V <sub>DD</sub> - 2.5V                             | -18  |      |      | mA   |
| Open drain output leakage current (P-ch Tr OFF in state) | I <sub>LOL</sub>  | S0toS15<br>S16/T15toS23/T8<br>T0toT7   | V <sub>DD</sub> = 5.5V<br>V <sub>OL</sub> = V <sub>DD</sub> - 35V    |      |      | -20  | μA   |
| Pull-down resistance* <sup>1</sup>                       | R <sub>L</sub>  | S0toS15<br>S16/T15toS23/T8<br>T0toT7   | V <sub>DD</sub> = 5V<br>V <sub>FDP</sub> = V <sub>DD</sub> - 35V     | 60   | 100  | 270  | kΩ   |
| High impedance I/O leakage current                       | I <sub>Iz</sub>   | PAtoPF, PI<br>PX0toPX2, PY2, PY3, EC<br>INT, TEX* <sup>3</sup> , RST* <sup>2</sup> | V <sub>DD</sub> = 5.5V<br>V <sub>I</sub> = 0, 5.5V                   |      |      | ±10  | μA   |
| Current power supply                                     | I <sub>DD1</sub>  | V <sub>DD</sub>  | Entire output pins open  |      | 7    | 20   | mA   |
|  |   |  | V <sub>DD</sub> = 5.5V, 4.19MHz crystal oscillation (C1 = C2 = 22pF) |      |      |      |      |
|  | I <sub>DD2</sub>  |  | V <sub>DD</sub> = 3V, 32kHz crystal oscillation (C1 = C2 = 18pF)     |      | 50   | 250  | μA   |
|  | I <sub>DDSP1</sub>  |  | SLEEP mode   |      | 5    | 12   | mA   |
|  |   |  | V <sub>DD</sub> = 5.5V, 4.19MHz oscillation                          |      |      |      |      |
|  | I <sub>DDSP2</sub>  |  | V <sub>DD</sub> = 3V, 32kHz oscillation                              |      | 40   | 200  | μA   |
|  | I <sub>DDs1</sub>   |  | STOP mode  |      | 7    | 40   | μA   |
| V <sub>DD</sub> = 3V, 32kHz with T/C                     |   |  |  |      |      |      |      |
| I <sub>DDs2</sub>  | V <sub>DD</sub> = 5.5V, 32kHz without T/C (For mask option select counter, Pin is fixed.) |  |  | 10   | μA   |      |      |
| Input capacitance  | C <sub>IN</sub>   | PAtoPF, PI, PX<br>PY2, PY3,<br>EXTAL,<br>TEX, RST, INT, EC                         | F <sub>C</sub> = 1MHz<br>0V other than the measured pins             |      | 10   | 20   | pF   |

\*1) In case the incorporated pull-down resistance has been selected with mask option.

\*2) RST pin specifies the input current when the pull-up resistance is selected, and specifies leakage current when nonresistance is selected.

\*3) The TEX pin specifies the input current when the 32kHz oscillation is selected by the mask option, and specifies the leakage current when the counter mode is selected.

**AC characteristics**(1) Clock timing ( $T_a = -20^{\circ}\text{C}$  to  $+75^{\circ}\text{C}$ ,  $V_{DD} = 4.5\text{V}$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

| Item   | Symbol               | Pin             | Condition                                | Min.                      | Typ.   | Max. | Unit          |
|--|----------------------|-----------------|--|---------------------------|--------|------|---------------|
| System clock frequency                           | $f_c$                | XTAL<br>EXTAL   | Fig.1, Fig.2                             | 1                         |        | 5    | MHz           |
| System clock input pulse width                   | $t_{XL}$<br>$t_{XH}$ | EXTAL           | Fig.1, Fig.2<br>External clock drive     | 90                        |        |      | ns            |
| System clock input rising and falling times      | $t_{CR}$<br>$t_{CF}$ | EXTAL           | Fig.1, Fig.2<br>External clock drive     |                           |        | 200  | ns            |
| System clock frequency                           | $f_{CS}$             | TEX*2<br>TX     | $V_{DD} = 2.5$ to $5.5\text{V}$<br>Fig.3 |                           | 32.768 |      | kHz           |
| Event count clock input pulse width              | $t_{EL}$<br>$t_{EH}$ | $\overline{EC}$ | Fig.4                                    | $t_{sys}^{*1}$<br>$+0.05$ |        |      | $\mu\text{s}$ |
| Event count clock input rising and falling times | $t_{ER}$<br>$t_{EF}$ | $\overline{EC}$ | Fig.4                                    |                           |        | 20   | ms            |
| Event count input clock pulse width              | $t_{TL}$<br>$t_{TH}$ | TEX*3           | Fig.4                                    | 10                        |        |      | $\mu\text{s}$ |
| Event count input clock rising and falling times | $t_{TR}$<br>$t_{TF}$ | TEX*3           | Fig.4                                    |                           |        | 20   | ms            |

\*1)  $t_{sys}$  in the EXTAL input clock is  $t_{sys} = 8/f_c$  $t_{sys}$  in the TEX input clock is  $t_{sys} = 4/f_{cs}$ 

\*2) Specified when the crystal oscillation mode is selected by the mask option.

\*3) Specified when the counter mode is selected by the mask option

Note) When adjusting the frequency accurately, there may be cases in which they may differ from Fig.2.

Fig.1 Clock timing

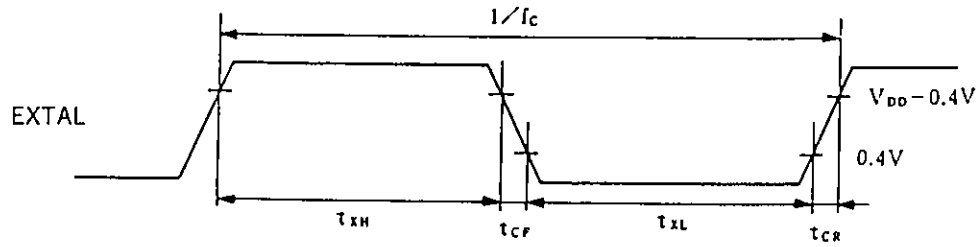


Fig.2 Clock applying condition

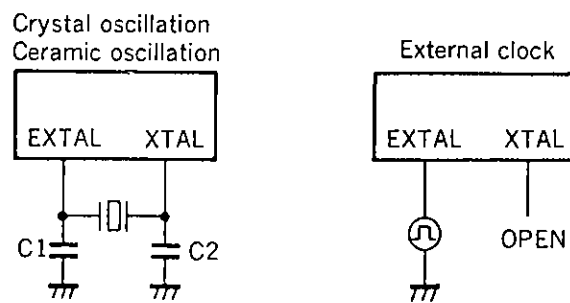


Fig.3 32kHz clock applying condition

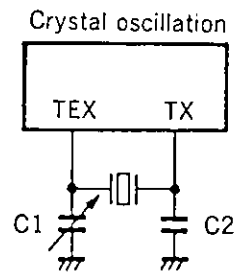
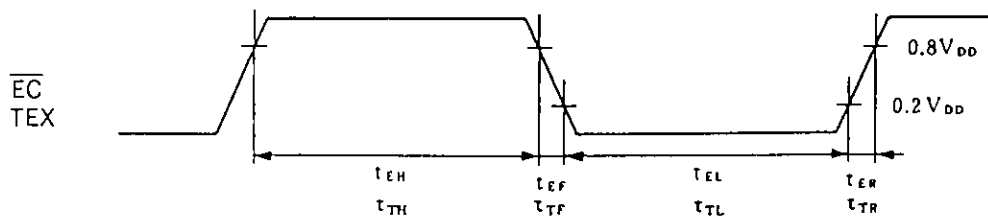


Fig.4 Event count clock timing



(2) Serial transfer ( $T_a = -20^{\circ}\text{C}$  to  $+75^{\circ}\text{C}$ ,  $V_{DD} = 4.5\text{V}$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

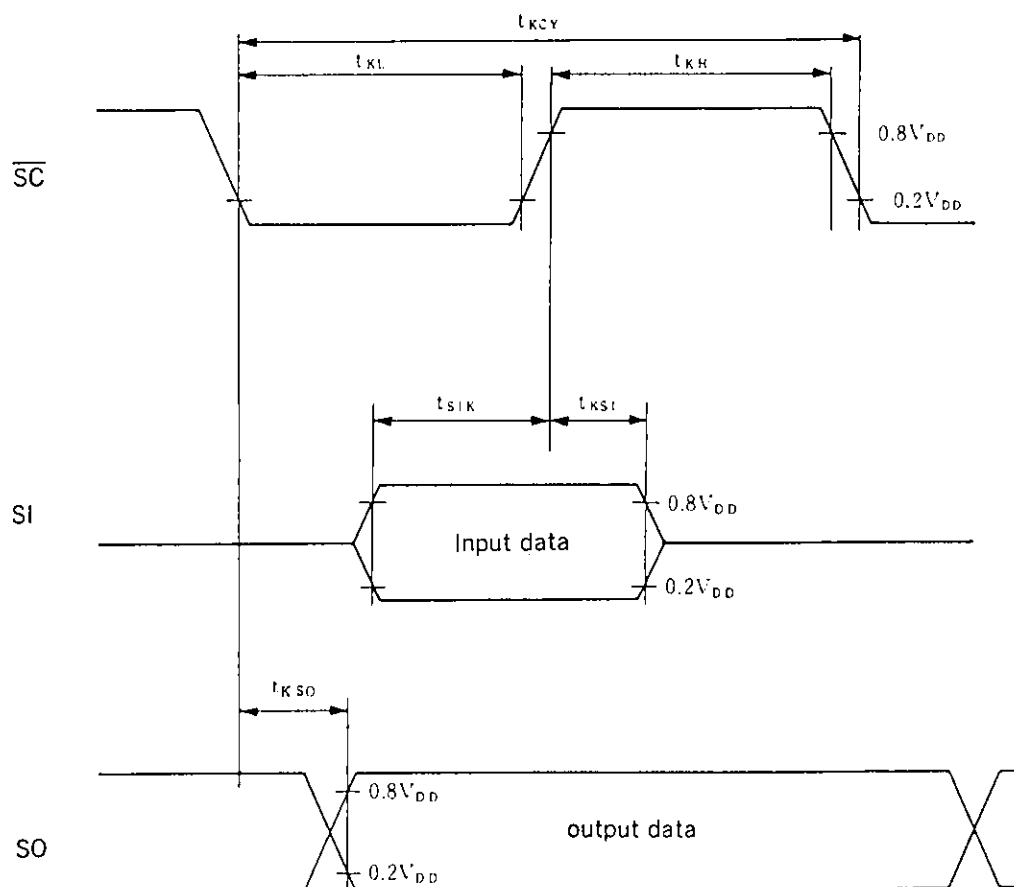
| Item   | Symbol                             | Pin                    | Condition                          | Min.                    | Max.                   | Unit          |
|--|------------------------------------|------------------------|------------------------------------|-------------------------|------------------------|---------------|
| Serial transfer clock ( $\overline{\text{SC}}$ ) cycle time                | $t_{\text{KCY}}$                   | $\overline{\text{SC}}$ | Input mode                         | $t_{\text{sys}}/4+1.42$ |                        | $\mu\text{s}$ |
|  |                                    |                        | Output mode                        | $t_{\text{SIO}}$        |                        | $\mu\text{s}$ |
| Serial transfer clock ( $\overline{\text{SC}}$ ) high and low level widths | $t_{\text{KH}}$<br>$t_{\text{KL}}$ | $\overline{\text{SC}}$ | Input mode                         | $t_{\text{sys}}/8+0.7$  |                        | $\mu\text{s}$ |
|  |                                    |                        | Output mode                        | $t_{\text{SIO}}/2-0.1$  |                        | $\mu\text{s}$ |
| Serial data input setup time (against $\overline{\text{SC}} \uparrow$ )    | $t_{\text{SIH}}$                   | SI                     | $\overline{\text{SC}}$ input mode  | 0.1                     |                        | $\mu\text{s}$ |
|  |                                    |                        | $\overline{\text{SC}}$ output mode | 0.2                     |                        | $\mu\text{s}$ |
| Serial data input hold time (against $\overline{\text{SC}} \uparrow$ )     | $t_{\text{KSI}}$                   | SI                     | $\overline{\text{SC}}$ input mode  | $t_{\text{sys}}/8+0.5$  |                        | $\mu\text{s}$ |
|  |                                    |                        | $\overline{\text{SC}}$ output mode | 0.1                     |                        | $\mu\text{s}$ |
| Data output delay time from $\overline{\text{SC}}$ falling                 | $t_{\text{KSO}}$                   | SO                     |                                    |                         | $t_{\text{sys}}/8+0.5$ | $\mu\text{s}$ |

Note) 1.  $t_{\text{sys}}$  in the EXTAL input clock is  $t_{\text{sys}} = 8/f_c$  (It cannot be used in the TEX input clock.)

$t_{\text{SIO}}$  is turned into either  $2t_{\text{sys}}$ ,  $4t_{\text{sys}}$  or  $16t_{\text{sys}}$  by means of a program.

Note) 2. The load of data output delay time is  $50\text{pF} + 1\text{TTL}$ .

Fig.5 Serial transfer timing



(3) A/D converter (Ta = -20°C to +75°C, V<sub>SS</sub> = 0V)

| Analog input voltage | Pin        | Condition            | Digital conversion value |
|----------------------|------------|----------------------|--------------------------|
| 0.0 to 0.33V         | AD0 to AD7 | V <sub>DD</sub> = 5V | 000                      |
| 0.82 to 1.29V        |            |                      | 001                      |
| 1.78 to 2.21V        |            |                      | 010                      |
| 2.69 to 3.06V        |            |                      | 011                      |
| 3.56 to 4.06V        |            |                      | 100                      |
| 4.62 to 5.0V         |            |                      | 101                      |

Note) The digital conversion value are the values when FF<sub>H</sub> address in the program are read.

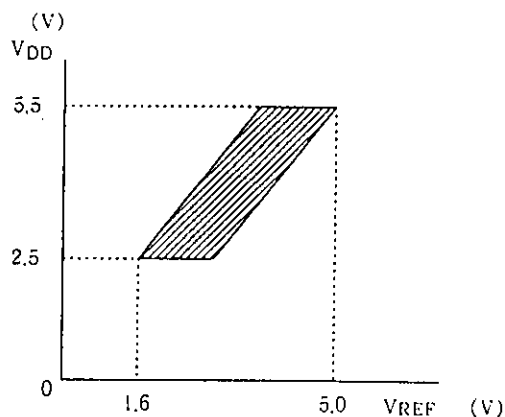
(4) Power supply voltage detection reset function (Ta = -20°C to +75°C, V<sub>SS</sub> = 0V)

| Item  | Symbol            | Pin             | Condition  | Min. | Typ. | Max. | Unit |
|---|-------------------|-----------------|--|------|------|------|------|
| Power supply voltage detection reset function operating voltage range | V <sub>LPOP</sub> | V <sub>DD</sub> | Voltage range allowing system operation (32kHz system operation at V <sub>DD</sub> = 4.5V or less.)          | 2.5  |      | 5.5  | V    |
| Power supply voltage drop detection function                          | V <sub>POP</sub>  | V <sub>DD</sub> | When V <sub>REF</sub> pin voltage is 3.3V Flag set during voltage falling System reset during voltage rising | 3.8  | 4.0  | 4.2  | V    |

The chart in Fig.6 shows the relationship between the power supply voltage V<sub>DD</sub> and reference voltage V<sub>REF</sub> of the power supply voltage detection reset function.

Note) The chart in Fig.6 serves as guide to the function operation area obtained using average devices. Individual adjustment is needed when zener diodes and others are connected to the V<sub>REF</sub> pin.

Fig.6 Power supply voltage detection reset function chart



(5) Others (Ta = -20°C to +75°C, V<sub>DD</sub> = 4.5V to 5.5V, V<sub>SS</sub> = 0V)

| Item  | Symbol                              | Pin | Condition           | Min.                    | Max. | Unit |
|---|-------------------------------------|-----|---------------------|-------------------------|------|------|
| External interruption high and low level widths | t <sub>IH</sub> , t <sub>IL</sub>   | INT | Edge detection mode | t <sub>sys</sub> + 0.05 |      | μs   |
| Reset input low level width                     | t <sub>RSL</sub>                    | RST |                     | 2t <sub>sys</sub> *1    |      | μs   |
| Wake-up input high level width                  | t <sub>WPH</sub>                    | WP  | STOP mode           | 500                     |      | ns   |
|   |                                     |     | SLEEP mode          | t <sub>sys</sub> + 0.05 |      | μs   |
| Wake-up input high and low level widths         | t <sub>PWH</sub> , t <sub>PWL</sub> | PA  |                     | 500                     |      | ns   |

Note) t<sub>sys</sub> in the EXTAL input clock is 8/fc

t<sub>sys</sub> in the TEX input clock is 4/fc

\*1) For reset during operating in TEX input clock, hold the low level more than the oscillation stabilizing time of EXTAL input clock.

Fig.7 Interruption input timing

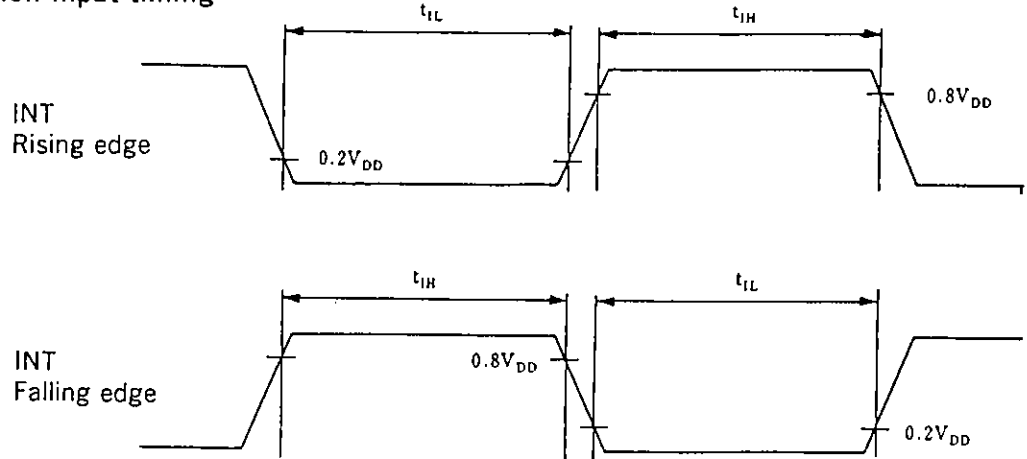


Fig.8 Reset input timing

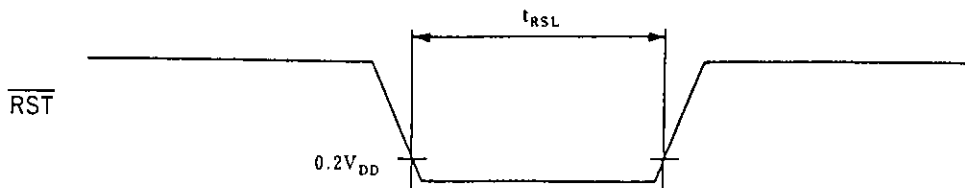


Fig.9 Wake-up input timing

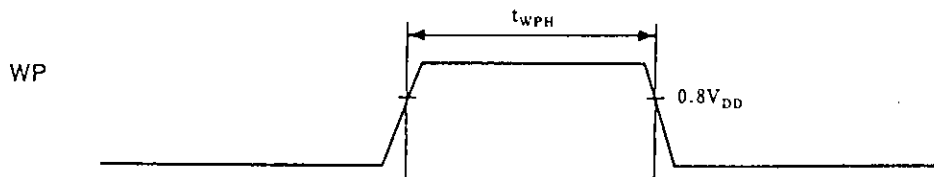
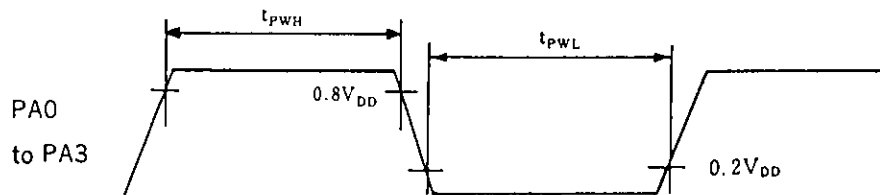


Fig.10 Wake-up input timing

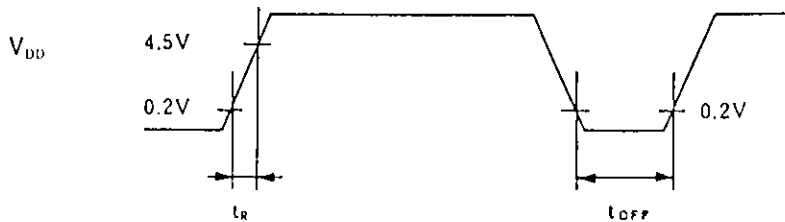


Power on reset\* ( $T_a = -20^{\circ}C$  to  $+75^{\circ}C$ ,  $V_{SS} = 0V$ )

| Item                      | Symbol    | Pin      | Condition                 | Min. | Max. | Unit |
|---------------------------|-----------|----------|---------------------------|------|------|------|
| Power supply rising time  | $t_R$     | $V_{DD}$ | Power on reset            | 0.05 | 50   | ms   |
| Power supply cut-off time | $t_{OFF}$ |          | Repetitive power on reset | 1    |      | ms   |

\* Specified only when power on reset function is selected.

Fig.11 Power on reset

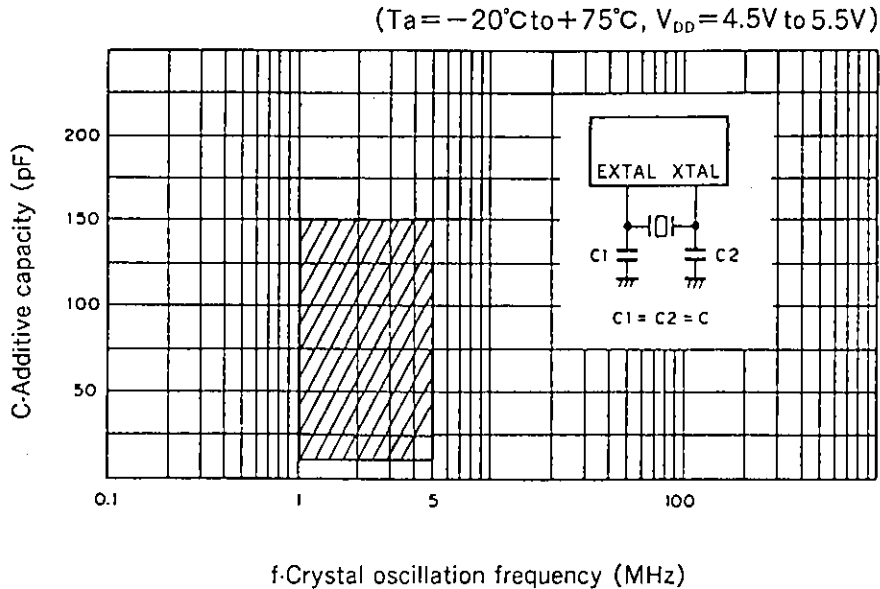


The power supply should rise smoothly.

Notes on Operation

See Fig.12 additive capacity calculation chart and select the appropriate capacity when using the crystal oscillator.

Fig.12 Crystal oscillation circuit additive capacity calculation chart

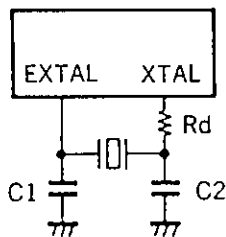


(Note) The above chart shows a range in which the average quartz resonator has a relatively fast oscillation rising edge and stable characteristics. The capacity should be selected to correspond to the appropriate constant for each quartz resonator, should the frequency of the quartz resonator be accurately adjusted.

Fig.13 shows recommended circuits and oscillators. Use the trimmer capacitor to C1, in the case of accurate adjustment of the oscillation frequency.

Fig.13 Oscillation recommended circuit

( i ) Main clock (4.19MHz)

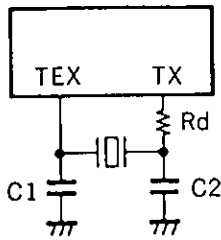


(i)

| Manufacturer         | Model         | Frequency | C1           | C2           | Rd |
|----------------------|---------------|-----------|--------------|--------------|----|
| MURATA MFG CO., LTD. | CSA4.19MG040  | 4.19 MHz  | 100pF        | 100pF        | —  |
|                      | CST4.19MGW040 | 4.19 MHz  | — (built in) | — (built in) | —  |

| Manufacturer                | Model     | Frequency | C1                  | C2   | Rd    |
|-----------------------------|-----------|-----------|---------------------|------|-------|
| CITIZEN WATCH CO., LTD.     | CSA-309   | 4.19 MHz  | 10pF (20pF trimmer) | 10pF | —     |
| NIHON DENPA KOGYO CO., LTD. | AT-51     | 4.19 MHz  | 15pF (20pF trimmer) | 15pF | 6.8kΩ |
| KINSEKI LTD.                | HC-49/U-S | 4.19 MHz  | 22pF                | 22pF | 3.3kΩ |

(ii) Sub clock (32kHz)

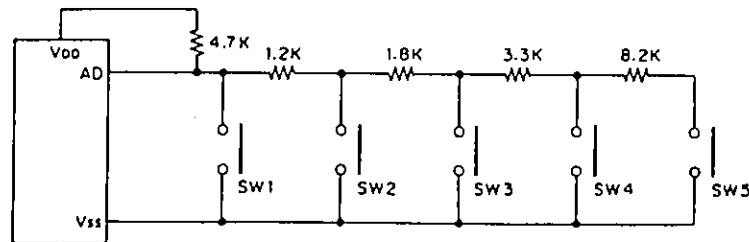


(ii)

| Manufacturer                | Model   | Frequency  | C1                  | C2   | Rd    |
|-----------------------------|---------|------------|---------------------|------|-------|
| CITIZEN WATCH CO., LTD.     | CFS-308 | 32.768 kHz | 18pF (20pF trimmer) | 18pF | —     |
| NIHON DENPA KOGYO CO., LTD. | MX-38T  | 32.768 kHz | 22pF (20pF trimmer) | 22pF | 470kΩ |
| KINSEKI LTD.                | P3      | 32.768 kHz | 22pF (20pF trimmer) | 22pF | 330kΩ |

When using the A/D converter as the key input, it is recommended that the circuit structure shown in Fig.14 be used.

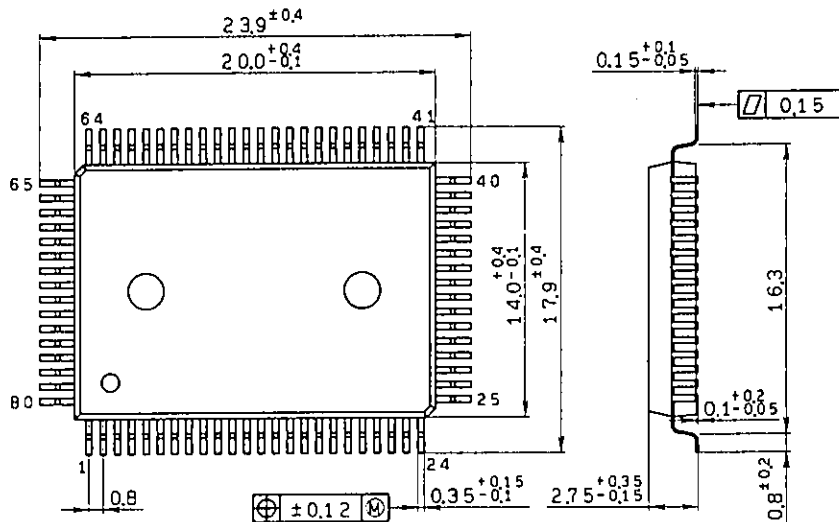
Fig.14 Recommended example of key input circuit by A/D converter



(Precision of resistance is all within  $\pm 5\%$ )

Package Outline Unit : mm

80pin QFP (Plastic) 1.6g



|            |                 |
|------------|-----------------|
| SONY NAME  | QFP-80P-L01     |
| EIAJ NAME  | QFP080-P-1420-A |
| JEDEC CODE |                 |



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