SONY

CXD2720Q-2

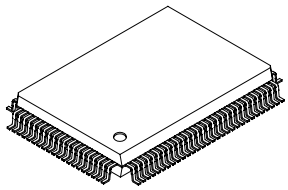
Single-Chip Digital Signal Processor for Karaoke

Description

The CXD2720Q-2 is a digital signal processor LSI for Karaoke, suitable for use in LD/CD/CD-G/video CD and the like.

A large capacity DRAM and AD/DA converters are built in, and Karaoke functions such as key control and microphone echo are contained on a single chip.

100 pin QFP (Plastic)



Features

- 3-channel 1-bit AD converter and decimation filter
  S/N ratio: 88 dB
  THD + N: 0.016%
  Filter pass band ripple: less than ±0.008dB
  Filter stop band attenuation: less than –62dB
  (all characteristics are typical values)
- 2-channel 1-bit DA converter and oversampling filter
  S/N ratio: 98dB
  THD + N: 0.006%
  Filter pass band ripple: less than ±0.2dB
  Filter stop band attenuation: less than –41dB
  (all characteristics are typical values)
- In addition to analog input/output, 2-channel input/2-channel output of digital input/output are provided. The interface also supports a variety of formats.
- 128K-bit DRAM for key control and microphone echo processing

Functions

- Key controller pitch setting can be varied to a maximum of ±1 octave with a precision of 14 bits
- Two key controllers are provided.
  For their pitches, either of common or independent setting is possible
- Key controller can be used for voice
- Microphone echo delay time can be varied to a maximum of 185ms (when fs = 44.1kHz)
- Voice parametric equalizer
- Mixing function to support sound multiplexing software
- Digital de-emphasis function
- Soft mute function

Structure

Silicon gate CMOS

Applications

Equipment having Karaoke function, such as LD/CD, compact music center, video games, etc.

Absolute Maximum Ratings

(Ta = 25°C, V_{SS} = 0V)

• Supply voltage	V_{DD}	V_{SS} – 0.5 to +7.0	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5 (5.0 typ.)	V
• Operating temperature	Ta	–20 to +75	°C

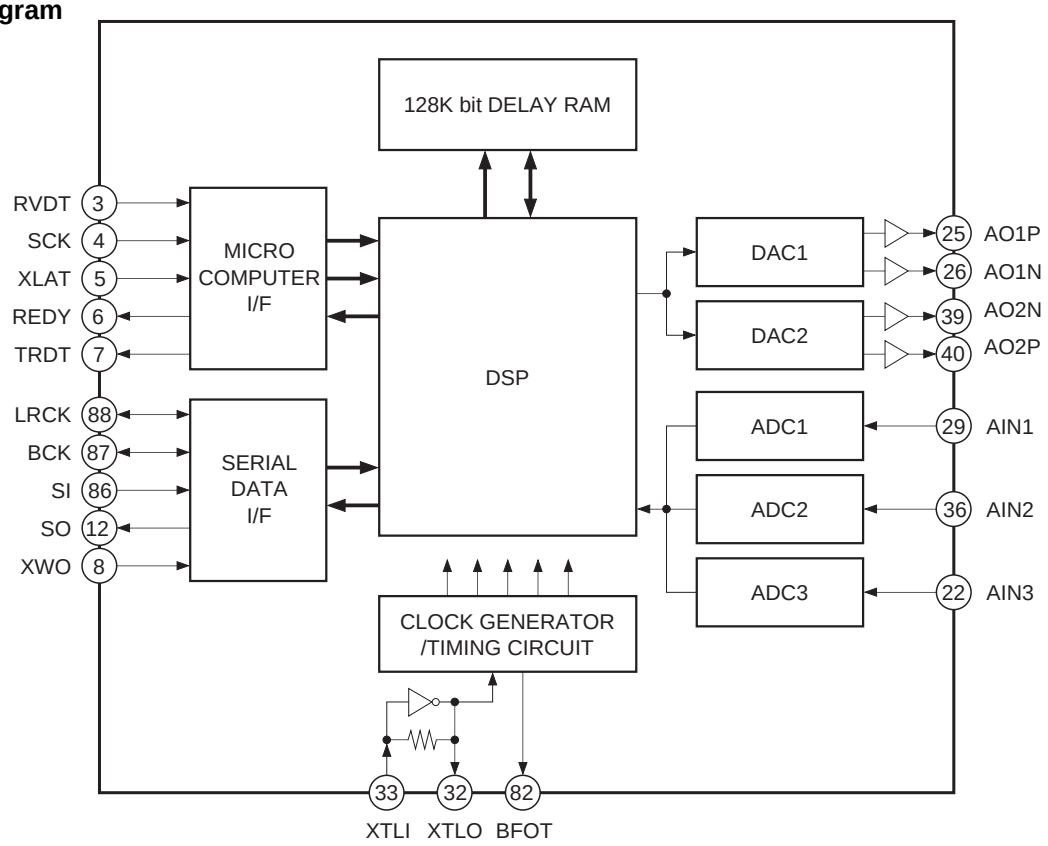
Input/Output Capacitance

• Input capacitance	C_{IN}	9 (max.)	pF
• Output capacitance	C_{OUT}	11 (max.)	pF
• Input/output capacitance	$C_{I/O}$	11 (max.)	pF

* Measurement conditions: V_{DD} = V_I = 0V, F = 1MHz

E97315-PS

Block Diagram



Pin Configuration

Pin Description

Pin No.	Symbol	I/O	Description
1	AV_S0	—	DRAM digital GND.
2	$V_{SS}0$	—	Digital GND.
3	RVDT	I	Data input for microcomputer interface.
4	SCK	I	Shift clock input for microcomputer interface.
5	XLAT	I	Latch input for microcomputer interface.
6	REDY	O	Transmission enabling signal output for microcomputer interface. Transmission prohibited when Low.
7	TRDT	O	Serial data output for microcomputer interface.
8	XWO	I	Window open input for synchronization. Normally High.
9	XRST	I	System reset input. Resets when Low.
10	$V_{SS}1$	—	Digital GND.
11	$V_{DD}0$	—	Digital power supply.
12	SO	O	1-sampling 2-channel serial data output.
13	XS24	I	Serial data 24-/32-bit slot selection. 24-bit slot when Low. (valid for slave mode)
14	TST0	I	Test pin. Normally set Low.
15	TST1	I	Test pin. Normally set Low.
16	TST2	I	Test pin. Normally set Low.
17	TST3	I	Test pin. Normally set Low.
18	TST4	I	Test pin. Normally set Low.
19	TST5	I	Test pin. Normally set Low.
20	$V_{SS}2$	—	Digital GND.
21	AV_S3	—	CH3 AD converter GND.
22	AIN3	I	CH3 AD converter analog input (for microphone input).
23	AV_D3	—	CH3 AD converter power supply.
24	AV_D4	—	CH1 DA converter power supply.
25	AO1P	O	CH1 DA converter analog positive phase output.
26	AO1N	O	CH1 DA converter analog reversed phase output.
27	AV_S4	—	CH1 DA converter GND.
28	AV_S1	—	CH1 AD converter GND.
29	AIN1	I	CH1 AD converter analog input.
30	AV_D1	—	CH1 AD converter power supply.
31	XV_{DD}	—	Digital power supply for master clock.
32	XTLO	O	Crystal oscillator circuit output.
33	XTLI	I	Crystal oscillator circuit input.
34	XV_{SS}	—	Digital GND for master clock.
35	AV_S2	—	CH2 AD converter GND.

Pin No.	Symbol	I/O	Description
36	AIN2	I	CH2 AD converter analog input.
37	AV_D2	—	CH2 AD converter power supply.
38	AV_D5	—	CH2 DA converter power supply.
39	AO2N	O	CH2 DA converter analog reversed phase output.
40	AO2P	O	CH2 DA converter analog positive phase output.
41	AV_S5	—	CH2 DA converter GND.
42	$V_{SS}3$	—	Digital GND.
43	$V_{DD}1$	—	Digital power supply.
44 to 52	NC		Normally open.
53	$V_{SS}4$	—	Digital GND.
54 to 68	NC		Normally open.
69	$V_{SS}5$	—	Digital GND.
70	$V_{DD}2$	—	Digital power supply.
71 to 79	NC		Normally open.
80	$V_{SS}6$	—	Digital GND.
81	X768	I	Test input pin. Normally set Low.
82	BFOT	O	Clock, frequency-divider output (384fs).
83	INVI	I	Test pin. Normally set Low.
84	NC		Normally open.
85	NC		Normally open.
86	SI	I	1-sampling 2-channel serial data input.
87	BCK	I/O	Serial bit transmission clock for serial input/output data SI and SO.
88	LRCK	I/O	Sampling frequency clock for serial input/output data SI and SO.
89	XMST	I	BCK, LRCK master/slave mode switching input. Master mode when Low.
90	$V_{SS}7$	—	Digital GND.
91 to 98	NC		Normally open.
99	$V_{DD}3$	—	Digital power supply.
100	AV_D0	—	Digital power supply for DRAM.

DC Characteristics

(AV_D0 to 5 = XV_{DD} = $V_{DD}0$ to 3 = 5V ± 10%, AV_S0 to 5 = XV_{SS} = $V_{SS}0$ to 7 = 0V, Ta = –20 to +75°C)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Input voltage (1)	High level	V_{IH}		0.7V_{DD}			V	*1, *4, *5
	Low level	V_{IL}				0.3V_{DD}	V	*1, *4, *5
Input voltage (2)	High level	V_{IH}		0.8V_{DD}			V	*3
	Low level	V_{IL}				0.2V_{DD}	V	*3
Input voltage (3)		V_{IN}	Analog input	V_{SS}		V_{DD}	V	*2
Output voltage (1)	High level	V_{OH}	I_{OH} = –2.0mA	V_{DD} – 0.8			V	*6, *7, *8
	Low level	V_{OL}	I_{OL} = 4.0mA			0.4	V	*6, *7, *8, *9
Output voltage (2)	High level	V_{OH}	I_{OH} = –6.0mA	V_{DD} – 0.8			V	*10
	Low level	V_{OL}	I_{OL} = 4.0mA			0.4	V	*10
Output voltage (3)	High level	V_{OH}	I_{OH} = –12.0mA	V_{DD}/2			V	*11
	Low level	V_{OL}	I_{OL} = 12.0mA			V_{DD}/2	V	*11
Input leak current (1)		I_I	V_{IH} = V_{DD}, V_{SS}	–10		10	µA	*1, *3, *5
Input leak current (2)		I_I	V_{IH} = V_{DD}, V_{SS}	–40		40	µA	*4
Output leak current		I_{OZ}	V_{IH} = V_{DD}, V_{SS}	–40		40	µA	*8, *9
Feedback resistance		R_{FB}		250k	1M	2.5M	Ω	Resistance between *5 and *11.
Current consumption		I_{DD}	fs = 44.1kHz		79	90	mA	

*1 RVDT, SCK, XLAT, XWO, XRST, XS24, TST0 to TST5, X768, SI, XMST

*2 AIN1, AIN2, AIN3

*3 INVI

*4 During input to bidirectional pins BCK, LRCK

*5 XTLI

*6 During output from bidirectional pins BCK, LRCK

*7 SO, BFOT

*8 TRDT

*9 REDY

*10 AO1P, AO1N, AO2N, AO2P

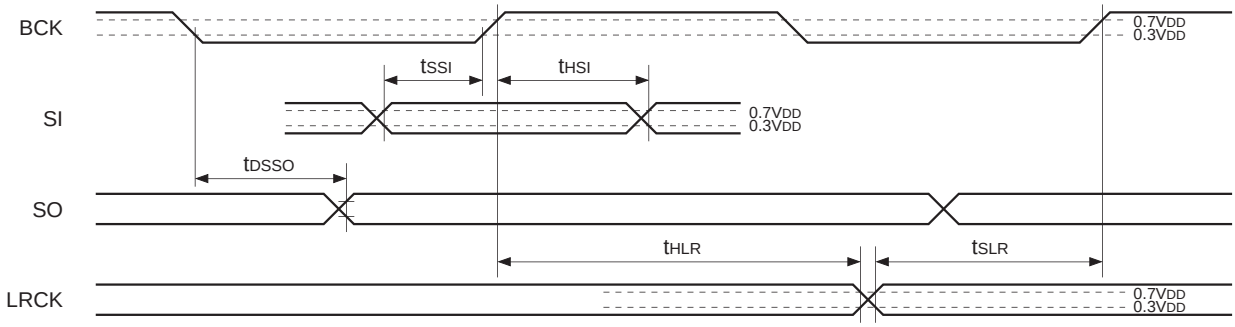
*11 XTLO

AC Characteristics

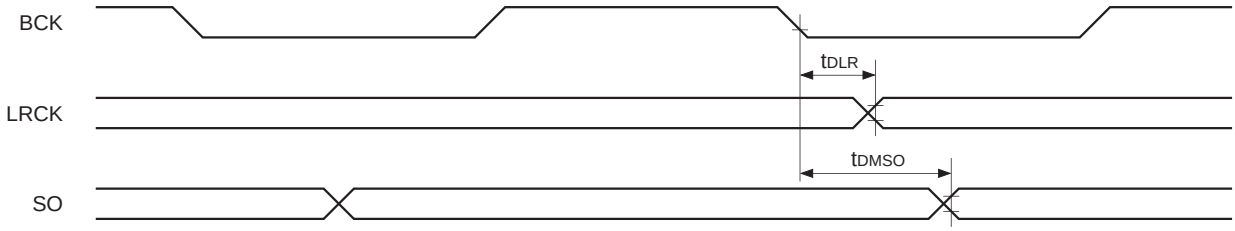
(AV_D0 to 5 = XV_{DD} = $V_{DD}0$ to 3 = 5V±10%, AV_S0 to 5 = XV_{SS} = $V_{SS}0$ to 7 = 0V, Ta = –20 to +75°C)

Serial Audio Interface Timing

[Slave mode]



[Master mode]

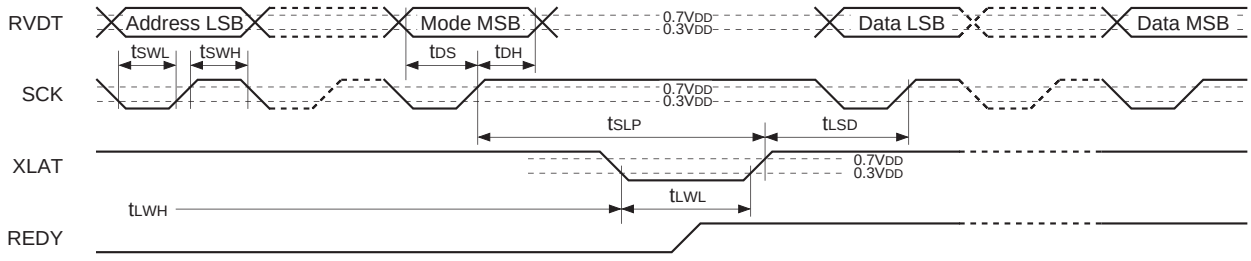


Item	Symbol	Conditions	Min.	Max.	Unit
SI setup time	t_{SSI}	Slave mode	20		ns
SI hold time	t_{HSI}	Slave mode	40		ns
SO delay time	t_{DSSO}	Slave mode, CL = 60pF		50	ns
LRCK setup time	t_{SLR}	Slave mode	20		ns
LRCK hold time	t_{HLR}	Slave mode	40		ns
LRCK delay time	t_{DLR}	Master mode, CL = 120pF		50	ns
SO delay time	t_{DMSO}	Master mode, CL = 60pF		100	ns

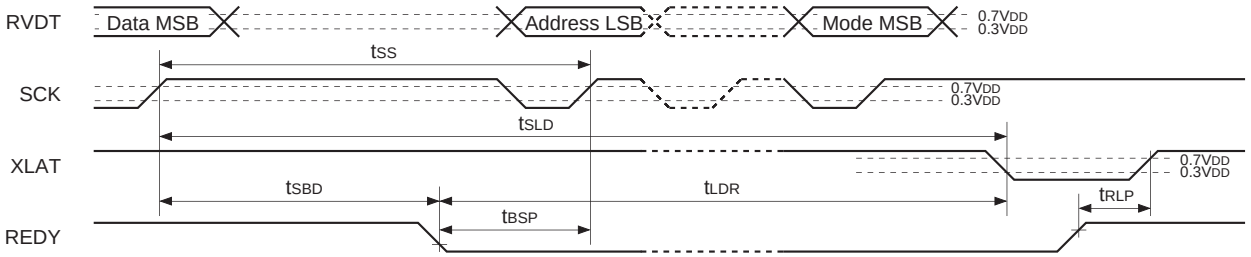
Microcomputer Interface Timing

[Write]

• Transmission timing for address section, transmission mode section, data section LSB

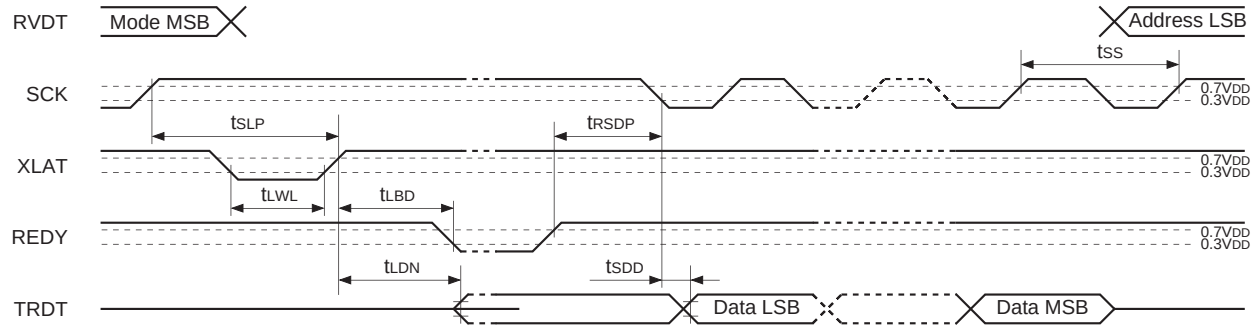


• Transmission timing from data section MSB to address section and transmission mode section



[Read]

• Transmission timing for address section and transmission mode section is the same as for write.



Item	Symbol	Min.	Max.	Unit
RVDT setup time relative to SCK rise	t_{DS}	20		ns
RVDT data hold time from SCK rise	t_{DH}	1t + 20		ns
SCK Low level width	t_{SWL}	1t + 20		ns
SCK High level width	t_{SWH}	1t + 20		ns
XLAT Low level width	t_{LWL}	1t + 20		ns
XLAT High level width	t_{LWH}	1t + 20		ns
SCK rise preceding time relative to XLAT rise	t_{SLP}	20		ns
SCK rise wait time relative to XLAT rise	t_{LSD}	3t + 20		ns
Delay time to REDY fall relative to XLAT rise.	t_{LBD}		3t + 50	ns
Delay time to REDY fall relative to SCK rise	t_{SBD}		4t + 50	ns
REDY fall preceding time relative to SCK rise	t_{BSP}	20		ns
REDY rise preceding time relative to XLAT rise	t_{RLP}	20		ns
REDY rise preceding time relative to SCK fall	t_{RSDP}	20		ns
XLAT fall wait time relative to SCK rise	t_{SLD}	3t + 20		ns
XLAT fall delay time relative to REDY fall	t_{LDR}	20		ns
Delay time from XLAT rise until TRDT data becomes active	t_{LDN}		3t + 80	ns
Delay time from SCK rise until TRDT data becomes high-impedance	t_{SDF}		3t + 80	ns
Delay time from SCK fall until TRDT data is verified	t_{SDD}		2t + 70	ns
SCK rise wait time for next transmission	t_{SS}	2t + 40		ns

Note 1) t is the cycle of 1/2 the clock frequency applied to the XTLI pin. (384fs)

Note 2) REDY and TRDT pins are the values for CL = 60pF.

Analog Characteristics (AV_D0 to 5 = $V_{DD}0$ to 3 = XV_{DD} = 5.0V, AV_S0 to 5 = $V_{SS}0$ to 7 = XV_{SS} = 0.0V, Ta = 25°C, DSP: each function = OFF, gain = 1)

[1] ADC + DAC connection total characteristics

The measurement circuit in Figure 1-1 is used. Unless otherwise indicated, the measurement conditions are as given below.

- Input signal ...1.0Vrms, 1kHz
- fs.....44.1kHz
- Rin 0Ω

Item	Measurement conditions	Min.	Typ.	Max.	Unit
S/N ratio	1.0Vrms, EIAJ (with "A" weighting filter)	80	88		dB
THD + N	1.0Vrms, EIAJ		0.016	0.03	%
	0.5Vrms, EIAJ		0.012		
Dynamic range	EIAJ		92		dB
Channel separation	Only ADC characteristics using DAC1, EIAJ		108		dB
Level difference between channels	Only ADC characteristics using DAC1		0.05		dB
Analog full-scale input level*1	Rin = 0Ω		1.26		Vrms
	Rin = 22kΩ		2.06		
ADC input impedance			34.6		kΩ
Analog current consumption			21		mA

*1 Analog input level which outputs digital full scale.
An optional analog input signal level Vin (Vrms) of 1.26Vrms or more can be set in digital full scale by the measurement circuit external resistor Rin.
The calculation formula for external resistor Rin is:

$$Rin = 27.5 \times Vin - 34.6\ [k\Omega] \quad \ldots\ldots(1)$$

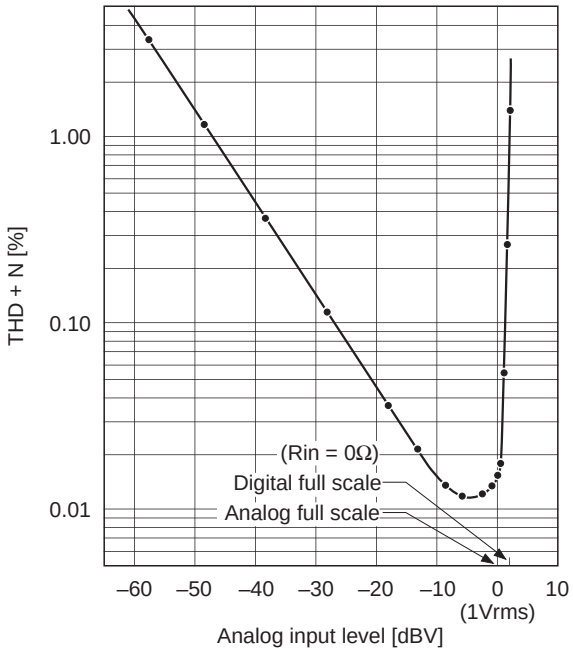
However, THD + N characteristics deteriorate for full-scale output as shown in Graph 1, so use of up to 80% (when Rin = 0Ω, 0.8 × 1.26 (Vrms) = 1.0 (Vrms) → "analog full scale") of the analog signal level is recommended for digital full-scale output.
In this case, the Rin calculation formula is the same as formula (1), except that Vin becomes 1.25 × Vin. Note that this change causes the output level after ADC + DAC to change.
Most of the above specifications are measurement values for analog full scale.

[2] DAC unit characteristics

Use the measurement circuit in Figure 1-2. Unless otherwise specified, the measurement conditions are as follows.

- Input signal ....0dB, 1kHz, 16 bits
- fs.....44.1kHz

Item	Measurement conditions	Min.	Typ.	Max.	Unit
S/N ratio	EIAJ (with "A" weighting filter)		98		dB
THD + N	EIAJ (0dB)		0.006		%
	EIAJ (–1dB)		0.004		
Dynamic range	EIAJ (–60dB)		98		dB
Channel separation	EIAJ		120		dB
Level difference between channels	EIAJ		0.05		dB
Output level	EIAJ (Measure at OUT in Figure 1-2.)		2.0		Vrms



Graph 1.

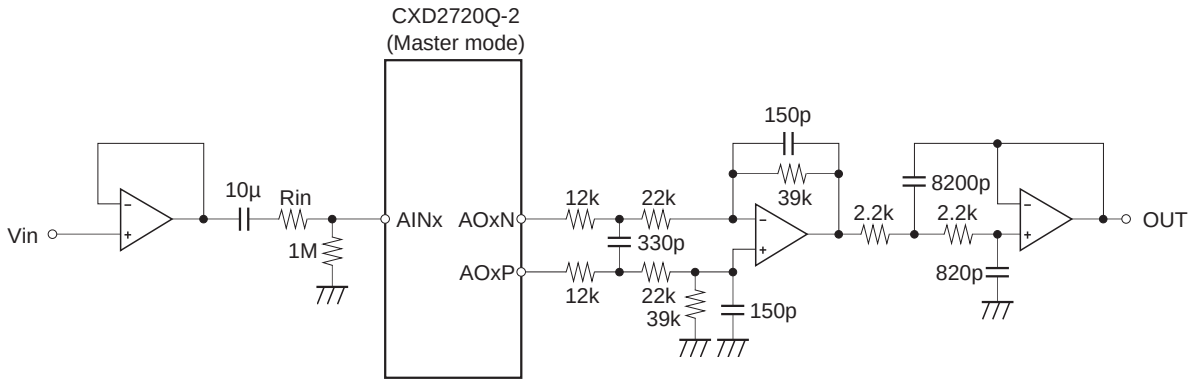


Figure 1-1. ADC + DAC Measurement Circuit Diagram

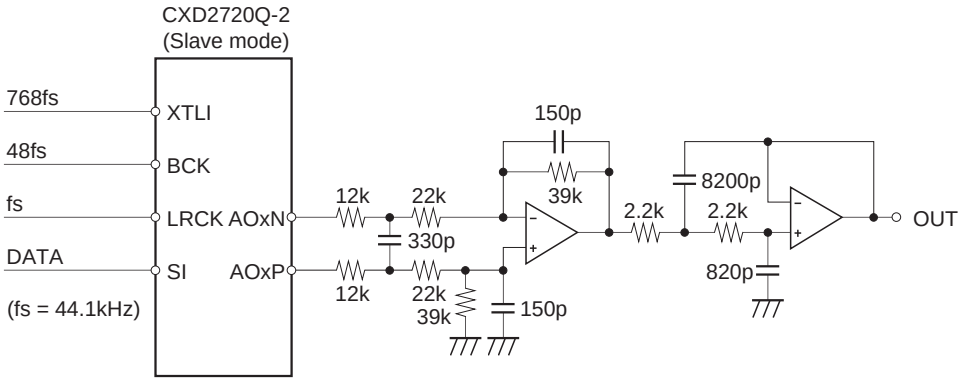


Figure 1-2. DAC Measurement Circuit Diagram

Description of Functions

1. Master/Slave Modes

[Relevant pins] XMST, LRCK, BCK

When connecting multiple CXD2720Q-2s, or when using as a pair with a D/A converter such as the CXD2558M, one of the CXD2720Q-2 should be in master mode to supply LRCK and BCK.

The clock applied to LRCK and BCK in slave mode must be synchronized to either the crystal oscillator clock of the XTLI and XTLO pins or the external clock input from the XTLI pin

XMST	Mode	LRCK, BCK I/O
H	Slave mode	Input
L	Master mode	Output

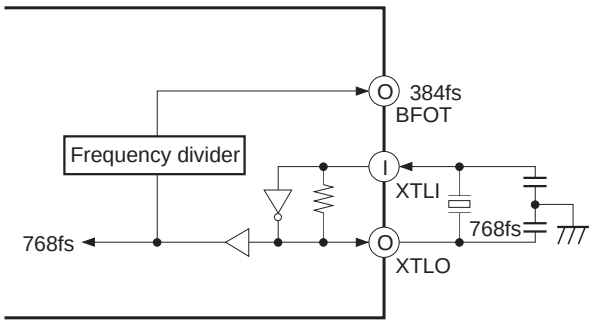
Table 1-1. LRCK, BCK Mode Setting

2. Master Clock System

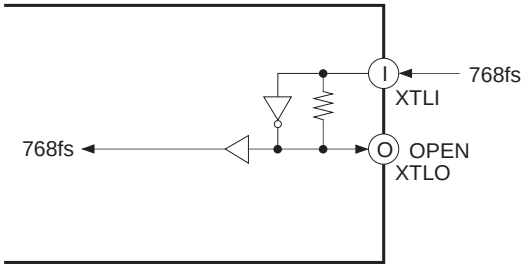
[Relevant pins] XTLI, XTLO, BFOT

768fs (fs = 44.1kHz) is assumed for the master clock system, and the connection is as shown below. (Please inquire with regard to use at other than fs = 44.1kHz.)

(1) Master



(2) Slave



3. Input/Output Synchronization Circuit

[Relevant pins] LRCK, XWO

During normal operation, synchronization is performed automatically to input LRCK (in slave mode), and phase is matched with serial input data, but if there is a lot of jitter on LRCK, or during power input, synchronization may be impossible. In this case, forced synchronization can be done by making the XWO pin Low for 2/Fs or more. Forced synchronization operation is done by the timing of the second LRCK rising edge after the XWO pin is made Low. When synchronization is completed, return the XWO pin to High.

4. Reset Circuit

[Relevant pins] XRST, XTLI, XTLO

This LSI must be reset after power is turned ON.

Reset is done by making the XRST pin Low for 1/Fs or more after supply voltage satisfies the recommended operating condition, and the crystal oscillator clock of the XTLI, XTLO pins or the external clock input from the XTLI pin is correctly applied.

5. Serial Audio Interface (SIF)

[Relevant pins] SI, SO, BCK, LRCK, XS24, XMST

Serial data is used for the external communication of the digital audio data.

The CXD2720Q-2 has one system each for input and output, and each one inputs/outputs 2 channels of data at 1 sampling cycles. Either the 32-bit clock mode or 24-bit clock mode can be selected. In master mode, the 32-bit clock mode is fixed.

(1) Pin Configuration

The pins shown in the table below are assigned to SIF.

Pin name	I/O	Function
SI	I	Serial input; taken synchronized to BCK.
SO	O	Serial output; output synchronized to BCK.
BCK	I/O	BCK input/output; either 32-bit clock mode (64fs) or 24-bit clock mode (48fs). BCK output supports 32-bit clock mode only.
LRCK	I/O	LRCK input/output (1fs).
XS24	I	SI0 slot number (24/32) selection input. Low: 24-bit slot; High: 32-bit slot. Valid only in slave mode. Set High in master mode.
XMST	I	BCK, LRCK master mode/slave mode switching input. Low: master mode; High: slave mode.

Table 5-1. Pin Configuration

(2) Operation Modes

The LRCK/BCK mode and SI/SO system settings can be selected by the setup register settings as follows.

LRCK/BCK Mode Setting

Setup register	Function	Contents
SQ11	LRCK format	"0" : normal, "1" : IIS
SQ10	LRCK polarity selection	"0" : Lch High, "1" : Lch Low
SQ09	BCK polarity selection relative to LRCK edge	"0" : edge↓, "1" : edge↑

Table 5-2. LRCK/BCK Mode Setting

SI/O System Register Setting

SI system

Setup register	Function	Contents
SQ08	SI data list	"0" : MSB first, "1" : LSB first
SQ07	SI frontward/rearward truncation	"0" : Forward truncation, "1" : Rearward truncation
SQ06 SQ05	SI data word length SI data word length	SQ06 SQ05 0 0 : 16 bits 1 1 : 24 bits

Table 5-3. SI System Register Setting

SO system

Setup register	Function	Contents
SQ04	SO data list	"0" : MSB first, "1" : LSB first
SQ03	SO forward/rearward truncation	"0" : Forward truncation, "1" : Rearward truncation
SQ02 SQ01	SO data word length	SQ02 SQ01 0 0 : 16 bits 0 1 : 18 bits 1 0 : 20 bits 1 1 : 24 bits

Table 5-4. SO System Register Setting

(3) SIF Format

Serial I/F have one input/output system each, and except for slot number, the following formats can be set independently for input and output, by setting the setup register. It can also be made to support IIS format, to enable connection to Philips and other devices. The timing charts for each data format are given on the following pages.

32-bit slot (XS24 = High)

SI format \ Setup register			SQ05	SQ06	SQ07	SQ08	Supplement
MSB first	24 bits	Forward truncation	1	1	0	0	Supports 20, 16 bits
MSB first	16 bits	Rearward truncation	0	0	1	0	
LSB first	24 bits	Rearward truncation	1	1	1	1	Supports 20, 16 bits

Table 5-5. 32-bit Slot Serial IN

SO format \ Setup register			SQ01	SQ02	SQ03	SQ04
MSB first	16 bits	Rearward truncation	0	0	1	0
MSB first	18 bits	Rearward truncation	1	0	1	0
MSB first	20 bits	Rearward truncation	0	1	1	0
MSB first	24 bits	Rearward truncation	1	1	1	0
MSB first	24 bits	Forward truncation	1	1	0	0
LSB first	24 bits	Rearward truncation	1	1	1	1

Table 5-6. 32-bit Slot Serial OUT

24-bit slot (XS24 = Low)

SI format \ Setup register			SQ05	SQ06	SQ07	SQ08	Supplement
MSB first	16 bits	Rearward truncation	0	0	1	0	
MSB first	24 bits		1	1	*	0	Supports 20, 16 bits for forward truncation
LSB first	24 bits		1	1	*	1	Supports 20, 16 bits for rearward truncation

Table 5-7. 24-bit Slot Serial IN

SO format \ Setup register			SQ01	SQ02	SQ03	SQ04
MSB first	16 bits	Rearward truncation	0	0	1	0
MSB first	18 bits	Rearward truncation	1	0	1	0
MSB first	20 bits	Rearward truncation	0	1	1	0
MSB first	24 bits		1	1	*	0
LSB first	24 bits		1	1	*	1

Table 5-8. 24-bit Slot Serial OUT

Note 1) When performing 20-bit and 16-bit data input in serial IN 24-bit data format, fill the lower 4 and 8 bits with “0”, respectively.

Note 2) * means “don't care”.

Digital Audio Data Input Timing (with polarities: SQ11 = 0, SQ10 = 0, SQ09 = 0)

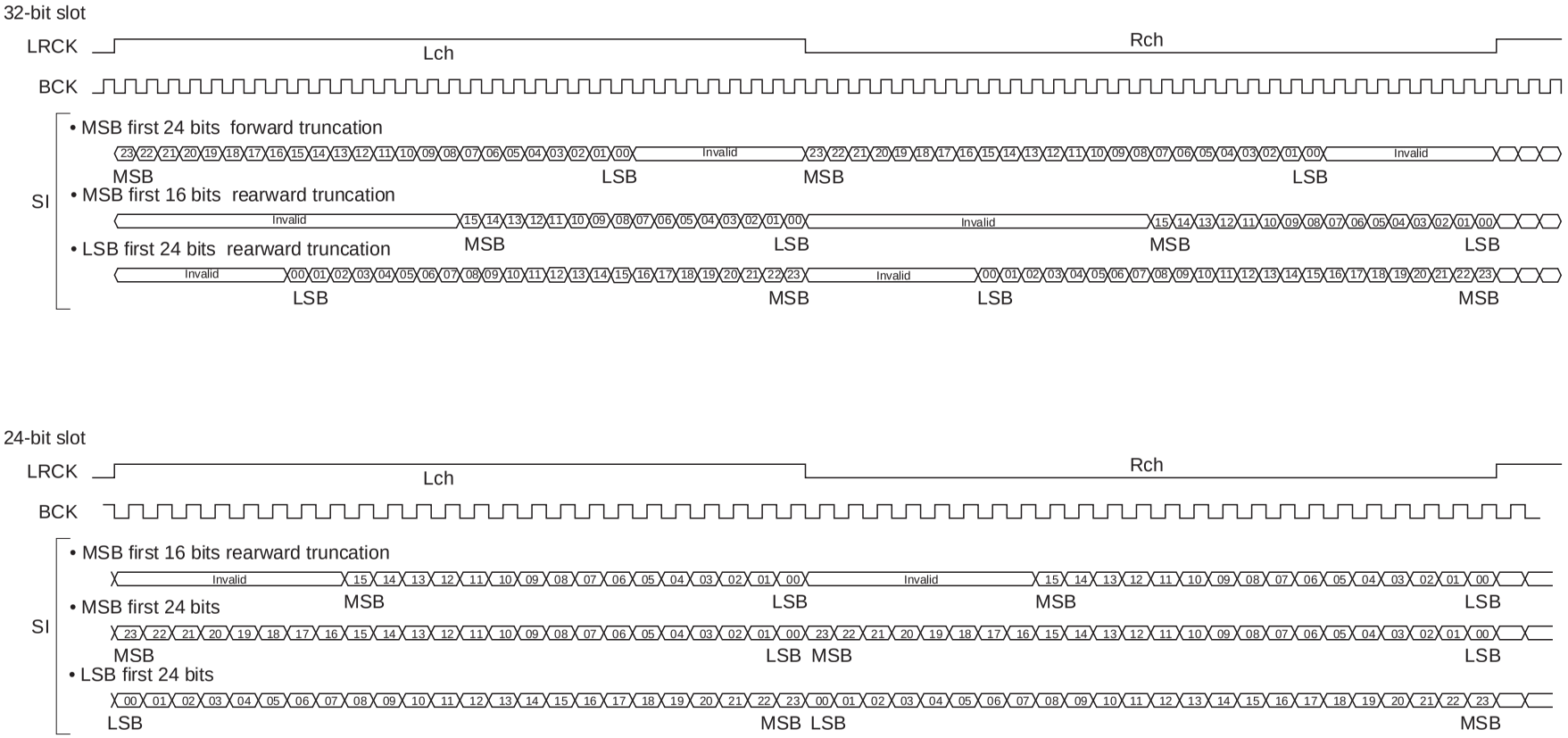


Figure 5-1.

Digital Audio Data Output Timing (with polarities: SQ11 = 0, SQ10 = 0, SQ09 = 0)

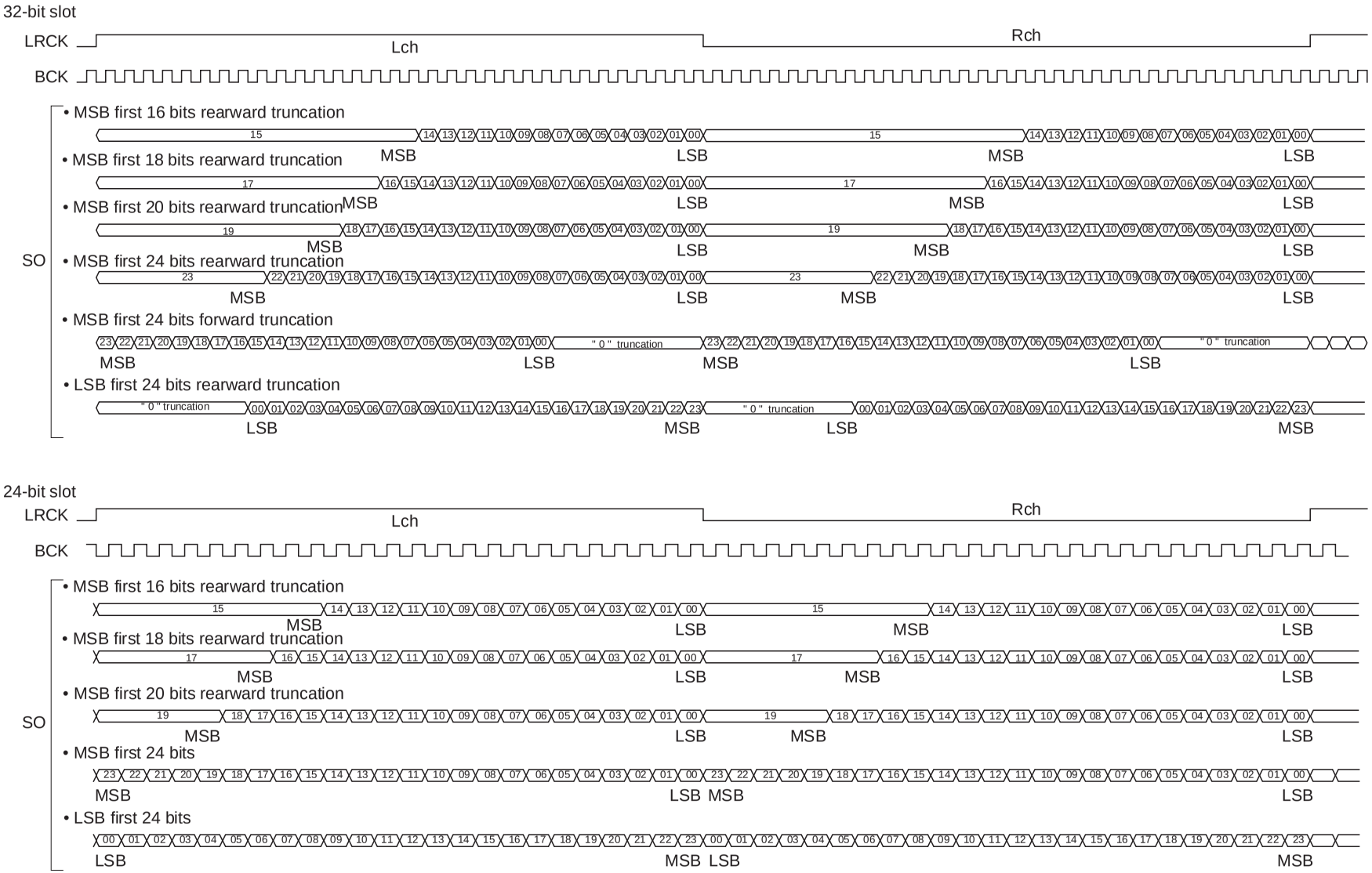


Figure 5-2.

6. Microcomputer Interface

[Relevant pins] RVDT, TRDT, SCK, XLAT, REDY

The CXD2720Q-2 performs serial audio interface format setting, volume, coefficient settings of microphone echo delay amount and others by serial data from the microcomputer.

Further, bidirectional communication such as internal data read from the CXD2720Q-2 to the microcomputer can be done at the rate of once in 1 LRCK.

(1) Pin Structure

The five external pins indicated in the table below are allocated for microcomputer interface.

Microcomputer interface begins operation when XLAT is received, so RVDT, TRDT, SCK and REDY are connected in common, and by controlling (wiring) only XLAT separately, multiple CXD2720Q-2s can be used.

Pin name	I/O	Function
RVDT	I	Serial data input from microcomputer.
TRDT	O	Serial data output to microcomputer. High impedance state unless this pin is set to internal data read state by the microcomputer. Therefore, it is preferable to perform pull-up or pull-down so that potential is not unstable when this pin is not active.
SCK	I	Shift clock for serial data. Input data from RVDT is taken according to SCK rise, and output data from TRDT is sent out according to SCK fall.
XLAT	I	Interprets the 8 bits of RVDT before this signal rises as transmission mode data, and the bits before that as address data.
REDY	O	Transmission prohibited while at Low level. Transmission enabled at High. This pin is an open drain, and must be pulled up externally.

Table 6-1. Microcomputer Interface External Pins

(2) Description of Communication Formats

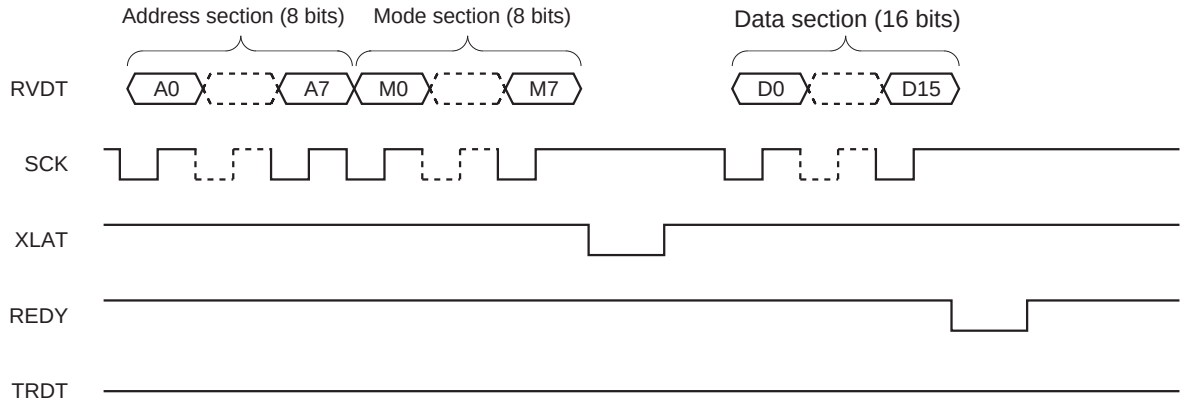
The data transmission timing between the microcomputer interface and coefficient RAM and setup register is called the SV cycle, and is generated once in 1LRCK.
The SV cycle is generated immediately preceding the signal processing program, so it has absolutely no effect on signal processing, and there is no risk of the sound being cut.

In read/write modes,

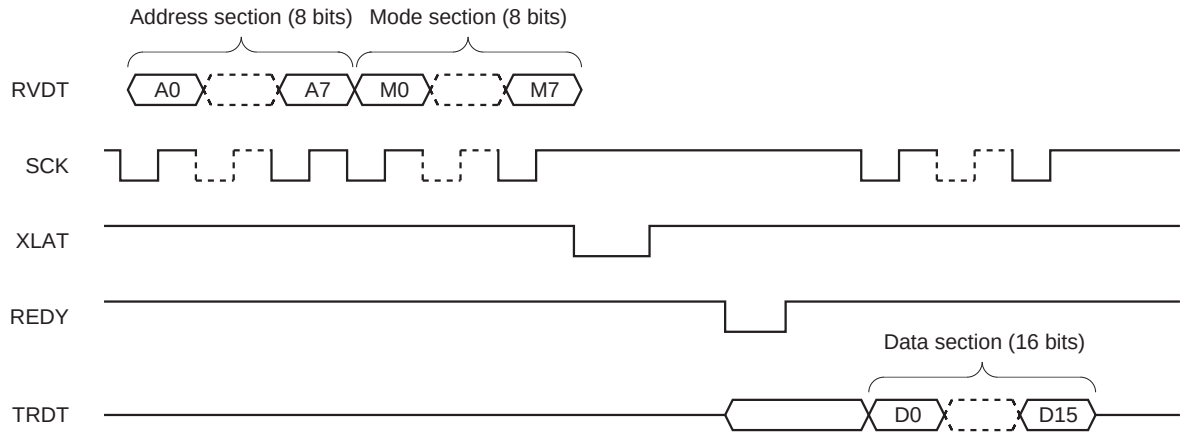
Address section + Mode section + Data section

act as one package of data to perform data transmission between the microcomputer and the CXD2720Q-2.

[Write] • For coefficient RAM



[Read] • For coefficient RAM



Note) For both read and write, the data section is 24 bits for the setup register.

Figure 6-1. Examples of Communication

(3) Data Structure

Data structure is classified in three types, as shown in the table below. All data communication is done with LSB first.

Name	Bit length	Contents	Remarks
A0 to A7	8	Address section	
M0 to M7	8	Transmission mode section	
D0 to D15/SQ00 to SQ23	16/24	Data section	Coefficient RAM is 16 bits; setup register is 24 bits

Table 6-2. Data Structure

(3)-1. Transmission Mode Section

The transmission mode section is 8 bits and has the following functions.

Bit	Name	Function	
M7	XVMT	SO Mute	0: ON (No sound) 1: OFF
M6		Reserve	
M5			
M4	VS1	Data type	VS1 VS0 0 0 Setup register 1 0 Coefficient RAM (K-RAM)
M3	VS0		
M2		Reserve	
M1			
M0	VRD	Send/Receive	0: Receive 1: Send **Note)** Polarity as seen from the CXD2720Q-2

Table 6-3. Transmission Mode Section

(3)-2. Address Section

The coefficient RAM has a 192-word structure, so the address section is 8 bits. The setup register has a 1-word structure, so the address section data may be optional.

(3)-3. Data Section

Sixteen SCK are required, as the coefficient RAM has a 16-bit structure (D0 to D15). The setup register has a 24-bit structure (SQ00 to SQ23), so twenty-four SCK are required.

(4) Details of Communication Methods

The definitions of signal timing required for control from the microcomputer are given below.

(4)-1. Write

First, address section data and mode section data are sent from the microcomputer, synchronized to SCK, to the RVDT pin.
The address section data is 8 bits both for the coefficient RAM and setup register, and the setup register transmits optional data for 1 word length. Address section data is sent with LSB first.
Mode section data is fixed at 8 bits regardless of content.

The phase relationship between SCK and RV data (data applied to the RVDT pin) has the following restrictions:

- RV data must be verified before SCK rise ($t_{DS} \geq 20$ns).
- RV data must be held for $1t$ + 20ns or more after SCK rise (t_{DH}).

SCK itself has the following restrictions:

- SCK Low level must be $1t$+ 20ns or more (t_{SWL}).
- SCK High level must also be $1t$ + 20ns or more (t_{SWH}).

After raising SCK which corresponds to mode section final data, XLAT is raised ($t_{SLP} \geq 20$ns). XLAT Low level width must be maintained at $1t$ + 20ns or more (t_{LWL}). Further, fall timing restrictions are:

- for the preceding transmission, if REDY falls due to SCK, as for write, $3t$ + 20ns or more is required. (t_{SLD})
- for the preceding transmission, if REDY falls due to XLAT, as for read, 20ns or more is required. (t_{LDR})

Further, if preceding transmissions have been performed and REDY = Low, it is necessary to wait for REDY = High to raise XLAT.

The procedure until this point is the same for write and read.

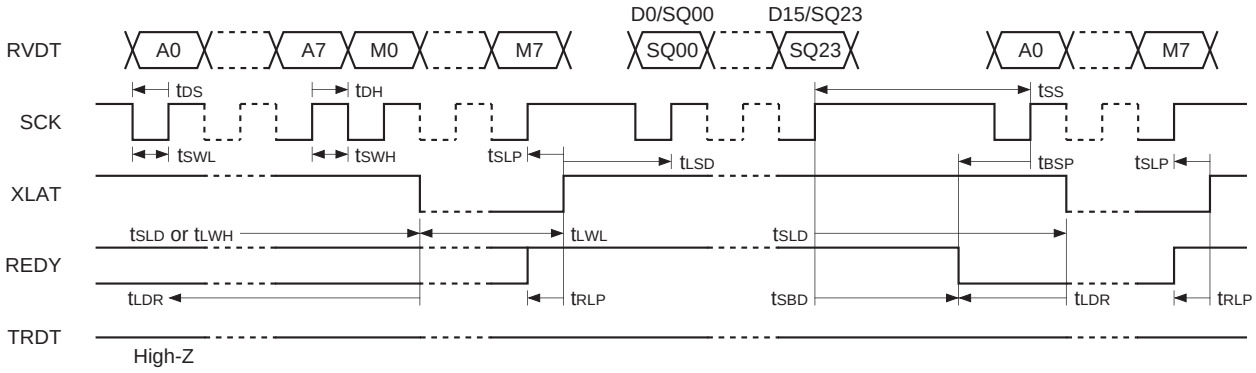


Figure 6-2. Write Timing

Data section write begins after XLAT rise, and here also transmission must be with LSB first, with t_{DS} and t_{DH} restrictions. In addition, after raising XLAT at the starting point for sending to the data section, wait for 3t + 20ns or more for the first SCK rise. (t_{LSD})

When 16 bits (coefficient RAM) or 24 bits (setup register) of this write is repeated, REDY = Low within 4t + 50ns, and the microcomputer is informed of waiting status for the SV cycle, which is the dedicated data rewrite cycle by microcomputer interface. (t_{SBD})
When REDY goes High again, the corresponding data is written.

The next communication restarts by using the REDY signal as follows.

- When REDY = Low, the SCK for the next transmission can rise ($t_{BSP} \geq$ 20ns).
- In the same way, when REDY = Low, the XLAT for the next transmission can fall ($t_{LDR} \geq$ 20ns).

REDY will fall due to this transmission, but it is prohibited for XLAT to rise for the next transmission before the REDY rises. Be sure to raise the next XLAT after REDY rises ($t_{RLP} \geq$ 20ns).

In order to restart the next transmission without using the REDY signal, the following conditions must be observed:

- There should be 2t + 40ns or more left between the SCK rise for the final data section and the SCK rise for the next transmission (t_{SS}).
- In the same way, the XLAT for the next transmission can fall after waiting 3t + 20ns or more after the final data section SCK rise (t_{SLD}).

The tss and t_{SLD} here are shorter times than $t_{SBD} \leq$ 4t + 50ns, so the restriction conditions are not much strict. However, even in this case the rise of XLAT for the next transmission must come after REDY rise ($t_{RLP} \geq$ 20ns).

Further, the restriction for XLAT fall at the starting point of this write from t_{SLD} can be:

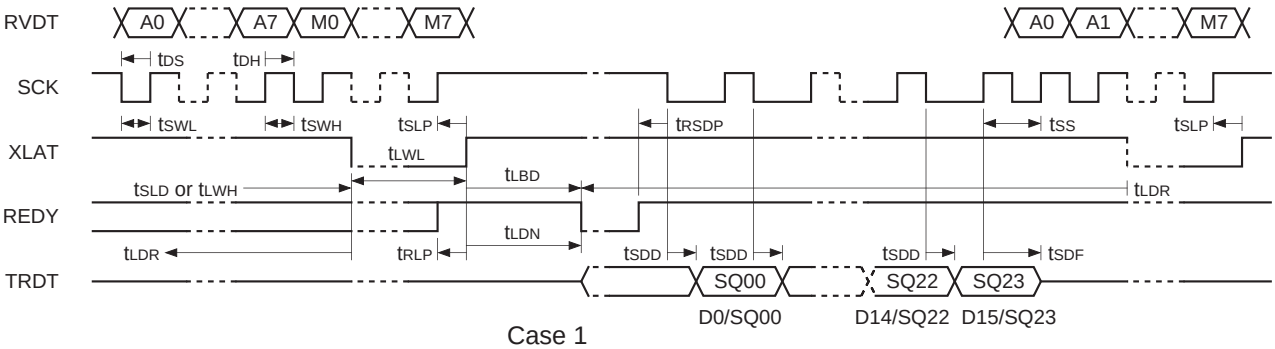
- $t_{SLD} \geq$ 3t + 20ns if the preceding transmission was “write”.

(4)-2. Read

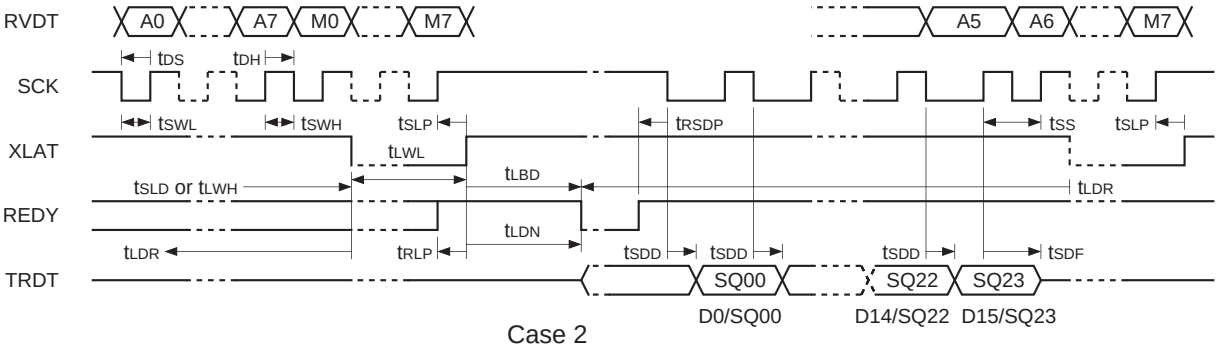
First, address section and mode section data are transmitted synchronized to SCK, and XLAT is raised matched with this; the procedure until this point is the same as for write, so the description is omitted here.

Read differs from write in that after XLAT rise, REDY falls within 3t + 50ns (t_{LBD}), and the microcomputer is informed of SV cycle waiting.
At this time, the TRDT pin changes from high-impedance state to active state ($t_{LDN} \leq 3t + 80ns$) simultaneously with REDY fall. When the read data is ready, the REDY pin changes from Low to High. When the data read out from the TRDT pin is made TR, and SCK falls ($t_{RSDP} \geq 20ns$) when the REDY pin goes High, the first TR data is defined within 2t + 70ns (t_{SDD}). The microcomputer reads this data at SCK rise. The TR data is read in order from the LSB with 16 bits for the coefficient RAM and 24 bits for the setup register by adding SCK, the corresponding data is all read, and then read is completed.

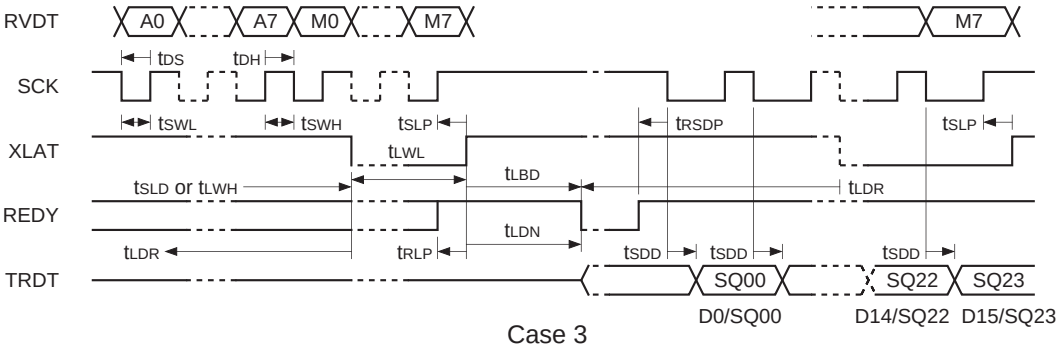
Next, the method for restarting transmission after read is completed is described.
As in Case 1, there is a method for sending address section and mode section data consecutively after reading all of the 16- or 24-bit data. There should be 2t + 40ns or more left between the SCK rise for the final data read and the next SCK rise (tss), and this is established by the conditions $t_{SWL} \geq 1t + 20ns$ and $t_{SWH} \geq 1t + 20ns$. Further, at this read REDY changes from High to Low, but it is prohibited for the XLAT for the next transmission to fall before this. If REDY = Low has been verified, XLAT can fall ($t_{LDR} \geq 20$ ns).
Also, while 16- or 24-bit data is being read from the TRDT pin, address and mode section data writing to the RVDT pin for the next transmission can be started.
In Case 3, the final section of read data and the final data in the mode section overlap, and this allows shifting to the next transmission processing in the shortest possible time after data read.
It is also possible to have data read and address and mode section write overlap partially, as shown in Case 2.



Case 1



Case 2



Case 3

Figure 6-3. Read Timing

7. Setup Register

When the setup register is selected for microcomputer interface transmission mode, the following settings are possible for serial audio interface and DAC.

Data section bit	Control		When system reset is Low
SQ23 to 12	Reserve bit	Must be Low for setup register setting change	All Low
SQ11	LRCK format	0: normal 1: IIS	Normal
SQ10	LRCK polarity selection	0: Lch High 1: Lch Low	Lch High
SQ09	BCK polarity selection relative to LRCK edge	0: Falling edge 1: Rising edge	Falling edge
SQ08	SI data list	0: MSB first 1: LSB first (24-bit rearward truncation)	MSB first
SQ07	SI frontward/rearward truncation	0: Frontward truncation (valid only for MSB first/24 bits/32 slots) 1: Rearward truncation	Frontward truncation
SQ06, 05	SI data word length	SQ06 SQ05 0 0 : 16 bits 1 1 : 24 bits	16 bits
SQ04	SO data list	0: MSB first 1: LSB first	LSB first
SQ03	SO frontward/rearward truncation	0: Frontward truncation 1: Rearward truncation	Frontward truncation
SQ02, 01	SO data word length	SQ02 SQ01 0 0 : 16 bits 0 1 : 18 bits 1 0 : 20 bits 1 1 : 24 bits	16 bits
SQ00	DAC forced mute	0: ON 1: OFF	ON

Table 7-1.

8. Coefficient RAM Setting

When the coefficient RAM is selected in microcomputer interface transmission mode, the coefficient parameters such as each section's volumes and microphone echo delay amount can be set. Data settings other than those given following in Tables 8-1 and 8-2 are “don't care”.

(1) Fixed Values for System Initialization

When the system is initialized, the coefficient RAM must be set at the fixed values, shown below, for internal operation.

Address	Fixed value			Address	Fixed value		
	fs = 44.1kHz	fs = 48kHz	fs = 32kHz		fs = 44.1kHz	fs = 48kHz	fs = 32kHz
01H	68A9H	6A30H	623EH	36H	0000H		
02H	5121H	5460H	447CH	3BH	0008H		
03H	0000H			43H	0000H		
19H	0000H			46H	0000H		
1AH	0000H			48H	0001H		
1BH	4000H			50H	0008H		
1CH	4000H			72H	0092H		
20H	0010H			73H	0209H		
21H	4000H			74H	02CDH		
23H	4000H			75H	0109H		
24H	1600H			76H	FDA0H		
25H	2A00H			77H	FD19H		
26H	3FF8H			78H	0189H		
27H	8000H			79H	058AH		
28H	0000H			7AH	016DH		
2DH	0008H			7BH	F7BEH		
31H	4000H			7CH	F72AH		
32H	1600H			7DH	0A4EH		
33H	2A00H			7EH	2706H		
34H	3FF8H			7FH	34EEH		
35H	8000H						

Table 8-1.

(2) Setting Data

The relationships between the coefficient RAM and each function during DSP operation are as follows.

Address	Name	Function	Setting value
00H	Ki	SI data input level control	Refer to Table 12-1
04H	Ke	De-emphasis ON/OFF	Refer to Table 9
05H	DC1a1	DC cut1 coefficient for accompaniment	Refer to Table 14-1
06H	DC1a0	DC cut1 coefficient for accompaniment	Refer to Table 14-1
07H	DC1b	DC cut1 coefficient for accompaniment	Refer to Table 14-1
08H	DC2a1	DC cut2 coefficient for voice	Refer to Table 14-1
09H	DC2a0	DC cut2 coefficient for voice	Refer to Table 14-1
0AH	DC2b	DC cut2 coefficient for voice	Refer to Table 14-1
0BH	PEQa	PEQ coefficient for voice	Refer to Table 14-3
0CH	PEQb1	PEQ coefficient for voice	Refer to Table 14-3
0DH	PEQb2	PEQ coefficient for voice	Refer to Table 14-3
0EH	PEQg	PEQ coefficient for voice	Refer to Table 14-4
0FH	KisLm	SI CH1 data → Lch mix	Refer to Table 12-1
10H	KisRc	SI CH2 data → Lch mix	Refer to Table 12-1
11H	KiaLm	ADC CH1 data → Lch mix	Refer to Table 12-1
12H	KiaRc	ADC CH2 data → Lch mix	Refer to Table 12-1
13H	KisRm	SI CH2 data → Rch mix	Refer to Table 12-1
14H	KisLc	SI CH1 data → Rch mix	Refer to Table 12-1
15H	KiaRm	ADC CH2 data → Rch mix	Refer to Table 12-1
16H	KiaLc	ADC CH1 data → Rch mix	Refer to Table 12-1
17H	KiaML	ADC CH3 (Mic) data → Lch mix	Refer to Table 12-1
18H	KiaMR	ADC CH3 (Mic) data → Rch mix	Refer to Table 12-1
1DH	nRpR	Pitch ratio for Lch	Refer to Table 10-1
1EH	nRpR_R	Pitch ratio for Rch	Refer to Table 10-1
1FH	Kp	Pitch ratio switching for LR independent/LR common	Common/8000H; independent/0000H
2EH	Ks	Key control ON/OFF	ON/8000H; OFF/0000H
3CH	KLf	Lch IIR4 output mix	Refer to Table 12-1
3DH	KRf	Rch IIR4 output mix	Refer to Table 12-1
3EH	KLpc	Lch pitch control output mix	Refer to Table 12-1
3FH	KRpc	Rch pitch control output mix	Refer to Table 12-1
40H	KLpt	Lch data → Echo mix	Refer to Table 12-1
41H	KRpt	Lch data → Echo mix	Refer to Table 12-1
42H	KdryE	Microphone PEQ output → Echo mix	Refer to Table 12-1

Table 8-2 (1). Coefficient RAM Setting Data (1/2)

Address	Name	Function	Setting value
44H	Tdo	Microphone echo delay amount	Refer to Table 12-1
45H	Kre	Microphone echo read tap volume	Refer to Table 12-2
47H	Tre	Microphone echo read tap address	Refer to Table 11-1
49H	Krd	Microphone echo input sound mix	Refer to Table 12-1
4AH	Kfb	Microphone echo reverberation sound mix	Refer to Table 12-1
4BH	HCa1	Microphone echo high cut	Refer to Table 14-2
4CH	HCa0	Microphone echo high cut	Refer to Table 14-2
4DH	HCb	Microphone echo high cut	Refer to Table 14-2
51H	KdryL	Microphone input direct sound Lch mix	Refer to Table 12-1
52H	KdryR	Microphone input direct sound Rch mix	Refer to Table 12-1
53H	Keff	Microphone input echo mix	Refer to Table 12-1
54H	KLm	Key control Lch data → Lch mix	Refer to Table 12-1
55H	KRm	Key control Rch data → Rch mix	Refer to Table 12-1
56H	KLmc	Key control Rch data → Lch mix	Refer to Table 12-1
57H	KRmc	Key control Lch data → Rch mix	Refer to Table 12-1
58H	KLo	System volume Lch	Refer to Table 12-1
59H	KRo	System volume Rch	Refer to Table 12-1
5AH	Kmut	Fade in/out Lch and Rch	Refer to Table 12-1
60H	IIR1a1	Pitch control input IIR_1 coefficient	Refer to Table 14-5
61H	IIR1a0	Pitch control input IIR_1 coefficient	Refer to Table 14-5
62H	IIR1b	Pitch control input IIR_1 coefficient	Refer to Table 14-5
63H	IIR2a1	Pitch control input IIR_2 coefficient	Refer to Table 14-5
64H	IIR2a0	Pitch control input IIR_2 coefficient	Refer to Table 14-5
65H	IIR2b	Pitch control input IIR_2 coefficient	Refer to Table 14-5
66H	IIR3a1	IIR_3 coefficient	Refer to Table 14-5
67H	IIR3a0	IIR_3 coefficient	Refer to Table 14-5
68H	IIR3b	IIR_3 coefficient	Refer to Table 14-5
69H	IIR4a1	IIR_4 coefficient	Refer to Table 14-5
6AH	IIR4a0	IIR_4 coefficient	Refer to Table 14-5
6BH	IIR4b	IIR_4 coefficient	Refer to Table 14-5

Table 8-2. Coefficient RAM Setting Data (2/2)

* Refer to 13. DSP Signal Flow regarding the names.

9. De-emphasis Settings

[Relevant coefficients] Ke (address = 04H)

		Ke
OFF		0000H
ON	fs = 44.1kHz	AC19H
	fs = 48kHz	AB50H
	fs = 32kHz	B01DH

Table 9. Settings for De-emphasis ON/OFF Coefficients

10. Key Controller Setting

[Relevant coefficients] nRpR (address = 1DH), nRpR_R (addresas = 1EH), Kp (address = 1FH), Ks (address = 2EH)

(1) Key Controller Pitch Ratio

nRpR (D15,.....,D2) is a 2's complement format with a decimal point between D14 and D13, and sets the desired pitch ratio directly. (VnRpR has the same type of setting as nRpR.)

$$nRpR = \sum_{n=2}^{15} Dn \times 2^{n-14}$$

The expression range for the pitch ratio is: $-2.0 \leq nRpR \leq 2.0 - 2^{-12}$

but for practical use it is: $-0.5 \leq nRpR \leq 1.0$
or ±1 octave.

Use within a range of ± half an octave is recommended for quality of sound, although it depends on the aim and the source.
Also, the algorithm is such that allophones will not be generated even when nRpR setting value is changed.
This applies to nRpR_R (Rch pitch ratio).

(2) L/R Common Setting and L/R Independent Setting of Pitch Ratio

The pitch ratio value can be set commonly or independently for Lch and Rch. It is recommended that the common value be set when the key controller is used as the music key controller, and the independent values be set when it is used as the voice effect.

Kp (address = 1FH) is used to switch the settings of the common value and independent values.
The common value is set when Kp is 8000H. nRpR (address = 1DH) is valid, and nRpR_R (address = 1EH) setting value is invalid for both Lch and Rch in the pitch ratio.
The independent values are set when Kp is 0000H. nRPR is valid for Lch, and nRpR_R is valid for Rch in the pitch ratio.

(3) Notes on Key Controller OFF

The pitch does not change when nRpR and nRpR_R are set to 0000H (OFF) when the key controller is OFF, but depending on the internal state during OFF, there is no guarantee that the input value will be output as is. During OFF, after setting nRpR and nRpR_R to 0000H (OFF), set the pitch control section to through state.

(4) Examples of Key Controller Setting

Examples of pitch ratio setting are illustrated below.
nRpR setting values are hexadecimal notation with D15 as MSB and D2 as LSB for a total of 14 bits.
(D1 and D0 can be optional data.)

CENT	nPpR, nRpR_R	CENT	nPpR, nRpR_R
0	0000H	0	0000H
+50	01E0H	–50	FE2EH
+100	03CEH	–100	FC69H
+150	05CAH	–150	FAB1H
+200	07D6H	–200	F905H
+250	09F1H	–250	F765H
+300	0C1BH	–300	F5D2H
+350	0E56H	–350	F44AH
+400	10A2H	–400	F2CCH
+450	12FFH	–450	F15AH
+500	156EH	–500	EFF3H
+550	17EEH	–550	EE95H
+600	1A82H	–600	ED42H
+650	1D29H	–650	EBF8H
+700	1FE4H	–700	EAB8H
+750	22B3H	–750	E980H
+800	2597H	–800	E852H
+850	2892H	–850	E72CH
+900	2BA2H	–900	E60EH
+950	2EC9H	–950	E4F9H
+1000	3208H	–1000	E3ECH
+1050	3560H	–1050	E2E6H
+1100	38D0H	–1100	E1E8H
+1150	3C5BH	–1150	E0F1H
+1200	4000H	–1200	E000H

Table 10-1. Pitch Ratio Setting Examples

The numeric representation format for pitch ratio here is:

$$nRpR = \sum_{n=2}^{15} Dn \times 2^{n-14}$$

The numeric representation range is: $-2.0 \leq nRpR \leq 2.0 - 2^{-12}$
Also, the relationship formula with music word cent value C is:

$$nRpR = 2^{\frac{C}{1200}} - 1,\ C = 1200 \log^2 [nRpR + 1]\ [cent]$$

The semitone at average ratio is 100 [cent].

11. Microphone Echo Delay Amount Setting

[Relevant coefficients] Tdo (address = 44H), Tre (address = 47H)

Microphone echo delay amount can be varied by setting coefficient Tdo (12 bits from D14 to D3) values. The relationships between the coefficient and the delay amount differ depending on fs used as shown in Table 11-1.

Coefficient Tre (12 bits from D14 to D3) is microphone input echo initial delay time.
Set in the range of 0008H to Tdo.

Setting value Tdo	Delay		
	fs = 44.1kHz	fs = 48kHz	fs = 32kHz
0008H 0010H 0018H · · · 4096 step · · 7ff0H 7ff8H 0000H	0.045ms · · · · 0.045ms/step · setting possible · · · 185.760ms	0.042ms · · · · 0.042ms/step · setting possible · · · 170.667ms	0.063ms · · · · 0.063ms/step · setting possible · · · 256.000ms

Table 11-1. Microphone Echo Delay Amount Setting

12. Input/Output Level Settings

[Relevant coefficients] Ki (address = 00H), KisLm (address = 0FH), KisRc (address = 10H), KiaLm (address = 11H), KiaRc (address = 12H), KisRm (address = 13H), KisLc (address = 14H), KiaRm (address = 15H), KiaLc (address = 16H), Kre (address = 45H), Krd (address = 49H), Kfb (address = 4AH), KLf (address = 3CH), KRf (address = 3DH), KLpc (address = 3EH), KRpc (address = 3FH), KLpt (address = 40H), KRpt (address = 41H), KdryE (address = 42H), KdryL (address = 51H), KdryR (address = 52H), Keff (address = 53H), KLm (address = 54H), KRm (address = 55H), KLmc (address = 56H), KRmc (address = 57H), KLo (address = 58H), KRo (address = 59H), Kmut (address = 5AH)

The input/output levels and volumes are 2's complement format with a decimal point between D15 and D14, and hexadecimal notation with D15 as MSB and D0 as LSB.
The coefficient and level relationships are as follows.

D15 to D0	Level
8000H	0dB
↓	↓
FFFFH	–90.31dB
0000H	–∞

Table 12-1. Input/Output Level Settings (other than Kre)

D15 to D0	Level
8000H	+12.04dB
↓	↓
FFFFH	–78.27dB
0000H	–∞

Table 12-2. Input/Output Level Settings (Kre)

The input/output levels for 8001H to FFFEH are determined by the following formulas.

$$\text{(Coefficient value)} = [\,(-1) \times D15 + \sum_{n=0}^{14} Dn \times 2^{n-15}] \times (-1) \quad \text{for other than Kre}$$

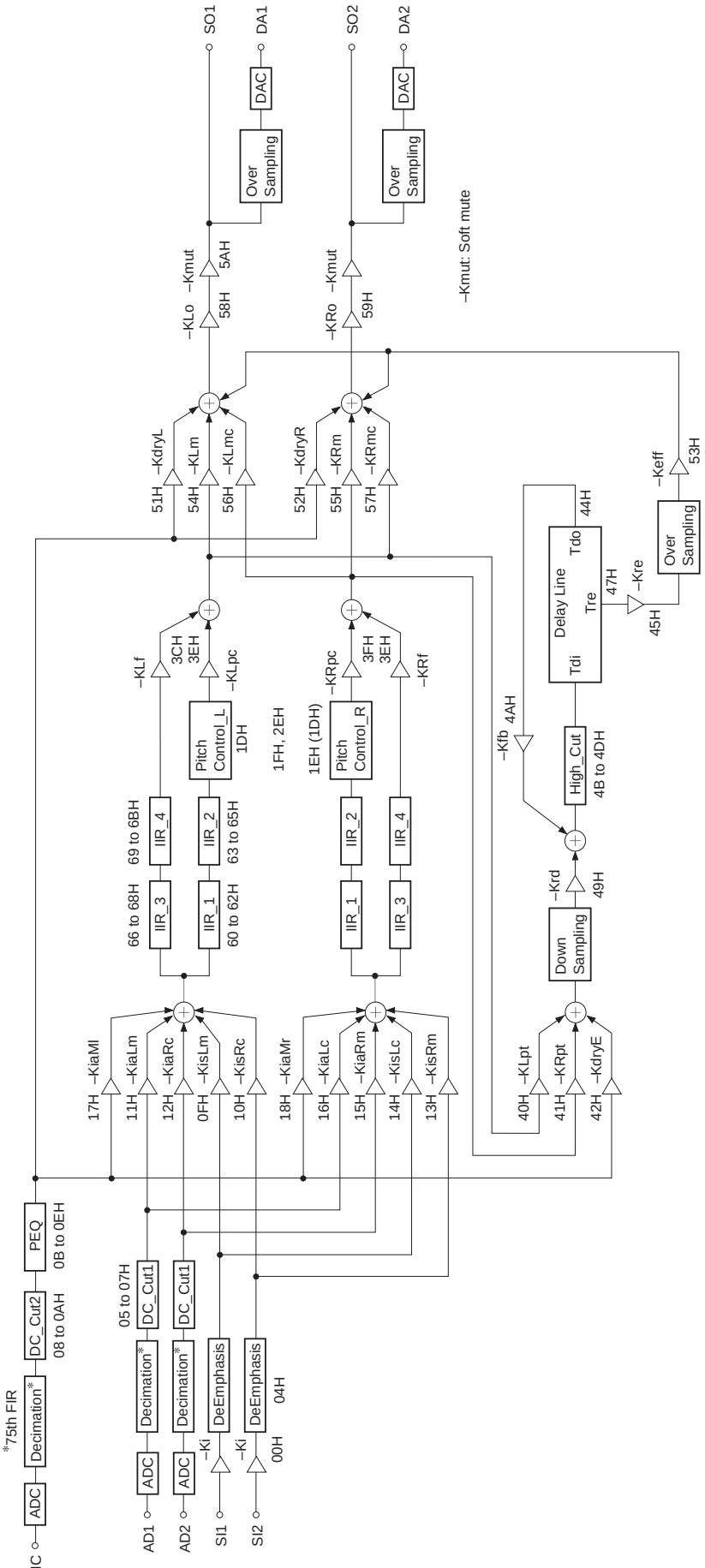
$$\text{(Coefficient value)} = [\,(-1) \times D15 + \sum_{n=0}^{14} Dn \times 2^{n-15}] \times (-4) \quad \text{for Kre}$$

Input/output level = 20log [coefficient value] dB

* D15 to D0 are negative values, but the calculation is (–1) × (D15 to D0).

* Kmut is the coefficient of the soft mute.
This approaches the specified value approximately every 45µs.
For example, when the output with its level of 0dB (8000H) is set to OFF (0000H), it takes approximately 1.49s to change from 8000H to 0000H.

13. DSP Signal Flow



* Refer to the coefficient RAM setting for information on each coefficient.

14. Filter Coefficient Table

[Relevant coefficients] DC1a1 (address = 05H), DC1a0 (address = 06H), DC1b (address = 07H), DC2a1 (address = 08H), DC2a0 (address = 09H), DC2b (address = 0AH), PEQa (address = 0BH), PEQb1 (address = 0CH), PEQb2 (address = 0DH), PEQg (address = 0EH), HCa1 (address = 4BH), HCa0 (address = 4CH), HCb (address = 4DH), IIR*b (address = 62, 65, 68, 6BH), IIR*a1 (address = 60, 63, 66, 69H), IIR*a0 (address = 61, 64, 67, 6AH)

The cut-off frequencies and PEQ gain, Q, and center frequency settings for each signal flow filter are shown in Tables 14-1 (1) to 14-5 (3).

Note) • If the above setting values are changed during DSP operation, the output level becomes unstable for several 1/fs.
• The coefficients differ depending on fs used. Please inquire with regard to use at fs other than this value.

(1) DC Cut1 for Accompaniment/ DC Cut2 for Voice

Cut-off frequency (Hz)	DC1a1 DC2a1	DC1a0 DC2a0	DC1b DC2b	Cut-off frequency (Hz)	DC1a1 DC2a1	DC1a0 DC2a0	DC1b DC2b
20	7FD1	802F	7FA2	270	7D95	826B	7B2B
30	7FBA	8046	7F74	280	7D7F	8281	7AFE
40	7FA2	805E	7F45	290	7D68	8298	7AD1
50	7F8B	8075	7F17	300	7D52	82AE	7AA4
60	7F74	808C	7EE9	310	7D3B	82C5	7A77
70	7F5D	80A3	7EBA	320	7D25	82DB	7A4B
80	7F46	80BA	7E8C	330	7D0F	82F1	7A1E
90	7F2F	80D1	7E5E	340	7CF8	8308	79F1
100	7F18	80E8	7E30	350	7CE2	831E	79C5
110	7F01	80FF	7E02	360	7CCC	8334	7998
120	7EEA	8116	7DD4	370	7CB6	834A	796C
130	7ED3	812D	7DA6	380	7CA0	8360	7940
140	7EBC	8144	7D78	390	7C8A	8376	7914
150	7EA5	815B	7D4B	400	7C73	838D	78E7
160	7E8E	8172	7D1D	410	7C5D	83A3	78BB
170	7E77	8189	7CEF	420	7C47	83B9	788F
180	7E61	819F	7CC2	430	7C31	83CF	7863
190	7E4A	81B6	7C94	440	7C1B	83E5	7837
200	7E33	81CD	7C67	450	7C05	83FB	780B
210	7E1C	81E4	7C39	460	7BEF	8411	77DF
220	7E06	81FA	7C0C	470	7BDA	8426	77B4
230	7DEF	8211	7BDF	480	7BC4	843C	7788
240	7DD9	8227	7BB2	490	7BAE	8452	775C
250	7DC2	823E	7B85	500	7B98	8468	7731
260	7DAC	8254	7B58	OFF	0000	8000	0000

Table 14-1 (1). Coefficients of DC Cut1 for Accompaniment / DC Cut2 for Voice (fs = 44.1kHz)

Cut-off frequency (Hz)	DC1a1 DC2a1	DC1a0 DC2a0	DC1b DC2b	Cut-off frequency (Hz)	DC1a1 DC2a1	DC1a0 DC2a0	DC1b DC2b
20	7FD5	802B	7FAA	270	7DC6	823A	7B8D
30	7FBF	8041	7F7F	280	7DB2	824E	7B64
40	7FAA	8056	7F54	290	7D9D	8263	7B3B
50	7F95	806B	7F2A	300	7D88	8278	7B11
60	7F7F	8081	7EFF	310	7D74	828C	7AE8
70	7F6A	8096	7ED5	320	7D5F	82A1	7ABF
80	7F55	80AB	7EAA	330	7D4B	82B5	7A96
90	7F40	80C0	7E80	340	7D36	82CA	7A6D
100	7F2A	80D6	7E55	350	7D22	82DE	7A44
110	7F15	80EB	7E2B	360	7D0D	82F3	7A1B
120	7F00	8100	7E01	370	7CF9	8307	79F2
130	7EEB	8115	7DD7	380	7CE4	831C	79C9
140	7ED6	812A	7DAC	390	7CD0	8330	79A0
150	7EC1	813F	7D82	400	7CBB	8345	7977
160	7EAC	8154	7D58	410	7CA7	8359	794E
170	7E97	8169	7D2E	420	7C93	836D	7926
180	7E82	817E	7D04	430	7C7E	8382	78FD
190	7E6D	8193	7CDA	440	7C6A	8396	78D5
200	7E58	81A8	7CB1	450	7C56	83AA	78AC
210	7E43	81BD	7C87	460	7C42	83BE	7884
220	7E2E	81D2	7C5D	470	7C2D	83D3	785B
230	7E1A	81E6	7C34	480	7C19	83E7	7833
240	7E05	81FB	7C0A	490	7C05	83FB	780A
250	7DF0	8210	7BE0	500	7BF1	840F	77E2
260	7DDB	8225	7BB7	OFF	0000	8000	0000

Table 14-1 (2). Coefficients of DC Cut1 for Accompaniment / DC Cut2 for Voice (fs = 48kHz)

Cut-off frequency (Hz)	DC1a1 DC2a1	DC1a0 DC2a0	DC1b DC2b	Cut-off frequency (Hz)	DC1a1 DC2a1	DC1a0 DC2a0	DC1b DC2b
20	7FBF	8041	7F7F	270	7CB1	834F	7963
30	7F9F	8061	7F3F	280	7C93	836D	7926
40	7F7F	8081	7EFF	290	7C74	838C	78E9
50	7F5F	80A1	7EBF	300	7C56	83AA	78AC
60	7F40	80C0	7E80	310	7C37	83C9	786F
70	7F20	80E0	7E40	320	7C19	83E7	7833
80	7F00	8100	7E01	330	7BFB	8405	77F6
90	7EE0	8120	7DC1	340	7BDD	8423	77BA
100	7EC1	813F	7D82	350	7BBF	8441	777E
110	7EA1	815F	7D43	360	7BA0	8460	7741
120	7E82	817E	7D04	370	7B82	847E	7705
130	7E63	819D	7CC6	380	7B64	849C	76C9
140	7E43	81BD	7C87	390	7B47	84B9	768E
150	7E24	81DC	7C48	400	7B29	84D7	7652
160	7E05	81FB	7C0A	410	7B0B	84F5	7616
170	7DE6	821A	7BCC	420	7AED	8513	75DB
180	7DC6	823A	7B8D	430	7ACF	8531	759F
190	7DA7	8259	7B4F	440	7AB2	854E	7564
200	7D88	8278	7B11	450	7A94	856C	7529
210	7D69	8297	7AD3	460	7A77	8589	74EE
220	7D4B	82B5	7A96	470	7A59	85A7	74B3
230	7D2C	82D4	7A58	480	7A3C	85C4	7478
240	7D0D	82F3	7A1B	490	7A1E	85E2	743D
250	7CEE	8312	79DD	500	7A01	85FF	7403
260	7CD0	8330	79A0	OFF	0000	8000	0000

Table 14-1 (3). Coefficients of DC Cut1 for Accompaniment / DC Cut2 for Voice (fs = 32kHz)

(2) Microphone Echo High Cut

Cut-off frequency (Hz)	HCa1	HCa0	HCb	Cut-off frequency (Hz)	HCa1	HCa0	HCb
1000	100E	EFF2	5FE2	5600	40CC	BF34	FE68
1100	1177	EE89	SD11	5700	41B5	BE4B	FC95
1200	12D8	ED28	SA4E	5800	429F	BD61	FAC2
1300	1432	EBCE	579A	5900	4389	BC77	F8EE
1400	1586	EA7A	54F3	6000	4173	BB8D	F719
1500	16D3	E92D	5259	6100	455E	BAA2	F543
1600	181A	E7E6	4FCB	6200	464A	B9B6	F36C
1700	195B	E6A5	4D48	6300	4136	B8CA	F194
1800	1A97	E569	4AD0	6400	4822	B7DE	EFBB
1900	1BCE	E432	4863	6500	4910	B6F0	EDE0
2000	1CFF	E301	4600	6600	49FF	B601	EC02
2100	1E2C	E1D4	43A6	6700	4AEE	B512	EA23
2200	1F55	E0AB	4155	6800	4BDF	B421	E841
2300	2079	DF87	3F0D	6900	4CD1	B32F	E65D
2400	2199	DE67	3CCD	7000	4DC5	B23B	E476
2500	22B5	DD4B	3A94	7100	4EBA	B146	E28C
2600	23CE	DC32	3863	7200	4FB0	B050	E09F
2700	24E3	DB1D	3639	7300	50A9	AF57	DEAE
2800	25F4	DA0C	3416	7400	51A3	AE5D	DCBA
2900	2703	D8FD	31F9	7500	529F	AD61	DAC1
3000	280E	D7F2	2FE2	7600	539D	AC63	D8C5
3100	2917	D6E9	2DD0	7700	549E	AB62	D6C4
3200	2A1D	D5E3	2BC4	7800	55A1	AA5F	D4BE
3300	2B21	D4DF	29BD	7900	56A6	A95A	D2B3
3400	2C22	D3DE	27BB	8000	57AE	A852	D0A3
3500	2D21	D2DF	25BD	8100	58B9	A747	CE8E
3600	2E1D	D1E3	23C4	8200	59C7	A639	CC72
3700	2F18	D0E8	21CF	8300	5AD8	A528	CA50
3800	3011	CFEF	1FDD	8400	5BEC	A414	C828
3900	3108	CEF8	1DEF	8500	5D03	A2FD	C5F9
4000	31FD	CE03	1C04	8600	5E1F	A1E1	C3C2
4100	32F1	CD0F	1A1C	8700	5F3E	A0C2	C184
4200	33E3	CC1D	1838	8800	6061	9F9F	BF3E
4300	34D5	CB2B	1655	8900	6188	9E78	BCEF
4400	35C5	CA3B	1475	9000	62B4	9D4C	BA98
4500	36B3	C94D	1298	9100	63E4	9C1C	B837
4600	37A1	C85F	10BC	9200	651A	9AE6	B5CC
4700	388E	C772	0EE2	9300	6654	99AC	B357
4800	397B	C685	0D09	9400	6794	986C	B0D7
4900	3A66	C59A	0B32	9500	68DA	9726	AE4C
5000	3B51	C4AF	095C	9600	6A25	95DB	ABB5
5100	3C3B	C3C5	0788	9700	6B77	9489	A911
5200	3D26	C2DA	05B3	9800	6CD0	9330	A660
5300	3E0F	C1F1	03E0	9900	6E2F	91D1	A3A1
5400	3EF9	C107	020D	10000	6F96	906A	A0D4
5500	3FE2	C01E	003A	OFF	0000	8000	0000

Table 14-2 (1). Coefficients of Microphone Echo High Cut (fs = 44.1kHz)

Cut-off frequency (Hz)	HCa1	HCa0	HCb	Cut-off frequency (Hz)	HCa1	HCa0	HCb
1000	0EE4	F11C	6237	5600	3CA5	C35B	06B5
1100	1035	EFCB	5F95	5700	3D7C	C284	0507
1200	1180	EE80	5CFF	5800	3E52	C1AE	035A
1300	12C4	ED3C	5A76	5900	3F29	C0D7	01AC
1400	1403	EBFD	57F8	6000	4000	C000	0000
1500	153C	EAC4	5586	6100	40D6	BF2A	FE54
1600	1670	E990	531F	6200	41AD	BE53	FCA6
1700	179E	E862	50C3	6300	4283	BD7D	FAF9
1800	18C7	E739	4E70	6400	435A	BCA6	F94B
1900	19EC	E614	4C26	6500	4431	BBCF	F79D
2000	1B0C	E4F4	49E6	6600	4509	BAF7	F5EE
2100	1C28	E3D8	47AE	6700	45E1	BA1F	F43E
2200	1D40	E2C0	457F	6800	46BA	B946	F28C
2300	1E53	EIAD	4358	6900	4793	B86D	F0DA
2400	1F63	E09D	4138	7000	486C	B794	EF27
2500	2070	DF90	3F1F	7100	4947	B6B9	ED71
2600	2179	DE87	3D0D	7200	4A22	B5DE	EBBB
2700	227E	DD82	3B02	7300	4AFF	B501	EA02
2800	2381	DC7F	38FD	7400	4BDC	B424	E847
2900	2480	DB80	36FE	7500	4CBA	B346	E68B
3000	257D	DA83	3504	7600	4D9A	B266	E4CB
3100	2677	D989	3311	7700	4E7B	B185	E30A
3200	276E	D892	3122	7800	4F5D	B0A3	E146
3300	2863	D79D	2F38	7900	5041	AFBF	DF7E
3400	2956	D6AA	2D53	8000	5126	AEDA	DDB4
3500	2A46	D5BA	2B73	8100	520C	ADF4	DBE7
3600	2B34	D4CC	2996	8200	52F5	AD0B	DA16
3700	2C20	D3E0	27BE	8300	53DF	AC21	D842
3800	2D0A	D2F6	25EA	8400	54CB	AB35	D66A
3900	2DF3	D20D	2419	8500	SSB9	AA47	D18D
4000	2ED9	D127	224C	8600	56A9	A957	D2AD
4100	2FBE	D042	2082	8700	579C	A864	D0C8
4200	30A2	CF5E	1EBA	8800	5891	A76F	CEDE
4300	3184	CE7C	1CF6	8900	5988	A678	CCEF
4400	3265	CD9B	1B35	9000	5A82	A57E	CAFC
4500	3345	CCBB	1975	9100	5B7F	A481	C902
4600	3423	CBDD	17B9	9200	5C7E	A382	C703
4700	3500	CB00	15FE	9300	5D81	A27F	C4FE
4800	35DD	CA23	1445	9400	5E86	A17A	C2F3
4900	36B8	C948	128F	9500	5F8F	A071	C0E1
5000	3793	C86D	10D9	9600	609C	9F64	BEC8
5100	386C	C794	0F26	9700	61AC	9E54	BCA8
5200	3945	C6BB	0D74	9800	62BF	9D41	BA81
5300	3A1E	C5E2	0BC2	9900	63D7	9C29	B852
5400	3AF6	C50A	0A12	10000	64F3	9B0D	B61A
5500	3BCE	C432	0863	OFF	0000	8000	0000

Table 14-2 (2). Coefficients of Microphone Echo High Cut (fs = 48kHz)

Cut-off frequency (Hz)	HCa1	HCa0	HCb	Cut-off frequency (Hz)	HCa1	HCa0	HCb
1000	153C	EAC4	5586	5600	54CB	AB35	D66A
1100	1707	E8F9	51F0	5700	5631	A9CF	D39E
1200	18C7	E739	4E70	5800	579C	A864	D0C8
1300	1A7D	E583	4B05	5900	590C	A6F4	CDE7
1400	1C28	E3D8	47AE	6000	5A82	A57E	CAFC
1500	1DCA	E236	446A	6100	5BFE	A402	C803
1600	1F63	E09D	4138	6200	5D81	A27F	C4FE
1700	20F5	DF0B	3E15	6300	5F0A	A0F6	C1EB
1800	227E	DD82	3B02	6400	609C	9F64	BEC8
1900	2401	DBFF	37FD	6500	6235	9DCB	BB96
2000	257D	DA83	3504	6600	63D7	9C29	B852
2100	26F3	D90D	3219	6700	6582	9A7E	B4FB
2200	2863	D79D	2F38	6800	6738	98C8	B190
2300	29CE	D632	2C62	6900	68F8	9708	AE10
2400	2B34	D4CC	2996	7000	6AC3	953D	AA7A
2500	2C95	D36B	26D4	7100	6C9B	9365	A6CA
2600	2DF3	D20D	2419	7200	6E7F	9181	A301
2700	2F4C	D0B4	2166	7300	7072	8F8E	9F1C
2800	30A2	CF5E	1EBA	7400	7274	8D8C	9B18
2900	31F5	CE0B	1C15	7500	7486	8B7A	96F4
3000	3345	CCBB	1975	7600	76A9	8957	92AE
3100	3492	CB6E	16DB	7700	78DF	8721	8E42
3200	35DD	CA23	1445	7800	7B29	84D7	89AE
3300	3725	C8DB	11B4	7900	7D88	8278	84EF
3400	386C	C794	0F26	8000	7FFF	8001	8001
3500	39B2	C64E	0C9B	8100	8290	7D70	7AE0
3600	3AF6	C50A	0A12	8200	853C	7AC4	7588
3700	3C39	C3C7	078C	8300	8805	77FB	6FF5
3800	3D7C	C284	0507	8400	8AEF	7511	6A22
3900	3EBE	C142	0283	8500	8DFB	7205	6409
4000	4000	C000	0000	8600	912F	6ED1	5DA2
4100	4141	BEBF	FD7D	8700	948B	6B75	56E9
4200	4283	BD7D	FAF9	8800	9816	67EA	4FD3
4300	43C6	BC3A	F874	8900	9BD3	642D	4859
4400	4509	BAF7	F5EE	9000	9FC8	6038	4070
4500	464D	B9B3	F365	9100	A3FA	5C06	380C
4600	4793	B86D	F0DA	9200	A870	5790	2F20
4700	48DA	B726	EE4C	9300	AD31	52CF	259D
4800	4A22	B5DE	EBBB	9400	B247	4DB9	1B71
4900	4B6D	B493	E925	9500	B7BC	4844	1088
5000	4CBA	B346	E68B	9600	BD9B	4265	04CA
5100	4E0A	B1F6	E3EB	9700	C3F3	3C0D	F81A
5200	4F5D	B0A3	E146	9800	CAD3	352D	EA59
5300	50B3	AF4D	DE9A	9900	D250	2DB0	DB5F
5400	520C	ADF4	DBE7	10000	DA82	257E	CAFC
5500	536A	AC96	D92C	OFF	0000	8000	0000

Table 14-2 (3). Coefficients of Microphone Echo High Cut (fs = 32kHz)

(3) PEQ for Voice

Center frequency (Hz)	PEQa	PEQb1	PEQb2
250.0	023D	7DAE	847B
280.6	0282	7D64	8505
315.0	02CF	7D10	859F
353.6	0325	7CB2	864B
396.9	0385	7C47	870B
445.4	03F0	7BCF	87E1
500.0	0467	7B48	88CF
561.2	04EC	7AAE	89D9
630.0	0580	7A01	8B01
707.1	0624	793D	8C4A
793.7	06DB	785E	8DB7
890.9	07A6	7762	8F4D
1000.0	0886	7643	910E
1122.5	097E	74FD	92FE
1259.9	0A91	738B	9524
1414.2	0BC0	71E5	9781
1587.4	0D0D	7004	9A1C
1781.8	0E7C	6DE0	9CFA
2000.0	100E	6B6D	A01E
2244.9	11C7	68A1	A38F
2519.8	13A8	656E	A752
2828.4	15B5	61C6	AB6C
3174.8	17F1	5D97	AFE4
3563.6	1A5E	58CF	B4BE
4000.0	1CFF	535A	BA00
4489.8	1FD8	4D24	BFB2
5039.7	22ED	4617	C5DC
5656.9	2642	3E23	CC85
6349.6	29DB	353B	D3B8
7127.2	2DC1	2B5C	DB84
8000.0	31FD	2097	E3FC

Table 14-3 (1). Coefficients of PEQ for Voice (fs = 44.1kHz)

Gain (dB)	PEQg
0.0	0000
0.5	01E5
1.0	03E7
1.5	0608
2.0	0849
2.5	0AAC
3.0	0D33
3.5	0FE1
4.0	12B7
4.5	15B8
5.0	18E7
5.5	1C46
6.0	1FD9
6.5	23A1
7.0	27A3
7.5	2BE2
8.0	3061
8.5	3524
9.0	3A30
9.5	3F88
10.0	4531
10.5	4B30
11.0	518A
11.5	5844
12.0	5F64

Table 14-4.

Center frequency (Hz)	PEQa	PEQb1	PEQb2
250.0	020F	7DDF	8420
280.6	024F	7D9B	849F
315.0	0295	7D4E	852C
353.6	02E5	7CF8	85CB
396.9	033D	7C97	867C
445.4	03A0	7C29	8742
500.0	040E	7BAD	881E
561.2	0489	7B21	8914
630.0	0512	7A82	8A25
707.1	05AA	79CF	8B55
793.7	0653	7904	8CA8
890.9	070F	781E	8E1F
1000.0	07DF	7719	8FC0
1122.5	08C6	75F0	918D
1259.9	09C5	749F	938B
1414.2	0ADF	7320	95BF
1587.4	0C16	716B	982D
1781.8	0D6C	6F79	9AD9
2000.0	0EE4	6D41	9DC9
2244.9	1080	6AB8	A101
2519.8	1243	67D2	A488
2828.4	1430	6181	A861
3174.8	1649	60B6	AC94
3563.6	1892	5C61	B125
4000.0	1B0C	576C	B61A
4489.8	1DBC	51C6	BB7A
5039.7	20A5	4B58	C14B
5656.9	23CA	4410	C795
6349.6	2730	3BDC	CE62
7127.2	2ADE	32B1	D5BD
8000.0	2ED9	2893	DDB4

Table 14-3 (2). Coefficients of PEQ for Voice (fs = 48kHz)

Center frequency (Hz)	PEQa	PEQb1	PEQb2
250.0	0311	7CC8	8623
280.6	036E	7C60	86DE
315.0	03D7	7BEC	87AF
353.6	074B	7B68	8898
396.9	04CD	7AD2	899B
445.4	055D	7A2A	8ABC
500.0	05FE	796B	8BFD
561.2	06B0	7892	8D62
630.0	0776	779D	8EEE
707.1	0852	7686	90A5
793.7	0945	754A	928B
890.9	0A51	73E2	94A4
1000.0	0B79	7248	96F4
1122.5	0CC0	7075	9981
1259.9	0E27	6E61	9C4F
1414.2	0FB1	6C01	9F64
1587.4	1161	694A	A2C3
1781.8	1339	662F	A673
2000.0	153C	62A2	AA7A
2244.9	176D	5E93	AEDC
2519.8	19CF	59EF	B39F
2828.4	1C64	54A3	B8C9
3174.8	1F30	4E99	BE62
3563.6	2237	47BF	C470
4000.0	257D	4000	CAFC
4489.8	2907	374E	D20F
5039.7	2CDB	2DA6	D9B8
5656.9	3103	2312	E207
6349.6	3589	17B5	EB14
7127.2	3A80	0BDA	F502
8000.0	3FFF	0000	0000

Table 14-3 (3). Coefficients of PEQ for Voice (fs = 32kHz)

(4) First-Stage IIR Filter

Cut-off frequency (Hz)	Used as LPF			Used as HPF			Cut-off frequency (Hz)	Used as LPF			Used as HPF		
	IIR*a1	IIR*a0	IIR*b	IIR*a1	IIR*a0	IIR*b		IIR*a1	IIR*a0	IIR*b	IIR*a1	IIR*a0	IIR*b
3000	16D3	E92D	5259	96D4	96D4	5259	7100	2D9F	D261	24C0	ADA0	ADA0	24C0
3100	1777	E889	5110	9778	9778	5110	7200	2E1D	D1E3	23C4	AE1E	AE1E	23C4
3200	181A	E7E6	4FCB	981B	981B	4FCB	7300	2E9B	D165	22C9	AE9C	AE9C	22C9
3300	18BB	E745	4E88	98BC	98BC	4E88	7400	2F18	D0E8	21CF	AF19	AF19	21CF
3400	195B	E6A5	4D48	995C	995C	4D48	7500	2F95	D06B	20D5	AF96	AF96	20D5
3500	19FA	E606	4C0B	99FB	99FB	4C0B	7600	3011	CFEF	1FDD	B012	B012	1FDD
3600	1A97	E569	4AD0	9A98	9A98	4AD0	7700	308C	CF74	1EE6	B08D	B08D	1EE6
3700	1B33	E4CD	4998	9B34	9B34	4998	7800	3108	CEF8	1DEF	B109	B109	1DEF
3800	1BCE	E432	4863	9BCF	9BCF	4863	7900	3183	CE7D	1CF9	B184	B184	1CF9
3900	1C67	E399	4730	9C68	9C68	4730	8000	31FD	CE03	1C04	B1FE	B1FE	1C04
4000	1CFF	E301	4600	9D00	9D00	4600	8100	3277	CD89	1B10	B278	B278	1B10
4100	1D96	E26A	44D2	9D97	9D97	44D2	8200	32F1	CD0F	1A1C	B2F2	B2F2	1A1C
4200	1E2C	E1D4	43A6	9E2D	9E2D	43A6	8300	336A	CC96	192A	B36B	B36B	192A
4300	1EC1	E13F	427C	9EC2	9EC2	427C	8400	33E3	CC1D	1838	B3E4	B3E4	1838
4400	1F55	E0AB	4155	9F56	9F56	4155	8500	345C	CBA4	1746	B45D	B45D	1746
4500	1FE7	E019	4030	9EF8	9FE8	4030	8600	34D5	CB2B	1655	B4D6	B4D6	1655
4600	2079	DF87	3F0D	A07A	A07A	3F0D	8700	354D	CAB3	1565	B54E	B54E	1565
4700	2109	DEF7	3DEC	A10A	A10A	3DEC	8800	35C5	CA3B	1475	B5C6	B5C6	1475
4800	2199	DE67	3CCD	A19A	A19A	3CCD	8900	363C	C9C4	1386	B63D	B63D	1386
4900	2228	DDD8	3BAF	A229	A229	3BAF	9000	36B3	C94D	1298	B6B4	B6B4	1298
5000	22B5	DD4B	3A94	A2B6	A2B6	3A94	9100	372B	C8D5	11A9	B72C	B72C	11A9
5100	2342	DCBE	397B	A343	A343	397B	9200	37A1	C85F	10BC	B7A2	B7A2	10BC
5200	23CE	DC32	3863	A3CF	A3CF	3863	9300	3818	C7E8	0FCF	B819	B819	0FCF
5300	2459	DBA7	374D	A45A	A45A	374D	9400	388E	C772	0EE2	B88F	B88F	0EE2
5400	24E3	DB1D	3639	A4E4	A4E4	3639	9500	3905	C6FB	0DF5	B906	B906	0DF5
5500	256C	DA94	3527	A56D	A56D	3527	9600	397B	C685	0D09	B97C	B97C	0D09
5600	25F4	DA0C	3416	A5F5	A5F5	3416	9700	39F0	C610	0C1E	B9F1	B9F1	0C1E
5700	267C	D984	3306	A67D	A67D	3306	9800	3A66	C59A	0B32	BA67	BA67	0B32
5800	2703	D8FD	31F9	A704	A704	31F9	9900	3ADC	C524	0A47	BADD	BADD	0A47
5900	2789	D877	30EC	A78A	A78A	30EC	10000	3B51	C4AF	095C	BB52	BB52	095C
6000	280E	D7F2	2FE2	A80F	A80F	2FE2	10100	3BC6	C43A	0872	BBC7	BBC7	0872
6100	2893	D76D	2ED8	A894	A894	2ED8	10200	3C3B	C3C5	0788	BC3C	BC3C	0788
6200	2917	D6E9	2DD0	A918	A918	2DD0	10300	3CB1	C34F	069D	BCB2	BCB2	069D
6300	299A	D666	2CCA	A99B	A99B	2CCA	10400	3D26	C2DA	05B3	BD27	BD27	05B3
6400	2A1D	D5E3	2BC4	AA1E	AA1E	2BC4	10500	3D9A	C266	04CA	BD9B	BD9B	04CA
6500	2A9F	D561	2AC0	AAA0	AAA0	2AC0	10600	3E0F	C1F1	03E0	BE10	BE10	03E0
6600	2B21	D4DF	29BD	AB22	AB22	29BD	10700	3E84	C17C	02F6	BE85	BE85	02F6
6700	2BA1	D45F	28BC	ABA2	ABA2	28BC	10800	3EF9	C107	020D	BEFA	BEFA	020D
6800	2C22	D3DE	27BB	AC23	AC23	27BB	10900	3F6E	C092	0123	BF6F	BF6F	0123
6900	2CA1	D35F	26BC	ACA2	ACA2	26BC	11000	3FE2	C01E	003A	BFE3	BFE3	003A
7000	2D21	D2DF	25BD	AD22	AD22	25BD	OFF	0000	8000	0000	0000	8000	0000

Table 14-5 (1). Coefficients of First-Stage IIR Filter (fs = 44.1kHz)

Cut-off frequency (Hz)	Used as LPF			Used as HPF			Cut-off frequency (Hz)	Used as LPF			Used as HPF		
	IIR*a1	IIR*a0	IIR*b	IIR*a1	IIR*a0	IIR*b		IIR*a1	IIR*a0	IIR*b	IIR*a1	IIR*a0	IIR*b
3000	153C	EAC4	5586	953D	953D	5586	7100	2ABD	D543	2A84	AABE	AABE	2A84
3100	15D6	EA2A	5452	95D7	95D7	5452	7200	2B34	D4CC	2996	AB35	AB35	2996
3200	1670	E990	531F	9671	9671	531F	7300	2BAA	D456	28AA	ABAB	ABAB	28AA
3300	1707	E8F9	51F0	9708	9708	51F0	7400	2C20	D3E0	27BE	AC21	AC21	27BE
3400	179E	E862	50C3	979F	979F	50C3	7500	2C95	D36B	26D4	AC96	AC96	26D4
3500	1833	E7CD	4F98	9834	9834	4F98	7600	2D0A	D2F6	25EA	AD0B	AD0B	25EA
3600	18C7	E739	4E70	98C8	98C8	4E70	7700	2D7F	D281	2501	AD80	AD80	2501
3700	195A	E6A6	4D4A	995B	995B	4D4A	7800	2DF3	D20D	2419	ADF4	ADF4	2419
3800	19EC	E614	4C26	99ED	99ED	4C26	7900	2E66	D19A	2332	AE67	AE67	2332
3900	1A7D	E583	4B05	9A7E	9A7E	4B05	8000	2ED9	D127	224C	AEDA	AEDA	224C
4000	1B0C	E4F4	49E6	9B0D	9B0D	49E6	8100	2F4C	D0B4	2166	AF4D	AF4D	2166
4100	1B9B	E465	48C9	9B9C	9B9C	48C9	8200	2FBE	D042	2082	AFBF	AFBF	2082
4200	1C28	E3D8	47AE	9C29	9C29	47AE	8300	3030	CFD0	1F9E	B031	B031	1F9E
4300	1CB4	E34C	4696	9CB5	9CB5	4696	8400	30A2	CF5E	1EBA	B0A3	B0A3	1EBA
4400	1D40	E2C0	457F	9D41	9D41	457F	8500	3113	CEED	1DD8	B114	B114	1DD8
4500	1DCA	E236	446A	9DCB	9DCB	446A	8600	3184	CE7C	1CF6	B185	B185	1CF6
4600	1E53	E1AD	4358	9E54	9E54	4358	8700	31F5	CE0B	1C15	B1F6	B1F6	1C15
4700	1EDC	E124	4247	9EDD	9EDD	4247	8800	3265	CD9B	1B35	B266	B266	1B35
4800	1F63	E09D	4138	9F64	9F64	4138	8900	32D5	CD2B	1A55	B2D6	B2D6	1A55
4900	1FEA	E016	402A	9FEB	9FEB	402A	9000	3345	CCBB	1975	B346	B346	1975
5000	2070	DF90	3F1F	A071	A071	3F1F	9100	33B4	CC4C	1897	B3B5	B3B5	1897
5100	20F5	DF0B	3E15	A0F6	A0F6	3E15	9200	3423	CBDD	17B9	B424	B424	17B9
5200	2179	DE87	3D0D	A17A	A17A	3D0D	9300	3492	CB6E	16DB	B493	B493	16DB
5300	21FC	DE04	3C07	A1FD	A1FD	3C07	9400	3500	CB00	15FE	B501	B501	15FE
5400	227E	DD82	3B02	A27F	A27F	3B02	9500	356E	CA92	1522	B56F	B56F	1522
5500	2300	DD00	39FE	A301	A301	39FE	9600	35DD	CA23	1445	B5DE	B5DE	1445
5600	2381	DC7F	38FD	A382	A382	38FD	9700	364A	C9B6	136A	B64B	B64B	136A
5700	2401	DBFF	37FD	A402	A402	37FD	9800	36B8	C948	128F	B6B9	B6B9	128F
5800	2480	DB80	36FE	A481	A481	36FE	9900	3725	C8DB	11B4	B726	B726	11B4
5900	24FF	DB01	3600	A500	A500	3600	10000	3793	C86D	10D9	B794	B794	10D9
6000	257D	DA83	3504	A57E	A57E	3504	10100	3800	C800	0FFF	B801	B801	0FFF
6100	25FA	DA06	340A	A5FB	A5FB	340A	10200	386C	C794	0F26	B86D	B86D	0F26
6200	2677	D989	3311	A678	A678	3311	10300	38D9	C727	0E4D	B8DA	B8DA	0E4D
6300	26F3	D90D	3219	A6F4	A6F4	3219	10400	3945	C6BB	0D74	B946	B946	0D74
6400	276E	D892	3122	A76F	A76F	3122	10500	39B2	C64E	0C9B	B9B3	B9B3	0C9B
6500	27E9	D817	302D	A7EA	A7EA	302D	10600	3A1E	C5E2	0BC2	BA1F	BA1F	0BC2
6600	2863	D79D	2F38	A864	A864	2F38	10700	3A8A	C576	0AEA	BA8B	BA8B	0AEA
6700	28DD	D723	2E45	A8DE	A8DE	2E45	10800	3AF6	C50A	0A12	BAF7	BAF7	0A12
6800	2956	D6AA	2D53	A957	A957	2D53	10900	3B62	C49E	093B	BB63	BB63	093B
6900	29CE	D632	2C62	A9CF	A9CF	2C62	11000	3BCE	C432	0863	BBCF	BBCF	0863
7000	2A46	D5BA	2B73	AA47	AA47	2B73	OFF	0000	8000	0000	0000	8000	0000

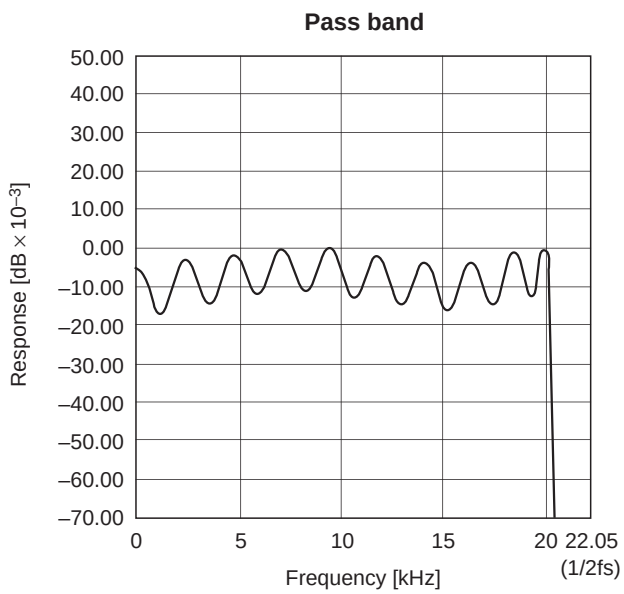
Table 14-5 (2). Coefficients of First-Stage IIR Filter (fs = 48kHz)

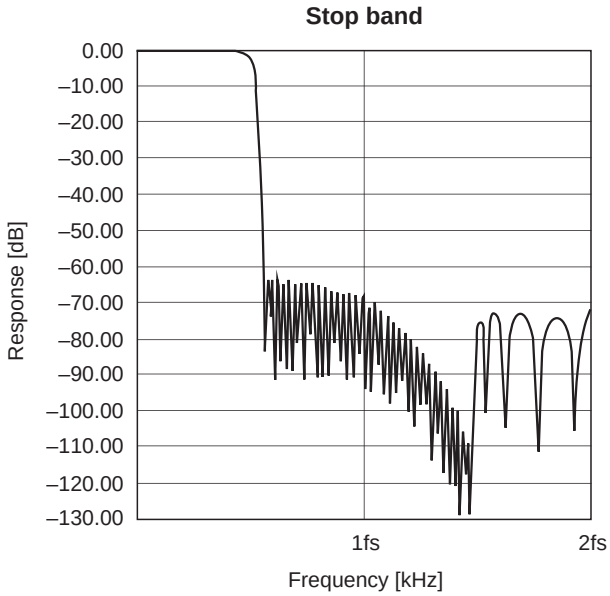
Cut-off frequency (Hz)	Used as LPF			Used as HPF			Cut-off frequency (Hz)	Used as LPF			Used as HPF		
	IIR*a1	IIR*a0	IIR*b	IIR*a1	IIR*a0	IIR*b		IIR*a1	IIR*a0	IIR*b	IIR*a1	IIR*a0	IIR*b
3000	1DCA	E236	446A	9DCB	9DCB	446A	7100	3A54	C5AC	0B56	BA55	BA55	0B56
3100	1E98	E168	42CF	9E99	9E99	42CF	7200	3AF6	C50A	0A12	BAF7	BAF7	0A12
3200	1F63	E09D	4138	9F64	9F64	4138	7300	3B98	C468	08CF	BB99	BB99	08CF
3300	202D	DFD3	3FA4	A02E	A02E	3FA4	7400	3C39	C3C7	078C	BC3A	BC3A	078C
3400	20F5	DF0B	3E15	A0F6	A0F6	3E15	7500	3CDB	C325	0649	BCDC	BCDC	0649
3500	21BA	DE46	3C8A	A1BB	A1BB	3C8A	7600	3D7C	C284	0507	BD7D	BD7D	0507
3600	227E	DD82	3B02	A27F	A27F	3B02	7700	3E1D	C1E3	03C5	BE1E	BE1E	03C5
3700	2341	DCBF	397D	A342	A342	397D	7800	3EBE	C142	0283	BEBF	BEBF	0283
3800	2401	DBFF	37FD	A402	A402	37FD	7900	3F5F	C0A1	0141	BF60	BF60	0141
3900	24C0	DB40	367F	A4C1	A4C1	367F	8000	4000	C000	0000	C000	C000	0000
4000	257D	DA83	3504	A57E	A57E	3504	8100	40A0	BF60	FEBF	C0A1	C0A1	FEBF
4100	2639	D9C7	338D	A63A	A63A	338D	8200	4141	BEBF	FD7D	C142	C142	FD7D
4200	26F3	D90D	3219	A6F4	A6F4	3219	8300	41E2	BE1E	FC3B	C1E3	C1E3	FC3B
4300	27AC	D854	30A7	A7AD	A7AD	30A7	8400	4283	BD7D	FAF9	C284	C284	FAF9
4400	2863	D79D	2F38	A864	A864	2F38	8500	4324	BCDC	F9B7	C325	C325	F9B7
4500	2919	D6E7	2DCC	A91A	A91A	2DCC	8600	43C6	BC3A	F874	C3C7	C3C7	F874
4600	29CE	D632	2C62	A9CF	A9CF	2C62	8700	4467	BB99	F731	C468	C468	F731
4700	2A82	D57E	2AFB	AA83	AA83	2AFB	8800	4509	BAF7	F5EE	C50A	C50A	F5EE
4800	2B34	D4CC	2996	AB35	AB35	2996	8900	45AB	BA55	F4AA	C5AC	C5AC	F4AA
4900	2BE5	D41B	2834	ABE6	ABE6	2834	9000	464D	B9B3	F365	C64E	C64E	F365
5000	2C95	D36B	26D4	AC96	AC96	26D4	9100	46F0	B910	F220	C6F1	C6F1	F220
5100	2D45	D2BB	2575	AD46	AD46	2575	9200	4793	B86D	F0DA	C794	C794	F0DA
5200	2DF3	D20D	2419	ADF4	ADF4	2419	9300	4836	B7CA	EF94	C837	C837	EF94
5300	2EA0	D160	22BF	AEA1	AEA1	22BF	9400	48DA	B726	EE4C	C8DB	C8DB	EE4C
5400	2F4C	D0B4	2166	AF4D	AF4D	2166	9500	497E	B682	ED04	C97F	C97F	ED04
5500	2FF8	D008	200F	AFF9	AFF9	200F	9600	4A22	B5DE	EBBB	CA23	CA23	EBBB
5600	30A2	CF5E	1EBA	B0A3	B0A3	1EBA	9700	4AC8	B538	EA70	CAC9	CAC9	EA70
5700	314C	CEB4	1D67	B14D	B14D	1D67	9800	4B6D	B493	E925	CB6E	CB6E	E925
5800	31F5	CE0B	1C15	B1F6	B1F6	1C15	9900	4C14	B3EC	E7D8	CC15	CC15	E7D8
5900	329D	CD63	1AC5	B29E	B29E	1AC5	10000	4CBA	B346	E68B	CCBB	CCBB	E68B
6000	3345	CCBB	1975	B346	B346	1975	10100	4D62	B29E	E53B	CD63	CD63	E53B
6100	33EB	CC15	1828	B3EC	B3EC	1828	10200	4E0A	B1F6	E3EB	CE0B	CE0B	E3EB
6200	3492	CB6E	16DB	B493	B493	16DB	10300	4EB3	B14D	E299	CEB4	CEB4	E299
6300	3537	CAC9	1590	B538	B538	1590	10400	4F5D	B0A3	E146	CF5E	CF5E	E146
6400	35DD	CA23	1445	B5DE	B5DE	1445	10500	5007	AFF9	DFF1	D008	D008	DFF1
6500	3681	C97F	12FC	B682	B682	12FC	10600	50B3	AF4D	DE9A	D0B4	D0B4	DE9A
6600	3725	C8DB	11B4	B726	B726	11B4	10700	515F	AEA1	DD41	D160	D160	DD41
6700	37C9	C837	106C	B7CA	B7CA	106C	10800	520C	ADF4	DBE7	D20D	D20D	DBE7
6800	386C	C794	0F26	B86D	B86D	0F26	10900	52BA	AD46	DA8B	D2BB	D2BB	DA8B
6900	390F	C6F1	0DE0	B910	B910	0DE0	11000	536A	AC96	D92C	D36B	D36B	D92C
7000	39B2	C64E	0C9B	B9B3	B9B3	1C9B	OFF	0000	8000	0000	0000	8000	0000

Table 14-5 (3). Coefficients of First-Stage IIR Filter (fs = 32kHz)

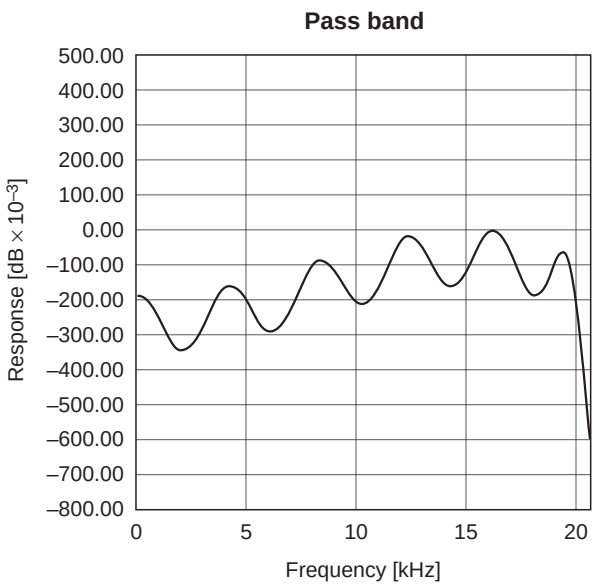
Filter Characteristics

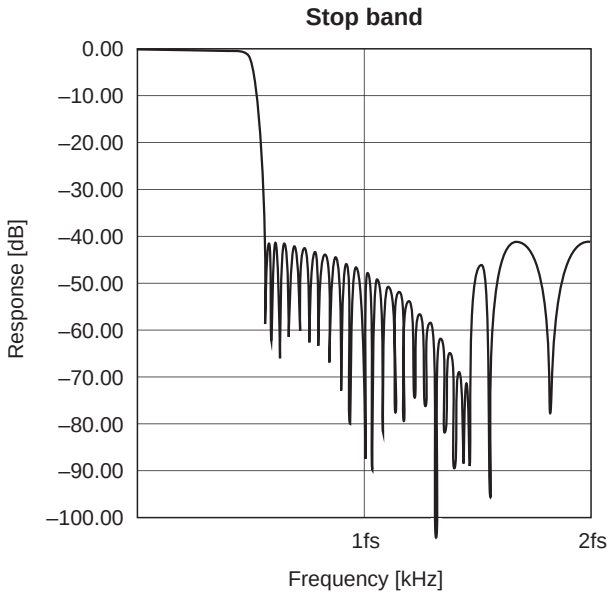
ADC Filter Characteristics (75th + 15th FIR)



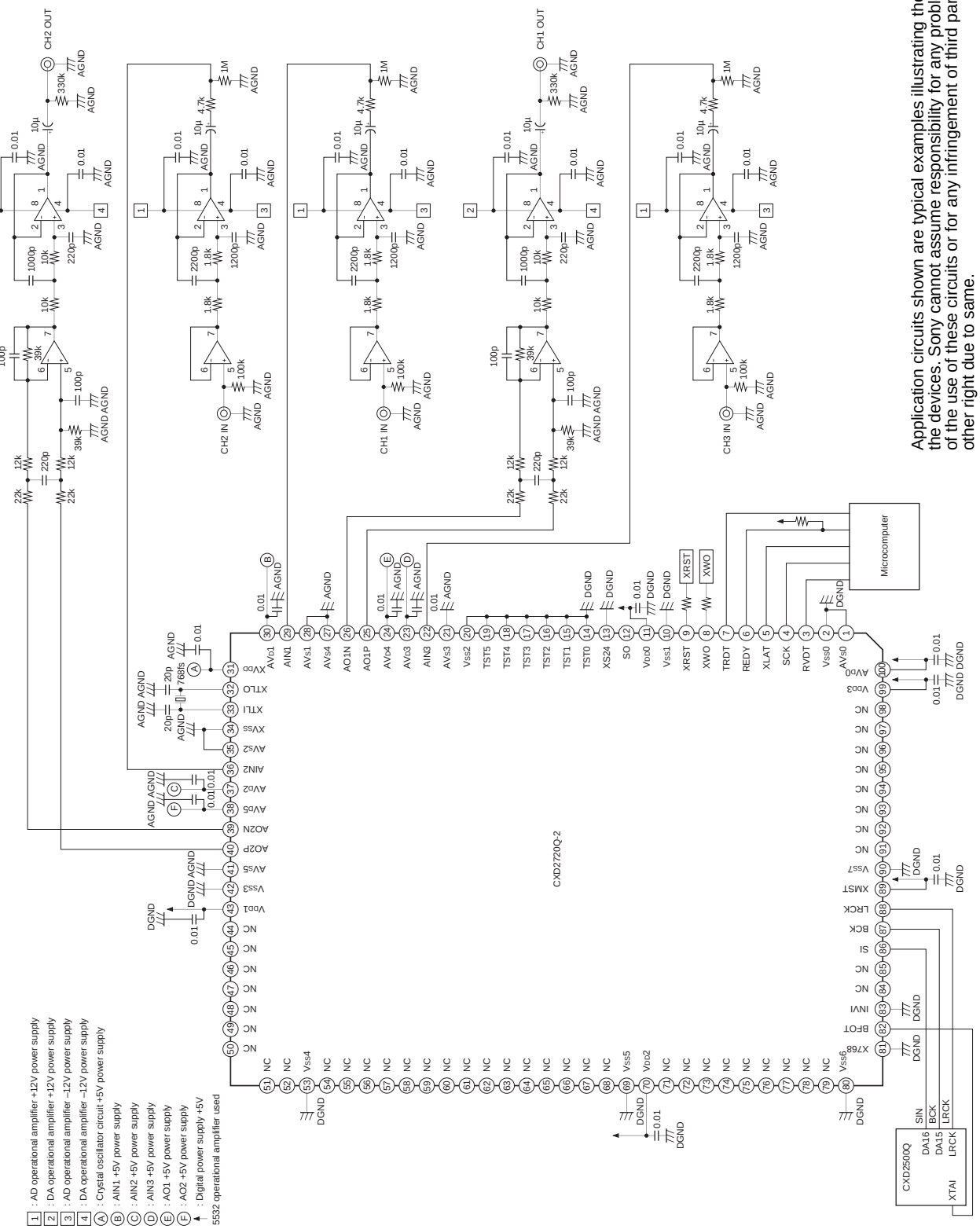


DAC Filter Characteristics (43rd + 7th FIR)





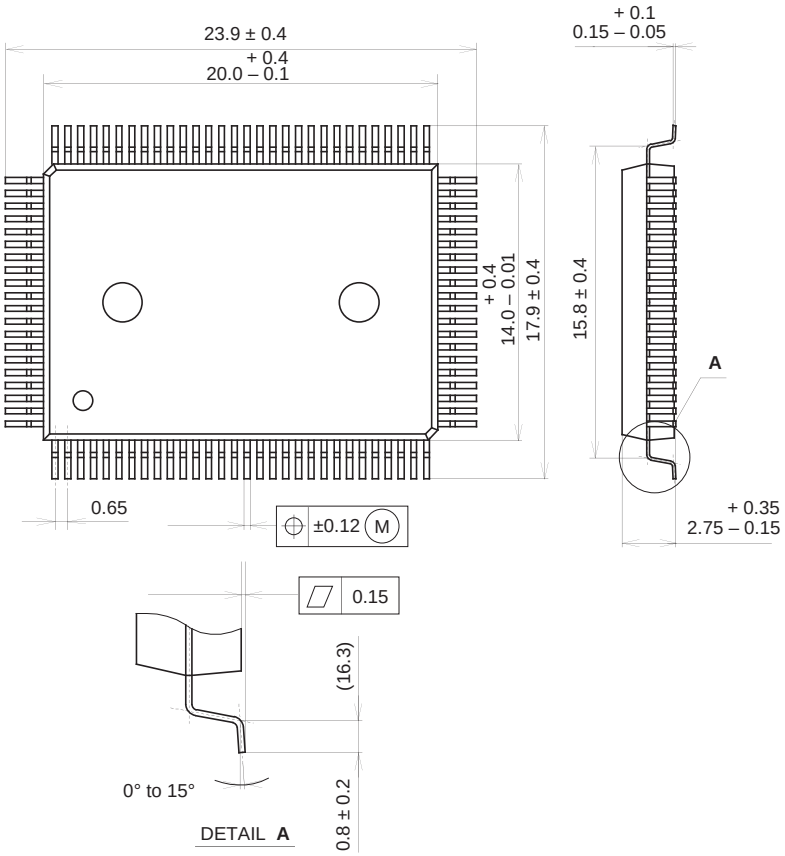
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

100PIN QFP (PLASTIC)



SONY CODE	QFP-100P-L01
EIAJ CODE	*QFP100-P-1420-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.4g

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