

CD Digital Signal Processor with Built-in Digital Servo and DAC

Description

The CXD2548R is a digital signal processor LSI for CD players. This LSI incorporates a digital servo, digital filter, zero detection circuit, 1-bit DAC and analog low-pass filter on a single chip.

Features

- All digital signal processing during playback is performed with a single chip
- Highly integrated mounting possible due to a built-in RAM

Digital Signal Processor (DSP) Block

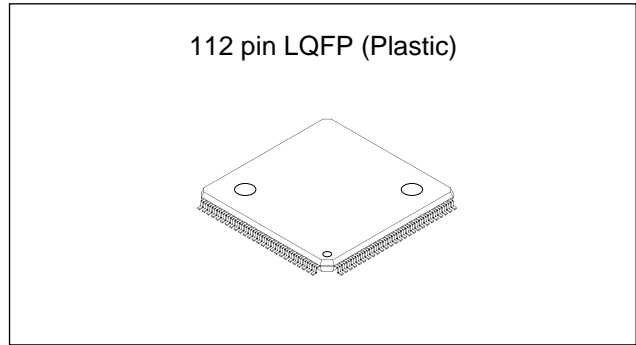
- Playback mode which supports CAV (Constant Angular Velocity)
 - Frame jitter free
 - 0.5 × to 2.5 × continuous playback possible
 - Allows relative rotational velocity readout
 - Supports spindle external control
- Wide capture range playback mode
 - Spindle rotational velocity following method
 - Supports normal-speed, double-speed playback
- 16K RAM
- EFM data demodulation
- Enhanced EFM frame sync signal protection
- SEC strategy-based error correction
- Subcode demodulation and Sub Q data error detection
- Digital spindle servo
 - 16-bit traverse counter
 - Asymmetry compensation circuit
 - CPU interface on serial bus
 - Error correction monitor signal, etc. output from a new CPU interface
 - Servo auto sequencer
 - Digital audio interface outputs
 - Digital level meter, peak meter

Digital Servo (DSSP) Block

- Microcomputer software-based flexible servo control
- Offset cancel function for servo error signal
- Auto gain control function for servo loop
- E:F balance, focus bias adjustment functions
- Surf jump function supporting micro two-axis

Digital Filter, DAC and Analog Low-Pass Filter Blocks

- Digital de-emphasis
- Digital attenuation
- Zero detection function
- 8Fs oversampling digital filter
- S/N: 100dB or more (master clock: 384Fs, typ.)
- THD + N: 0.007% or more (master clock: 384Fs, typ.)
- Rejection band attenuation: -60dB or more



Applications

CD players

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings

- Supply voltage V_{DD} -0.3 to +7.0 V
- Input voltage V_I -0.3 to +7.0 V
- Output voltage V_O -0.3 to +7.0 V
- Storage temperature T_{stg} -40 to +125 °C
- Supply voltage difference
 - $V_{SS} - AV_{SS}$ -0.3 to +0.3 V
 - $V_{DD} - AV_{DD}$ -0.3 to +0.3 V

Recommended Operating Conditions

- Supply voltage V_{DD}^{Note} -3.4 to +5.25 V
- Operating temperature T_{opr} -20 to +75 °C

Note) The V_{DD} (Min.) for the CXD2548R varies according to the playback speed selection.

| Playback speed | V_{DD} (min.) [V] | | |
|----------------|---------------------|-----------|------------|
| | CD-DSP block | DAC block | DSSP block |
| 2 × | 3.4V | 4.5V | 3.4V |
| 1 × | 3.4V | 3.4V | 3.4V |
| 1 ×*1 | 3.4V | / | 3.4V |

*1 When the internal operation of the CD-DSP side is set to double-speed mode and the crystal oscillation frequency is halved, normal-speed playback results.

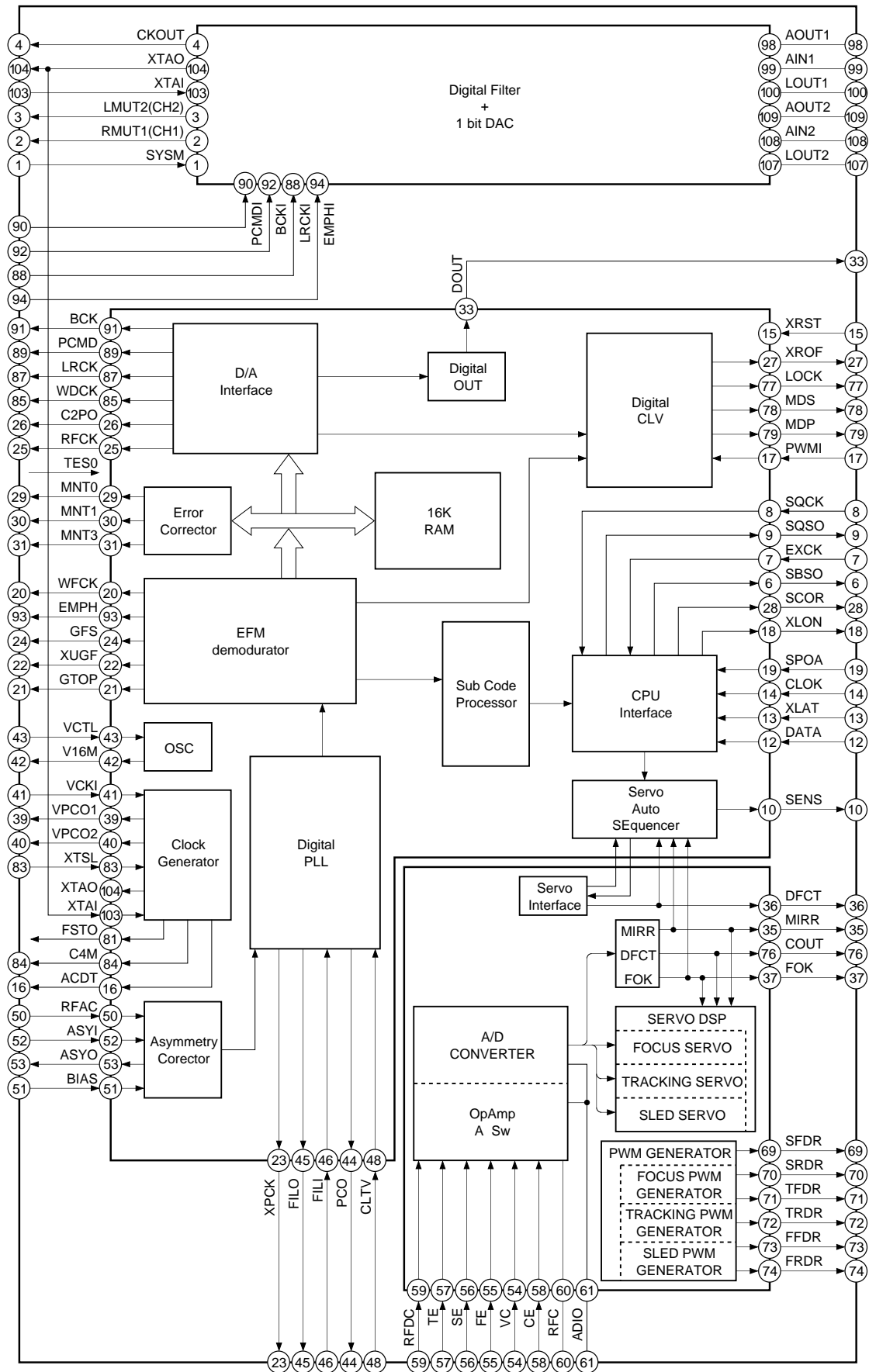
I/O Capacitance

- Input pin C_i 12 (Max.) pF
- Output pin C_o 12 (Max.) pF

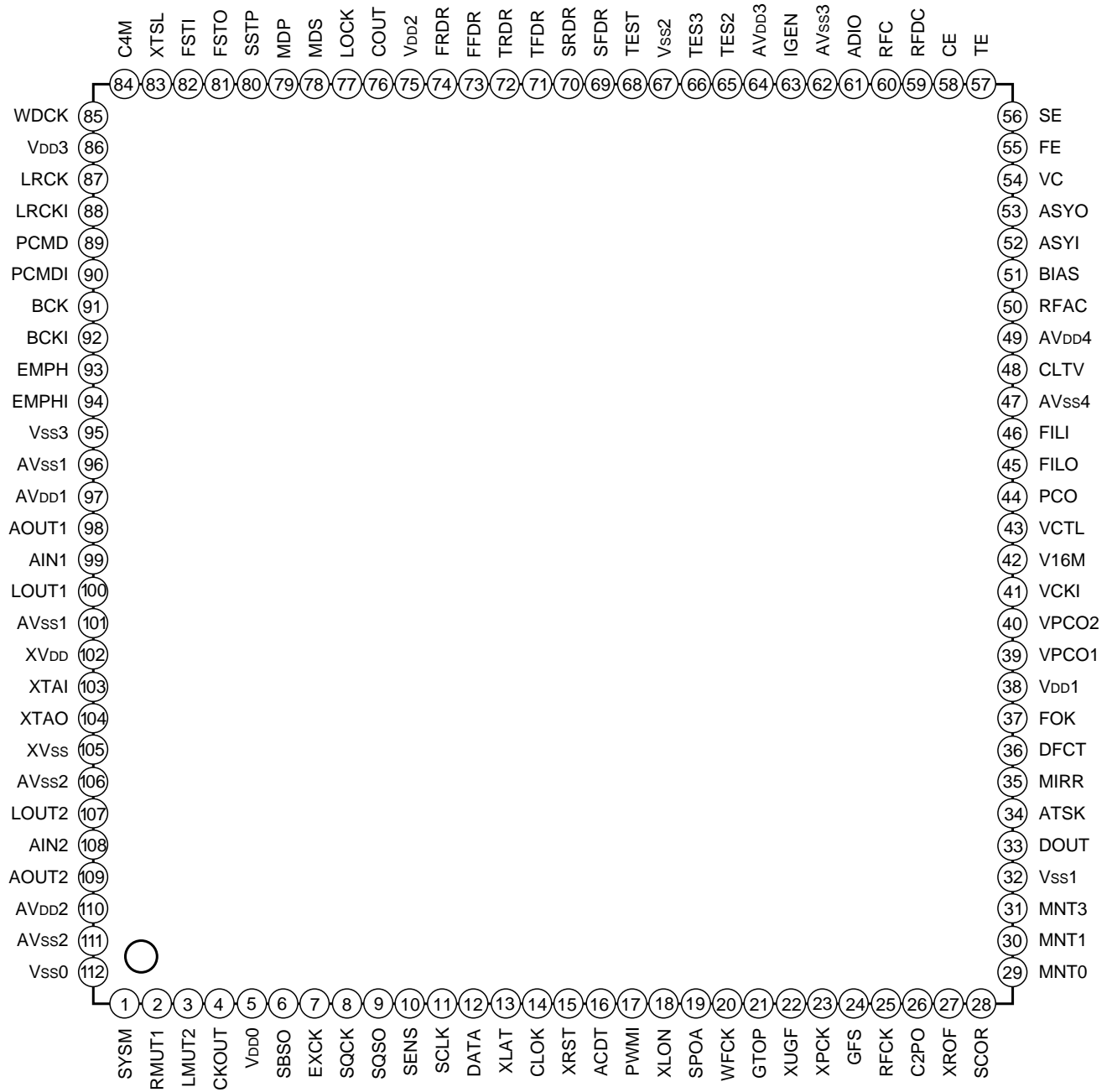
Note) Measurement conditions $V_{DD} = V_I = 0V$
 $f_m = 1MHz$

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Block Diagram



Pin Configuration



Pin Description

| Pin No. | Symbol | I/O | | Description |
|---------|------------------|-----|------|--|
| 1 | SYSM | I | | System mute input. (high = on, low = off) |
| 2 | RMUT1 | O | 1, 0 | R ch zero detection output. (high = on, low = off) |
| 3 | LMUT2 | O | 1, 0 | L ch zero detection output. (high = on, low = off) |
| 4 | CKOUT | O | 1, 0 | DAC master clock frequency division output. Either the clock input from XTAI $\times 1$, $\times 1/2$ or $\times 1/4$, or low output is selected and output. |
| 5 | V _{DD0} | | | Digital power supply. |
| 6 | SBSO | O | 1, 0 | Sub P to W serial output. |
| 7 | EXCK | I | | SBSO readout clock input. |
| 8 | SQCK | I | | SQSO readout clock input. |
| 9 | SQSO | O | 1, 0 | Sub Q 80-bit and PCM peak and level data 16-bit output. |
| 10 | SENS | O | 1, 0 | SENS output to CPU. |
| 11 | SCLK | I | | SENS serial data readout clock input. |
| 12 | DATA | I | | Serial data input from CPU. |
| 13 | XLAT | I | | Latch input from CPU. Serial data is latched at the falling edge. |
| 14 | CLOK | I | | Serial data transfer clock input from CPU. |
| 15 | XRST | I | | System reset. Reset when low. |
| 16 | ACDT | O | 1, 0 | Normally not used. Leave open. |
| 17 | PWMI | I | | Spindle motor external control input. |
| 18 | XLON | O | 1, 0 | Microcomputer extension interface (output). |
| 19 | SPOA | I | | Microcomputer extension interface (input A). |
| 20 | WFCK | O | 1, 0 | WFCK (Write Flame Clock) output. |
| 21 | GTOP | O | 1, 0 | GTOP output. |
| 22 | XUGF | O | 1, 0 | XUGF output. |
| 23 | XPCK | O | 1, 0 | XPLCK output. |
| 24 | GFS | O | 1, 0 | GFS output. |
| 25 | RFCK | O | 1, 0 | RFCK output. |
| 26 | C2PO | O | 1, 0 | C2PO output. |
| 27 | XROF | O | 1, 0 | XRAOF output. |
| 28 | SCOR | O | 1, 0 | Outputs a high signal when either subcode sync S0 or S1 is detected. |
| 29 | MNT0 | O | 1, 0 | MNT0 output. |
| 30 | MNT1 | O | 1, 0 | MNT1 output. |
| 31 | MNT3 | O | 1, 0 | MNT3 output. |
| 32 | V _{SS1} | | | Digital GND. |
| 33 | DOUT | O | 1, 0 | Digital Out output pin. |
| 34 | ATSK | I | | Anti-shock pin. |
| 35 | MIRR | O | 1, 0 | Mirror signal output. |
| 36 | DFCT | O | 1, 0 | Defect signal output. |

| Pin No. | Symbol | I/O | | Description |
|---------|-------------------|-----|---------|---|
| 37 | FOK | O | 1, 0 | Focus OK signal output. |
| 38 | V _{DD1} | | | Digital power supply. |
| 39 | VPCO1 | O | 1, Z, 0 | Wide-band EFM PLL charge pump output. |
| 40 | VPCO2 | O | 1, Z, 0 | Wide-band EFM PLL VCO2 charge pump output. |
| 41 | VCKI | I | | Wide-band EFM PLL VCO2 oscillation input. |
| 42 | V16M | O | 1, 0 | Wide-band EFM PLL VCO2 oscillation output. |
| 43 | VCTL | I | | Wide-band EFM PLL VCO2 control input. |
| 44 | PCO | O | 1, Z, 0 | Master PLL charge pump output. |
| 45 | FILO | O | Analog | Master PLL filter output (slave = digital PLL). |
| 46 | FILI | I | | Master PLL filter input. |
| 47 | AV _{ss4} | | | Analog GND. |
| 48 | CLTV | I | | Master VCO control voltage input. |
| 49 | AV _{DD4} | | | Analog power supply. |
| 50 | RFAC | I | | EFM signal input. |
| 51 | BIAS | I | | Asymmetry circuit constant current input. |
| 52 | ASYI | I | | Asymmetry comparator voltage input. |
| 53 | ASYO | O | 1, 0 | EFM full-swing output (low = V _{ss} , high = V _{DD}). |
| 54 | VC | I | | Center voltage input. |
| 55 | FE | I | | Focus error signal input. |
| 56 | SE | I | | Sled error signal input. |
| 57 | TE | I | | Tracking error signal input. |
| 58 | CE | I | | Center error signal input. |
| 59 | RFDC | I | | RF signal input. Input range: 2.15 to 5.0V. (when DV _{DD} = AV _{DD} = 5.0V) |
| 60 | RFC | I | | Connects an RF signal LPF time-constant capacitor. |
| 61 | ADIO | O | | Operational amplifier output. |
| 62 | AV _{ss3} | | | Analog GND. |
| 63 | IGEN | I | | Connects an operational amplifier current source reference resistor. |
| 64 | AV _{DD3} | | | Analog power supply. |
| 65 | TES2 | I | | Test pin. Normally fixed to low. |
| 66 | TES3 | I | | Test pin. Normally fixed to low. |
| 67 | V _{ss2} | | | Digital GND. |
| 68 | TEST | I | | Test pin. Normally fixed to low. |
| 69 | SFDR | O | 1, 0 | Sled drive output. |
| 70 | SRDR | O | 1, 0 | Sled drive output. |
| 71 | TFDR | O | 1, 0 | Tracking drive output. |
| 72 | TRDR | O | 1, 0 | Tracking drive output. |
| 73 | FFDR | O | 1, 0 | Focus drive output. |

| Pin No. | Symbol | I/O | | Description |
|---------|-------------------|-----|--------|---|
| | | | | |
| 74 | FRDR | O | 1, 0 | Focus drive output. |
| 75 | V _{DD2} | | | Digital power supply. |
| 76 | COUT | O | 1, 0 | Track count signal output. |
| 77 | LOCK | O | 1, 0 | GFS is sampled at 460Hz; when GFS is high, this pin outputs a high signal. If GFS is low eight consecutive samples, this pin outputs low. |
| 78 | MDS | O | 1, 0 | Spindle motor servo control output. |
| 79 | MDP | O | 1, 0 | Spindle motor servo control output. |
| 80 | SSTP | I | | Disc innermost track detection signal input. |
| 81 | FSTO | O | 1, 0 | 2/3-frequency division output for Pins 103 and 104. |
| 82 | FSTI | I | | Digital servo reference clock input. |
| 83 | XTSL | I | | Crystal selection input. Low when the crystal is 16.9344MHz; high when the crystal is 33.8688MHz. |
| 84 | C4M | O | 1, 0 | 4.2336MHz output. |
| 85 | WDCK | O | 1, 0 | D/A interface. Word clock $f = 2F_s$ |
| 86 | V _{DD3} | | | Digital power supply. |
| 87 | LRCK | O | 1, 0 | D/A interface. LR clock $f = F_s$ |
| 88 | LRCKI | I | | LR clock input to DAC (48-bit slot). |
| 89 | PCMD | O | 1, 0 | D/A interface. Serial data. (two's complement, MSB first) |
| 90 | PCMDI | I | | Audio data input to DAC (48-bit slot). |
| 91 | BCK | O | 1, 0 | D/A interface. Bit clock. |
| 92 | BCKI | I | | Bit clock input to DAC (48-bit slot). |
| 93 | EMPH | O | 1, 0 | Outputs a high signal when the playback disc has emphasis, and a low signal when there is no emphasis. |
| 94 | EMPHI | I | | DAC de-emphasis ON/OFF. (high = on, low = off) |
| 95 | V _{SS3} | | | Digital GND. |
| 96 | AV _{SS1} | | | L ch, analog GND. |
| 97 | AV _{DD1} | | | L ch, analog power supply. |
| 98 | AOUT1 | O | Analog | L ch, analog output. |
| 99 | AIN1 | I | | L ch, operational amplifier input. |
| 100 | LOUT1 | O | Analog | L ch, LINE output. |
| 101 | AV _{SS1} | | | L ch, analog GND. |
| 102 | XV _{DD} | | | Master clock analog power supply. |
| 103 | XTAI | I | | Master clock 16.9344MHz crystal oscillation circuit input, or 33.8688MHz input. |
| 104 | XTAO | O | 1, 0 | Master clock 16.9344MHz crystal oscillation circuit output. |
| 105 | XV _{SS} | | | Master clock analog GND. |
| 106 | AV _{SS2} | | | R ch, analog GND. |
| 107 | LOUT2 | O | Analog | R ch, LINE output. |
| 108 | AIN2 | I | | R ch, operational amplifier input. |
| 109 | AOUT2 | O | Analog | R ch, analog output. |

| Pin No. | Symbol | I/O | | Description |
|---------|-------------------|-----|--|----------------------------|
| 110 | AV _{DD2} | | | R ch, analog power supply. |
| 111 | AV _{SS2} | | | R ch, analog GND. |
| 112 | V _{SS0} | | | Digital GND. |

- Notes)**
- PCMD is a MSB first, two's complement output.
 - GTOP is used to monitor the frame sync protection status. (High: sync protection window released.)
 - XUGF is the frame sync obtained from the EFM signal, and negative pulse. It is the signal before sync protection.
 - XPLCK is the inverse of the EFM PLL clock. The PLL is designed so that the falling edge and the EFM signal transition point coincide.
 - The GFS signal goes high when the frame sync and the insertion timing match.
 - RFCK is derived from the crystal accuracy, and has a cycle of 136 μ s (during normal speed).
 - C2PO represents the data error status.
 - XRAOF is generated when the 16K RAM exceeds the $\pm 4F$ jitter margin.

Electrical Characteristics

1. DC Characteristics

(V_{DD} = AV_{DD} = 5.0V ± 5%, V_{SS} = AV_{SS} = 0V, Topr = -20 to +75°C)

| Item | | | Conditions | Min. | Typ. | Max. | Unit | Applicable pins |
|-----------------------------------|---------------------------|---------------------|------------------------------|-----------------------|------|--------------------|------|-----------------|
| Input voltage (1) | High level input voltage | V _{IH} (1) | | 0.7V _{DD} | | | V | *1 |
| | Low level input voltage | V _{IL} (1) | | | | 0.3V _{DD} | V | |
| Input voltage (2) | High level input voltage | V _{IH} (2) | Schmitt input | 0.8V _{DD} | | | V | *2 |
| | Low level input voltage | V _{IL} (2) | | | | 0.2V _{DD} | V | |
| Input voltage (3) | Input voltage | V _{IN} (3) | Analog input | V _{SS} | | V _{DD} | V | *3, 7, 8, 10 |
| Output voltage (1) | High level output voltage | V _{OH} (1) | I _{OH} = -4mA | V _{DD} - 0.8 | | V _{DD} | V | *4 |
| | Low level output voltage | V _{OL} (1) | I _{OL} = 4mA | 0 | | 0.4 | V | |
| Output voltage (2) | High level output voltage | V _{OH} (2) | I _{OH} = -2mA | V _{DD} - 0.8 | | V _{DD} | V | *5 |
| | Low level output voltage | V _{OL} (2) | I _{OL} = 4mA | 0 | | 0.4 | V | |
| Output voltage (3) | High level output voltage | V _{OH} (3) | I _{OH} = -0.28mA | V _{DD} - 0.5 | | V _{DD} | V | *6 |
| | Low level output voltage | V _{OL} (3) | I _{OL} = 0.36mA | 0 | | 0.4 | V | |
| Input leak current (1) | | I _{LI} (1) | V _I = 0 to 5.5V | -10 | | 10 | μA | *1, 2 |
| Input leak current (2) | | I _{LI} (2) | V _I = 1.5 to 3.5V | -20 | | 20 | μA | *7 |
| Input leak current (3) | | I _{LI} (3) | V _I = 0 to 5.0V | -40 | | 600 | μA | *8 |
| Tri-state pin output leak current | | I _{LO} | V _O = 0 to 5.5V | -5 | | 5 | μA | *9 |

Applicable pins

*1 XTSL, DATA, XLAT, TEST, TES2, TES3, SSTP, ATSK, PWMI, SYSM, EMPHI, PCMDI

*2 CLOK, XRST, EXCK, SQCK, VCKI, LRCKI, BCKI, SPOA, SCLK

*3 CLTV, FILI, RFAC, VCTL, AIN1, AIN2, ASYI

*4 MDP, PCO, PDO, VPCO1, VPCO2

*5 ASYO, DOUT, FSTO, C4M, SBSO, SQSO, SCOR, EMPH, LOCK, WDCK, SENS, MDS, MNT0, MNT1, MNT3, WFCK, V16M, CKOUT, LMUT2, RMUT1, XLON, LRCK, PCMD, BCK, GTOP, XUGF, XPCK, GFS, RFCK, C2PO, XRAOF, MIRR, DFCT, COUT, FFDR, FRDR, TFDR, TRDR, SFDR, SRDR

*6 FILO

*7 TE, SE, FE, CE, VC

*8 RFDC

*9 SENS, MDS, MDP, PDO, PCO, VPCO1, VPCO2

*10 RFC

2. AC Characteristics

(1) XTAI pin

(a) When using self-excited oscillation

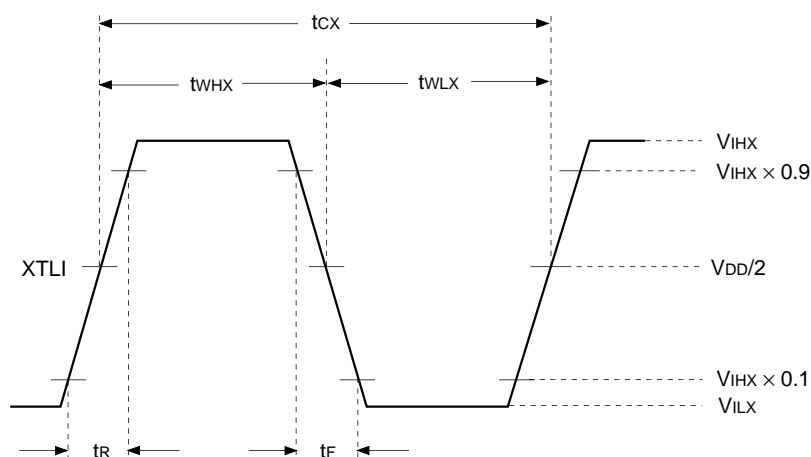
(Topr = -20 to +75°C, VDD = AVDD = 5.0V ± 5%)

| Item | Symbol | Min. | Typ. | Max. | Unit |
|-----------------------|------------------|------|------|------|------|
| Oscillation frequency | f _{MAX} | 7 | | 34 | MHz |

(b) When inputting pulses to XTAI pin

(Topr = -20 to +75°C, VDD = AVDD = 5.0V ± 5%)

| Item | Symbol | Min. | Typ. | Max. | Unit |
|------------------------|---------------------------------|-----------------------|------|-------|------|
| High level pulse width | t _{WHX} | 13 | | 500 | ns |
| Low level pulse width | t _{WLX} | 13 | | 500 | ns |
| Pulse cycle | t _{CK} | 26 | | 1,000 | ns |
| Input high level | V _{IHX} | V _{DD} - 1.0 | | | V |
| Input low level | V _{ILX} | | | 0.8 | V |
| Rise time, fall time | t _R , t _F | | | 10 | ns |



(c) When inputting sine waves to XTLI pin via a capacitor

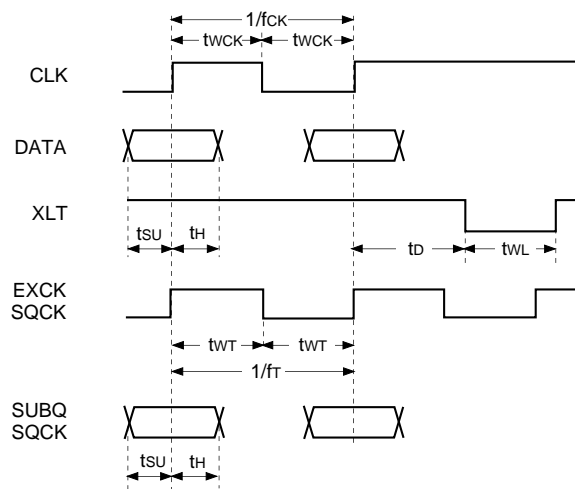
(Topr = -20 to +75°C, VDD = AVDD = 5.0V ± 5%)

| Item | Symbol | Min. | Typ. | Max. | Unit |
|-----------------|----------------|------|------|-----------------------|------------------|
| Input amplitude | V _I | 2.0 | | V _{DD} + 0.3 | V _{p-p} |

(2) CLOK, DATA, XLAT, SQCK, and EXCK pins

($V_{DD} = AV_{DD} = 5.0V \pm 5\%$, $V_{SS} = AV_{SS} = 0V$, $T_{opr} = -20$ to $+75^{\circ}C$)

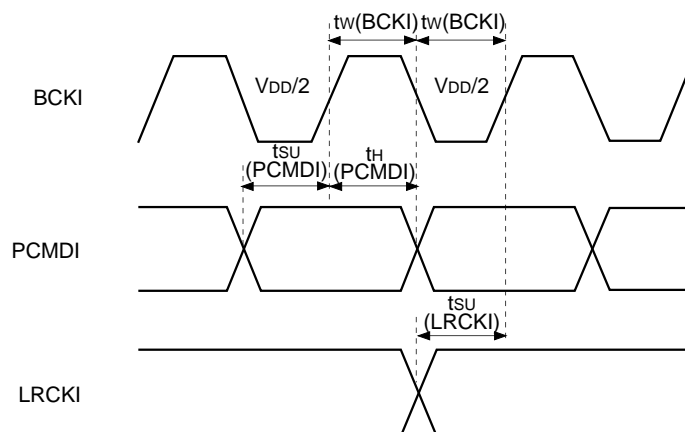
| Item | Symbol | Min. | Typ. | Max. | Unit |
|------------------------|-----------|------------|------|-------------|------|
| Clock frequency | f_{CK} | | | 0.65 | MHz |
| Clock pulse width | t_{WCK} | 750 | | | ns |
| Setup time | t_{SU} | 300 | | | ns |
| Hold time | t_H | 300 | | | ns |
| Delay time | t_D | 300 | | | ns |
| Latch pulse width | t_{WL} | 750 | | | ns |
| EXCK, SQCK frequency | f_T | | | 0.65^{*1} | MHz |
| EXCK, SQCK pulse width | f_{WT} | 750^{*1} | | | ns |



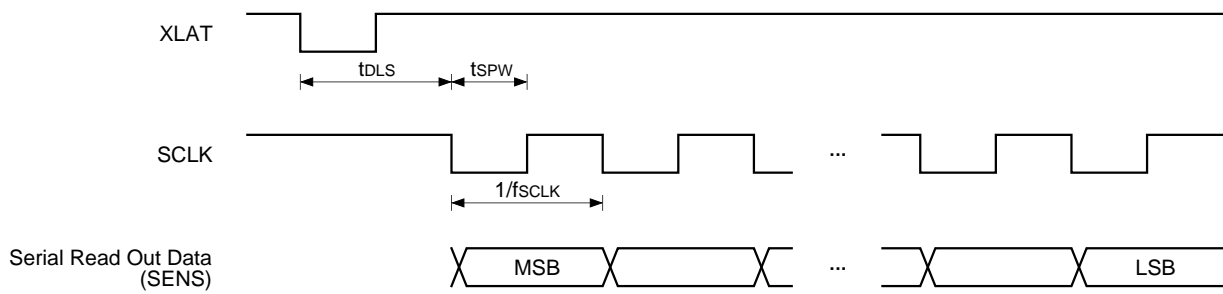
*1 In quasi double-speed playback mode, except when SQSO is Sub Q Read, the SQCL maximum operating frequency is 300kHz and its minimum pulse width is 1.5 μ s.

(3) BCKI, LRCKI and PCMDI pins ($V_{DD} = AV_{DD} = 5.0V \pm 5\%$, $V_{SS} = AV_{SS} = 0V$, $T_{opr} = -20$ to $+75^{\circ}C$)

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---------------------|----------|------------|------|------|------|------|
| BCK pulse width | t_w | | 94 | | | ns |
| DATAL, R setup time | t_{SU} | | 18 | | | ns |
| DATAL, R hold time | t_H | | 18 | | | ns |
| LRCK setup time | t_{SU} | | 18 | | | ns |



(4) SCLK pin



| Item | Symbol | Min. | Typ. | Max. | Unit |
|------------------|------------|------|------|------|---------|
| SCLK frequency | f_{SCLK} | | | 1 | MHz |
| SCLK pulse width | t_{SPW} | 500 | | | ns |
| Delay time | t_{DLS} | 15 | | | μ s |

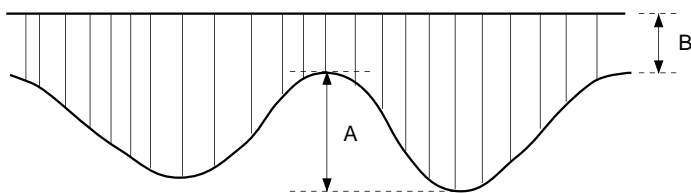
(5) COUT, MIRR and DFCT pins

Operating frequency ($V_{DD} = AV_{DD} = 5.0V \pm 5\%$, $V_{SS} = AV_{SS} = 0V$, $T_{opr} = -20$ to $+75^\circ C$)

| Item | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|----------------------------------|-------------|------|------|------|------|------------|
| COUT maximum operating frequency | f_{COUT} | 40 | | | kHz | *1 |
| MIRR maximum operating frequency | f_{MIRR} | 40 | | | kHz | *2 |
| DFCT maximum operating frequency | f_{DFCTH} | 5 | | | kHz | *3 |

*1 When using a high-speed traverse TZC

*2



When the RF signal continuously satisfies the following conditions during the above traverse.

• $A = 0.6$ to $1.3V$

• $\frac{B}{A + B} = 25\%$ or less

*3 During complete RF signal omission

When settings related to DFCT signal generation are Typ.

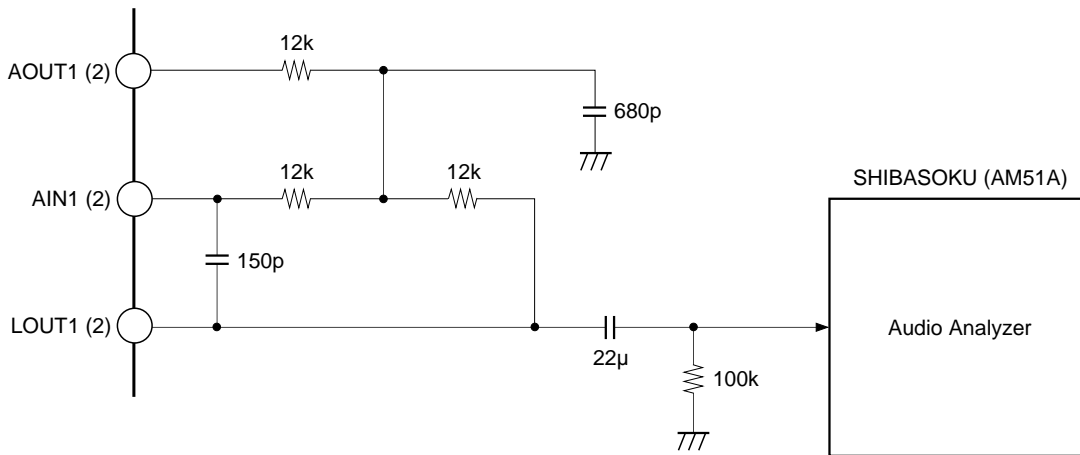
1-bit DAC and LPF Block Analog Characteristics

Analog characteristics ($V_{DD} = AV_{DD} = 5.0V$, $V_{SS} = AV_{SS} = 0V$, $T_a = 25^{\circ}C$)

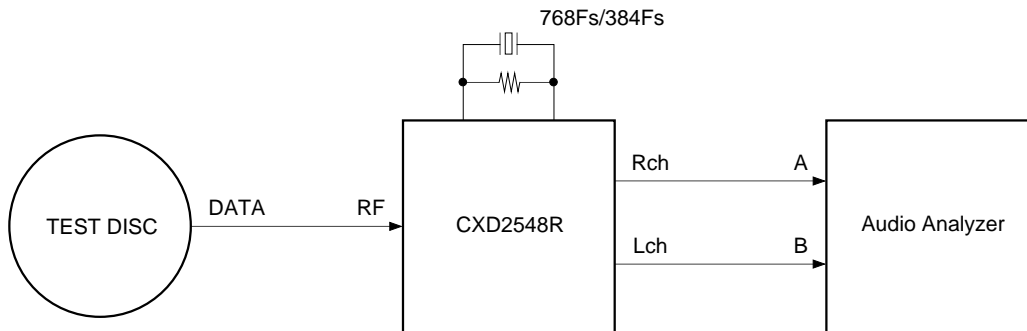
| Item | Symbol | Conditions | Crystal | Min. | Typ. | Max. | Unit |
|---------------------------|--------|--|---------|------|--------|--------|------|
| Total harmonic distortion | THD | 1kHz, 0dB data | 384Fs | | 0.0050 | 0.0070 | % |
| | | | 768Fs | | 0.0045 | 0.0065 | |
| Signal-to-noise ratio | S/N | 1kHz, 0dB data (Using A-weighting filter) | 384Fs | 96 | 100 | | dB |
| | | | 768Fs | 96 | 100 | | |

Fs = 44.1kHz in all cases.

The total harmonic distortion and signal-to-noise ratio measurement circuits are shown below.



LPF external circuit diagram



Block diagram of analog characteristics measurement

($V_{DD} = AV_{DD} = 5.0V$, $V_{SS} = AV_{SS} = 0V$, $T_{opr} = -20$ to $+75^{\circ}C$)

| Item | Symbol | Min. | Typ. | Max. | Unit | Applicable pins |
|-----------------|-----------|------|-------|------|-----------|-----------------|
| Output voltage | V_{OUT} | | 1.15* | | Vrms | *1 |
| Load resistance | R_L | 8 | | | $k\Omega$ | *1 |

* When a sine wave of 1kHz and 0dB is output.

Applicable pins

*1 LOUT1, LOUT2

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[5] Application Circuit

| | |
|---------------------------------|-----|
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|---------------------------------|-----|

| | |
|------------------------------|---------------------------|
| Explanation of abbreviations | AVRG: Average |
| | AGCNTL: auto gain control |
| | FCS: Focus |
| | TRK: Tracking |
| | SLD: Sled |
| | DFCT: Defect |

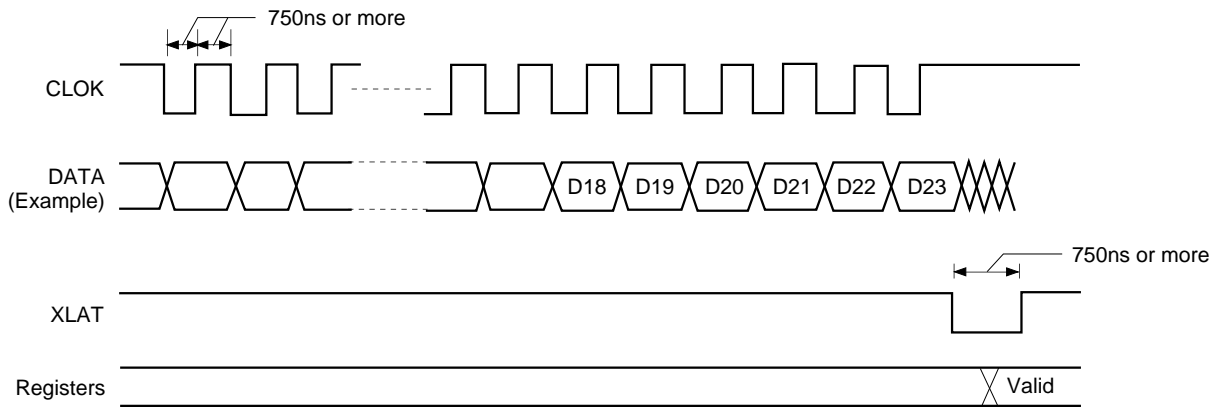
[1] CPU Interface

§1-1. CPU Interface Timing

• CPU Interface

This interface uses DATA, CLOK, and XLAT to set the modes.

The interface timing chart is shown below.



- The internal registers are initialized by a reset when XRST = 0.

Note) Be sure to set SQCK to high when XLAT is low.

Command Table (\$340X)

| Register | Command | Address 1 | | Address 2 | | Address 3 | | Address 4 | | | Data 1 | | | | Data 2 | | | | | | |
|----------|---------|------------|------------|------------|-----|-----------|----|-----------|----|-----|--------|-----|-----|-----|--------|-----|-----|------------------------------------|-----|-----|--|
| | | D23 to D20 | D19 to D16 | D15 to D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | | | | |
| 3 | SELECT | 0 0 1 1 | 0 1 0 0 | 0 0 0 0 | 0 | 0 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K00) SLED INPUT GAIN | | | |
| | | | | | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K01) SLED LOW BOOST FILTER A-H |
| | | | | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K02) SLED LOW BOOST FILTER A-L |
| | | | | | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K03) SLED LOW BOOST FILTER B-H |
| | | | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K04) SLED LOW BOOST FILTER B-L |
| | | | | | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K05) SLED OUTPUT GAIN |
| | | | | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K06) FOCUS INPUT GAIN |
| | | | | | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K07) SLED AUTO GAIN |
| | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K08) FOCUS HIGH CUT FILTER A |
| | | | | | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K09) FOCUS HIGH CUT FILTER B |
| | | | | | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K0A) FOCUS LOW BOOST FILTER A-H |
| | | | | | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K0B) FOCUS LOW BOOST FILTER A-L |
| | | | | | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K0C) FOCUS LOW BOOST FILTER B-H |
| | | | | | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K0D) FOCUS LOW BOOST FILTER B-L |
| | | | | | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K0E) FOCUS PHASE COMPENSATE FILTER A |
| | | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K0F) FOCUS DEFECT HOLD GAIN |

Command Table (\$342X)

| Register | Command | Address 1 | | Address 2 | | Address 3 | | Address 4 | | | Data 1 | | | | Data 2 | | | | | | | |
|----------|---------|------------|------------|------------|-----|-----------|----|-----------|----|-----|--------|-----|-----|-----|--------|-----|-----|---|---|---|---|--|
| | | D23 to D20 | D19 to D16 | D15 to D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | | | | | |
| 3 | SELECT | 0 0 1 1 | 0 1 0 0 | 0 0 1 0 | 0 | 0 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K20) TRACKING PHASE COMPENSATE FILTER A | | | | |
| | | | | | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | KRAM DATA (K21) TRACKING PHASE COMPENSATE FILTER B | |
| | | | | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | KRAM DATA (K22) TRACKING OUTPUT GAIN |
| | | | | | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | KRAM DATA (K23) TRACKING AUTO GAIN |
| | | | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | KRAM DATA (K24) FOCUS GAIN DOWN HIGH CUT FILTER A |
| | | | | | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | KRAM DATA (K25) FOCUS GAIN DOWN HIGH CUT FILTER B |
| | | | | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | KRAM DATA (K26) FOCUS GAIN DOWN LOW BOOST FILTER A-H |
| | | | | | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | KRAM DATA (K27) FOCUS GAIN DOWN LOW BOOST FILTER A-L |
| | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | KRAM DATA (K28) FOCUS GAIN DOWN LOW BOOST FILTER B-H |
| | | | | | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | KRAM DATA (K29) FOCUS GAIN DOWN LOW BOOST FILTER B-L |
| | | | | | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | KRAM DATA (K2A) FOCUS GAIN DOWN PHASE COMPENSATE FILTER A |
| | | | | | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | KRAM DATA (K2B) FOCUS GAIN DOWN DEFECT HOLD GAIN |
| | | | | | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | KRAM DATA (K2C) FOCUS GAIN DOWN PHASE COMPENSATE FILTER B |
| | | | | | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | KRAM DATA (K2D) FOCUS GAIN DOWN OUTPUT GAIN |
| | | | | | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | KRAM DATA (K2E) NOT USED |
| | | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | KRAM DATA (K2F) NOT USED |

Command Table (\$34FX to 3FX)

| Register | Command | Address | | | | | | | | | | | | | | | | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | |
|------------|---------|------------|-----|-----|-----|------|------|------|------|------|------|------|------|------|------|------|------|--------|------|------|------|--------|------|------|--|--------------------------------------|------------|--|---------------------------------------|--------|--|--|--|
| | | D23 to D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | | | | | | | | | | |
| 3 | SELECT | 0 0 1 1 | | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | FBL9 | FBL8 | FBL7 | FBL6 | FBL5 | FBL4 | FBL3 | FBL2 | FBL1 | | | | | FOCUS BIAS LIMIT | | | | | | | |
| | | 0 0 1 1 | | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | FB9 | FB8 | FB7 | FB6 | FB5 | FB4 | FB3 | FB2 | FB1 | | | | | FOCUS BIAS DATA | | | | | | | |
| | | 0 0 1 1 | | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | TV9 | TV8 | TV7 | TV6 | TV5 | TV4 | TV3 | TV2 | TV1 | TV0 | | | | | TRVSC DATA | | | | | | |
| | | D23 to D20 | | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | | | | | | | | | |
| | | 0 0 1 1 | | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | FS1 | FS0 | FTZ | FG6 | FG5 | FG4 | FG3 | FG2 | FG1 | FG0 | | | | | FOCUS SEARCH SPEED/ VOLTAGE/AUTO GAIN | | | | | |
| | | 0 0 1 1 | | 0 | 1 | 1 | 1 | 0 | 0 | DTZC | TJ5 | TJ4 | TJ3 | TJ2 | TJ1 | TJ0 | SFJP | TG6 | TG5 | TG4 | TG3 | TG2 | TG1 | TG0 | | | | | DTZC/TRACK JUMP VOLTAGE/AUTO GAIN | | | | |
| | | 0 0 1 1 | | 0 | 1 | 1 | 1 | 1 | 1 | FZSH | FZSL | SM5 | SM4 | SM3 | SM2 | SM1 | SM0 | AGS | AGJ | AGGF | AGVT | AGV2 | AGHS | AGHT | | | | | FZSL/SLED MOVE/ Voltage/AUTO GAIN | | | | |
| | | 0 0 1 1 | | 1 | 0 | 0 | 0 | 0 | VCLM | VCLC | FLM | FLC0 | RFLM | RFLC | AGF | AGT | DFSW | LKSW | TBLM | TCLM | FLC1 | TLC2 | TLC1 | TLC0 | | | | | LEVEL/AUTO GAIN/ DFSW (Initialize) | | | | |
| | | 1 0 0 0 | | 1 | 0 | 0 | 1 | DAC | SD6 | SD5 | SD4 | SD3 | SD2 | SD1 | SD0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | SERIAL DATA READ MODE/SELECT | | | | |
| | | 1 0 0 1 | | 1 | 0 | 1 | 0 | 0 | FBON | FBSS | FBUP | FBV1 | FBV0 | 0 | TJD0 | FPS1 | FPS0 | TPS1 | TPS0 | CEIT | SJHD | INBK | MTI0 | | | | | FOCUS BIAS | | | | | |
| | | 1 0 0 1 | | 1 | 0 | 1 | 1 | SFO2 | SFO1 | SDF2 | SDF1 | MAX2 | MAX1 | SFOX | BTF | D2V2 | D2V1 | D1V2 | D1V1 | RINT | 0 | 0 | 0 | 0 | | | | | Operation for MIRR/ DFCT/FOK | | | | |
| | | D23 to D20 | | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | | | | | | | | | |
| 0 0 1 1 | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | TZC for COUT SLCT HPTZC (Default) | | | | | | | |
| 1 1 0 0 | | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | TZC for COUT SLCT DTZC | | | | | | | |
| D23 to D20 | | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | | | | | | | | | | | |
| 0 0 1 1 | | 1 | 1 | 1 | 0 | F1NM | F1DM | F3NM | F3DM | T1NM | T1UM | T3NM | T3UM | DFIS | TLCD | RFLP | 0 | 0 | 0 | MIRI | XT1D | | | | | Filter | | | | | | | |
| 1 1 1 1 | | 1 | 1 | 1 | 1 | 0 | AGG4 | XT4D | XT2D | 0 | DRR2 | DRR1 | DRR0 | 0 | ASFG | 0 | LPAS | SRO1 | 0 | AGHF | COT2 | | | | | Others | | | | | | | |

--: Don't care

Command Table (\$4X to EX)

| Register name | Command | Address | | | | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | | Data 5 | | | | Data 6 | | | | | |
|---------------|--|---------|-----|-----|-----|---------------|----------------|----------------|--------------|-------------|------|--------------|-------------|--------|------|--------|--------|--------------|--------------|------|-----|--------|-----|-----|-----|--------|----|----|----|---|---|
| | | D27 | D26 | D25 | D24 | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| 4 | Auto sequence | 0 | 1 | 0 | 0 | AS3 | AS2 | AS1 | AS0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | | |
| 5 | Blind (A, E), Overflow (C) | 0 | 1 | 0 | 1 | 0.18ms | 0.09ms | 0.05ms | 0.02ms | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | | |
| | Brake (B) | 0 | 1 | 0 | 0 | 0.36ms | 0.18ms | 0.09ms | 0.05ms | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | | |
| 6 | Kick (D) | 0 | 1 | 1 | 0 | 11.6ms | 5.8ms | 2.9ms | 1.45ms | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | | |
| 7 | Auto sequence (N) track jump count | 0 | 1 | 1 | 1 | 32768 | 16384 | 8192 | 4096 | 2048 | 1024 | 512 | 256 | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | — | — | — | — | — | — | — | — | | |
| 8 | Mode specification | 1 | 0 | 0 | 0 | GDROM | DOUT Mute | DOUT ON/OFF | WSEL | VCO SEL1 | 0 | SOCT SEL2 | VCO SEL2 | KSL3 | KSL2 | KSL1 | KSL0 | 0 | 0 | 1 | 0 | — | — | — | — | — | — | — | — | — | |
| 9 | Function specification | 1 | 0 | 0 | 1 | 0 | DSPB ON/OFF | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MCSL | CKOSL1 | CKOSL0 | ZDPL | ZMUT | — | — | — | — | — | — | — | — | — | — | — | |
| A | Audio CTRL | 1 | 0 | 1 | 0 | 0 | 0 | Mute | ATT | 0 | 0 | 0 | 0 | 0 | 0 | AD9 | AD8 | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 | FMUT | 0 | 0 | 0 | 0 | |
| B | Serial bus CTRL | 1 | 0 | 1 | 1 | SL1 | SL0 | CPUSR | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | |
| C | Spindle servo coefficient setting | 1 | 1 | 0 | 0 | Gain MDP1 | Gain MDP0 | Gain MDS1 | Gain MDS0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | |
| D | CLV CTRL | 1 | 1 | 0 | 1 | DCLV PWMMD | TB | TP | Gain CLVS | VP7 | VP6 | VP5 | VP4 | VP3 | VP2 | VP1 | VP0 | — | — | — | — | — | — | — | — | — | — | — | — | — | |
| E | CLV MODE | 1 | 1 | 1 | 0 | CM3 | CM2 | CM1 | CM0 | EPWM | SPDC | ICAP | SFSL | VC2C | HIFC | LPWR | VPON | Gain CAV1 | Gain CAV0 | FCSW | 0 | — | — | — | — | — | — | — | — | — | — |

—: Don't care

§1-3. CPU Command Presets

Command Preset Table (\$0X to 34X)

| Register | Command | Address | | | | | | | | | | | | | | | | | | | | | |
|----------|------------------|---------|-----|-----|-----|--------|-----|-----|-----|--------|-----|----|----|--------|----|----|----|--------|----|----|----|-----------------------------------|--|
| | | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | | Data 5 | | | | | |
| | | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| 0 | FOCUS CONTROL | 0 | 0 | 0 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | FOCUS SERVO OFF, 0V OUT | |
| 1 | TRACKING CONTROL | 0 | 0 | 0 | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | TRACKING GAIN UP FILTER SELECT 1 | |
| 2 | TRACKING MODE | 0 | 0 | 0 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | TRACKING SERVO OFF SLED SERVO OFF | |
| Register | Command | Address | | | | | | | | | | | | | | | | | | | | | |
| | | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | | Data 5 | | | | | |
| | | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| 3 | SELECT | 0 0 1 1 | 0 | 0 | 0 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SLED KICK LEVEL (±1 × basic value) (Default) |
| | | 0 0 1 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | KRAM DATA (\$3400XX to \$344FXX) |

—: Don't care

Command Preset Table (\$4X to EX)

| Register name | Command | Address | | | | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | | Data 5 | | | | Data 6 | | | |
|---------------|--|---------|-----|-----|-----|--------|-----|-----|-----|--------|-----|-----|-----|--------|-----|-----|-----|--------|-----|----|----|--------|----|----|----|--------|----|----|----|
| | | D27 | D26 | D25 | D24 | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 4 | Auto sequence | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| 5 | Blind (A, E), Overflow (C) | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| | Brake (B) | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| 6 | Kick (D) | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| 7 | Auto sequence (N) track jump count | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | — | — | — | — | — | — |
| 8 | Mode specification | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | — | — | — | — | — | — | — | — | — |
| 9 | Function specification | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | — | — | — | — | — | — | — | — | — |
| A | Audio CTRL | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| B | Serial bus CTRL | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| C | Spindle servo coefficient setting | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| D | CLV CTRL | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — |
| E | CLV MODE | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

—: Don't care

<Coefficient ROM Preset Values Table (1)>

| ADDRESS | DATA | CONTENTS |
|---------|------|---|
| K00 | E0 | SLED INPUT GAIN |
| K01 | 81 | SLED LOW BOOST FILTER A-H |
| K02 | 23 | SLED LOW BOOST FILTER A-L |
| K03 | 7F | SLED LOW BOOST FILTER B-H |
| K04 | 6A | SLED LOW BOOST FILTER B-L |
| K05 | 10 | SLED OUTPUT GAIN |
| K06 | 14 | FOCUS INPUT GAIN |
| K07 | 30 | SLED AUTO GAIN |
| K08 | 7F | FOCUS HIGH CUT FILTER A |
| K09 | 46 | FOCUS HIGH CUT FILTER B |
| K0A | 81 | FOCUS LOW BOOST FILTER A-H |
| K0B | 1C | FOCUS LOW BOOST FILTER A-L |
| K0C | 7F | FOCUS LOW BOOST FILTER B-H |
| K0D | 58 | FOCUS LOW BOOST FILTER B-L |
| K0E | 82 | FOCUS PHASE COMPENSATE FILTER A |
| K0F | 7F | FOCUS DEFECT HOLD GAIN |
| K10 | 4E | FOCUS PHASE COMPENSATE FILTER B |
| K11 | 32 | FOCUS OUTPUT GAIN |
| K12 | 20 | ANTI SHOCK INPUT GAIN |
| K13 | 30 | FOCUS AUTO GAIN |
| K14 | 80 | HPTZC / Auto Gain HIGH PASS FILTER A |
| K15 | 77 | HPTZC / Auto Gain HIGH PASS FILTER B |
| K16 | 80 | ANTI SHOCK HIGH PASS FILTER A |
| K17 | 77 | HPTZC / Auto Gain LOW PASS FILTER B |
| K18 | 00 | Fix* |
| K19 | F1 | TRACKING INPUT GAIN |
| K1A | 7F | TRACKING HIGH CUT FILTER A |
| K1B | 3B | TRACKING HIGH CUT FILTER B |
| K1C | 81 | TRACKING LOW BOOST FILTER A-H |
| K1D | 44 | TRACKING LOW BOOST FILTER A-L |
| K1E | 7F | TRACKING LOW BOOST FILTER B-H |
| K1F | 5E | TRACKING LOW BOOST FILTER B-L |
| K20 | 82 | TRACKING PHASE COMPENSATE FILTER A |
| K21 | 44 | TRACKING PHASE COMPENSATE FILTER B |
| K22 | 18 | TRACKING OUTPUT GAIN |
| K23 | 30 | TRACKING AUTO GAIN |
| K24 | 7F | FOCUS GAIN DOWN HIGH CUT FILTER A |
| K25 | 46 | FOCUS GAIN DOWN HIGH CUT FILTER B |
| K26 | 81 | FOCUS GAIN DOWN LOW BOOST FILTER A-H |
| K27 | 3A | FOCUS GAIN DOWN LOW BOOST FILTER A-L |
| K28 | 7F | FOCUS GAIN DOWN LOW BOOST FILTER B-H |
| K29 | 66 | FOCUS GAIN DOWN LOW BOOST FILTER B-L |
| K2A | 82 | FOCUS GAIN DOWN PHASE COMPENSATE FILTER A |
| K2B | 44 | FOCUS GAIN DOWN DEFECT HOLD GAIN |
| K2C | 4E | FOCUS GAIN DOWN PHASE COMPENSATE FILTER B |
| K2D | 1B | FOCUS GAIN DOWN OUTPUT GAIN |
| K2E | 00 | NOT USED |
| K2F | 00 | NOT USED |

<Coefficient ROM Preset Values Table (2)>

| ADDRESS | DATA | CONTENTS |
|---------|------|--|
| K30 | 80 | Fix* |
| K31 | 66 | ANTI SHOCK LOW PASS FILTER B |
| K32 | 00 | NOT USED |
| K33 | 7F | ANTI SHOCK HIGH PASS FILTER B-H |
| K34 | 6E | ANTI SHOCK HIGH PASS FILTER B-L |
| K35 | 20 | ANTI SHOCK FILTER COMPARATE GAIN |
| K36 | 7F | TRACKING GAIN UP2 HIGH CUT FILTER A |
| K37 | 3B | TRACKING GAIN UP2 HIGH CUT FILTER B |
| K38 | 80 | TRACKING GAIN UP2 LOW BOOST FILTER A-H |
| K39 | 44 | TRACKING GAIN UP2 LOW BOOST FILTER A-L |
| K3A | 7F | TRACKING GAIN UP2 LOW BOOST FILTER B-H |
| K3B | 77 | TRACKING GAIN UP2 LOW BOOST FILTER B-L |
| K3C | 86 | TRACKING GAIN UP PHASE COMPENSATE FILTER A |
| K3D | 0D | TRACKING GAIN UP PHASE COMPENSATE FILTER B |
| K3E | 57 | TRACKING GAIN UP OUTPUT GAIN |
| K3F | 00 | NOT USED |
| K40 | 04 | TRACKING HOLD FILTER INPUT GAIN |
| K41 | 7F | TRACKING HOLD FILTER A-H |
| K42 | 7F | TRACKING HOLD FILTER A-L |
| K43 | 79 | TRACKING HOLD FILTER B-H |
| K44 | 17 | TRACKING HOLD FILTER B-L |
| K45 | 6D | TRACKING HOLD FILTER OUTPUT GAIN |
| K46 | 00 | NOT USED |
| K47 | 00 | NOT USED |
| K48 | 02 | FOCUS HOLD FILTER INPUT GAIN |
| K49 | 7F | FOCUS HOLD FILTER A-H |
| K4A | 7F | FOCUS HOLD FILTER A-L |
| K4B | 79 | FOCUS HOLD FILTER B-H |
| K4C | 17 | FOCUS HOLD FILTER B-L |
| K4D | 54 | FOCUS HOLD FILTER OUTPUT GAIN |
| K4E | 00 | NOT USED |
| K4F | 00 | NOT USED |

* Fix indicates that normal preset values should be used.

§1-4. Description of SENS Signals

SENS output

| Microcomputer serial register (latching not required) | ASEQ = 1 | Output data length |
|--|--|--------------------|
| \$0X | FZC | — |
| \$1X | AS | — |
| \$2X | TZC | — |
| \$38 | AGOK*1 | — |
| \$38 | XAVEBSY*1 | — |
| \$30 to 37, \$3A to 3F | SSTP | — |
| \$3900 | VC In Reg. | 8 bit |
| \$3901 | SLD In Reg. | 8 bit |
| \$3902 | TRK In Reg. | 8 bit |
| \$3903 | FCS In Reg. | 8 bit |
| \$3904 | TE Avg Reg. | 9 bit |
| \$3908 | FE Avg Reg. | 9 bit |
| \$390C | VC Avg Reg. | 9 bit |
| \$391C | TRVSC Reg. | 9 bit |
| \$391D | FB Reg. | 9 bit |
| \$391E | RFDC In Reg. | 8 bit |
| \$391F | RFDC Avg Reg. | 8 bit |
| \$3920 to \$393F | Address 5-bit (M00 to 1F) data RAM data | 16 bit |
| \$3940 to \$397F | Address 6-bit (K00 to 3F) coefficient RAM data | 8 bit |
| \$4X | XBUSY | — |
| \$5X | FOK | — |
| \$6X | 0 | — |
| \$AX | GFS | — |
| \$EX | $\overline{\text{OV64}}$ | — |
| \$7X, 8X, 9X, BX, CX, DX, FX | 0 | — |

*1 \$38 outputs AGOK during AGT and AGF command settings, and XAVEBSY during AVRG measurement. SSTP is output in all other cases.

Note) The SENS output can be read from the SQSO pin when SOCT = 0, SL1 = 1 and SL0 = 0. (See "\$BX Commands".)

Description of SENS Signals

| | |
|--------------------------|--|
| SENS output | |
| XBUSY | Low while the auto sequencer is in operation, high when operation terminates. |
| FOK | Outputs the same signal as the FOK pin. High for "focus OK". |
| GFS | High when the regenerated frame sync is obtained with the correct timing. |
| $\overline{\text{OV64}}$ | Low when the EFM signal is lengthened by 64 channel lock pulses or more after passing through the sync detection filter. |

[2] Description of CD Signal Processing and DAC System Commands and Subcode Interface

2-1. Description of Commands and Data Sets

\$4X commands

| Command | AS3 | AS2 | AS1 | AS0 |
|---------------|-----|-----|-----|-----|
| CANCEL | 0 | 0 | 0 | 0 |
| FOCUS-ON | 0 | 1 | 1 | 1 |
| 1 TRACK JUMP | 1 | 0 | 0 | RXF |
| 10 TRACK JUMP | 1 | 0 | 1 | RXF |
| 2 NTRACK JUMP | 1 | 1 | 0 | RXF |
| N TRACK MOVE | 1 | 1 | 1 | RXF |

RXF = 0 FORWARD

RXF = 1 REVERSE

- When the Focus-on command (\$47) is canceled, \$02 is sent and the auto sequence is interrupted.
- When the Track jump/Move commands (\$48 to \$4F) are canceled, \$25 is sent and the auto sequence is interrupted.

\$5X commands

Auto sequence timer setting

Set timers: A, E, C, B

| Command | D23 | D22 | D21 | D20 |
|-----------------------------|--------|--------|--------|--------|
| Blind (A, E), Over flow (C) | 0.18ms | 0.09ms | 0.05ms | 0.02ms |
| Brake (B) | 0.36ms | 0.18ms | 0.09ms | 0.05ms |

e.g.) D2 = D0 = 1, D3 = D1 = 0 (Initial Reset)

A = E = C = 0.11ms

B = 0.23ms

\$6X commands

Auto sequence timer setting

Set timer: D

| Command | D23 | D22 | D21 | D20 |
|----------|--------|-------|-------|--------|
| KICK (D) | 11.6ms | 5.8ms | 2.9ms | 1.45ms |

e.g.) D3 = 0, D2 = D1 = D0 = 1 (Initial Reset)

D = 10.15ms

\$7X commands

Auto sequence track jump/move count setting (N)

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | |
|--|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| Auto sequence track jump count setting | 2 ¹⁵ | 2 ¹⁴ | 2 ¹³ | 2 ¹² | 2 ¹¹ | 2 ¹⁰ | 2 ⁹ | 2 ⁸ | 2 ⁷ | 2 ⁶ | 2 ⁵ | 2 ⁴ | 2 ³ | 2 ² | 2 ¹ | 2 ⁰ |

This command is used to set N when a 2N-track jump or N-track move is executed for auto sequence.

- The maximum track count is 65,535, but note that with a 2N-track jump the maximum track jump count depends on the mechanical limitations of the optical system.
- When the track jump count is from 0 to 15, the COUT signal is counted; when the count is 16 or over, the MIRR signal is counted.

\$8X commands

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | |
|--------------------|--------|-----------|-------------|------|----------|-----|------|----------|--------|------|------|------|
| | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 |
| Mode specification | CDROM | DOUT Mute | DOUT ON/OFF | WSEL | VCO SEL1 | 0 | SOCT | VCO SEL2 | KSL3 | KSL2 | KSL1 | KSL0 |

See "\$BX Commands".

| Data 4 | | | |
|--------|-----|----|----|
| D11 | D10 | D9 | D8 |
| 0 | 0 | 1 | 0 |

| Command bit | C2PO timing | Processing |
|-------------|-----------------------|---|
| CDROM = 1 | See Timing Chart 1-1. | CDROM mode; average value interpolation and pre-value hold are not performed. |
| CDROM = 0 | See Timing Chart 1-1. | Audio mode; average value interpolation and pre-value hold are performed. |

| Command bit | Processing |
|---------------|---|
| DOUT Mute = 1 | Digital Out output is muted. (DA output is not muted.) |
| DOUT Mute = 0 | If other mute conditions are not set, Digital Out is not muted. |

| Command bit | Processing |
|-----------------|--|
| DOUT ON/OFF = 1 | Digital Out is output from the DOUT pin. |
| DOUT ON/OFF = 0 | Digital Out is not output from the DOUT pin. |

| Command bit | Sync protection window width | Application |
|-------------|------------------------------|-------------------------------------|
| WSEL = 1 | ± 26 channel clock*1 | Anti-rolling is enhanced. |
| WSEL = 0 | ± 6 channel clock | Sync window protection is enhanced. |

*1 In normal-speed playback, channel clock = 4.3218MHz.

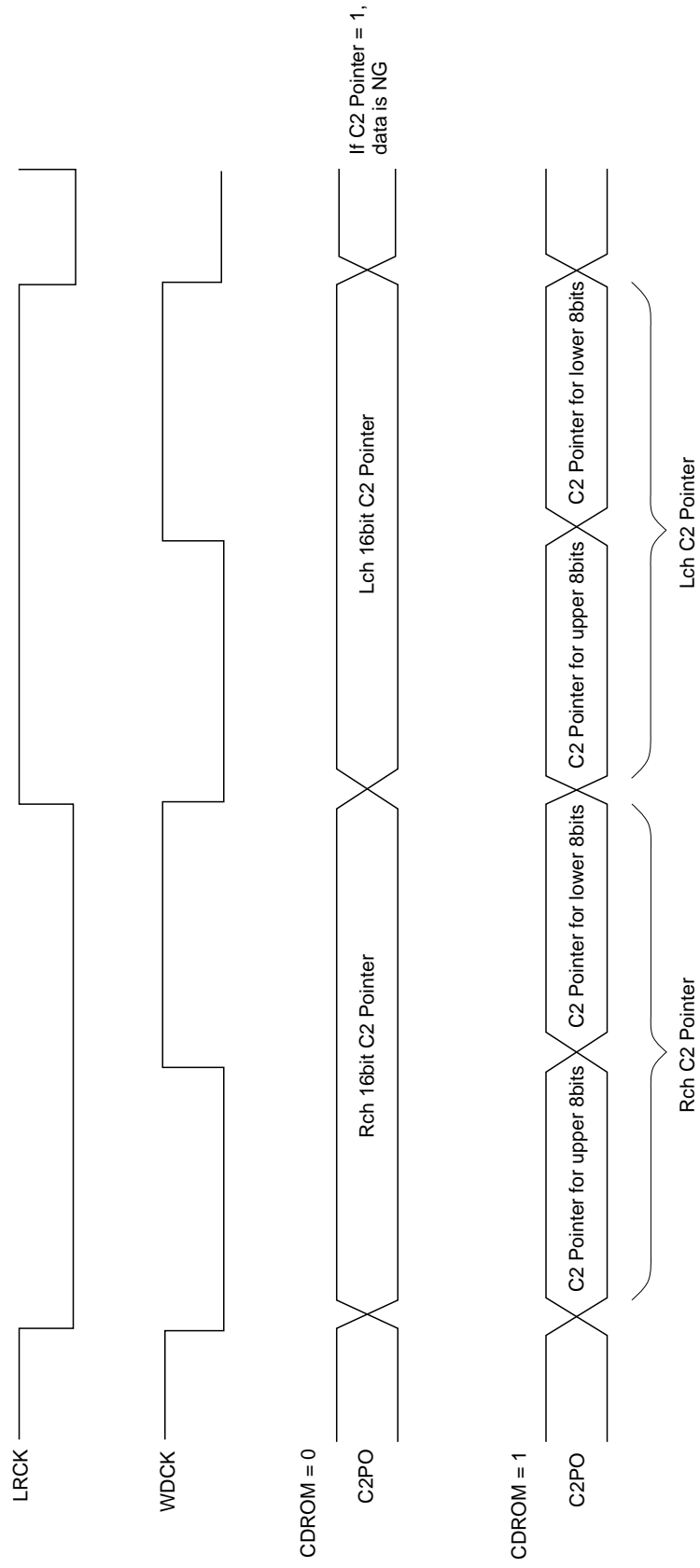
| Command bit | | | Processing |
|-------------|------|------|--|
| VCOSEL1 | KSL3 | KSL2 | |
| 0 | 0 | 0 | Multiplier PLL VCO1 is set to normal speed, and the output is 1/1 frequency-divided. |
| 0 | 0 | 1 | Multiplier PLL VCO1 is set to normal speed, and the output is 1/2 frequency-divided. |
| 0 | 1 | 0 | Multiplier PLL VCO1 is set to normal speed, and the output is 1/4 frequency-divided. |
| 0 | 1 | 1 | Multiplier PLL VCO1 is set to normal speed, and the output is 1/8 frequency-divided. |
| 1 | 0 | 0 | Multiplier PLL VCO1 is set to high speed*1, and the output is 1/1 frequency-divided. |
| 1 | 0 | 1 | Multiplier PLL VCO1 is set to high speed*1, and the output is 1/2 frequency-divided. |
| 1 | 1 | 0 | Multiplier PLL VCO1 is set to high speed*1, and the output is 1/4 frequency-divided. |
| 1 | 1 | 1 | Multiplier PLL VCO1 is set to high speed*1, and the output is 1/8 frequency-divided. |

*1 Approximately twice the normal speed

| Command bit | | | Processing |
|-------------|------|------|---|
| VCOSEL2 | KSL1 | KSL0 | |
| 0 | 0 | 0 | Wide-band PLL VCO2 is set to normal speed, and the output is 1/1 frequency-divided. |
| 0 | 0 | 1 | Wide-band PLL VCO2 is set to normal speed, and the output is 1/2 frequency-divided. |
| 0 | 1 | 0 | Wide-band PLL VCO2 is set to normal speed, and the output is 1/4 frequency-divided. |
| 0 | 1 | 1 | Wide-band PLL VCO2 is set to normal speed, and the output is 1/8 frequency-divided. |
| 1 | 0 | 0 | Wide-band PLL VCO2 is set to high speed*2, and the output is 1/1 frequency-divided. |
| 1 | 0 | 1 | Wide-band PLL VCO2 is set to high speed*2, and the output is 1/2 frequency-divided. |
| 1 | 1 | 0 | Wide-band PLL VCO2 is set to high speed*2, and the output is 1/4 frequency-divided. |
| 1 | 1 | 1 | Wide-band PLL VCO2 is set to high speed*2, and the output is 1/8 frequency-divided. |

*2 Approximately twice the normal speed

Timing Chart 2-1



\$9X commands

* Data 3 and subsequent data are DF/DAC function settings.

| Command | Data 1 | | | | Data 2 | Data 3 | | | | Data 4 | | | |
|------------------------|--------|-------------|-----|-----|------------|--------|------|--------|--------|--------|------|----|----|
| | D23 | D22 | D21 | D20 | D19 to D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| Function specification | 0 | DSPB ON/OFF | 0 | 0 | 0 0 0 0 | 0 | MCSL | CKOSL1 | CKOSL0 | ZDPL | ZMUT | — | — |

| Command bit | Processing |
|-------------|--------------------------------------|
| DSPB = 1 | Double-speed playback (CD-DSP block) |
| DSPB = 0 | Normal-speed playback (CD-DSP block) |

| Command bit | Processing |
|-------------|--|
| MCSL = 1 | DF/DAC block master clock selection. Crystal = 768Fs (33.8688MHz). |
| MCSL = 0 | DF/DAC block master clock selection. Crystal = 384Fs (16.9344MHz). |

| Command bit | | Processing |
|-------------|--------|--|
| CKOSL1 | CKOSL0 | |
| 0 | 0 | CKOUT pin output is the 1/1 frequency-divided crystal input. |
| 0 | 1 | CKOUT pin output is the 1/2 frequency-divided crystal input. |
| 1 | 0 | CKOUT pin output is the 1/4 frequency-divided crystal input. |
| 1 | 1 | CKOUT pin output is fixed low. |

| Command bit | Processing |
|-------------|---|
| ZDPL = 1 | Mute flag (LMUT2 and RMUT1 pins) polarity setting. Muted when high. |
| ZDPL = 0 | Mute flag (LMUT2 and RMUT1 pins) polarity setting. Muted when low. |

| Command bit | Processing |
|-------------|--------------------------|
| ZMUT = 1 | Zero detection mute on. |
| ZMUT = 0 | Zero detection mute off. |

\$AX commands

* Data 2 and subsequent data are DF/DAC function settings.

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | |
|------------|--------|-----|------|-----|--------|-----|------|------|--------|-----|-----|-----|
| | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 |
| Audio CTRL | 0 | 0 | Mute | ATT | 0 | 0 | OPSL | EMPH | SMUT | 0 | AD9 | AD8 |

| Data 4 | | | | Data 5 | | | | Data 6 | | | |
|--------|-----|-----|-----|--------|-----|-----|-----|--------|----|----|----|
| D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 | FMUT | 0 | 0 | 0 |

| Command bit | Processing |
|-------------|--|
| Mute = 1 | Mute on. Zero data is output from DSP. |
| Mute = 0 | Mute off. |

| Command bit | Processing |
|-------------|------------------|
| ATT = 1 | DSP output -12dB |
| ATT = 0 | Attenuation off |

| Command bit | Processing |
|-------------|--|
| OPSL = 1 | Set to 1 when changing the FMUT setting. |
| OPSL = 0 | Set to 0 when not changing the FMUT setting. |

| Command bit | Processing |
|-------------|------------------|
| EMPH = 1 | De-emphasis on. |
| EMPH = 0 | De-emphasis off. |

* If either the EMPHI pin or EMPH are high, de-emphasis is on.

| Command bit | Processing |
|-------------|----------------|
| SMUT = 1 | Soft mute on. |
| SMUT = 0 | Soft mute off. |

* If either the SYSM pin or SMUT are high, soft mute is on.

| | |
|-------------|------------------|
| Command bit | Processing |
| AD9 to 0 | Attenuation data |

The attenuation data is 10 bits, and is set as follows.

| Attenuation data | Audio output |
|------------------|--------------|
| 3FFh | 0dB |
| 3FEh | -0.0085dB |
| 3FEh | -0.017dB |
| : | |
| 001h | -60.198dB |
| 000h | -∞ |

| | |
|-------------|------------------|
| Command bit | Processing |
| FMUT = 1 | Forced mute on. |
| FMUT = 0 | Forced mute off. |

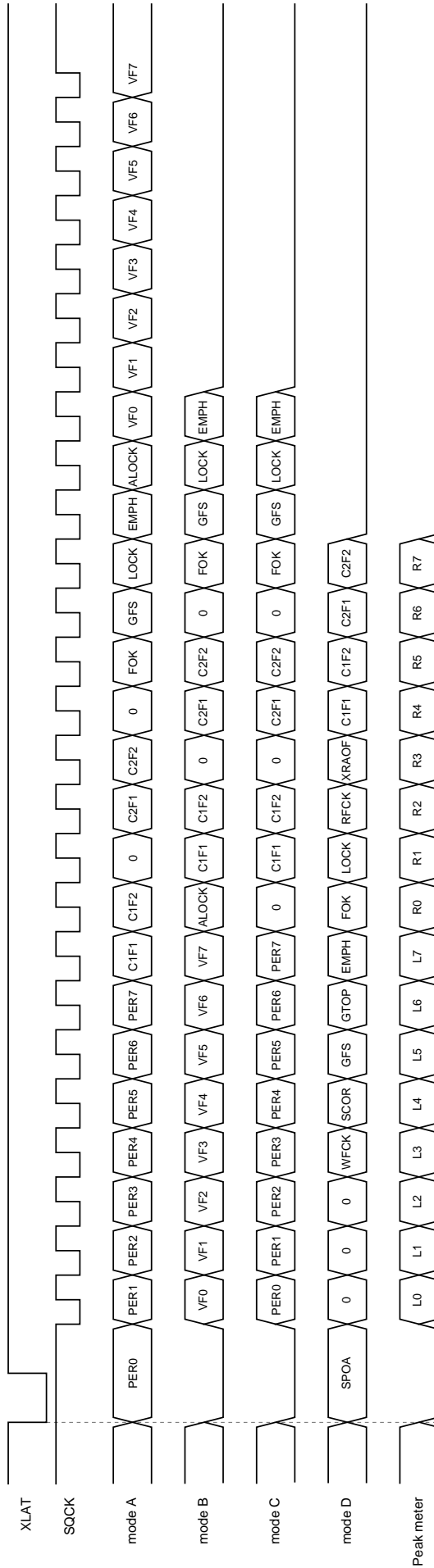
* FMUT can be set when OPSL is high.

\$BX commands

| Command | Data 1 | | | |
|-----------------|--------|-----|-------|----|
| | D3 | D2 | D1 | D0 |
| Serial bus CTRL | SL1 | SL0 | CPUSR | 0 |

| SOCT | SL1 | SL0 | mode |
|------|-----|-----|------------|
| 0 | 0 | 0 | SubQ |
| 0 | 0 | 1 | Peak meter |
| 0 | 1 | 0 | SENS |
| 0 | 1 | 1 | D |
| 1 | 0 | 0 | SubQ |
| 1 | 0 | 1 | A |
| 1 | 1 | 0 | B |
| 1 | 1 | 1 | C |

The SQSO pin output is switched to the various signals by setting the SOCT command of \$BX and the SL1 and SL0 commands of \$BX. Set SQCK to high at the fall of XLAT. Modes other than Sub Q and peak meter are loaded to the register when set at the fall of XLAT. Sub Q is loaded to the register with each SCOR, and peak meter is loaded during peak detection.



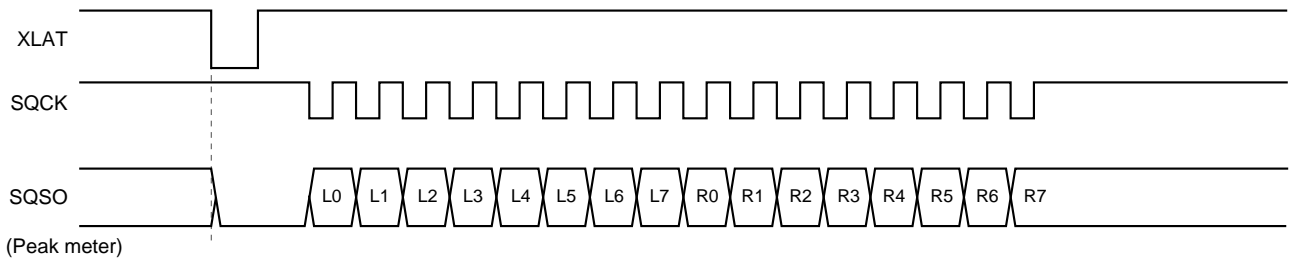
| Signal | Description |
|-----------------------|--|
| PER0 to 7 | RF jitter amount (used to adjust the focus bias). 8-bit binary data in PER0 = LSB, PER7 = MSB. |
| FOX | Focus OK |
| GFS | High when the frame sync and the insertion protection timing match. |
| LOCK | GFS is sampled at 460Hz; when GFS is high, a high signal is output. If GFS is low eight consecutive samples, a low signal is output. |
| EMPH | High when the playback disc has emphasis. |
| ALOCK | GFS is sampled at 460Hz; when GFS is high eight consecutive samples, a high signal is output. If GFS is low eight consecutive samples, a low signal is output. |
| VF0 to 7 | Used during CAV-W mode. Disc rotational speed measurement results. (See Timing Chart 2-3.) VF0 = LSB, VF7 = MSB. |
| SPOA | SPOA pin input |
| WFCK | Write frame clock output |
| SCOR | High when either subcode sync S0 or S1 is detected. |
| GTOP | High when the sync protection window is open. |
| RFCK | Read frame clock output |
| XRAOF | Low when the built-in 16K RAM exceeds the ± 4 frame jitter margin. |
| L0 to L7, R0 to R7 | Peak meter register output. Lch L0 to 7 and Rch R0 to 7 peak data. L0 and R0 are LSB. |

| C1F1 | C1F2 | C1 correction status |
|------|------|-------------------------|
| 0 | 0 | No Error |
| 1 | 0 | Single Error Correction |
| 1 | 1 | Irretrievable Error |

| C2F1 | C2F2 | C2 correction status |
|------|------|-------------------------|
| 0 | 0 | No Error |
| 1 | 0 | Single Error Correction |
| 1 | 1 | Irretrievable Error |

| Command bit | Processing |
|-------------|-------------------|
| CPUSR = 1 | XLON pin is high. |
| CPUSR = 0 | XLON pin is low. |

Peak Meter



Setting the SOCT command of \$8X to 0 and the SL1 and SL0 commands of \$BX to 0 and 1, respectively, results in peak detection mode. The SQSO output is connected to the peak register. The maximum PCM data values (absolute value, upper 8 bits) for Lch and Rch can be read from SQSO by inputting 16 clocks to SQCK. Peak detection is not performed during SQCK input, and the peak register does not change during readout. This SQCK input judgment uses a retriggerable monostable multivibrator with a time constant of 270µs to 400µs. The time during which SQCK input is high should be 270 µs or less. Also, peak detection is restarted 270µs to 400µs after SQCK input.

The peak detection register is reset with each readout (16 clocks input to SQCK). The maximum value during peak detection mode is detected and held in this status until the next readout. When switching to peak detection mode, readout should be performed one time initially to reset the peak detection register.

Peak detection can also be performed for previous value hold and average value interpolation data.

\$CX commands

| Command | D23 | D22 | D21 | D20 |
|---------------------------|-----------|-----------|-----------|-----------|
| Servo coefficient setting | Gain MDP1 | Gain MDP0 | Gain MDS1 | Gain MDS0 |
| CLV CTRL (\$DX) | | | | Gain CLVS |

• CLV mode gain setting: GCLVS

| Gain MDS1 | Gain MDS0 | Gain CLVS | GCLVS |
|-----------|-----------|-----------|-------|
| 0 | 0 | 0 | -12dB |
| 0 | 0 | 1 | -6dB |
| 0 | 1 | 0 | -6dB |
| 0 | 1 | 1 | 0dB |
| 1 | 0 | 0 | 0dB |
| 1 | 0 | 1 | +6dB |

• CLVP mode gain setting: GMDP, GMDS

| Gain MDP1 | Gain MDP0 | GMDP |
|-----------|-----------|------|
| 0 | 0 | -6dB |
| 0 | 1 | 0dB |
| 1 | 0 | +6dB |

| Gain MDS1 | Gain MDS0 | GMDS |
|-----------|-----------|------|
| 0 | 0 | -6dB |
| 0 | 1 | 0dB |
| 1 | 0 | +6dB |

\$DX commands

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | |
|----------|----------------|-----|-----|--------------|--------|-----|-----|-----|--------|-----|-----|-----|
| | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 |
| CLV CTRL | DCLV PWM MD | TB | TP | Gain CLVS | VP7 | VP6 | VP5 | VP4 | VP3 | VP2 | VP1 | VP0 |

See "\$CX Commands".

| Command bit | Description |
|-----------------|---|
| DCLV PWM MD = 1 | Digital CLV PWM mode specified. Both MDS and MDP are used. CLV-W and CAV-W modes can not be used. |
| DCLV PWM MD = 0 | Digital CLV PWM mode specified. Ternary MDP values are output. CLV-W and CAV-W modes can be used. |

| Command bit | Description |
|-------------|---|
| TB = 0 | Bottom hold at a cycle of RFCK/32 in CLVS mode. |
| TB = 1 | Bottom hold at a cycle of RFCK/16 in CLVS mode. |
| TP = 0 | Peak hold at a cycle of RFCK/4 in CLVS mode. |
| TP = 1 | Peak hold at a cycle of RFCK/2 in CLVS mode. |

| Command bit | Description |
|-------------------|---------------------------------------|
| VP0 to 7 = F0 (H) | Playback at half (normal) speed to |
| : | |
| VP0 to 7 = E0 (H) | Playback at normal (double) speed |

The rotational velocity R of the spindle can be expressed with the following equation.

$$R = \frac{256 - n}{32}$$

R: Relative velocity at normal speed = 1
n: VP0 to 7 setting value

Notes)

- 1) Values in parentheses are for when DSPB is 1.
- 2) Values when the crystal is 16.9344MHz and XTSL is low or when the crystal is 33.8688MHz and XTSL is high.
- 3) The VP0 to 7 setting values are valid in CAV-W mode.

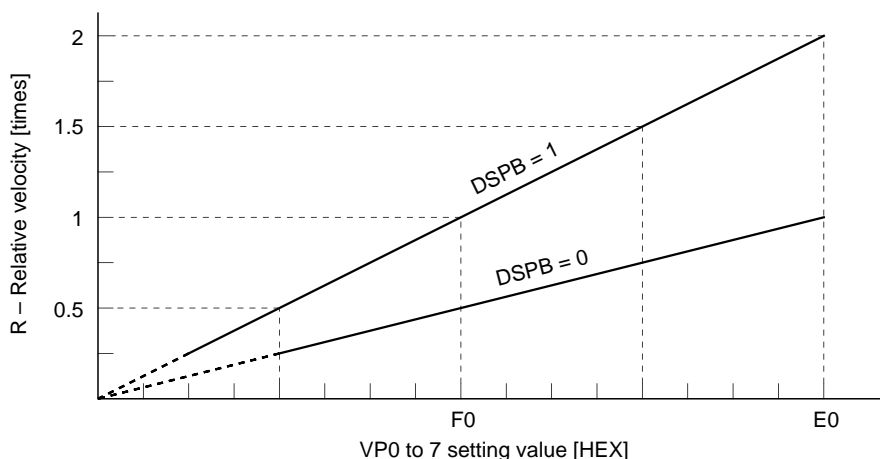


Fig. 2-1.

\$EX commands

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | |
|----------|--------|-----|-----|-----|--------|------|------|------|--------|------|------|------|
| | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 |
| CLV mode | CM3 | CM2 | CM1 | CM0 | EPWM | SPDC | ICAP | SFSL | VC2C | HIFC | LPWR | VPON |

| Command bit | | | | Mode | Description |
|-------------|-----|-----|-----|-------|---|
| CM3 | CM2 | CM1 | CM0 | | |
| 0 | 0 | 0 | 0 | STOP | Spindle stop mode. *1 |
| 1 | 0 | 0 | 0 | KICK | Spindle forward rotation mode. *1 |
| 1 | 0 | 1 | 0 | BRAKE | Spindle reverse rotation mode. Valid only when LPWR = 0 in any modes. *1 |
| 1 | 1 | 1 | 0 | CLVS | Rough servo mode. When the RF-PLL circuit isn't locked, this mode is used to pull the disc rotations within the RF-PLL capture range. |
| 1 | 1 | 1 | 1 | CLVP | PLL servo mode. |
| 0 | 1 | 1 | 0 | CLVA | Automatic CLVS/CLVP switching mode. Used for normal playback. |

*1 See Timing Charts 1-6 to 1-12.

| Command bit | | | | | | | | Mode | Description |
|-------------|------|------|------|------|------|------|------|-------|--|
| EPWM | SPDC | ICAP | SFSL | VC2C | HIFC | LPWR | VPON | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CLV-N | Crystal reference CLV servo. |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | CLV-W | Used for playback in CLV-W mode. *2 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | CAV-W | Spindle control with VP0 to 7. |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | CAV-W | Spindle control with the external PWM. |

*2 Figs. 3-1 and 3-2 show the control flow with the microcomputer software in CLV-W mode.

| Command | Data 4 | | | |
|----------|-----------|-----------|------|----|
| | D11 | D10 | D9 | D8 |
| SPD mode | Gain CAV1 | Gain CAV0 | FCSW | 0 |

| Gain CAV1 | Gain CAV0 | Gain |
|-----------|-----------|-------|
| 0 | 0 | 0dB |
| 0 | 1 | -6dB |
| 1 | 0 | -12dB |
| 1 | 1 | -18dB |

- This sets the gain when controlling the spindle with the phase comparator in CAV-W mode.

| Command bit | Processing |
|-------------|--|
| FCSW = 0 | The VPCO2 pin is not used and it is Hi-Z. |
| FCSW = 1 | The VPCO2 pin is used and the pin signal is the same as VPCO1. |

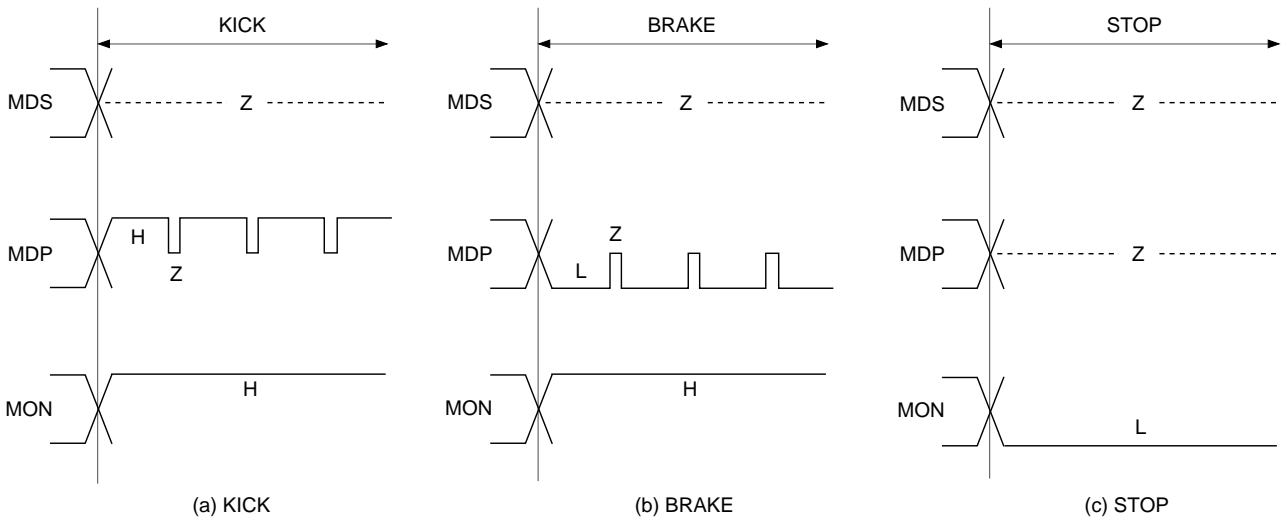
| Mode | DCLV PWM MD | LPWR | Command | Timing chart |
|-------|----------------|------|---------|--------------|
| CLV-N | 0 | 0 | KICK | 2-2 (a) |
| | | | BRAKE | 2-2 (b) |
| | | | STOP | 2-2 (c) |
| | 1 | 0 | KICK | 2-3 (a) |
| | | | BRAKE | 2-3 (b) |
| | | | STOP | 2-3 (c) |
| CLV-W | 0 | 0 | KICK | 2-4 (a) |
| | | | BRAKE | 2-4 (b) |
| | | | STOP | 2-4 (c) |
| | | 1 | KICK | 2-5 (a) |
| | | | BRAKE | 2-5 (b) |
| | | | STOP | 2-5 (c) |
| CAV-W | 0 | 0 | KICK | 2-6 (a) |
| | | | BRAKE | 2-6 (b) |
| | | | STOP | 2-6 (c) |
| | | 1 | KICK | 2-7 (a) |
| | | | BRAKE | 2-7 (b) |
| | | | STOP | 2-7 (c) |

| Mode | DCLV PWM MD | LPWR | Timing chart |
|-------|----------------|------|-----------------|
| CLV-N | 0 | 0 | 2-8 |
| | 1 | 0 | 2-9 |
| CLV-W | 0 | 0 | 2-10 |
| | | 1 | 2-11 |
| CAV-W | 0 | 0 | 2-12 (EPWM = 0) |
| | | 1 | 2-13 (EPWM = 0) |
| | | 0 | 2-14 (EPWM = 1) |
| | | 1 | 2-15 (EPWM = 1) |

Note) CLV-W and CAV-W modes support control only by the ternary output of the MDP pin.
Therefore, set DCLV PWM MD to 0 in CLV-W and CAV-W modes.

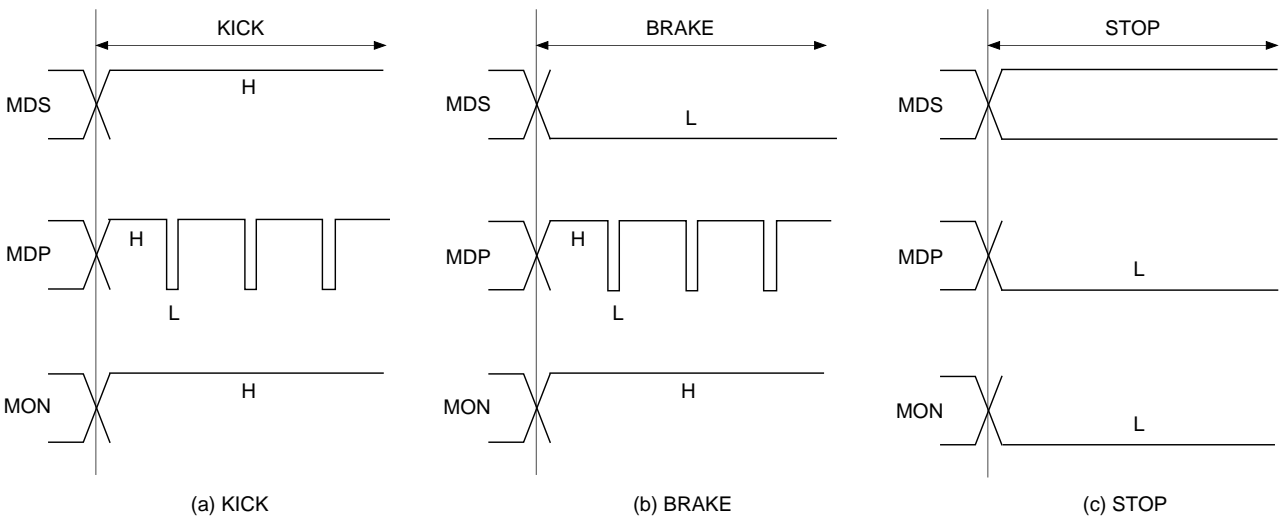
Timing Chart 2-2

CLV-N mode DCLV PWM MD = LPWR = 0



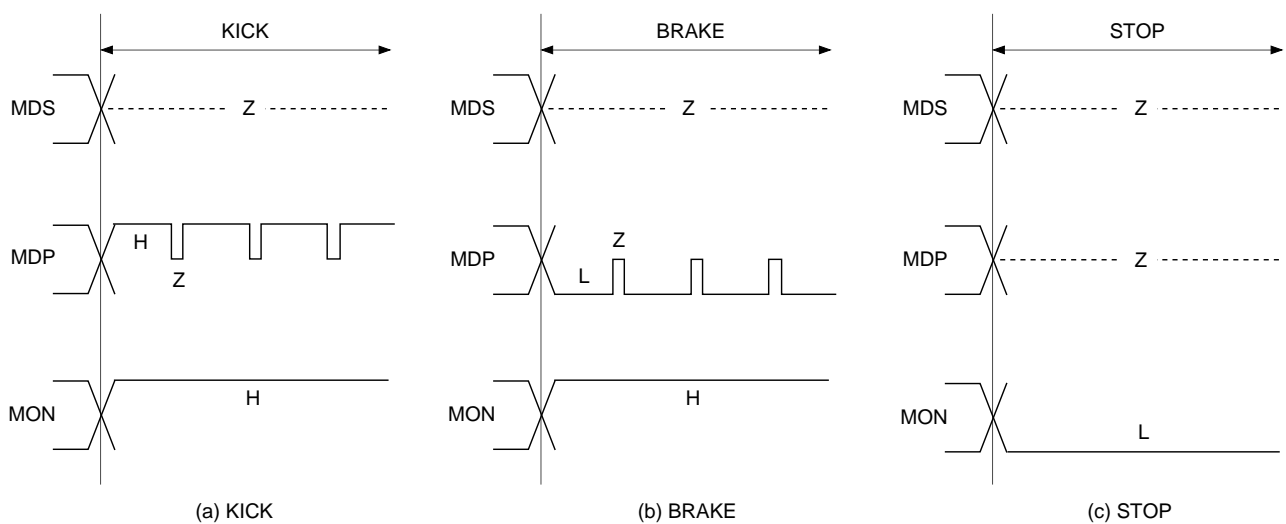
Timing Chart 2-3

CLV-N mode DCLV PWM MD = 1, LPWR = 0



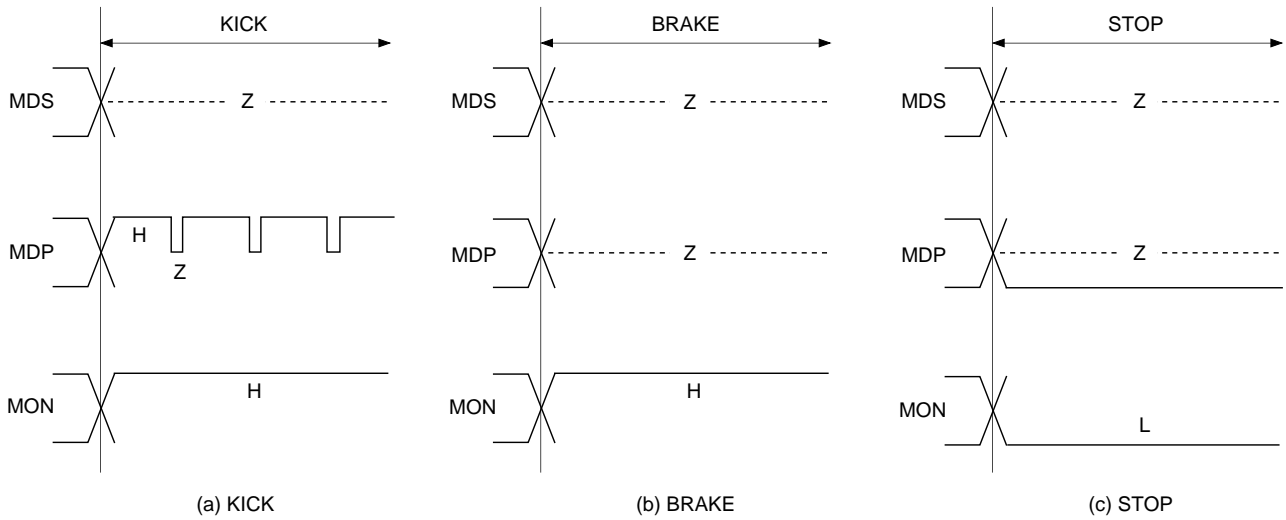
Timing Chart 2-4

CLV-W mode (when following the spindle rotational velocity) DCLV PWM MD = LPWR = 0



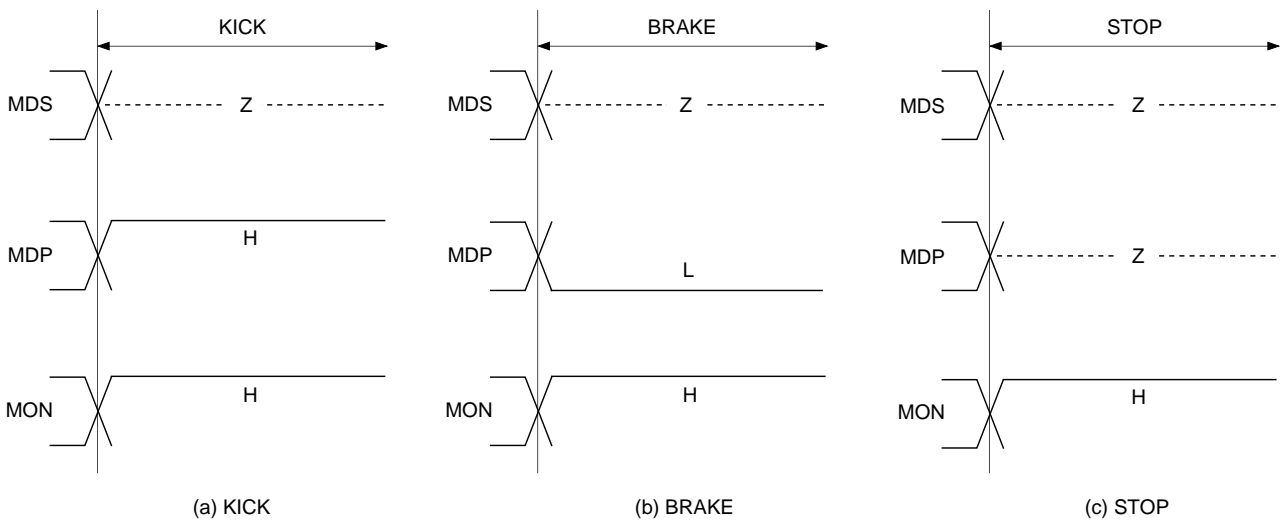
Timing Chart 2-5

CLV-W mode (when following the spindle rotational velocity) DCLV PWM MD = 0, LPWR = 1



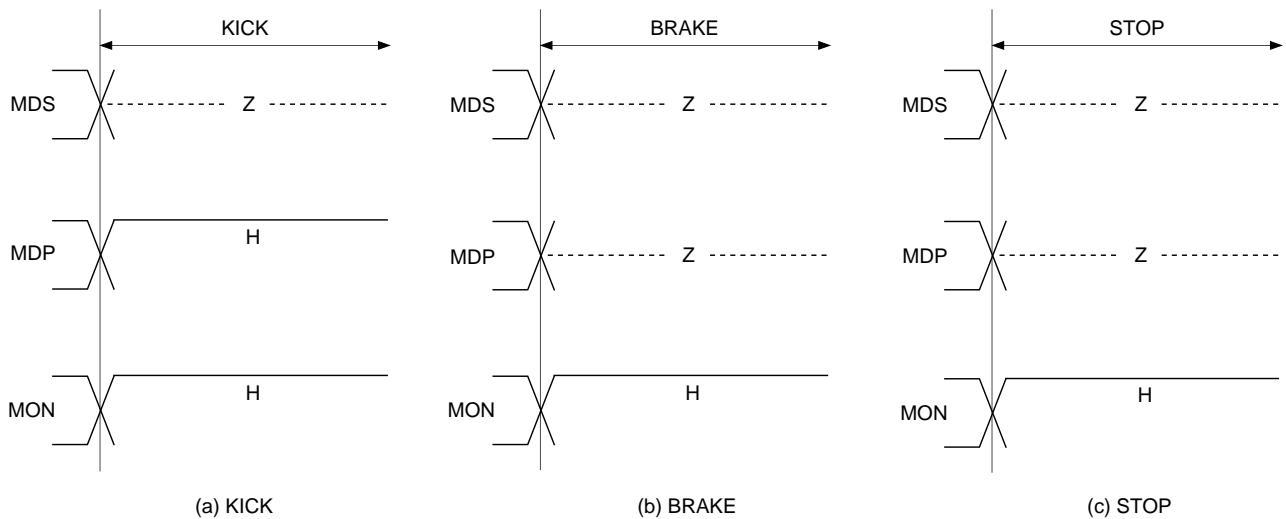
Timing Chart 2-6

CAV-W mode DCLV PWM MD = LPWR = 0



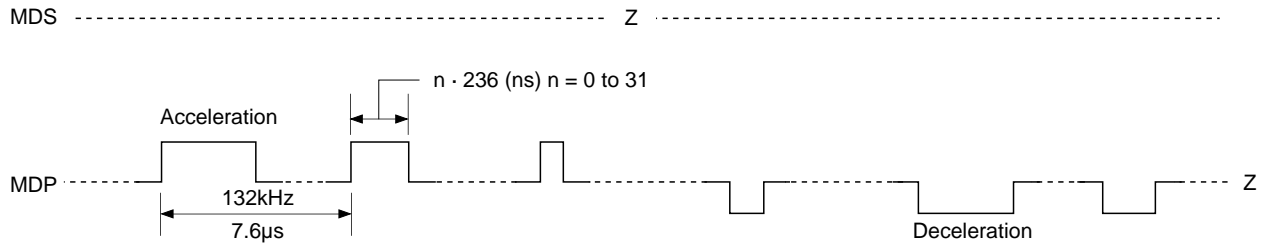
Timing Chart 2-7

CAV-W mode DCLV PWM MD = 0, LPWR = 1



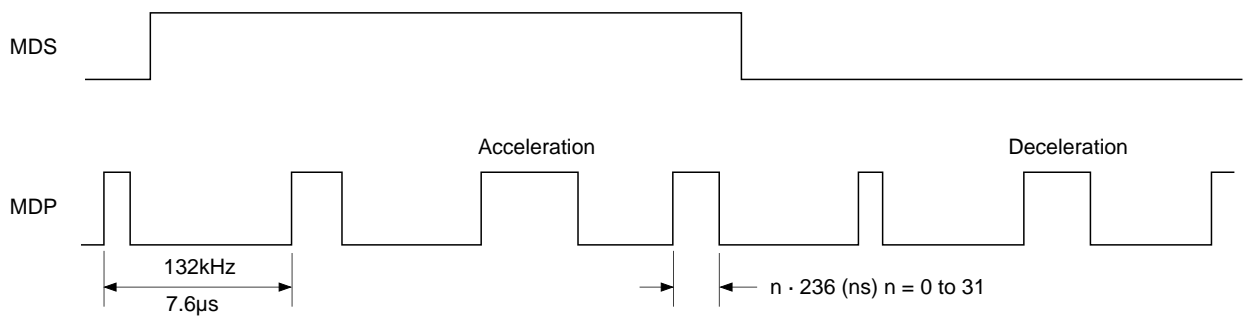
Timing Chart 2-8

CLV-N mode DCLV PWM MD = LPWR = 0



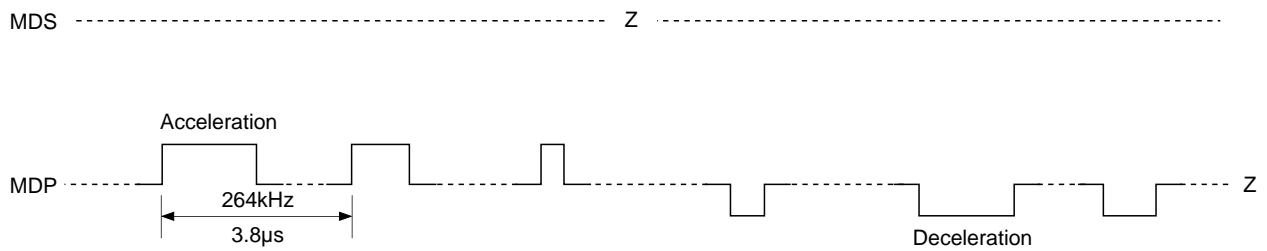
Timing Chart 2-9

CLV-N mode DCLV PWM MD = 1, LPWR = 0



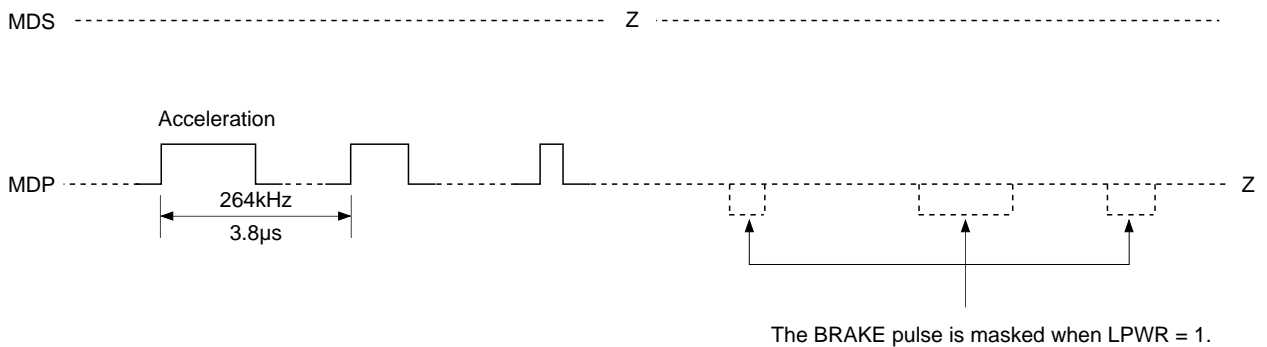
Timing Chart 2-10

CLV-W mode DCLV PWM MD = LPWR = 0



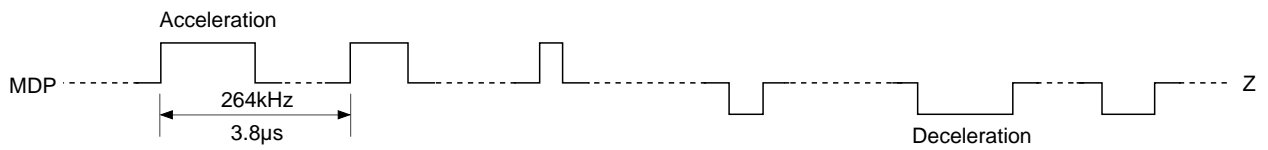
Timing Chart 2-11

CLV-W mode DCLV PWM MD = 0, LPWR = 1



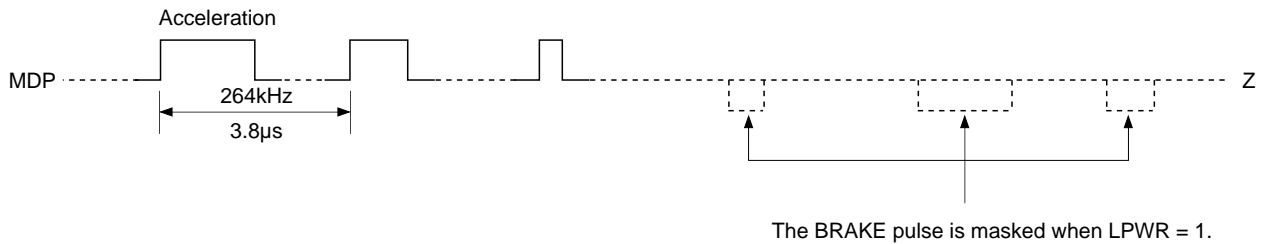
Timing Chart 2-12

CAV-W mode EPWM = DCLV PWM MD = LPWR = 0



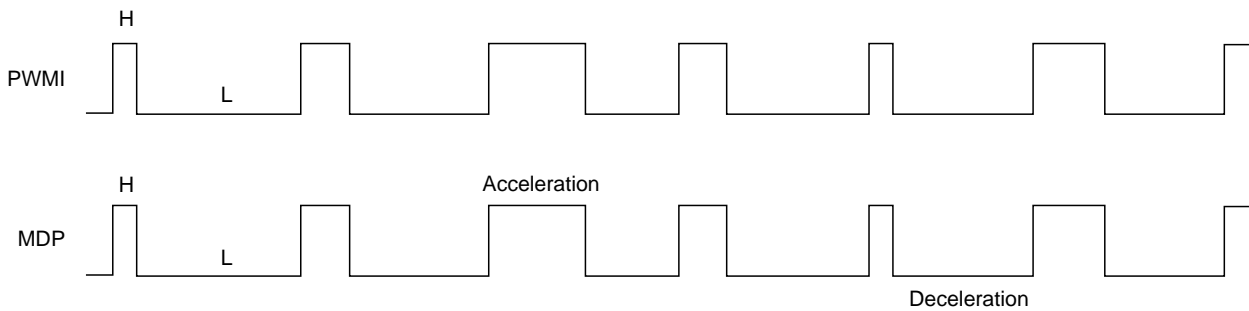
Timing Chart 2-13

CAV-W mode EPWM = 1, DCLV PWM MD = 0, LPWR = 1



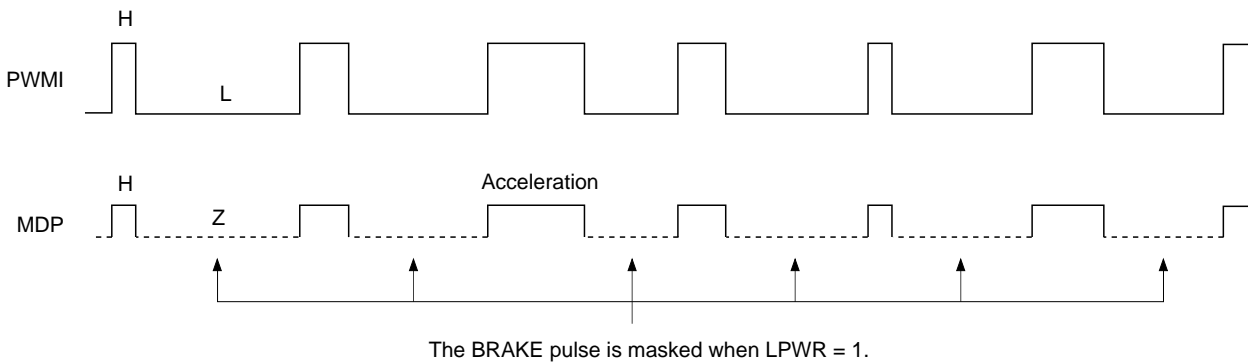
Timing Chart 2-14

CAV-W mode EPWM = 1, DCLV PWM MD = LPWR = 0



Timing Chart 2-15

CAV-W mode EPWM = 1, DCLV PWM MD = 0, LPWR = 1



Note) CLV-W and CAV-W modes support control only by the ternary output of the MDP pin. Therefore, set DCLV PWM MD to 0 in CLV-W and CAV-W modes.

2-2. Subcode Interface

There are two methods for reading out a subcode externally.

The 8-bit subcodes P to W can be read out from SBSO by inputting EXCK to the CXD2548R.

Sub Q can be read out after checking CRC of the 80 bits in the subcode frame.

Sub Q can be read out from the SQSO pin by inputting 80 clock pulses to the SQCK pin when SCOR comes correctly and CRCF is high.

P to W Subcode Readout

Data can be read out by inputting EXCK immediately after WFCK falls. (See Timing Chart 2-16.)

80-bit Sub Q Readout

Fig. 2-2 shows the peripheral block of the 80-bit Sub Q register.

- First, Sub Q, regenerated at one bit per frame, is input to the 80-bit serial/parallel register and the CRC check circuit.

- 96-bit Sub Q is input, and if the CRC is OK, it is output to SQSO with CRCF = 1. In addition, 80 bits are loaded into the parallel/serial register.

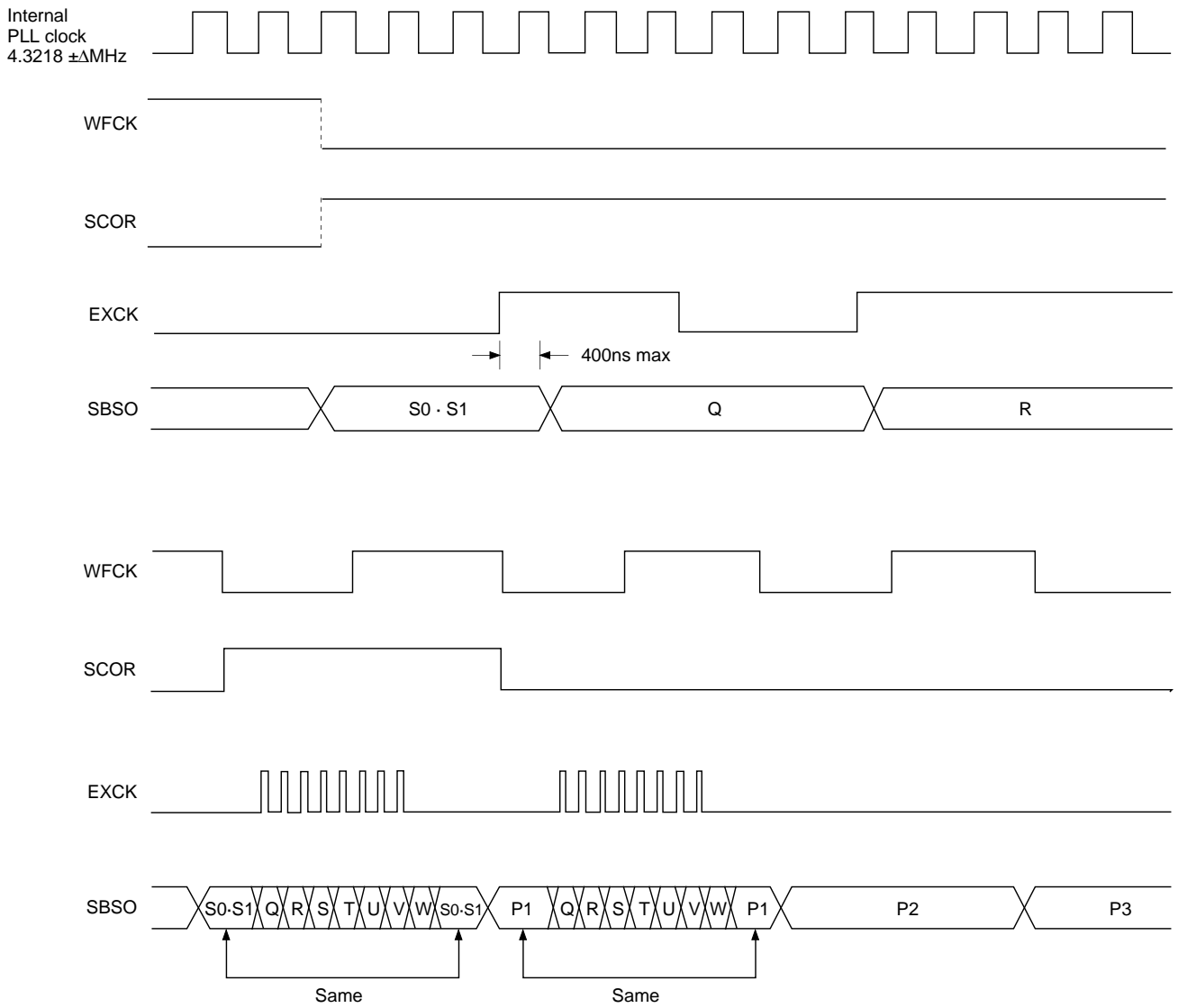
When SQSO goes high 400 μ s (monostable multivibrator time constant) or more after subcode readout, the CPU determines that new data (which passed the CRC check) has been loaded.

- When the 80-bit data is loaded, the order of the MSB and LSB is inverted within each byte. As a result, although the sequence of the bytes is the same, the bits within the bytes are now ordered LSB first.
- Once the 80-bit data load is confirmed, SQCK is input so that the data can be read.

The SQCK input is detected, and the retriggerable monostable multivibrator is reset while the input is low.

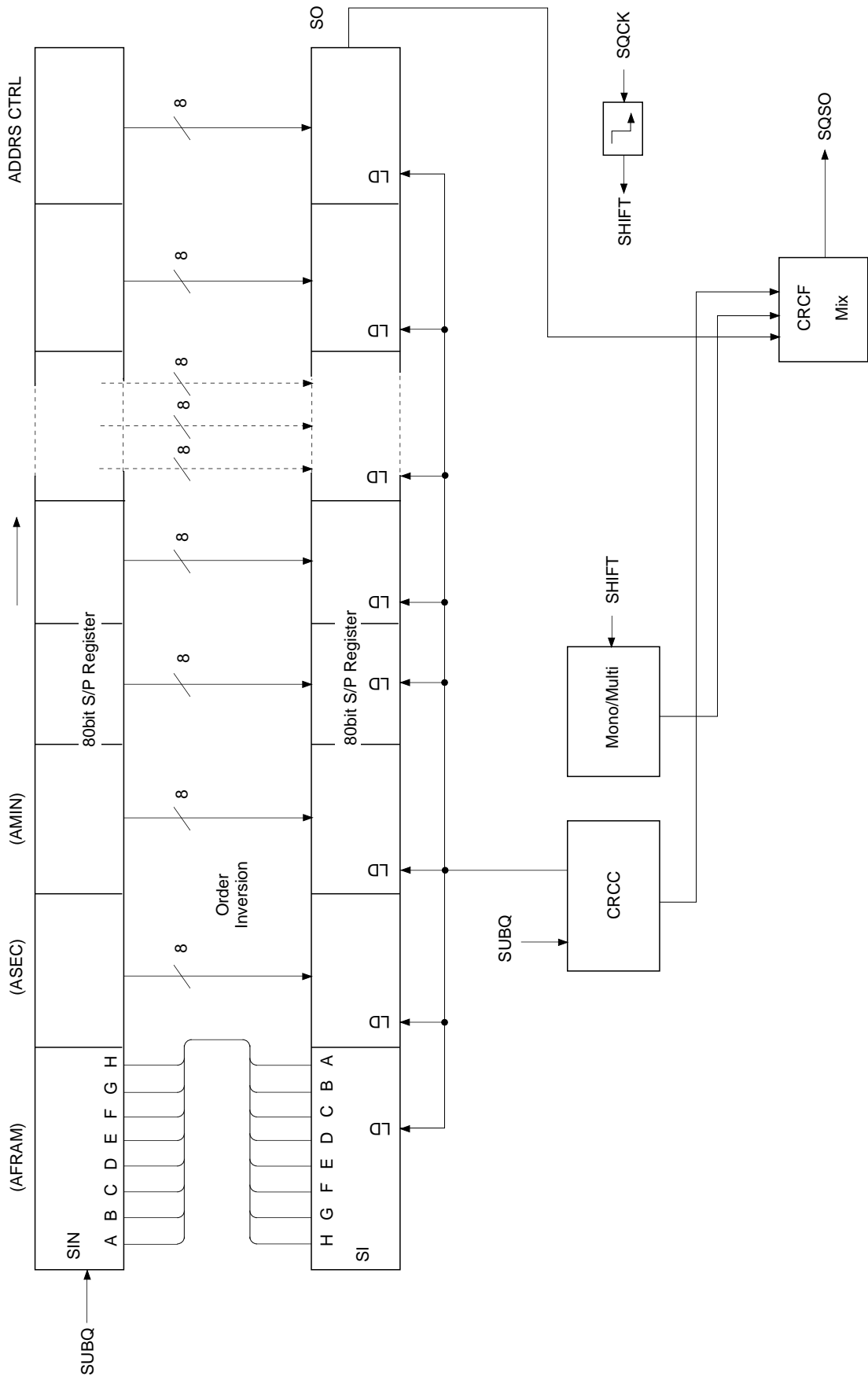
- The retriggerable monostable multivibrator has a time constant from 270 to 400 μ s. When the duration when SQCK is high is less than this time constant, the monostable multivibrator is kept reset; during this interval, the serial/parallel register is not loaded into the parallel/serial register.
- While the monostable multivibrator is being reset, data cannot be loaded in the 80-bit parallel/serial register. In other words, while reading out with a clock cycle shorter than this time constant, the register will not be rewritten by CRCOK and others.
- See Timing Chart 2-17.
- The high and low intervals for SQCK should be between 750ns and 120 μ s.

Timing Chart 2-16

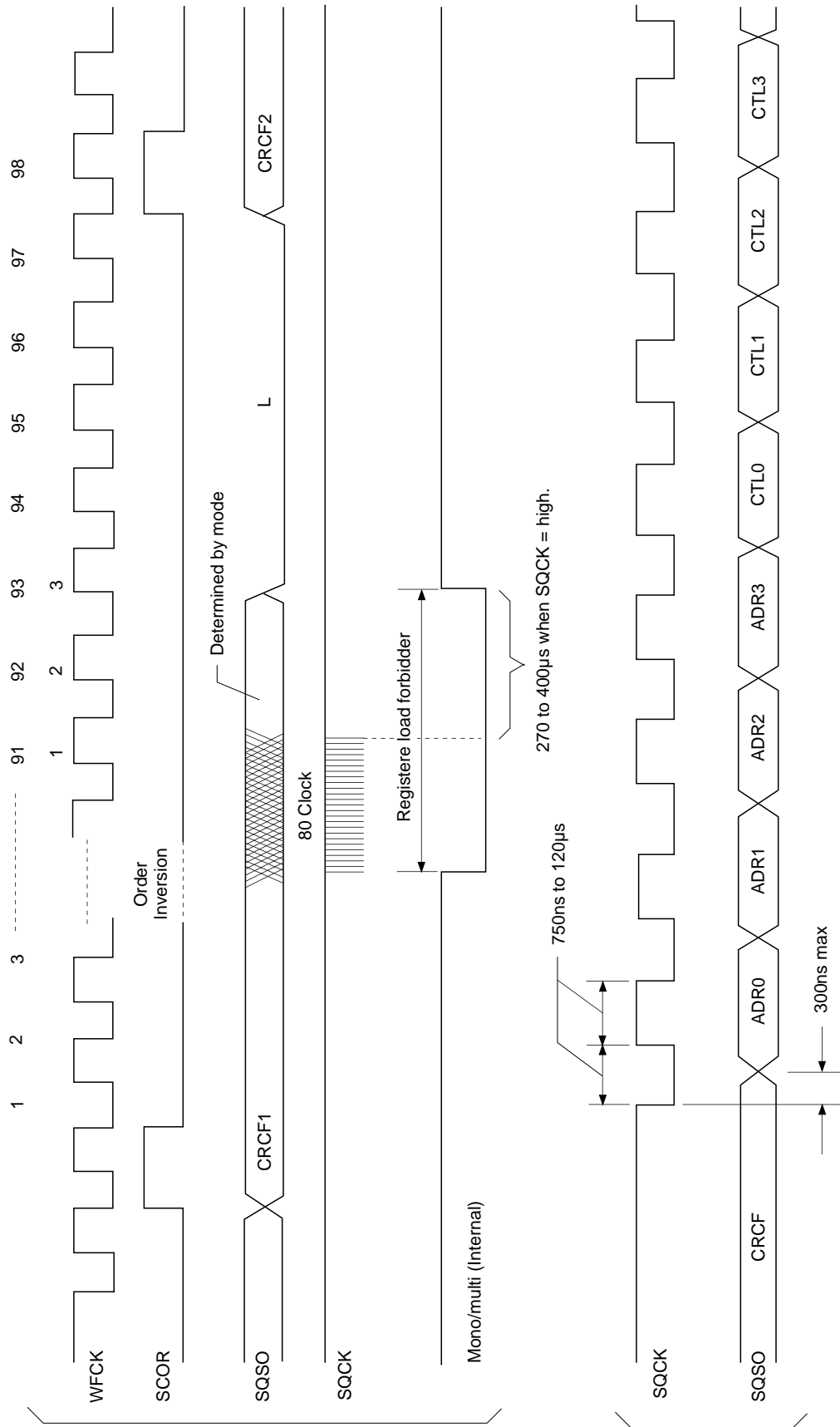


Sub Code P.Q.R.S.T.U.V.W Read Timing

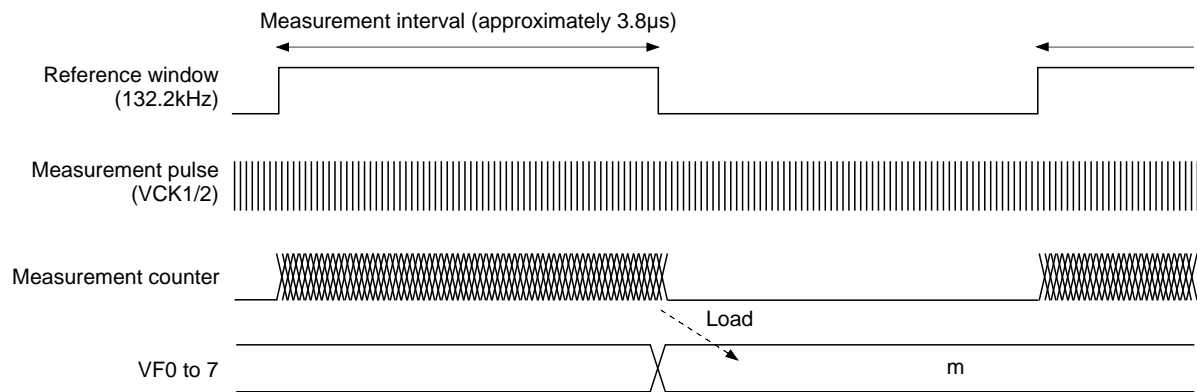
Fig. 2-2 Block Diagram



Timing Chart 2-17



Timing Chart 2-18



The relative velocity of the disc can be obtained with the following equation.

$$R = \frac{m + 1}{32} \text{ (R: Relative velocity, m: Measurement results)}$$

VF0 to 7 is the result obtained by counting VCKI/2 pulses while the reference signal (132.2kHz) generated from the crystal (384Fs) is high. This count is 31 when the disc is rotating at normal speed and 63 when it is rotating at double speed (when DSPB is low).

[3] Description of Other CD Signal Processing and DAC System Functions

3-1. Description of DSP Operating Modes

This LSI has three basic operating modes using a combination of spindle control and the PLL. The operations for each mode are described below.

(a) CLV-N Mode

This mode is compatible with the CXD2507AQ, and operation is the same as for the conventional control. The PLL capture range is $\pm 150\text{kHz}$.

(b) CLV-W Mode

This is the wide capture range mode. This mode allows PLL to follow the rotational velocity of the disc. This rotational following control has two types: using the built-in VCO2 or providing an external VCO. The spindle is the same CLV servo as for the conventional series. Operation using the built-in VCO2 is described below. (When using an external VCO, input the signal from the VPCO1 pin to the low-pass filter, use the output from the low-pass filter as the control voltage for the external VCO, and input the oscillation from the VCO to the VCKI pin.) While starting to rotate a disc and/or speeding up to the lock range from the condition that a disc stops, CAV-W mode should be used. Concretely saying, firstly send $\$E665$ to set CAV-W mode and kick a disc, secondly send $\$E60C$ to set CLV-W mode if ALOCK is high, which can be read out serially from the SQSO pin. CLV-W mode can be used while ALOCK is high. The microcomputer monitors the serial data output, and must return the operation to the speed adjusting state (CAV-W mode) when ALOCK becomes low. The control flow according to the microcomputer software in CLV-W mode is shown in Fig. 3-2.

In CLV-W mode (normal), low power consumption is achieved by setting LPWR to high. Control was formerly performed by applying acceleration and deceleration pulses to the spindle motor. However, when LPWR is set to high, deceleration pulses are not output, thereby achieving low power consumption mode.

CLV-W mode supports control only by the ternary output of the MDP pin. Therefore, when using CLV-W mode, set DCLV PWM MD to low.

Note) The capture range for this mode is theoretically up to the signal processing limit.

(c) CAV-W Mode

This is CAV mode. In this mode the external clock is fixed and it is possible to control spindle to variable rotational velocity. The rotational velocity is determined by the VP0 to 7 setting values or the external PWM. When controlling the spindle with VP0 to 7, setting CAV-W mode with $\$E665$ command and controlling VP0 to 7 with the $\$DX$ commands allows the rotational velocity to be varied from low speed to double speed. (See " $\$DX$ Commands".) Also, when controlling the spindle with the external PWM, the PWMI pin is binary input which becomes KICK during high intervals and BRAKE during low intervals.

The microcomputer can know the rotational velocity using V16M. And the reference for the velocity measurement is a signal of 132.3kHz obtained by 1/128 of the crystal (384 Fs). The velocity is obtained by counting V16M/2 pulses while the reference is high, and the result is output from the new CPU interface as 8 bits (VP0 to 7). These measurement results are 31 when the disc is rotating at normal speed or 63 when it is rotating at double speed. These values match those of the 256 - n for control with VP0 to 7.

In CAV-W mode, the spindle is set to the desired rotational velocity and the operation speed for the entire system follows this rotational velocity. Therefore, the cycles for the Fs system clock, PCM data and all other output signals from this LSI change according to the rotational velocity of the disc (excluding the servo output block).

Note) The capture range for this mode is theoretically up to the signal processing limit.

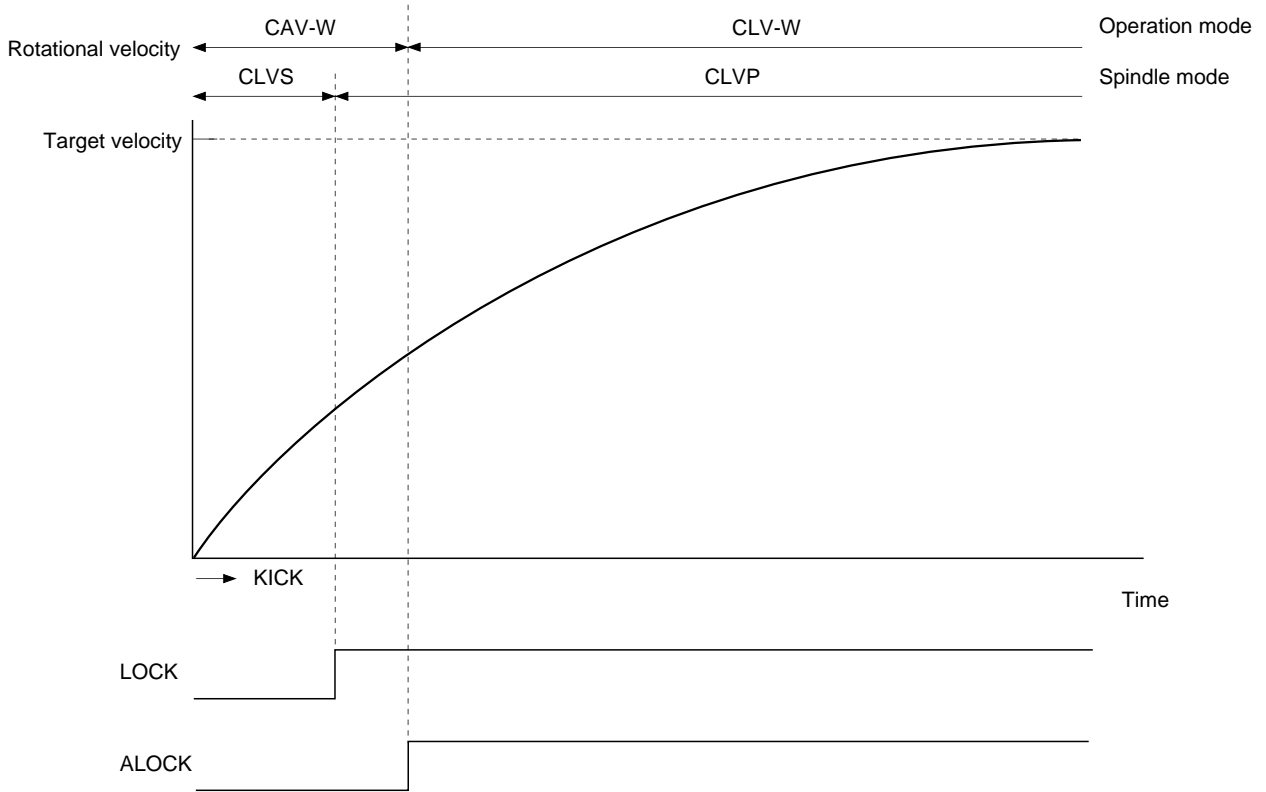


Fig. 3-1. Disc Stop to Regular Playback in CLV-W Mode

CLV-W Mode

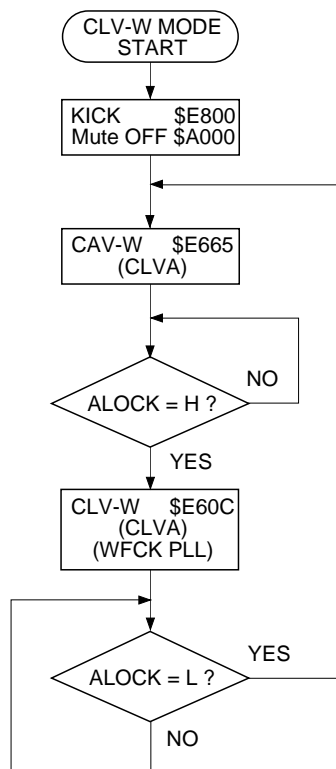


Fig. 3-2. CLV-W Mode Flow Chart

3-2. Frame Sync Protection

- In normal-speed playback, a frame sync is recorded approximately every 136 μ s (7.35kHz). This signal is used as a reference to recognize the data within a frame. Conversely, if the frame sync cannot be recognized, the data is processed as error data because the data cannot be recognized. As a result, recognizing the frame sync properly is extremely important for improving playability.
- In the CXD2548R, window protection and forward protection/backward protection have been adopted for frame sync protection. These functions achieve very powerful frame sync protection. There are two window widths: one for cases where a rotational disturbance affects the player and the other for cases where there is no rotational disturbance (WSEL = 0/1). In addition, the forward protection counter is fixed to 13, and the backward protection counter to 3. Concretely, when the frame sync is being played back normally and then cannot be detected due to scratches, a maximum of 13 frames are inserted. If frame sync cannot be detected for 13 frames or more, the window opens to resynchronize the frame sync. In addition, immediately after the window opens and the resynchronization is executed, if a proper frame sync cannot be detected within 3 frames, the window opens immediately.

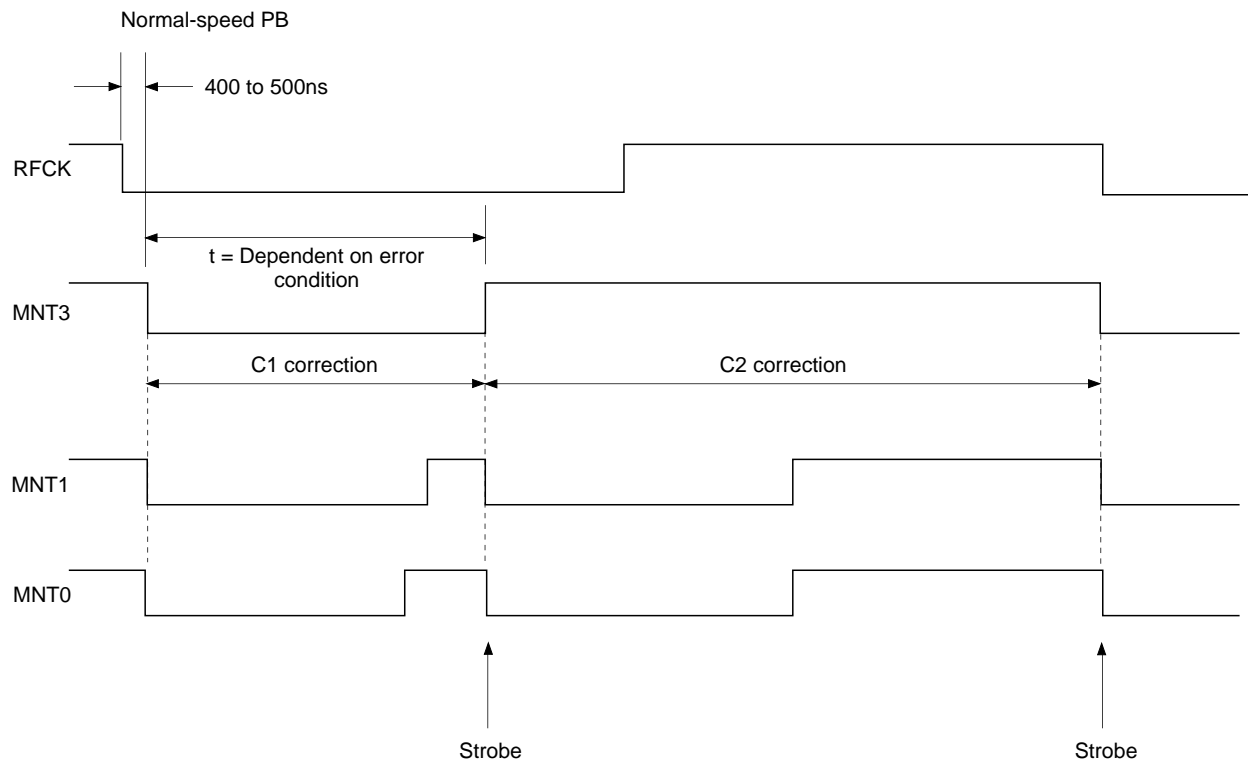
3-3. Error Correction

- In the CD format, one 8-bit data contains two error correction codes, C1 and C2. For C1 correction, the code is created with 28-byte information and 4-byte C1 parity. For C2 correction, the code is created with 24-byte information and 4-byte C2 parity. Both C1 and C2 are Reed Solomon codes with a minimum distance of 5.
- The CXD2548R's SEC strategy uses powerful frame sync protection and C1 and C2 error correction to achieve high playability.
- The correction status can be monitored externally. See Table 3-1.
- When the C2 pointer is high, the data in question was uncorrectable. Either the pre-value was held or an average value interpolation was made for the data.

| MNT3 | MNT1 | MNT0 | Description |
|------|------|------|--------------------------|
| 0 | 0 | 0 | No C1 errors |
| 0 | 0 | 1 | One C1 error corrected |
| 0 | 1 | 1 | C1 correction impossible |
| 1 | 0 | 0 | No C2 errors |
| 1 | 0 | 1 | One C2 error corrected |
| 1 | 1 | 1 | C2 correction impossible |

Table 3-1.

Timing Chart 3-1

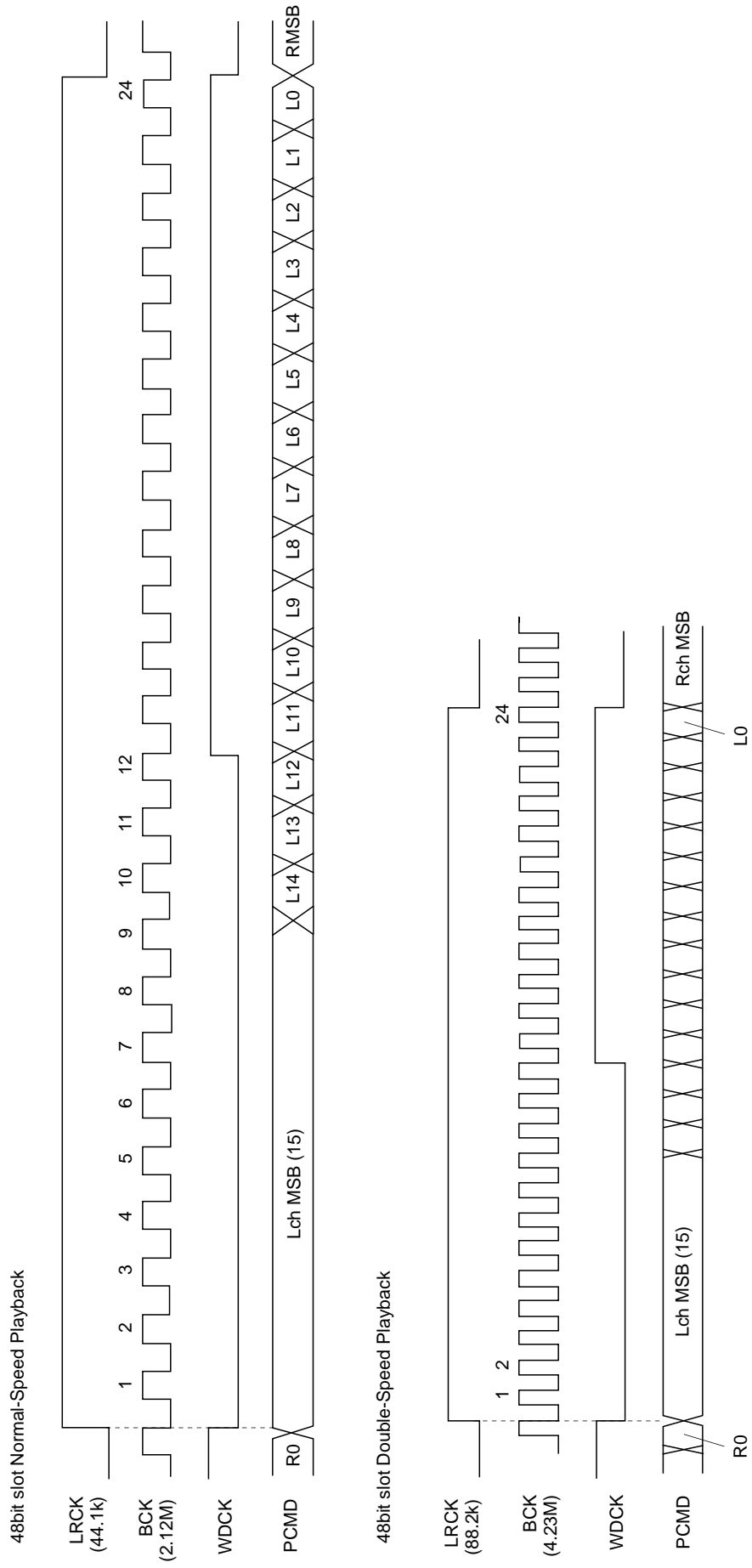


3-4. DA Interface

- The CXD2548R's DA interface is as follows.

This interface includes 48 cycles of the bit clock within one LRCK cycle, and is MSB first. When LRCK is high, the data is for the left channel.

Timing Chart 3-2



4-5. Digital Out

There are three Digital Out: the type 1 format for broadcasting stations, the type 2 form 1 format for home use, and the type 2 form 2 format for the manufacture of software.

The CXD2548R supports type 2 form 1.

Sub Q data which are matched twice in succession after a CRC check are input to the first four bits (bits 0 to 3) of the channel status.

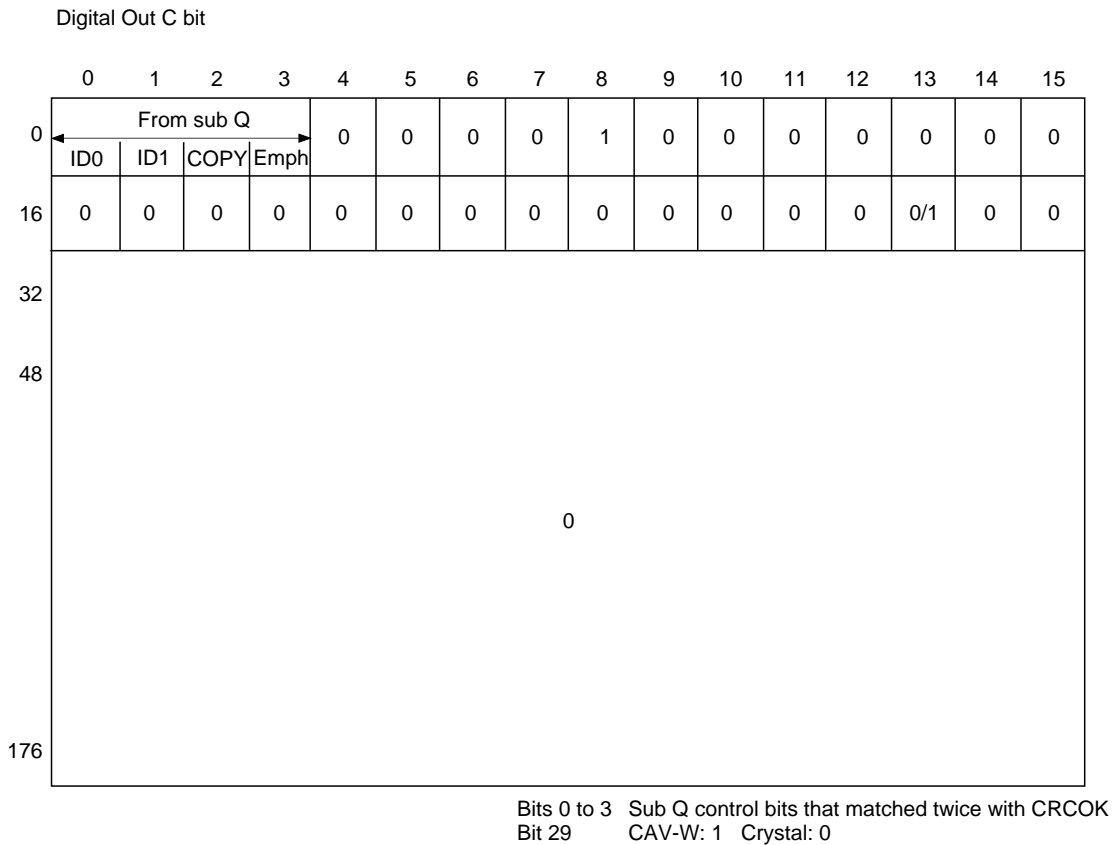


Table 3-2.

3-6. Servo Auto Sequence

This function performs a series of controls, including auto focus and track jumps. When the auto sequence command is received from the CPU, auto focus, 1-track jump, 2N-track jump and N-track move are executed automatically.

Servo is used in an exclusive manner during the auto sequence execution (when XBUSY = low), so that commands from the CPU are not transferred to the servo, but can be sent to the CXD2548R.

Connect the CPU and RF as shown in Fig. 3-3.

When CLOK goes from low to high while XBUSY is low, XBUSY does not become high for a maximum of 100µs after that point. This is to prevent the transfer of erroneous data to the servo when XBUSY changes from low to high by the monostable multivibrator, which is reset by CLOK being low (when XBUSY is low).

(a) Auto focus (\$47)

Focus search-up is performed, FOK and FZC are checked, and the focus servo is turned on.

If \$47 is received from the CPU, the focus servo is turned on according to Fig. 3-4. The auto focus starts with focus search-up, and note that the pickup should be lowered beforehand (focus search down). In addition, blind E of register 5 is used to eliminate FZC chattering. Concretely, the focus servo is turned on at the falling edge of FZC after FZC has been continuously high for a longer time than E.

CXD2548R connection diagram when using auto sequence (example)

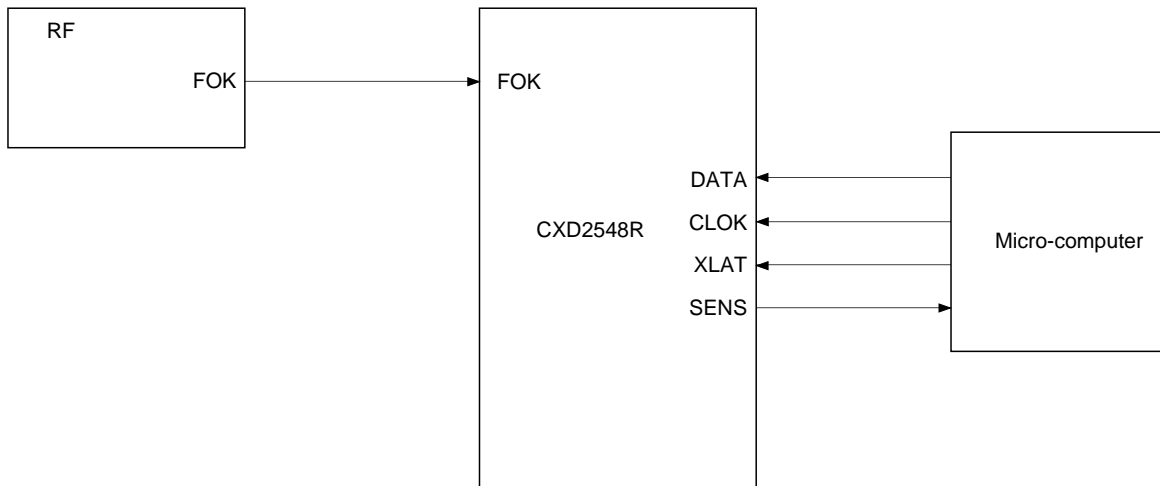


Fig. 3-3

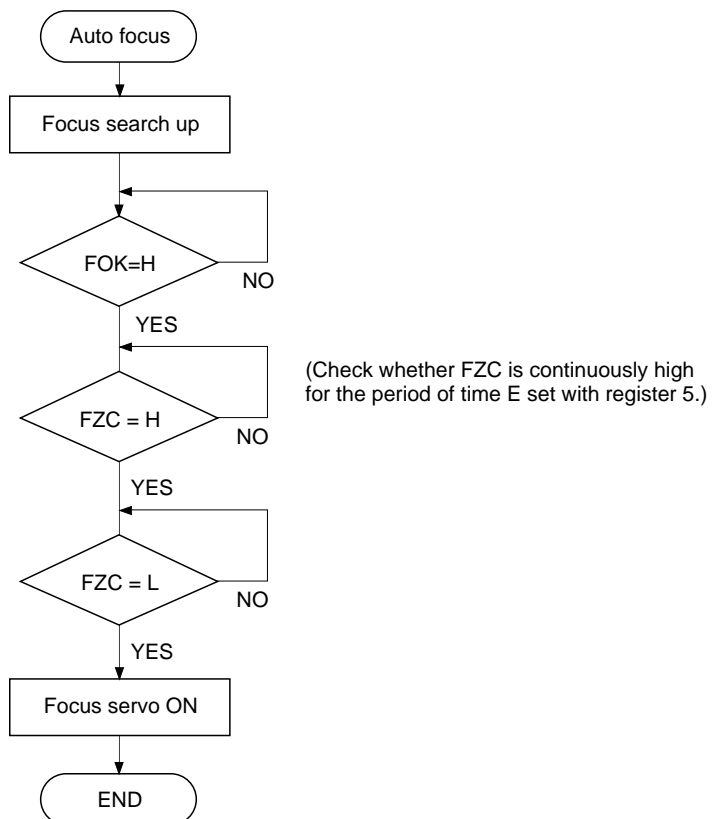


Fig. 3-4-(a). Auto Focus Flow Chart

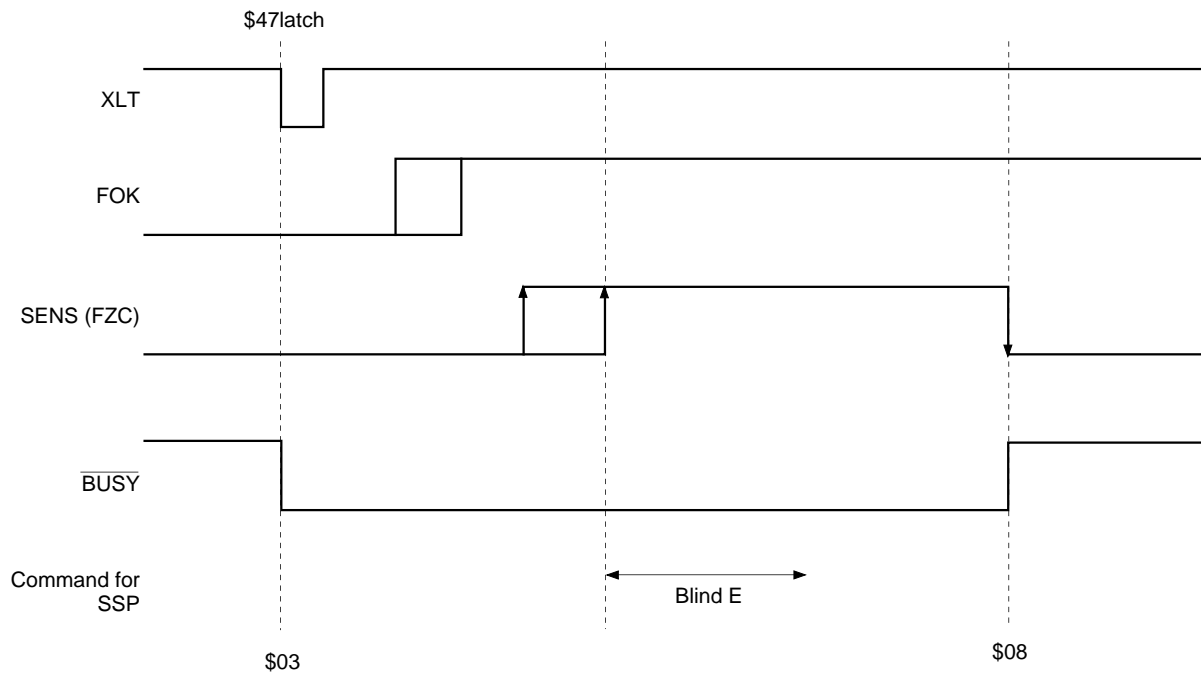


Fig. 3-4-(b). Auto Focus Timing Chart

(b) Track jump

1, 10 and 2N-track jumps are performed respectively. Always use this when the focus, tracking, and sled servos are on. Note that tracking gain-up and braking-on should be sent beforehand because they are not involved in this sequence.

- 1-track jump

When \$48 (\$49 for REV) is received from the CPU, a FWD (REV) 1-track jump is performed in accordance with Fig. 3-5. Set blind A and brake B with register 5.

- 10-track jump

When \$4A (\$4B for REV) is received from the CPU, a FWD (REV) 10-track jump is performed in accordance with Fig. 3-6. The principal difference from the 1-track jump is to kick the sled. In addition, after kicking the actuator, when 5 tracks have been counted through COUT, the brake is applied to the actuator. Then, when the actuator speed is found to have slowed up enough (determined by the COUT cycle becoming longer than the overflow C set with register 5), the tracking and sled servos are turned on.

- 2N-track jump

When \$4C (\$4D for REV) is received from the CPU, a FWD (REV) 2N-track jump is performed in accordance with Fig. 3-7. The track jump count N is set with register 7. Although N can be set to 2^{16} tracks, note that the setting is actually limited by the actuator. COUT is used for counting the number of jumps.

Although the 2N-track jump basically follows the same sequence as the 10-track jump, the one difference is that after the tracking servo is turned on, the sled continues to move only for "D", set with register 6.

- N-track move

When \$4E (\$4F for REV) is received from the CPU, a FWD (REV) N-track move is performed in accordance with Fig. 3-8. N can be set to 2^{16} tracks. COUT is used for counting the number of jumps. The N-track move is executed only by moving the sled, and is therefore suited for moving across several thousand to several ten-thousand tracks.

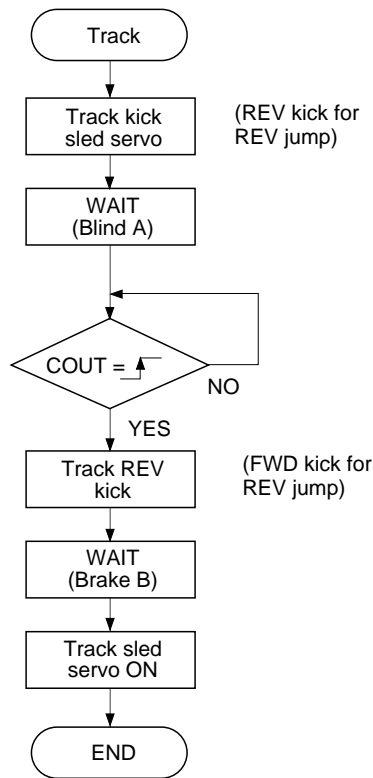


Fig. 3-5-(a). 1-Track Jump Flow Chart

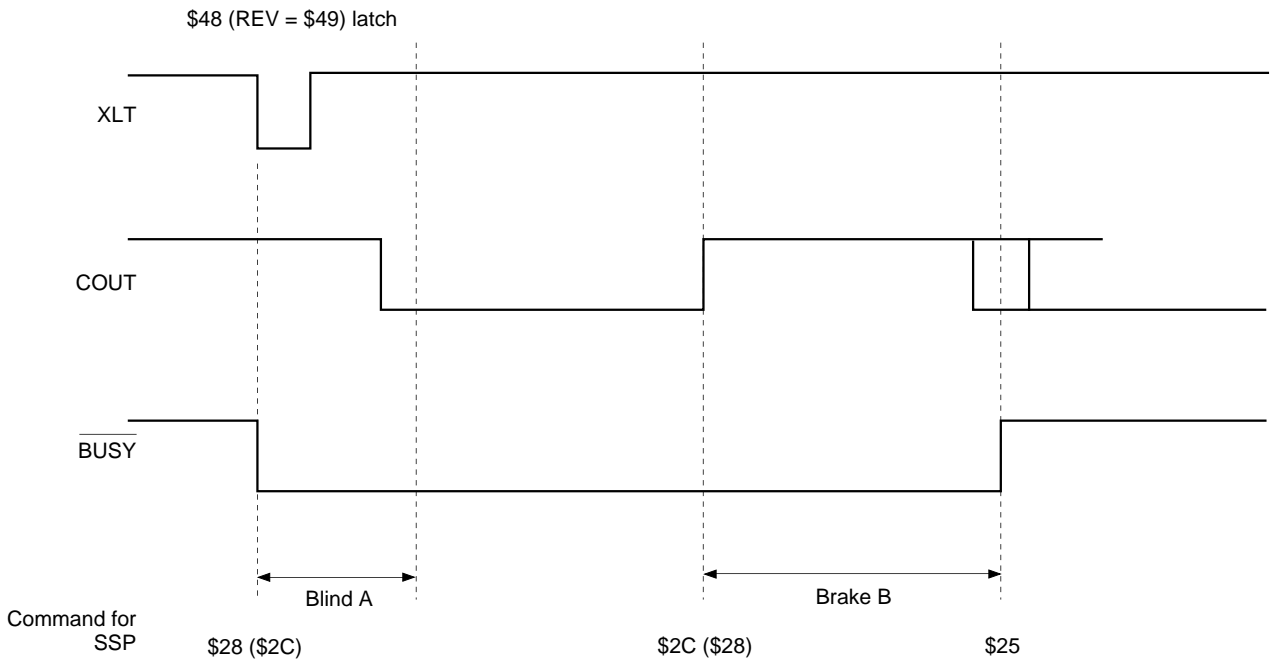


Fig. 3-5-(b). 1-Track Jump Timing Chart

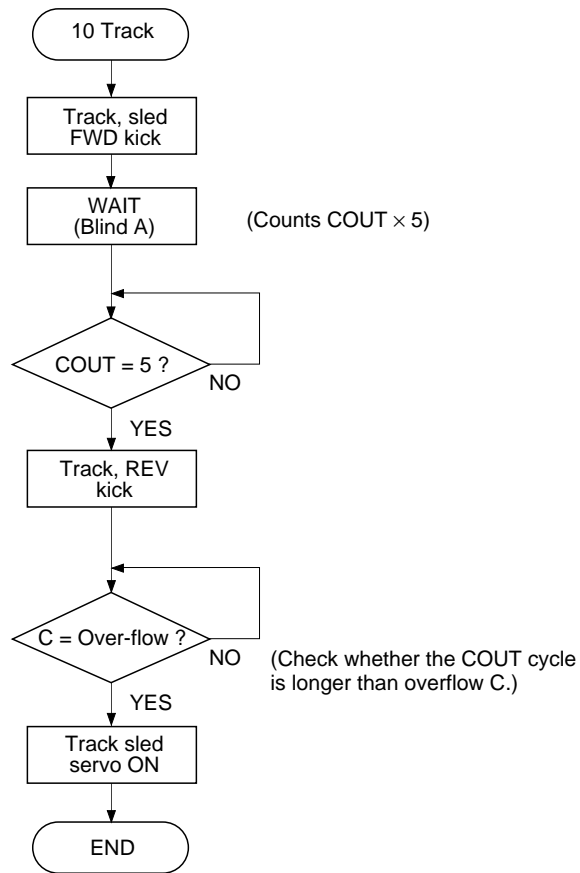


Fig. 3-6-(a). 10-Track Jump Flow Chart

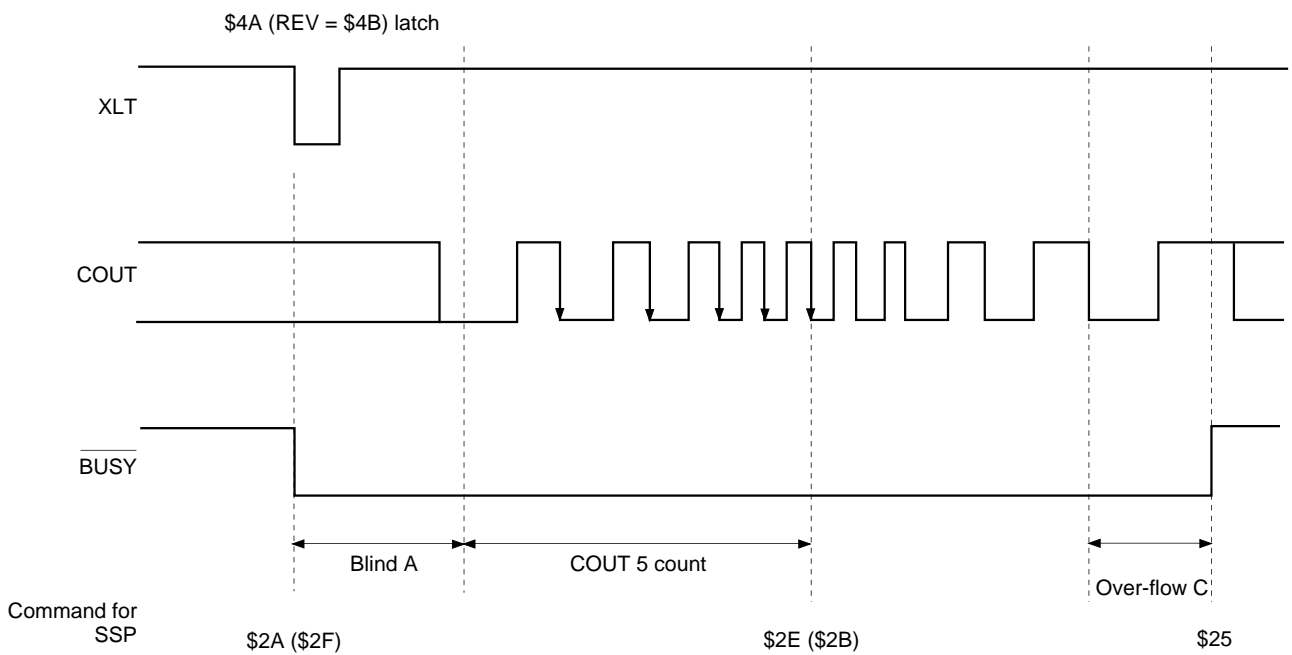


Fig. 3-6-(b). 10-Track Jump Timing Chart

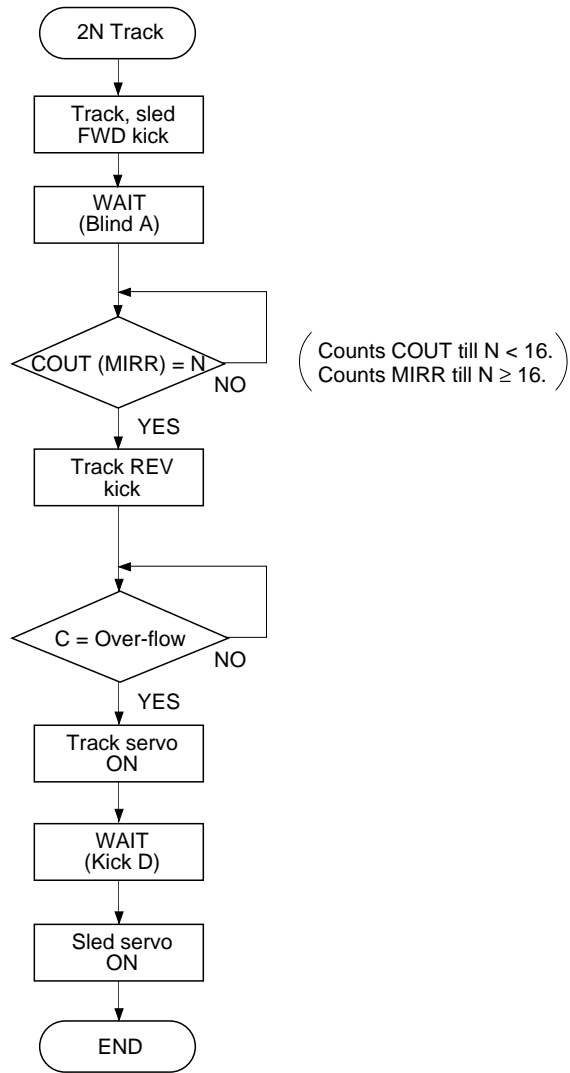


Fig. 3-7-(a). 2N-Track Jump Flow Chart

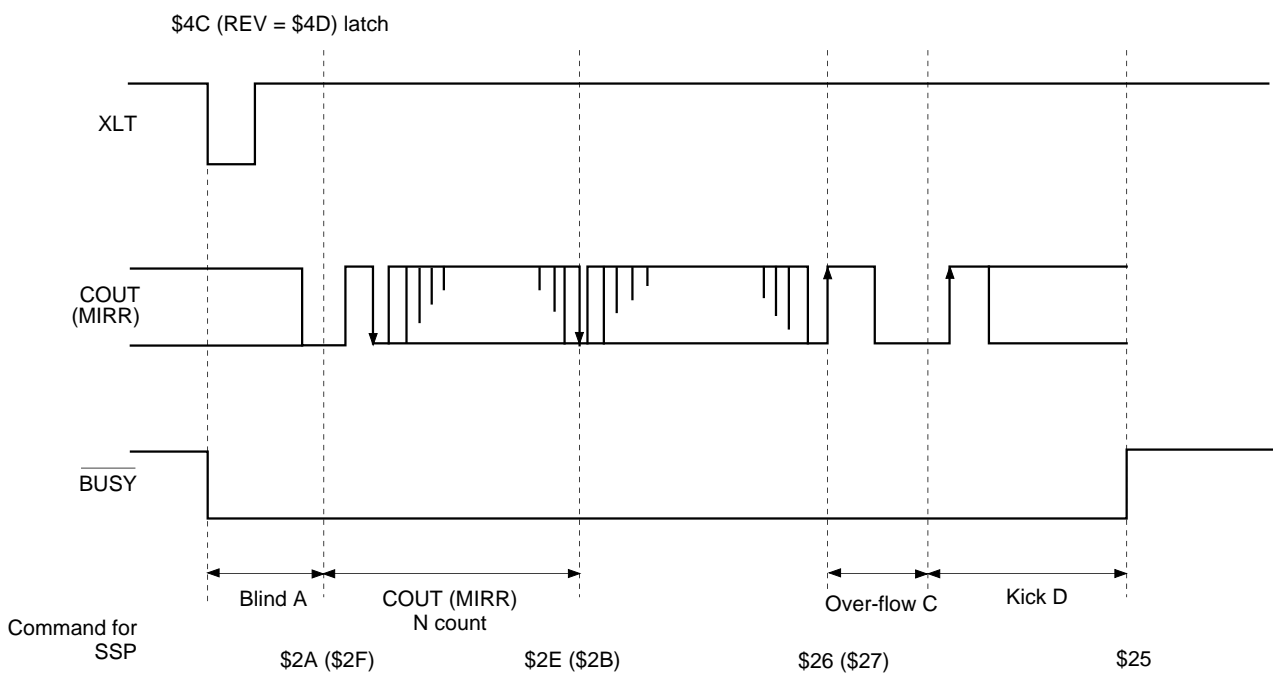


Fig. 3-7-(b). 2N-Track Jump Timing Chart

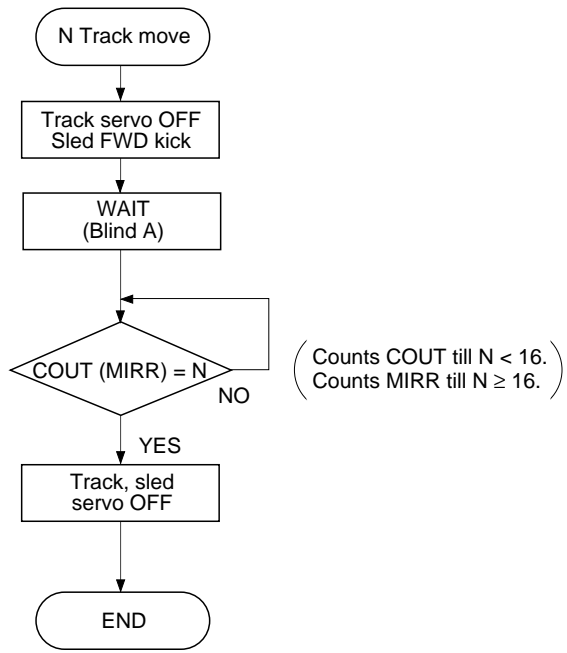


Fig. 3-8-(a). N-Track Move Flow Chart

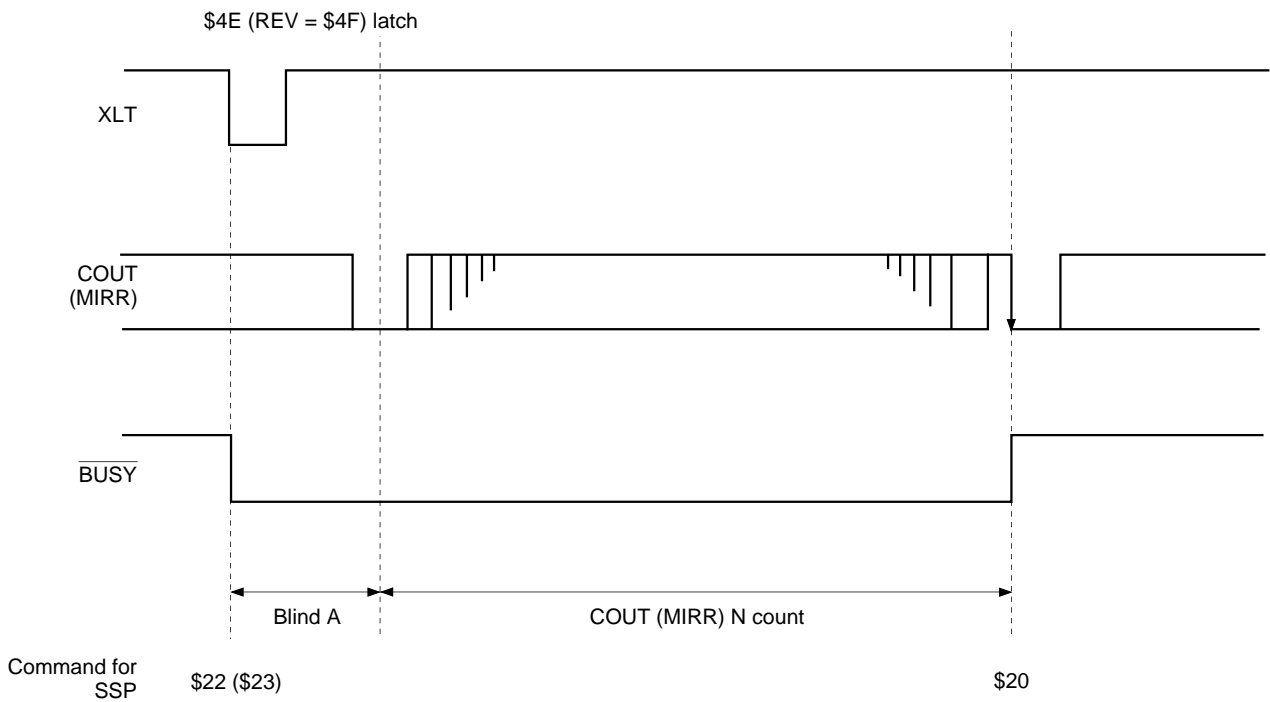


Fig. 3-8-(b). N-Track Move Timing Chart

3-7. Asymmetry Compensation

Fig. 3-9 shows the block diagram and circuit example.

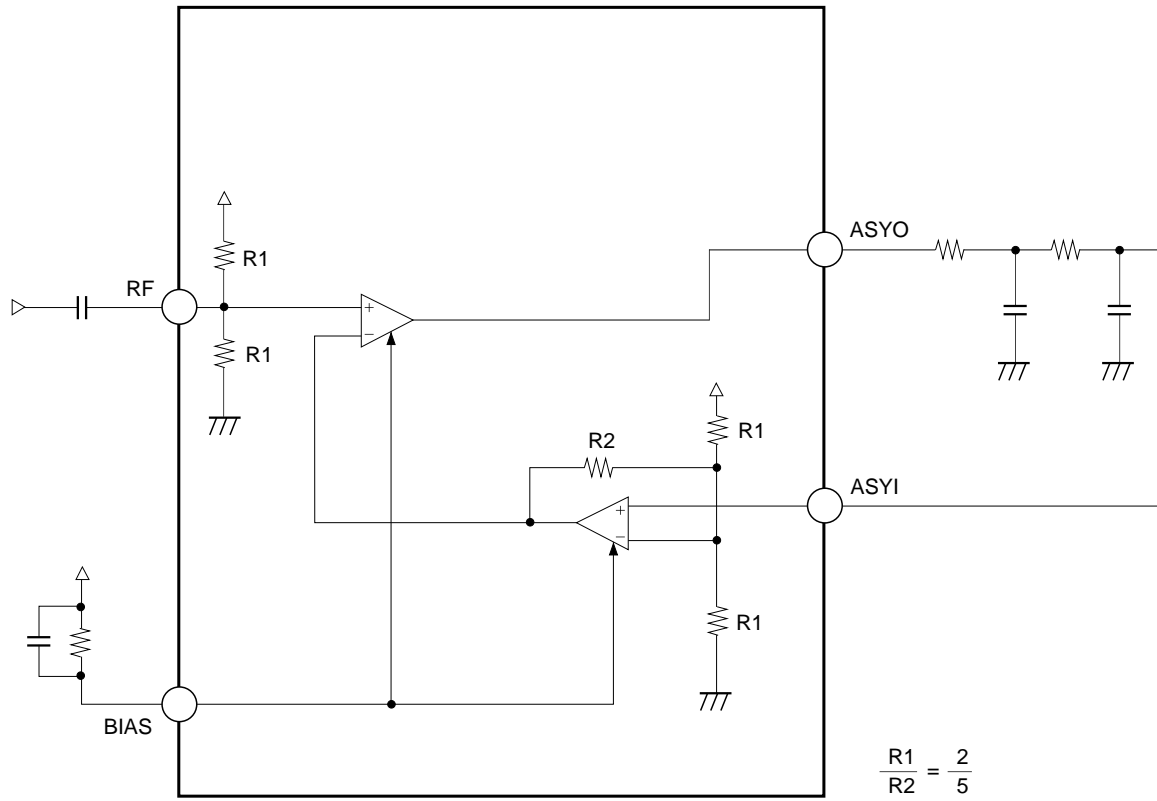


Fig. 3-9. Asymmetry Compensation Application Circuit

3-8. Channel Clock Regeneration by the Digital PLL Circuit

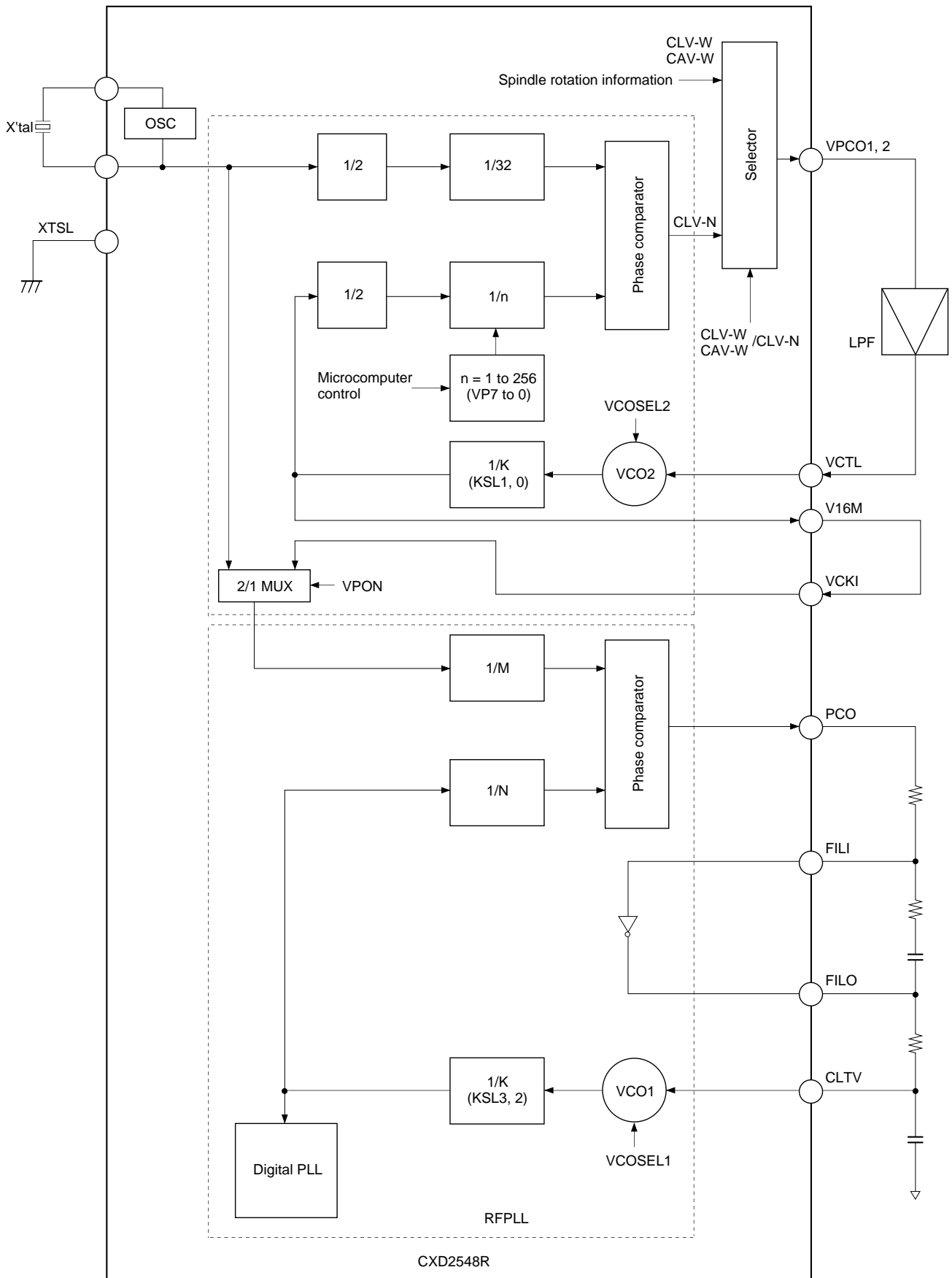
- The channel clock is necessary for demodulating the EFM signal regenerated by the optical system. Assuming T as the channel clock cycle, the EFM signal is modulated in an integer multiple of T from $3T$ to $11T$. In order to read the information in the EFM signal, this integer value must be read correctly. As a result, T , that is the channel clock, is necessary.
In an actual player, a PLL is necessary to regenerate the channel clock because the fluctuation in the spindle rotation alters the width of the EFM signal pulses.

The block diagram of this PLL is shown in Fig. 3-10.

The CXD2548R has a built-in three-stage PLL.

- The first-stage PLL is a wide-band PLL. When using the internal VCO2, an external LPF is necessary; when not using the internal VCO2, external LPF and VCO are necessary.
The output of this first-stage PLL is used as a reference for all clocks within the LSI.
- The second-stage PLL regenerates the high-frequency clock needed by the third-stage digital PLL.
- The third-stage PLL is a digital PLL that regenerates the actual channel clock.
- A new digital PLL has been provided for CLV-W mode to follow the rotational speed of the disc in addition to the conventional secondary loop.

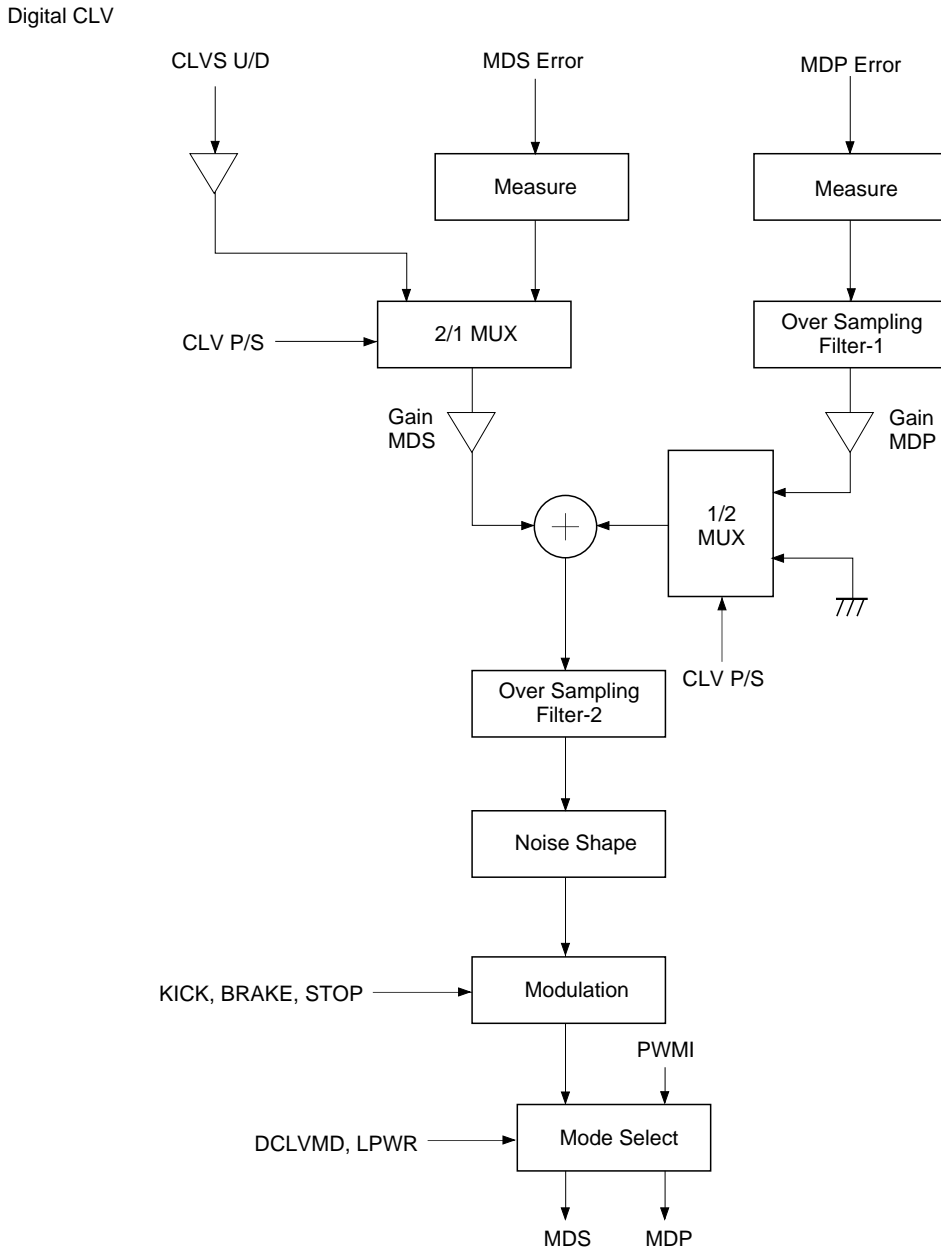
Block Diagram 3-10



3-9. Digital CLV

Fig. 3-11 shows the block diagram. Digital CLV outputs MDS error and MDP error with PWM, with sampling frequency increased up to 130Hz during normal-speed playback in CLVS, CLVP and other modes.

In addition, the digital spindle servo gain is variable.



CLVS U/D: Up/down signal from CLVS servo
 MDS error: Frequency error for CLVP servo
 MDP error: Phase error for CLVP servo
 PWMI: Spindle drive signal from the microcomputer

Fig. 3-11. Block Diagram

3-10. 1-bit DAC Block

(a) DAC block input timing

Timing Chart 3-3 shows the DAC block input timing chart.

Audio data is not transferred from the CD signal processor block to the DAC block inside the CXD2548R. This is to allow data to be sent to the DAC block via the audio DSP, etc.

When the data is input to the DAC block without using the audio DSP, the data must be connected outside the LSI. In this case, EMPH, LRCK, BCK and PCMD can be connected directly with EMPHI, LRCKI, BCKI and PCMDI.

(b) Description of DAC block functions

Zero data detection

When the condition where the lower 4 bits of the input data are DC and the remaining upper bits are all "0" or all "1" has continued about for 300ms, zero data is detected. Zero data detection is performed independently for the left and right channels.

Mute flag output

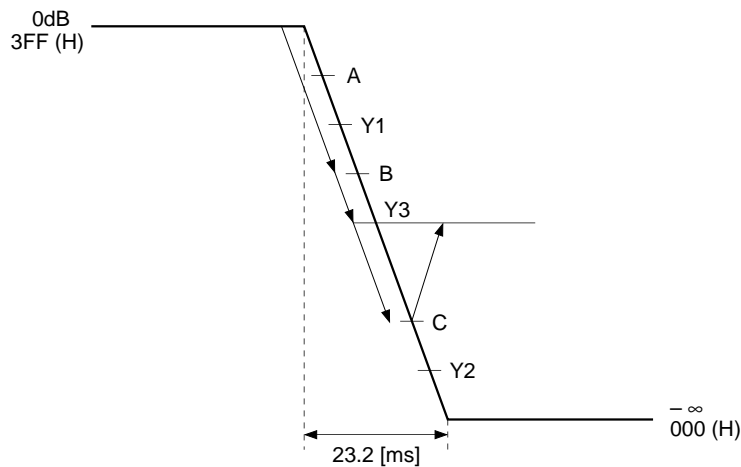
The LMUT and RMUT pins go active when any one of the following conditions is met.

The polarity can be selected with the ZDPL command of \$9X.

- When zero data is detected
- When a high signal is input to the SYSM pin
- When the SMUT command of \$AX is set

Attenuation operation

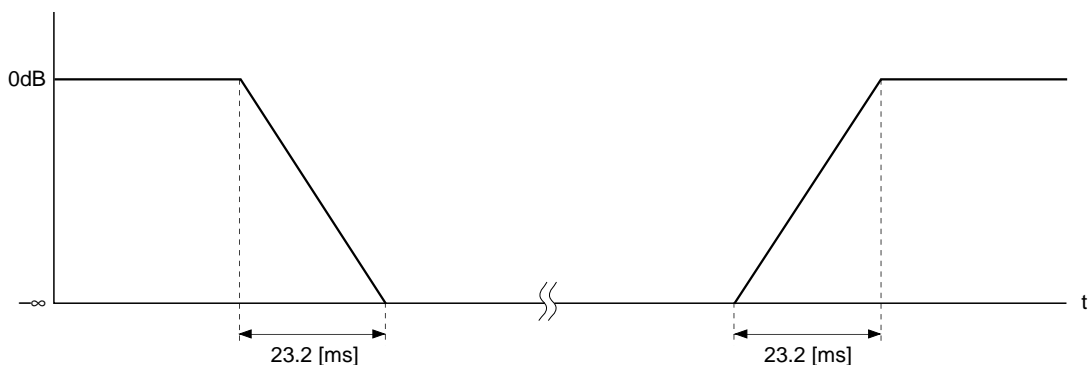
Assuming attenuation data X1, X2 and X3 ($X1 > X3 > X2$), the corresponding audio outputs are Y1, Y2 and Y3 ($Y1 > Y3 > Y2$). First, X1 is sent, followed by X2. If X2 is sent before X1 reaches Y1 (A in the figure), X1 continues approaching Y2. Next, if X3 is sent before X1 reaches Y2 (B or C in the figure), X1 then approaches Y3 from the value (B or C in the figure) at that point.



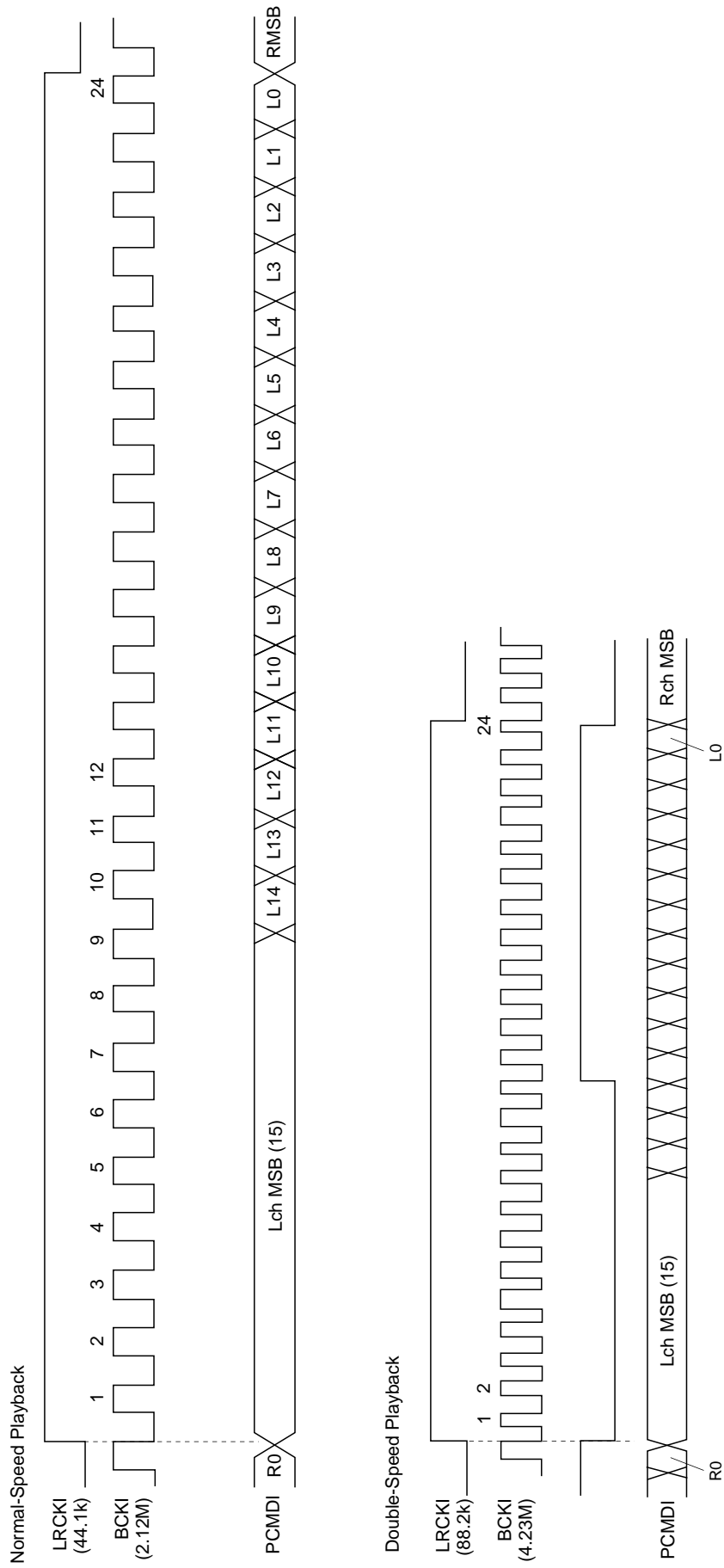
Soft mute

When any one of the following conditions is met, soft mute results and the input data is attenuated to "0".

- When attenuation data of 000 (high) is set
- When "Soft mute" in the operation controls for serial control is high
- When a high signal (= mute) is input to the input pin SYSM



Timing Chart 3-3



3-11. LPF Block

The CXD2548R contains an initial-stage secondary active LPF with numerous resistors and capacitors and an operational amplifier with reference voltage.

The resistors and capacitors are attached externally, allowing the cut-off frequency f_c to be determined flexibly. The reference voltage (V_c) is $(AV_{DD} - AV_{SS})/2$.

The LPF block application circuit is shown below.

In this circuit, the cut-off frequency is $f_c \approx 40\text{kHz}$.

The capacitance of the external capacitors when $f_c = 30\text{kHz}$ and 50kHz are noted below as a reference.

- When $f_c \approx 30\text{kHz}$:
 $C1 = 200\text{pF}$, $C2 = 910\text{pF}$
- When $f_c \approx 50\text{kHz}$:
 $C1 = 120\text{pF}$, $C2 = 560\text{pF}$

LPF Block Application Circuit

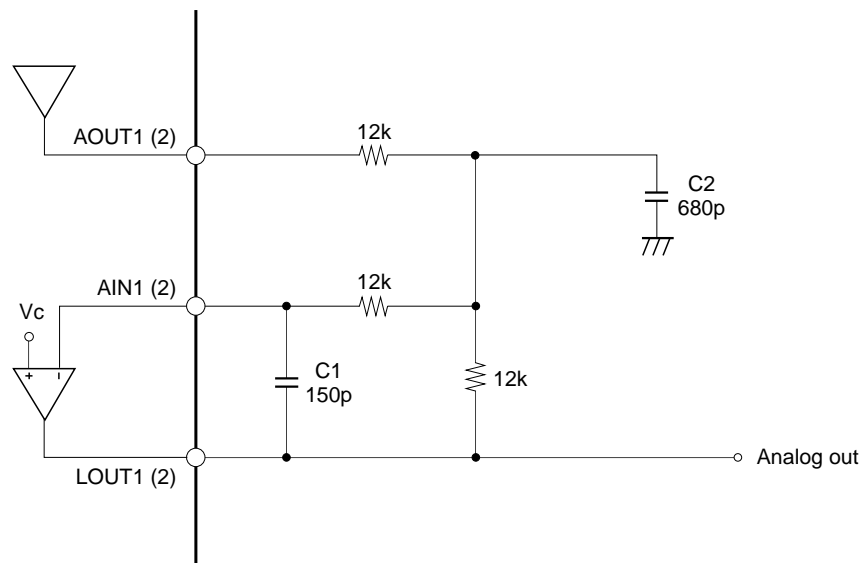


Fig. 3-12. LPF External Circuit

3-12. Setting the Playback Speed for the CD-DSP and 1-bit DAC Blocks (in CLV-N mode)

(a) CD-DSP block

In the CXD2548R, the following playback modes can be selected through different combinations of the crystal, XTSL pin and the DSPB command of \$9X.

CD-DSP block playback speed

| X'tal | XTSL | DSPB | CD-DSP block playback speed |
|-------|------|------|-----------------------------|
| 768Fs | 1 | 0 | 1 × |
| 768Fs | 1 | 1 | 2 × |
| 384Fs | 0 | 0 | 1 × |
| 384Fs | 0 | 1 | 2 × |
| 384Fs | 1 | 1 | 1 × ^{*1} |

Fs = 44.1kHz.

^{*1} Low power consumption mode. The CD-DSP processing speed is halved, allowing power consumption to be reduced.

(b) 1-bit DAC block

The operation speed for the DAC block is determined by the crystal and the MCSL command of \$9X regardless of the CD-DSP operating conditions noted above. This allows the playback modes for the DAC and CD-DSP blocks to be set independently.

1-bit DAC block playback speed

| X'tal | MCSL | DAC block playback speed |
|-------|------|--------------------------|
| 768Fs | 1 | 1 × |
| 768Fs | 0 | 2 × |
| 384Fs | 0 | 1 × |

Fs = 44.1kHz.

[4] Description of Servo Signal Processing System Functions and Commands

§4-1. General Description of the Servo Signal Processing System

(Voltages are the values for a 5V power supply.)

Focus servo

| | |
|----------------|--|
| Sampling rate: | 88.2kHz |
| Input range: | 2.5V center $\pm 1.0V$ |
| Output format: | 7-bit PWM |
| Others: | Offset cancel Focus bias adjustment Focus search Gain-down function Defect countermeasure Auto gain control |

Tracking servo

| | |
|----------------|---|
| Sampling rate: | 88.2kHz |
| Input range: | 2.5V center $\pm 1.0V$ |
| Output format: | 7-bit PWM |
| Others: | Offset cancel E:F balance adjustment Track jump Gain-up function Defect countermeasure Drive cancel Auto gain control Vibration countermeasure |

Sled servo

| | |
|----------------|------------------------|
| Sampling rate: | 345Hz |
| Input range: | 2.5V center $\pm 1.0V$ |
| Output format: | 7-bit PWM |
| Others: | Sled move |

FOK, MIRR, DFCT signals generation

| | |
|--------------------------|---|
| RF signal sampling rate: | 1.4MHz |
| Input range: | 2.15V to 5.0V |
| Others: | RF zero level automatic measurement The signal input from the RFDC pin is multiplied by a factor of 0.7 and loaded into the A/D converter. |

§4-2. Digital Servo Block Master Clock (MCK)

The FSTI pin is the reference clock input pin. The internal master clock (MCK) is generated by dividing the frequency of the signal input to FSTI. The frequency division ratio is 1/2 or 1/4.

Table 4-1 below shows the hypothetical case where the crystal clock generated from the digital signal processor block is 2/3 frequency-divided and input to the FSTI pin by externally connecting the FSTI pin and the FSTO pin.

The XT4D and XT2D command settings can be made with D13 and D12 of \$3F. (Default = 0)

The digital servo block is designed with an MCK frequency of 5.6448MHz.

| Mode | X'tal | FSTO | FSTI | XTSL | XT4D | XT2D | Frequency division ratio | MCK frequency |
|------|-------|-------|-------|------|------|------|--------------------------|---------------|
| 1 | 384Fs | 256Fs | 256Fs | * | 0 | 1 | 1/2 | 128Fs |
| 2 | 384Fs | 256Fs | 256Fs | 0 | 0 | 0 | 1/2 | 128Fs |
| 3 | 768Fs | 512Fs | 512Fs | * | 1 | 0 | 1/4 | 128Fs |
| 4 | 768Fs | 512Fs | 512Fs | 1 | 0 | 0 | 1/4 | 128Fs |

Fs = 44.1kHz, *: Don't care

Table 4-1.

§4-3. AVRG (Average) Measurement and Compensation

The CXD2548R has a circuit that measures AVRG of RFDC, VC, FE, and TE and a circuit that compensates them to control servo effectively.

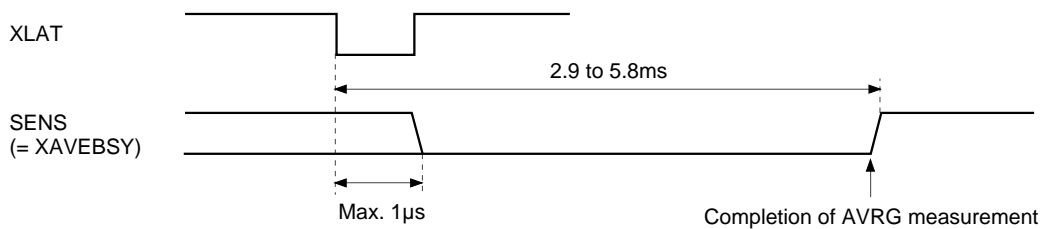
AVRG measurement and compensation is necessary to initialize the CXD2548R, and is able to cancel the offset by performing each AVRG measurement before playback operation and using these results for compensation.

The level applied to the VC, FE, RFDC and TE pins can be measured by setting D15 (VLCM), D13 (FLM), D11 (RFLM) and D4 (TCLM) of \$38 respectively to 1.

AVRG measurement consists of digitally measuring the level applied to each analog input pin by taking the average of 256 samples, and then loading these values into the AVRG register.

AVRG measurement requires approximately 2.9ms to 5.8ms after the command is received.

During AVRG measurement, if the upper 8 bits of the serial data are 38 (Hex), the completion of AVRG measurement operation can be confirmed through the SENS pin. (See Timing Chart 4-1.)



Timing Chart 4-1.

<Measurement>

• VC AVRG

The offset can be canceled by measuring the VC level which is the center voltage for the system and using that value to apply compensation to each input error signal.

• FE AVRG

The FE signal DC level is measured. In addition, compensation is applied to the FZC comparator level output from the SENS pin during FCS SEARCH (focus search) using these measurement results.

• TE AVRG

The TE signal DC level is measured.

• RE AVRG

The MIRR, DFCT and FOK signals are generated from the RF signal. However, the FOK signal is generated by comparing the RF signal at a certain level, so that it is necessary to establish a zero level which becomes the comparator level reference. Therefore, the RF signal is measured before playback operation, and compensation is applied to bring this level to the zero level.

An example of sending AVRG measurement and compensation commands is shown below.

(Example) \$380800 (RF Avg. measurement on)
\$382000 (FE Avg. measurement on)
\$380010 (TE Avg. measurement on)
\$388000 (VC Avg. measurement on)
(Complete each AVRG measurement before starting the next.)
\$38140A (RFLC, FLC0, FLC1 and TLC1 commands on)
(The required compensation should be turn on together; see Fig. 4-2.)

An interval of 5.8ms or more must be maintained between each command, or the SENS pin must be monitored to confirm that the previous command has been completed before the next AVRG command is sent.

<Compensation>

See Fig. 4-2 for the contents of each compensation below.

• RFLC

The difference by which the RF signal exceeds the RF AVRG value is input to the RF In register.

• TCL0

The value obtained by subtracting the VC AVRG value from the TE signal is input to the TRK In register.

• TCL1

The value obtained by subtracting the TE AVRG value from the TE signal is input to the TRK In register.

• VCLC

The value obtained by subtracting the VC AVRG value from the FE signal is input to the FCS In register.

• FLC1

The value obtained by subtracting the FE AVRG value from the FE signal is input to the FCS In register.

• FLC0

The value obtained by subtracting the FE AVRG value from the FE signal is input to the FZC register.

§4-4. E:F Balance Adjustment Function

When the disc is rotated with the laser on, and with the FCS (focus) servo on via FCS Search (focus search), the traverse waveform appears in the TE signal due to disc eccentricity.

In this condition, the low-frequency component can be extracted from the TE signal using the built-in TRK hold filter by setting D5 (TBLM) of \$38 to 1.

The extracted low-frequency component is loaded into the TRVSC register as a digital value, and the TRVSC register value is established when TBLM returns to 0.

Next, setting D2 (TLC2) of \$38 to 1 applies only the amount of compensation (subtraction) equal to the TRVSC register value to the values obtained from the TE and SE input pins, enabling the E:F balance offset to be adjusted. (See Fig. 4-2.)

§4-5. FCS Bias (Focus Bias) Adjustment Function

The FBIAS register value can be added to the FCS servo filter input by setting D14 (FBON) of \$3A to 1. (See Fig. 4-2.)

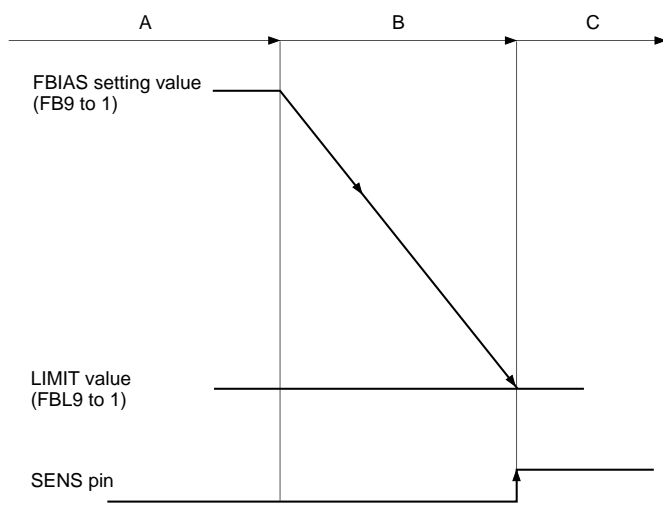
When the FBIAS register value is set to D11 = 0 and D10 = 1 by \$34F, data can be written using the 9-bit value of D9 to D1 (D9: MSB).

In addition, the RF jitter can be monitored by setting the SOCT and SLO commands of \$B to 1. (See "DSP Block Timing Chart".)

The FBIAS register can be used as a counter by setting D13 (FBSS) of \$3A to 1. It operates as an up/down counter. The FBIAS register functions as an up counter when D12 (FBUP) of \$3A = 1, and as a down counter when D12 (FBUP) of \$3A = 0.

The number of up and down steps can be changed by setting D11 and D10 (FBV1 and FBV0) of \$3A.

When using the FBIAS register as a counter, the counter stops when the value set beforehand in FBL9 to 1 of \$34 matches the FCSBIAS value. Also, if the upper 8 bits of the command register are \$3A at this time, the counter stop can be monitored through SENS.



Here, the FBIAS setting values FB9 to 1 and the FBIAS LIMIT values FBL9 to 1 are assumed to be set in status A. For example, if command registers FBUP = 0, FBV1 = 0, FBV0 = 0 and FBSS = 1 are set from this status, down count starts from status A and approaches the set LIMIT value. When the LIMIT value is reached and the FBIAS value matches FBL9 to 1, the counter stops and the SENS pin goes to high. Note that the up/down counter changes with each sampling cycle of the focus servo filter. The number of steps by which the count value changes can be selected from 1, 2, 4 or 8 steps by FBV1 and FBV0. When converted to FE input, 1 step corresponds to approximately 3.9 [mV].

A: Register mode
 B: Counter mode
 C: Counter mode (when stopped)

Fig. 4-1.

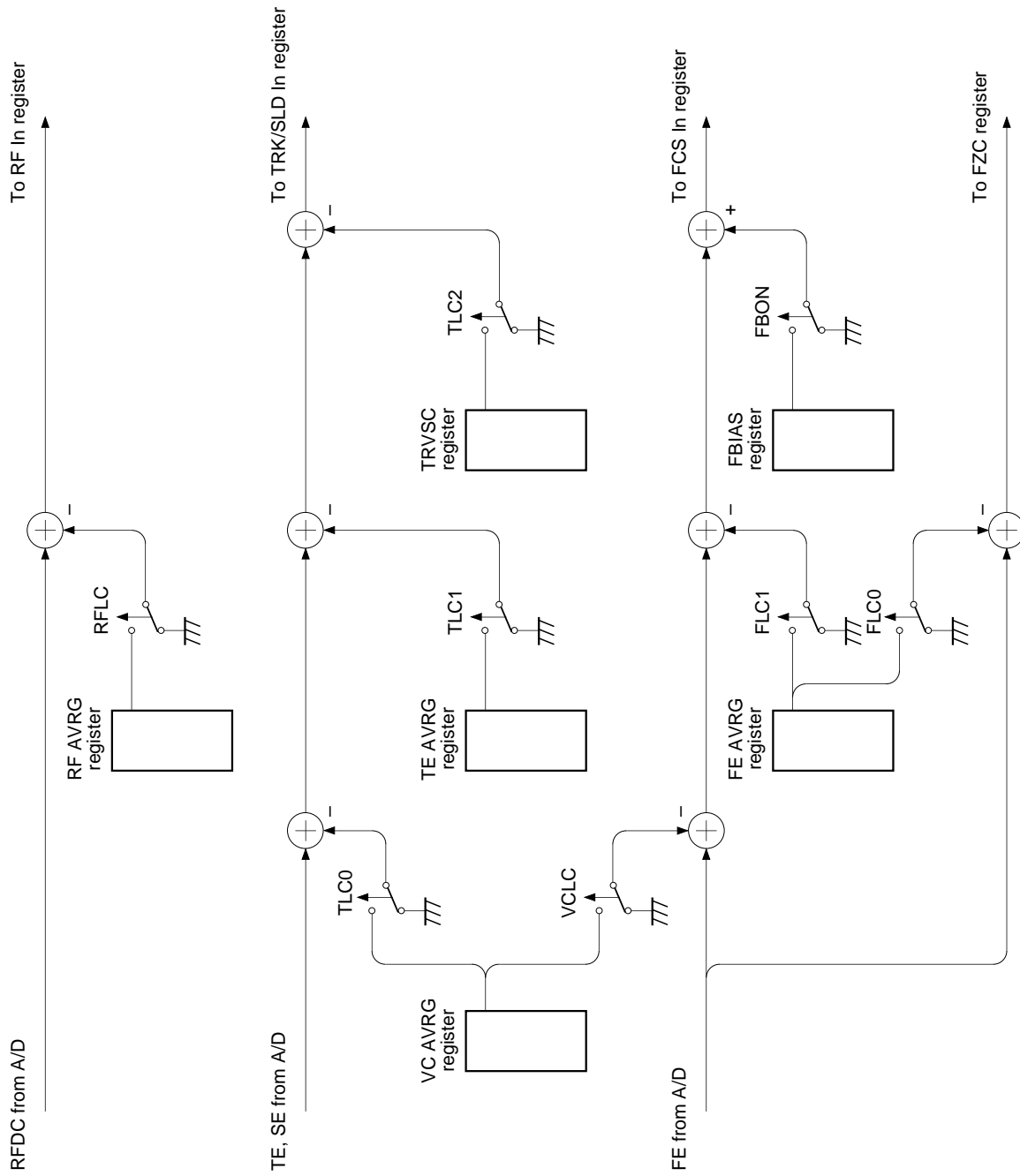


Fig. 4-2.

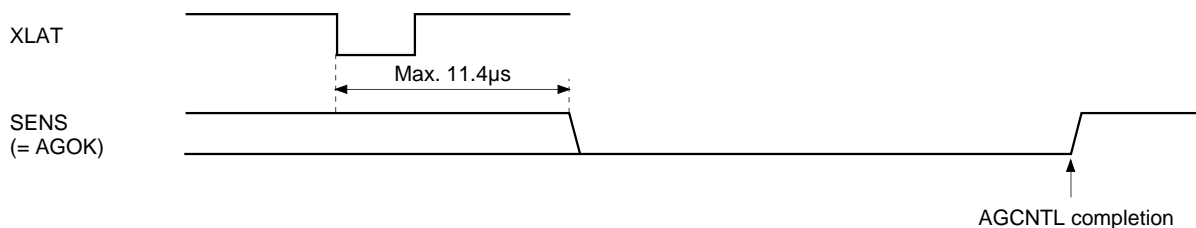
§4-6. AGCNTL (Auto Gain Control) Function

The AGCNTL function automatically adjusts the filter internal gain in order to obtain the appropriate gain with the servo loop. AGCNTL not only copes with the sensitivity variation of the actuator and photo diode, etc., but also obtains the optimal gain for each disc.

The AGCNTL command is sent when each servo is turned on. During AGCNTL operation, if the upper 8 bits of the serial data are 38 (Hex), the completion of AGCNTL operation can be confirmed through the SENS pin. (See Timing Chart 4-2 and "Description of SENS Signals".)

Setting D9 and D8 of \$38 to 1 set FCS (focus) and TRK (tracking) respectively to AGCNTL operation.

Note) During AGCNTL operation, each servo filter gain must be normal, and the anti-shock circuit (described hereafter) must be disabled.



Timing Chart 4-2.

Coefficient K13 changes for AGF (focus AGCNTL) and coefficients K23 and K07 change for AGT (tracking AGCNTL) due to AGCNTL.

These coefficients change from 01 to 7F (Hex), and they must also be set within this range when written externally.

After AGCNTL operation has completed, these coefficient values can be confirmed by reading them out from the SENS pin with the serial readout function (described hereafter).

AGCNTL related setting

The following settings can be changed with \$35, \$36 and \$37.

FG6 to FG0; AGF convergence gain setting, effective setting range: 00 to 57 (Hex)

TG6 to TG0; AGT convergence gain setting, effective setting range: 00 to 57 (Hex)

AGS; Self-stop on/off

AGJ; Convergence completion judgment time

AGGF; Internally generated sine wave amplitude (AGF)

AGGT; Internally generated sine wave amplitude (AGT)

AGV1; AGCNTL sensitivity 1 (during high sensitivity adjustment)

AGV2; AGCNTL sensitivity 2 (during low sensitivity adjustment)

AGHS; High sensitivity adjustment on/off

AGHT; High sensitivity adjustment time

Note) Converging servo loop gain values can be changed with the FG6 to 0 and TG6 to 0 setting values. In addition, these setting values must be within the effective setting range. The default settings aim for 0 dB at 1kHz. However, since convergence values vary according to the characteristics of each constituent element of the servo loop, FG and TG values should be set as necessary.

AGCNTL and default operation have two stages.

In the first stage, high sensitivity adjustment is performed for a certain period of time (select 256/128ms with AGHT), and the AGCNTL coefficient approaches the appropriate value roughly. The sensitivity at this time can be selected from two types with AGV1.

In the second stage, the AGCNTL coefficient approaches the appropriate value finely with relatively low sensitivity. The sensitivity for the second stage can be selected from two types with AGV2. In the second stage of default operation, when the AGCNTL coefficient reaches the appropriate value and stops changing, the CXD2548R confirms that the AGCNTL coefficient has not changed for a certain period of time (select 63/31ms with AGHJ), and then completes AGCNTL operation. (Self-stop mode)

This self-stop mode can be canceled by setting AGS to 0.

In addition, the first stage is omitted for AGCNTL operation when AGHS is set to 0.

An example of AGCNTL coefficient transitions during AGCNTL operation and the relationship between the various settings are shown in Fig. 4-3.

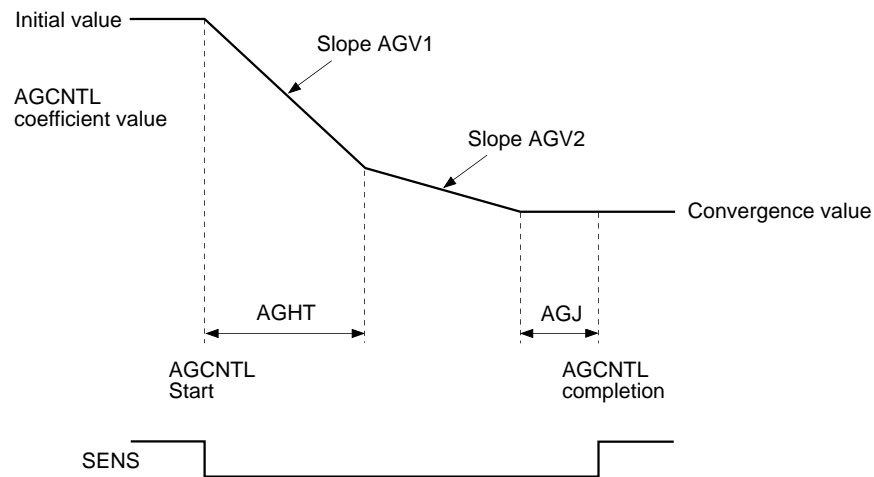


Fig. 4-3.

§4-7. FCS Servo and FCS Search (Focus Search)

The FCS servo is controlled by the 8-bit serial command \$0X. (See Table 4-2.)

| Register name | Command | D23 to D20 | D19 to D16 | |
|---------------|---------------|------------|------------|---|
| 0 | FOCUS CONTROL | 0 0 0 0 | 1 0 * * | FOCUS SERVO ON (FOCUS GAIN NORMAL) |
| | | | 1 1 * * | FOCUS SERVO ON (FOCUS GAIN DOWN) |
| | | | 0 * 0 * | FOCUS SERVO OFF, 0V OUT |
| | | | 0 * 1 * | FOCUS SERVO OFF, FOCUS SEARCH VOLTAGE OUT |
| | | | 0 * 1 0 | FOCUS SEARCH VOLTAGE DOWN |
| | | | 0 * 1 1 | FOCUS SEARCH VOLTAGE UP |

*: Don't care

Table 4-2.

FCS Search

FCS search is required in the course of turning on the FCS servo.

Fig. 4-4 shows the signals for sending commands \$00 → \$02 → \$03 and performing only FCS search.

Fig. 4-5 shows the signals for sending \$08 (FCS on) after that.

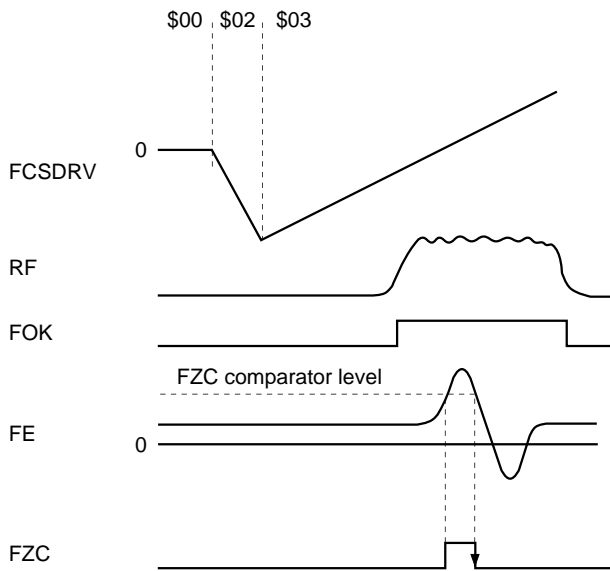


Fig. 4-4.

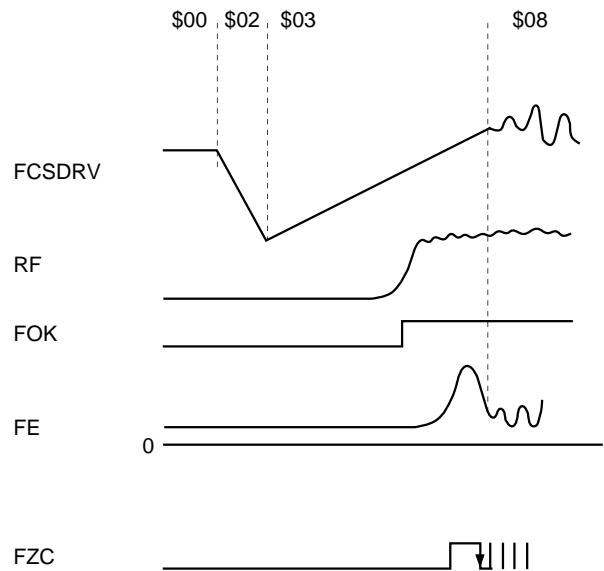


Fig. 4-5.

§4-8. TRK (Tracking) and SLD (Sled) Servo Control

TRK and SLD servo is controlled by the 8-bit command \$2X. (See Table 4-3.)

When the upper 4 bits of the serial data are 2 (Hex), TZG is output from the SENS pin.

| Register name | Command | D23 to D20 | D19 to D16 | |
|---------------|---------------|------------|------------|--------------------|
| 2 | TRACKING MODE | 0 0 1 0 | 0 0 * * | TRACKING SERVO OFF |
| | | | 0 1 * * | TRACKING SERVO ON |
| | | | 1 0 * * | FORWARD TRACK JUMP |
| | | | 1 1 * * | REVERSE TRACK JUMP |
| | | | * * 0 0 | SLED SERVO OFF |
| | | | * * 0 1 | SLED SERVO ON |
| | | | * * 1 0 | FORWARD SLED MOVE |
| | | | * * 1 1 | REVERSE SLED MOVE |

*: Don't care

Table 4-3.

TRK Servo

The TRK JUMP (track jump) height can be set with 6 bits (D13 to D8) of \$36.

In addition, when the TRK servo is on and D17 of \$1 is set to 1, the TRK servo filter assumes gain-up status. The filter also assumes gain-up status when vibration detection is performed with the LOCK signal low and the anti-shock circuit (described hereafter) enabled.

The gain-up filter used when TRK has assumed gain-up status has two types of structures which can be selected by setting D16 of \$1. (See Table 4-5.)

SLD Servo

The SLD MOV (sled move) output, composed of a basic value from 6 bits (D13 to D8) of \$37, is determined by multiplying this value by 1 ×, 2 ×, 3 ×, or 4 × magnification set using D17 and D16 when D19 = D18 = 0 is set with \$3. (See Table 4-4.)

SLD MOV must be performed continuously for 50μs or more. In addition, if the LOCK input signal goes low when the SLD servo is on, the SLD servo turns off.

Note) When the LOCK signal is low, the TRK servo is set to gain-up status and the SLD servo is turned off by the default. These operations are disabled by setting D6 (LKSW) of \$38 to 1.

| Register name | Command | D23 to D20 | D19 to D16 | |
|---------------|---------|------------|------------|------------------------------------|
| 3 | SELECT | 0 0 1 1 | 0 0 0 0 | SLED KICK LEVEL (basic value × ±1) |
| | | | 0 0 0 1 | SLED KICK LEVEL (basic value × ±2) |
| | | | 0 0 1 0 | SLED KICK LEVEL (basic value × ±3) |
| | | | 0 0 1 1 | SLED KICK LEVEL (basic value × ±4) |

Table 4-4.

§4-9. MIRR and DFCT Signal Generation

The RF signal obtained from the RFDC pin is sampled at approximately 1.4MHz and loaded. The MIRR and DFCT signals are generated from this RF signal.

MIRR Signal Generation

The loaded RF signal is applied to peak hold and bottom hold circuits.

An envelope is generated from the waveforms generated in these circuits, and the MIRR comparator level is generated from the average of these envelope waveforms.

The MIRR signal is generated by comparing this MIRR comparator level with the waveform generated by subtracting the bottom hold value from the peak hold value. (See Fig. 4-6.)

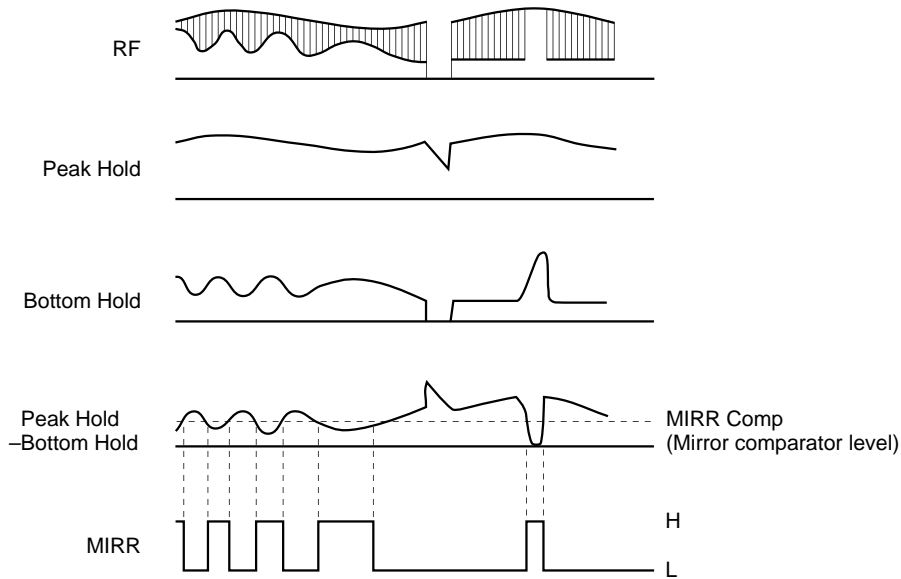


Fig. 4-6.

DFCT Signal Generation

The loaded RF signal is input to two peak hold circuits with different time constants, and the DFCT signal is generated by comparing the difference between these two peak hold waveforms with the DFCT comparator level. (See Fig. 4-7.)

The DFCT comparator level can be selected from four values using D13 and D12 of §3B.

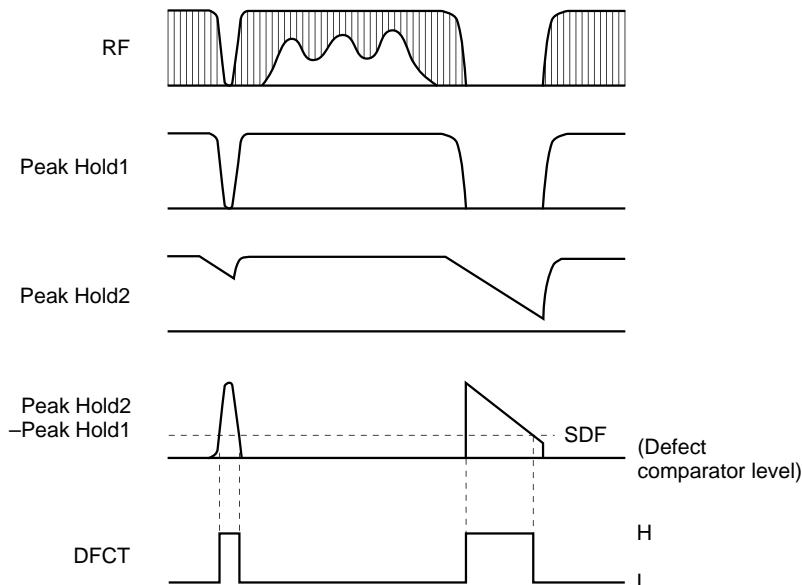


Fig. 4-7.

§4-10. DFCT Countermeasure Circuit

The DFCT countermeasure circuit performs operations to maintain the directionality of the servo so that the servo does not become easily dislocated due to scratches or defects on discs.

Specifically, these operations are achieved by performing scratch and defect detection with the DFCT signal generation circuit, and when DFCT goes high, applying the low frequency component of the error signal before DFCT went high to the FCS and TRK servo filter inputs. (See Fig. 4-8.)

In addition, these operations are activated by the default. They can be disabled by setting D7 (DFSW) of \$38 to 1.

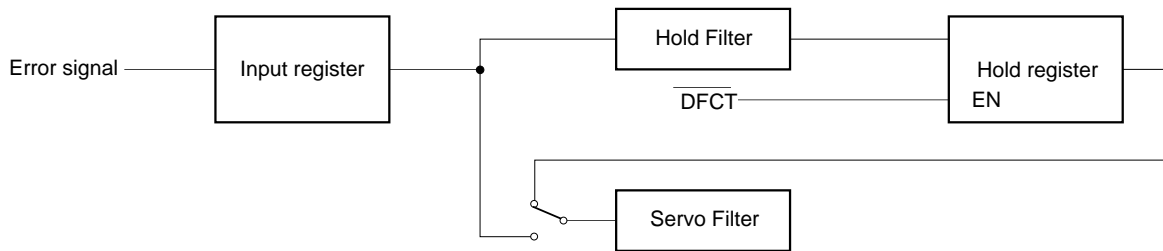


Fig. 4-8.

§4-11. Anti-Shock Circuit

When vibrations are produced in the CD player, this circuit forces the TRK filter to assume gain-up status so that the servo does not become easily dislocated. This circuit is for systems which require vibration countermeasures.

Concretely, vibrations are detected using an internal anti-shock filter and comparator circuit, and the gain is increased. (See Fig. 4-9.)

The comparator level is fixed to 1/16 of the maximum comparator input amplitude. However, the comparator level is practically variable by adjusting the anti-shock filter output coefficient K35.

This function can be turned on and off by D19 of \$1 when the brake circuit (described hereafter) is off. (See Table 4-5.)

This circuit can also support an external vibration detection circuit, and can set the TRK servo filter to gain-up status by inputting high level to the ATSK pin.

When the serial data is \$1, vibration detection can be monitored from the SENS pin.

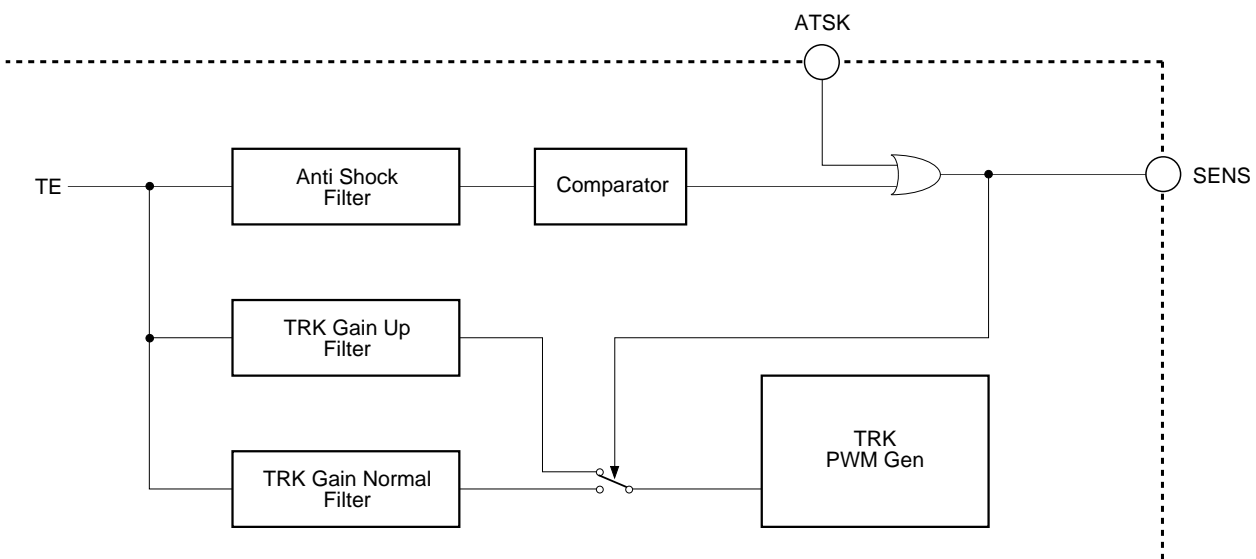


Fig. 4-9.

§4-12. Brake Circuit

Immediately after a long distance track jump it tends to be hard for the actuator to settle and for the servo to turn on.

The brake circuit prevents these phenomenon.

In principle, this circuit cuts unnecessary portions of the tracking drive and applies the brake by utilizing the 180° offset in the RF envelope and tracking error phase relationship which occurs when the actuator traverses the track in the radial direction from the inner track to the outer track and vice versa. (See Figs. 4-10 and 4-11.) Concretely, this operation is achieved by masking the tracking drive using the TRKCNCL signal generated by loading the MIRR signal at the edge of the TZC (Tracking Zero Cross) signal.

The brake circuit can be turned on and off by D18 of \$1. (See Fig. 4-5.)

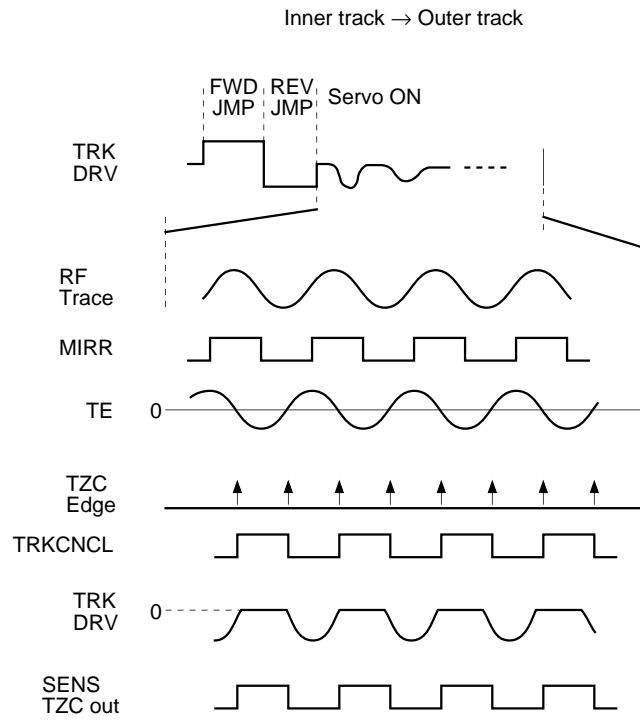


Fig. 4-10.

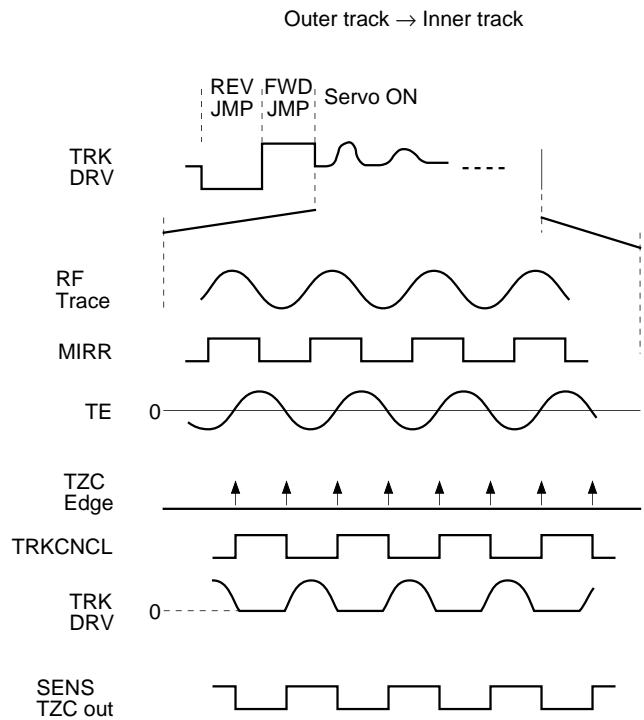


Fig. 4-11.

| Register name | Command | D23 to D20 | D19 to D16 | |
|---------------|------------------|------------|------------|----------------------------------|
| 1 | TRACKING CONTROL | 0 0 0 1 | 1 0 * * | ANTI SHOCK ON |
| | | | 0 * * * | ANTI SHOCK OFF |
| | | | * 1 * * | BRAKE ON |
| | | | * 0 * * | BRAKE OFF |
| | | | * * 0 * | TRACKING GAIN NORMAL |
| | | | * * 1 * | TRACKING GAIN UP |
| | | | * * * 1 | TRACKING GAIN UP FILTER SELECT 1 |
| | | | * * * 0 | TRACKING GAIN UP FILTER SELECT 2 |

*: Don't care

Fig. 4-5.

§4-13. COUT Signal

The COUT signal is output to count the number of tracks during traverse, etc. It is basically generated by loading the MIRR signal at both edges of the TZC signal. However, the used TZC signal can be selected and there are two types of output methods according to the COUT signal application.

For 1-track jumps, etc.

Fast phase COUT signal generation with a fast phase TZC signal.

For High-speed traverse

Reliable COUT signal generation with a delayed phase TZC signal.

This is because some time is required to generate the MIRR signal, and it is necessary to delay the TZC signal in accordance with the MIRR signal delay during high-speed traverse.

The COUT signal output method is switched with D16 when D19 = D18 = 1 and D17 = 0 are set with \$3. (When D16 = 1, for delayed phase and high-speed traverse.) In addition, the TZC signal delay can be selected from two values with D14 of \$36.

§4-14. Serial Readout Circuit

The following measurement and adjustment results can be read out from the SENS pin by inputting the readout clock to the SCLK pin by \$39. (See Fig. 4-12, Table 4-6 and "Description of SENS Signals".)

Specified commands

- \$390C VC AVRG measurement result
- \$3908 FE AVRG measurement result
- \$3904 TE AVRG measurement result
- \$391F RF AVRG measurement result
- \$3953 FCS AGCNTL coefficient result
- \$3963 TRK AGCNTL coefficient result
- \$391C TRVSC adjustment result
- \$391D FBIAS register value

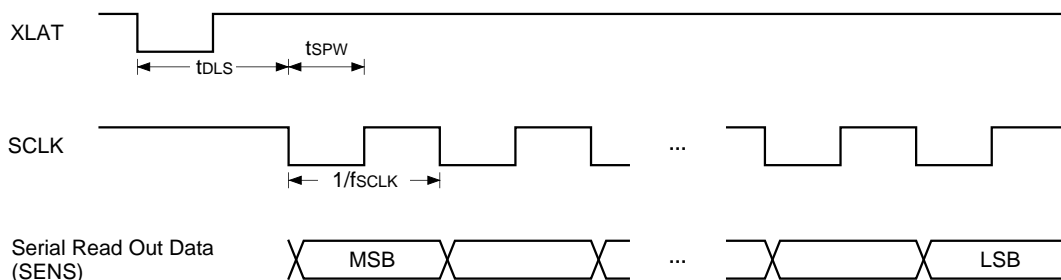


Fig. 4-12.

| Item | Symbol | Min. | Typ. | Max. | Unit |
|------------------|--------|------|------|------|------|
| SCLK frequency | fSCLK | | | 1 | MHz |
| SCLK pulse width | tSPW | 500 | | | ns |
| Delay time | tDLS | 15 | | | μs |

Table 4-6.

During readout, the upper 8 bits of the serial data must be 39 (Hex).

§4-15. Writing the Coefficient RAM

The coefficient RAM can be rewritten by \$34. All coefficients have default values in the built-in ROM, and transfer from the ROM to the RAM is completed approximately 40µs after the XRST pin rises. (The coefficient RAM cannot be rewritten during this period.)

After that, the characteristics of each built-in filter can be finely adjusted by rewriting the data for each address of the coefficient RAM.

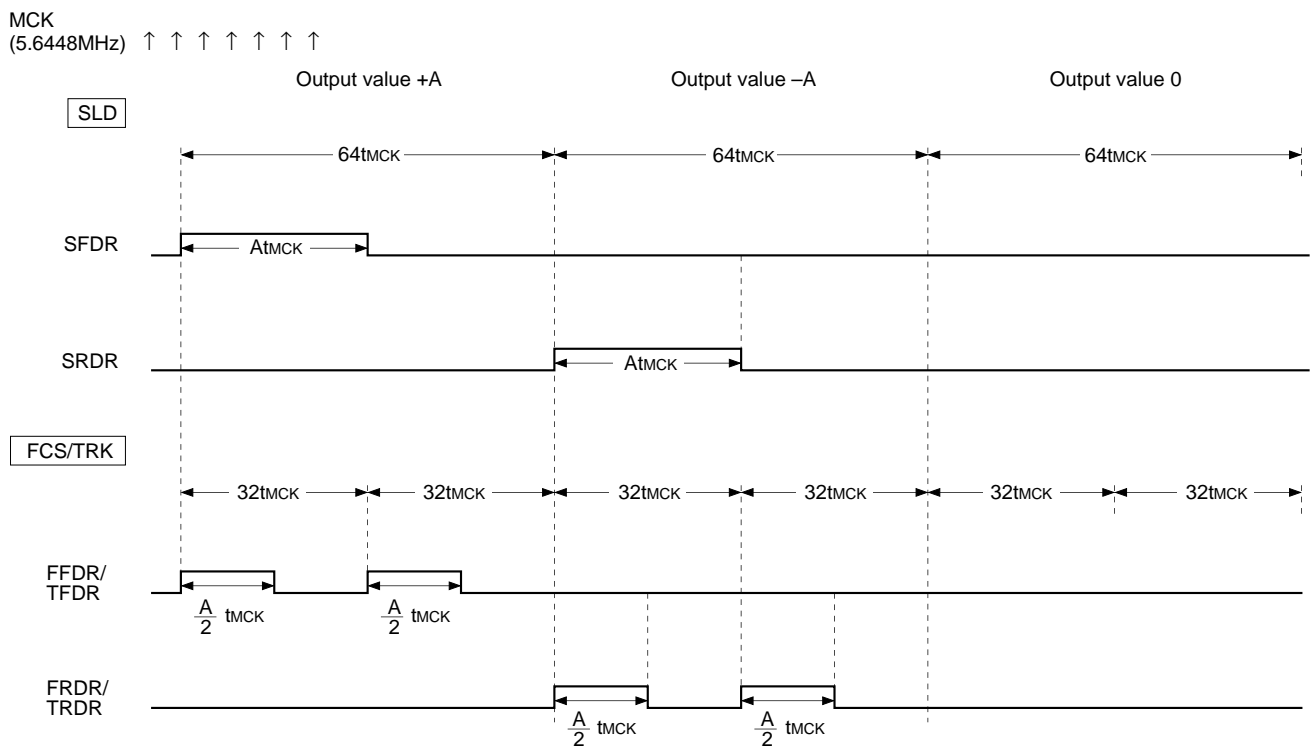
The coefficient rewrite command is comprised of 24 bits, with D14 to D8 of \$34 as the address (D15 = 0) and D7 to D0 as data.

§4-16. PWM Output

FCS, TRK and SLD outputs are output as PWM waveforms.

In particular, FCS and TRK permit accurate drive by using a double oversampling noise shaper.

Timing Chart 4-3 and Fig. 4-13 show examples of output waveforms and drive circuits.



$$tMCK = \frac{1}{5.6448MHz} \approx 180ns$$

Timing Chart 4-3.

Example of Drive Circuit

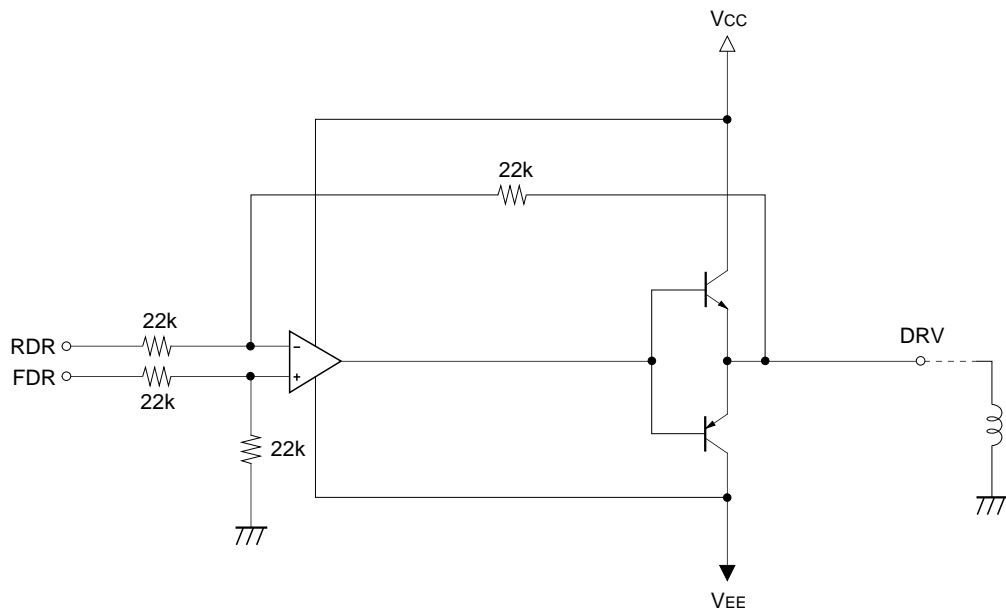


Fig. 4-13. Operational Amplifier Drive Circuit

§4-17. Servo Status Changes Produced by the LOCK Signal

When the LOCK signal becomes low, the TRK servo assumes the gain-up status and the SLD servo turns off in order to prevent SLD free-running.

Setting D6 (LKS) of \$38 to 1 deactivates this function.

In other words, neither the TRK servo nor the SLD servo change even when the LOCK signal becomes low.

This enables microcomputer control.

§4-18. Description of Commands and Data Sets

The following description contains portions which convert internal voltages into the values when they are output externally and describe them as input conversion or output conversion.

Input conversion converts these voltages into the voltages entering input pins before A/D conversion.

Output conversion converts PWM output values into analog voltage values.

Both types of conversion are calculated at $V_{DD} = 5.0V$. If this voltage changes, the conversion values also change proportionally. (Voltage conversion = $V_{DD}/5$; V_{DD} : used supply voltage)

\$34

| | | | | | | | | | | | | | | | |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | KA6 | KA5 | KA4 | KA3 | KA2 | KA1 | KA0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 |

When D15 = 0

KA6 to KA0: Coefficient address

KD7 to KD0: Coefficient data

| | | | | | | | | | | | | | | | |
|-----|-----|-----|-----|-----|-----|------|------|------|------|------|------|------|------|------|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 1 | 1 | 1 | 1 | 0 | FBL9 | FBL8 | FBL7 | FBL6 | FBL5 | FBL4 | FBL3 | FBL2 | FBL1 | — |

When D15 = D14 = D13 = D12 = D11 = 1 (\$34F)

D10 = 0

FBIAS LIMIT register write

FBL9 to FBL1: Data; data compared with FB9 to 1, FBL9 = MSB.

When using the FBIAS register in counter mode, counter operation stops when the value of FB9 to 1 matches with FBL9 to 1.

| | | | | | | | | | | | | | | | |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 1 | 1 | 1 | 0 | 1 | FB9 | FB8 | FB7 | FB6 | FB5 | FB4 | FB3 | FB2 | FB1 | — |

When D15 = D14 = D13 = D12 = 1. (\$34F)

D11 = 0, D10 = 1

FBIAS register write

FB9 to FB1: Data; FB9 is MSB two's complement data.

For FE input conversion, FB9 to FB1 = 01111111 corresponds to approximately +1V and FB9 to FB1 = 10000000 to -1V respectively. (when the supply voltage = 5V)

| | | | | | | | | | | | | | | | |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 1 | 1 | 1 | 0 | 0 | TV9 | TV8 | TV7 | TV6 | TV5 | TV4 | TV3 | TV2 | TV1 | TV0 |

When D15 = D14 = D13 = D12 = 1. (\$34F)

D11 = 0, D10 = 0

TRVSC register write

TV9 to TV0: Data; TV9 is MSB two's complement data.

For TE input conversion, TV9 to TV0 = 0011111111 corresponds to approximately +1V and TV9 to TV0 = 1100000000 to -1V respectively. (when the supply voltage = 5V)

- Note)**
- When the TRVSC register is read out, the data length is 9 bits. At this time, data corresponding to each bit of TV8 to TV0 during external write are read out.
 - When reading out internally measured values and then writing these values externally, set TV9 the same as TV8.

\$35

| | | | | | | | | | | | | | | | |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| FT1 | FT0 | FS5 | FS4 | FS3 | FS2 | FS1 | FS0 | FTZ | FG6 | FG5 | FG4 | FG3 | FG2 | FG1 | FG0 |

FT1, FT0, FTZ: Focus search-up speed
 Default value: 010 (3.36V/s)
 Focus drive output conversion

| FT1 | FT0 | FTZ | Focus search speed |
|-----|-----|-----|--------------------|
| 0 | 0 | 0 | 6.73V/s |
| 0 | 1 | 0 | 3.36 |
| 1 | 0 | 0 | 2.24 |
| 1 | 1 | 0 | 1.68 |
| 0 | 0 | 1 | 8.97 |
| 0 | 1 | 1 | 5.38 |
| 1 | 0 | 1 | 4.49 |
| 1 | 1 | 1 | 3.85 |

FS5 to FS0: Focus search limit voltage
 Default value: 011000 ($\pm 1.875V$)
 Focus drive output conversion
 FG6 to FG0: AGF convergence gain setting value
 Default value: 0101101

\$36

| | | | | | | | | | | | | | | | |
|-----|------|-----|-----|-----|-----|-----|-----|------|-----|-----|-----|-----|-----|-----|-----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | DTZC | TJ5 | TJ4 | TJ3 | TJ2 | TJ1 | TJ0 | SFJP | TG6 | TG5 | TG4 | TG3 | TG2 | TG1 | TG0 |

DTZC: DTZC delay (8.5/4.25 μ s)
 Default value: 0 (4.25 μ s)
 TJ5 to TJ0: Track jump voltage
 Default value: 001110 ($\approx \pm 1.09V$)
 Tracking drive output conversion
 SFJP: Surf jump mode on/off
 TRK PWM output is made by adding the tracking filter output and TJReg (TJ5 to 0), by setting D7 to 1 (on).
 TG6 to TG0: AGT convergence gain setting value
 Default value: 0101110

\$37

| | | | | | | | | | | | | | | | |
|------|------|-----|-----|-----|-----|-----|-----|-----|-----|------|------|------|------|------|------|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| FZSH | FZSL | SM5 | SM4 | SM3 | SM2 | SM1 | SM0 | AGS | AGJ | AGGF | AGGT | AGV1 | AGV2 | AGHS | AGHT |

FZSH, FZSL: FZC (Focus Zero Cross) slice level

Default value: 01 ($\pm 250\text{mV}$); FE input conversion

| FZSH | FZSL | Slice level |
|------|------|-------------|
| 0 | 0 | +500mV |
| 0 | 1 | +250 |
| 1 | 0 | +125 |
| 1 | 1 | +62.5 |

SM5 to SM0: Sled move voltage

Default value: 010000 ($\approx \pm 1.25\text{V}$)

Sled drive output conversion

AGS: AGCNTL self-stop on/off

Default value: 1 (on)

AGJ: AGCNTL convergence completion judgment time during low sensitivity adjustment (31/63ms)

Default value: 0 (63ms)

AGGF: Focus AGCNTL internally generated sine wave amplitude (small/large)

Default value: 1 (large)

AGGT: Tracking AGCNTL internally generated sine wave amplitude (small/large)

Default value: 1 (large)

| | FE/TE input conversion |
|----------------|------------------------|
| AGGF 0 (small) | 63mV |
| 1 (large) | 125 |
| AGGT 0 (small) | 125mV |
| 1 (large) | 250 |

AGV1: AGCNTL convergence sensitivity during high sensitivity adjustment; high/low

Default value: 1 (high)

AGV2: AGCNTL convergence sensitivity during low sensitivity adjustment; high/low

Default value: 0 (low)

AGHS: AGCNTL high sensitivity adjustment on/off

Default value: 1 (on)

AGHT: AGCNTL high sensitivity adjustment time (128/256ms)

Default value: 0 (256ms)

\$38

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------|-----|------|------|------|-----|-----|------|------|------|------|------|------|------|------|
| VCLM | VCLC | FLM | FLC0 | RFLM | RFLC | AGF | AGT | DFSW | LKSW | TBLM | TCLM | FLC1 | TLC2 | TLC1 | TLC0 |

- * VCLM: VC level measurement (on/off)
- VCLC: VC level compensation for FCS In register (on/off)
- * FLM: Focus zero level measurement (on/off)
- FLC0: Focus zero level compensation for FZC register (on/off)
- * RFLM: RF zero level measurement (on/off)
- RFLC: RF zero level compensation (on/off)
- AGF: Focus auto gain adjustment (on/off)
- AGT: Tracking auto gain adjustment (on/off)
- DFSW: Defect disable switch (on/off)
Setting this switch to 1 (on) disables the defect countermeasure circuit.
- LKSW: Lock switch (on/off)
Setting this switch to 1 disables the sled free-running prevention circuit.
- TBLM: Traverse center measurement (on/off)
- * TCLM: Tracking zero level measurement (on/off)
- FLC1: Focus zero level compensation for FCS In register (on/off)
- TLC2: Traverse center compensation (on/off)
- TLC1: Tracking zero level compensation (on/off)
- TLC0: VC level compensation for TRK/SLD In register (on/off)

Note) Commands marked with * are accepted every 2.9ms.
All commands are on when set to 1.

\$39

| | | | | | | | |
|-----|-----|-----|-----|-----|-----|-----|-----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| DAC | SD6 | SD5 | SD4 | SD3 | SD2 | SD1 | SD0 |

DAC: Serial data readout DAC mode (on/off)

SD6 to SD0: Serial readout data select

| SD6 | SD5 | Readout data | | | Readout data length |
|---------|---|--|------------|------------------------|---------------------|
| 1 | Coefficient RAM data for address = SD5 to SD0 | | | 8 bit | |
| 0 | 1 | Data RAM data for address = SD4 to SD0 | | | 16 bit |
| 0 | 0 | SD4 | SD3 to SD0 | | |
| | | 1 | 1 1 1 1 | RF AVRG register | 8 bit |
| | | | 1 1 1 0 | RFDC input signal | 8 bit |
| | | | 1 1 0 1 | FBIAS register | 9 bit |
| | | | 1 1 0 0 | TRVSC register | 9 bit |
| | | | 0 0 1 1 | RFDC envelope (bottom) | 8 bit |
| | | | 0 0 1 0 | RFDC envelope (peak) | 8 bit |
| | | 0 | 1 1 * * | VC AVRG register | 9 bit |
| | | | 1 0 * * | FE AVRG register | 9 bit |
| | | | 0 1 * * | TE AVRG register | 9 bit |
| 0 0 1 1 | FE input signal | | 8 bit | | |
| 0 0 1 0 | TE input signal | 8 bit | | | |
| 0 0 0 1 | SE input signal | 8 bit | | | |
| 0 0 0 0 | VC input signal | 8 bit | | | |

Note) Coefficients K40 to K4F cannot be read out.

*: Don't care

See the description for SRO1 of \$3F concerning readout methods for the above data.

\$3A

| | | | | | | | | | | | | | | | |
|-----|------|------|------|------|------|----|------|------|------|------|------|------|------|------|------|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | FBON | FBSS | FBUP | FBV1 | FBV0 | 0 | TJD0 | FPS1 | FPS0 | TPS1 | TPS0 | CEIT | SJHD | INBK | MT10 |

FBON: FBIAS (focus bias) register addition (on/off)
 The FBIAS register value is added to the signal loaded into the FCS In register by setting D14 to 1 (on).

FBSS: FBIAS (focus bias) register/counter switching
 The FCS BIAS register can be used as a counter by setting D13 to 1 (on).

FBUP: FBIAS (focus bias) counter up/down operation switching
 This performs counter up/down control when FBSS = 1. The FBIAS register functions as a down counter with D12 set to 0, and as an up counter when set to 1.

FBV1, FBV0: FBIAS (focus bias) counter voltage switching
 FCS BIAS count-up steps is decided by these bits.

| FBV1 | FBV0 | Number of steps |
|------|------|-----------------|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 4 |
| 1 | 1 | 8 |

The counter changes once for each sampling cycle of the focus servo filter. When MCK is 128Fs, the sampling frequency is 88.2kHz. When converted to FE input, 1 step is approximately 3.9 [mV].

TJD0: This sets the tracking servo filter data RAM to 0 when switched from track jump to servo on only when SFJP = 1 (during surf jump operation).

FPS1, FPS0: Gain setting when transferring data from the focus filter to the PWM block.

TPS1, TPS0: Gain setting when transferring data from the tracking filter to the PWM block.

This is effective for increasing the overall gain in order to widen the servo band. Operation when FPS1, FPS0 (TPS1, TPS0) = 00 is the same as usual (7-bit shift). However, 6dB, 12dB and 18dB can be selected independently for focus (tracking) by setting the relative gain to 0dB when FPS1, FPS0 (TPS1, TPS0) = 00.

| FPS1 | FPS0 | Relative gain |
|------|------|---------------|
| 0 | 0 | 0dB |
| 0 | 1 | +6dB |
| 1 | 0 | +12dB |
| 1 | 1 | +18dB |

| TPS1 | TPS0 | Relative gain |
|------|------|---------------|
| 0 | 0 | 0dB |
| 0 | 1 | +6dB |
| 1 | 0 | +12dB |
| 1 | 1 | +18dB |

CEIT: The CE pin input takes over the TE pin input by setting D3 to 1 (on). This means that the registers and filters for TE input are used for CE input.

SJHD: This holds the tracking filter output at the value when surf jump starts during surf jump.

INBK: When D2 is 0 (off), the brake circuit masks the tracking filter output signal with TRKCNCL which is generated by taking the MIRR signal at the TZC edge. When D2 is set to 1 (on), the tracking filter input is masked instead of the output.

MT10: The tracking filter input is masked when the MIRR signal is high by setting D1 to 1 (on).

\$3B

| | | | | | | | | | | | | | | | |
|------|------|------|------|------|------|------|-----|------|------|------|------|------|----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| SFO2 | SFO1 | SDF2 | SDF1 | MAX2 | MAX1 | SFOX | BTF | D2V2 | D2V1 | D1V2 | D1V1 | RINT | 0 | 0 | 0 |

SFOX, SFO2, SFO1: FOK slice level

Default value: 011 (313mV)

RFDC input conversion

| SFOX | SFO2 | SFO1 | Slice level |
|------|------|------|-------------|
| 0 | 0 | 0 | 179mV |
| 0 | 0 | 1 | 223 |
| 0 | 1 | 0 | 268 |
| 0 | 1 | 1 | 313 |
| 1 | 0 | 0 | 357 |
| 1 | 0 | 1 | 446 |
| 1 | 1 | 0 | 536 |
| 1 | 1 | 1 | 625 |

SDF2, SDF1: DFCT slice level
 Default value: 10 (179mV)
 RFDC input conversion

| SDF2 | SDF1 | Slice level |
|------|------|-------------|
| 0 | 0 | 89mV |
| 0 | 1 | 134 |
| 1 | 0 | 179 |
| 1 | 1 | 224 |

MAX2, MAX1: DFCT maximum time
 Default value: 00 (no timer limit)

| MAX2 | MAX1 | DFCT maximum time |
|------|------|-------------------|
| 0 | 0 | No timer limit |
| 0 | 1 | 2.00ms |
| 1 | 0 | 2.36 |
| 1 | 1 | 2.72 |

BTF: Bottom hold double-speed count-up mode for MIRR signal generation
 On/off (default: off)
 On when set to 1.

D2V2, D2V1: Peak hold 2 for DFCT signal generation
 Count-down speed setting
 Default value: 01 (0.492V/ms, 44.1kHz)
 [V/ms] unit items indicate RFDC input conversion; [kHz] unit items indicate the operating frequency of the internal counter.

| D2V2 | D2V1 | Count-down speed | |
|------|------|------------------|-------|
| | | [V/ms] | [kHz] |
| 0 | 0 | 0.246 | 22.05 |
| 0 | 1 | 0.492 | 44.1 |
| 1 | 0 | 0.984 | 88.2 |
| 1 | 1 | 1.969 | 176.4 |

D1V2, D1V1: Peak hold 1 for DFCT signal generation
 Count-down speed setting
 Default value: 01 (3.938V/ms, 352.8kHz)
 [V/ms] unit items indicate RFDC input conversion; [kHz] unit items indicate the operating frequency of the internal counter.

| D1V2 | D1V1 | Count-down speed | |
|------|------|------------------|--------|
| | | [V/ms] | [kHz] |
| 0 | 0 | 1.969 | 176.4 |
| 0 | 1 | 3.938 | 352.8 |
| 1 | 0 | 7.875 | 705.6 |
| 1 | 1 | 15.75 | 1411.2 |

RINT: This initializes the initial-stage registers of the circuits which generate MIRR, DFCT and FOK.

\$3E

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------|------|------|------|------|------|------|------|------|------|----|----|----|------|------|
| F1NM | F1DM | F3NM | F3DM | T1NM | T1UM | T3NM | T3UM | DFIS | TLCD | RFLP | 0 | 0 | 0 | MIRI | XT1D |

F1NM, F1DM: Quasi double accuracy setting for FCS servo filter first-stage

On when set to 1; default = 0.

F1NM: Gain normal

F1DM: Gain down

T1NM, T1UM: Quasi double accuracy setting for TRK servo filter first-stage

On when set to 1; default = 0.

T1NM: Gain normal

T1UM: Gain up

F3NM, F3DM: Quasi double accuracy setting for FCS servo filter third-stage

On when set to 1; default = 0.

Generally, the advance amount of the phase becomes large by partially setting the FCS servo third-stage filter which is used as the phase compensation filter to double accuracy.

F3NM: Gain normal

F3DM: Gain down

T3NM, T3UM: Quasi double accuracy setting for TRK servo filter third-stage

On when set to 1; default = 0.

Generally, the advance amount of the phase becomes large by partially setting the TRK servo third-stage filter which is used as the phase compensation filter to double accuracy.

T3NM: Gain normal

T3UM: Gain up

Note) Filter first- and third-stage quasi double accuracy settings can be set individually.

See "FILTER Composition" at the end of this specification concerning quasi double-accuracy.

DFIS: FCS hold filter input extraction node selection

0: M05 (Data RAM address 05); default

1: M04 (data RAM address 04)

TLCD: This command masks the TLC2 command set by D2 of \$38 only when FOK is low.

On when set to 1; default = 0

RFLP: This command passes the signal obtained from the RFDC pin through the LPF (low-pass filter) before the built-in A/D converter.

0: LPF off; default

1: LPF on

MIRI: MIRR input switching.

The MIRR signal can be input from an external source. When D1 is 0, the MIRR signal is used internally as usual. When D1 = 1, the MIRR signal can be input from an external source through the MIRR pin.

XT1D: The clock input from FSTI can be used as the master clock for the servo block regardless of the XTSL pin, XT2D and XT4D by setting D0 to 1.

\$3F

| | | | | | | | | | | | | | | | |
|-----|------|------|------|-----|------|------|------|----|------|----|------|------|------|------|------|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | AGG4 | XT4D | XT2D | 0 | DRR2 | DRR1 | DRR0 | 0 | ASFG | 0 | LPAS | SRO1 | SRO0 | AGHF | COT2 |

AGG4: This varies the amplitude of the internally generated sine wave using the AGGF and AGGT commands during AGC.
When AGG4 = 0, the default is used. When AGG4 = 1, the setting is as shown in the table below.

| AGGF (MSB) | AGGT (LSB) | TE/FE input conversion |
|------------|------------|------------------------|
| 0 | 0 | 31 [mV] |
| 0 | 1 | 63 [mV] |
| 1 | 0 | 125 [mV] |
| 1 | 1 | 250 [mV] |

These settings are the same as for both focus auto gain control and tracking auto gain control.

XT4D, XT2D: MCK (digital servo master clock) frequency division setting
This command forcibly sets the frequency division ratio to 1/2 or 1/4 when MCK is generated from the signal input to the FSTI pin.

| XT4D | XT2D | Frequency division ratio |
|------|------|-----------------------------|
| 0 | 0 | According to XTSL (default) |
| 0 | 1 | 1/2 |
| 1 | 0 | 1/4 |

DRR2 to DRR0: Partially clears the Data RAM values (0 write).
The following values are cleared when set to 1 (on) respectively; default = 0
DRR2: M08, M09, M0A
DRR1: M00, M01, M02
DRR0: M00, M01, M02 only when LOCK = low
Note) Set DRR1 and DRR0 for 50µs or more.

ASFG: When vibration detection is performed during anti-shock circuit operation, FCS servo filter is forcibly set to gain normal status.
On when set to 1; default = 0

LPAS: Built-in analog buffer low-current consumption mode
This mode reduces the total analog buffer current consumption for the VC, TE, SE and FE input by using a single operational amplifier.
On when set to 1; default = 0
Note) When using this mode, firstly check whether each error signal is properly A/D converted using the SRO1 and SRO0 commands of \$3F.

SRO1, SRO0: These commands are used to output various data continuously externally which have been specified with the \$39 command. (However, D15 (DAC) of \$39 must be set to 1.)
Digital output (SOCK, XOLT and SOUT) can be obtained from three specified pins by setting these commands to 1 respectively. The default is 0, 0.

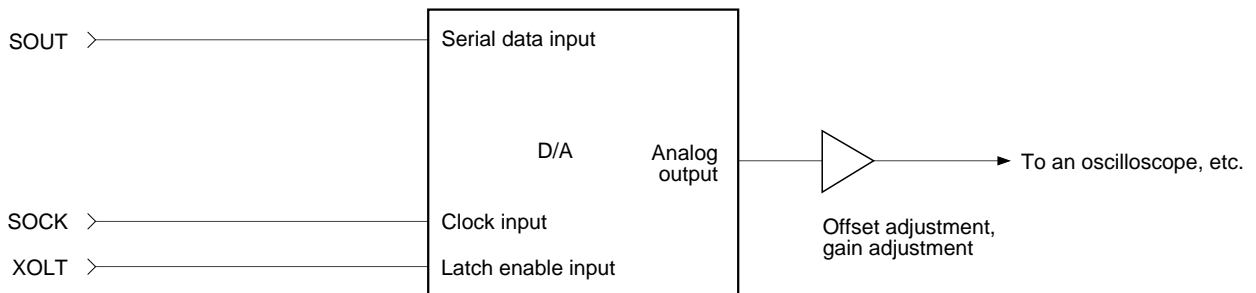
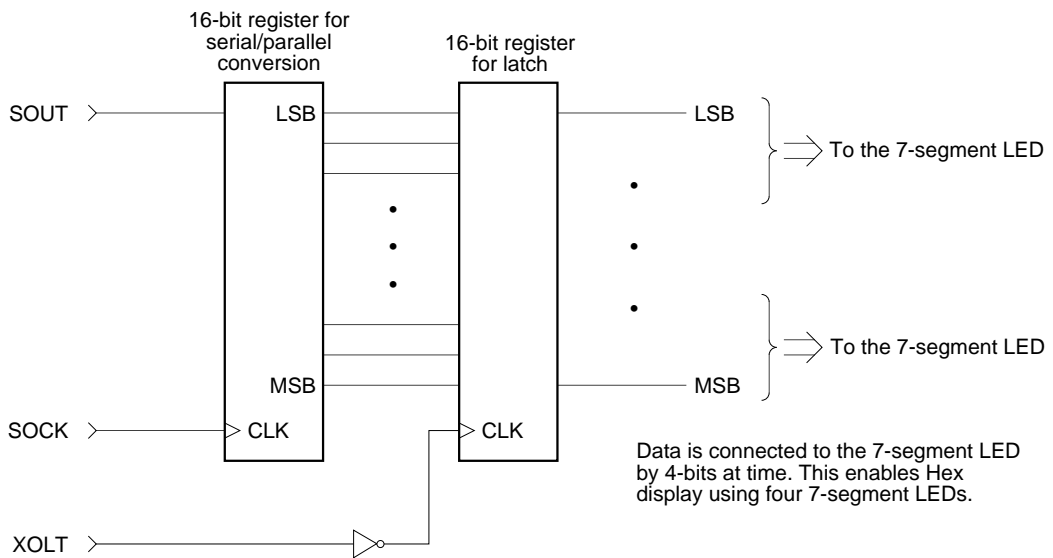
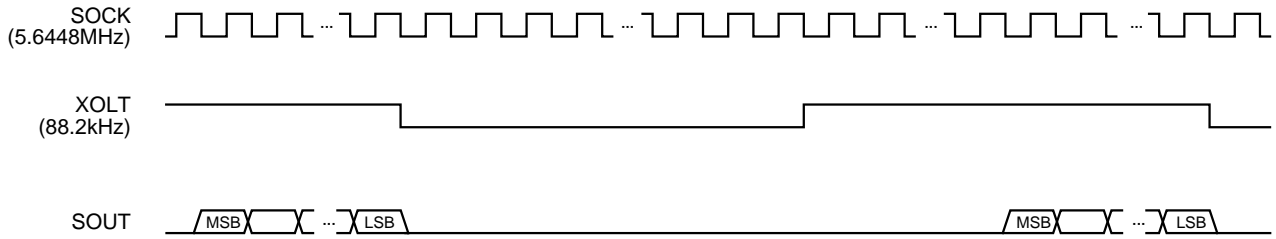
The output pins for each case are shown below.

| | SRO1 = 1 |
|------|----------|
| SOCK | XUGF |
| XOLT | GFS |
| SOUT | GTOP |

(See "Description of Data Readout" on the following page.)

AGHF: This halves the frequency of the internally generated sine wave during AGC.
COT2: The STZC signal is output from COUT by setting D0 to 1.
(STZC: TZC signal generated by sampling the TE signal at 700kHz)

Description of Data Readout



Waveforms can be monitored with an oscilloscope using a serial input-type D/A converter as shown above.

§4-19. List of Servo Filter Coefficients

<Coefficient Preset Value Table (1)>

| ADDRESS | DATA | CONTENTS |
|---------|------|---|
| K00 | E0 | SLED INPUT GAIN |
| K01 | 81 | SLED LOW BOOST FILTER A-H |
| K02 | 23 | SLED LOW BOOST FILTER A-L |
| K03 | 7F | SLED LOW BOOST FILTER B-H |
| K04 | 6A | SLED LOW BOOST FILTER B-L |
| K05 | 10 | SLED OUTPUT GAIN |
| K06 | 14 | FOCUS INPUT GAIN |
| K07 | 30 | SLED AUTO GAIN |
| K08 | 7F | FOCUS HIGH CUT FILTER A |
| K09 | 46 | FOCUS HIGH CUT FILTER B |
| K0A | 81 | FOCUS LOW BOOST FILTER A-H |
| K0B | 1C | FOCUS LOW BOOST FILTER A-L |
| K0C | 7F | FOCUS LOW BOOST FILTER B-H |
| K0D | 58 | FOCUS LOW BOOST FILTER B-L |
| K0E | 82 | FOCUS PHASE COMPENSATE FILTER A |
| K0F | 7F | FOCUS DEFECT HOLD GAIN |
| K10 | 4E | FOCUS PHASE COMPENSATE FILTER B |
| K11 | 32 | FOCUS OUTPUT GAIN |
| K12 | 20 | ANTI SHOCK INPUT GAIN |
| K13 | 30 | FOCUS AUTO GAIN |
| K14 | 80 | HPTZC / Auto Gain HIGH PASS FILTER A |
| K15 | 77 | HPTZC / Auto Gain HIGH PASS FILTER B |
| K16 | 80 | ANTI SHOCK HIGH PASS FILTER A |
| K17 | 77 | HPTZC / Auto Gain LOW PASS FILTER B |
| K18 | 00 | Fix* |
| K19 | F1 | TRACKING INPUT GAIN |
| K1A | 7F | TRACKING HIGH CUT FILTER A |
| K1B | 3B | TRACKING HIGH CUT FILTER B |
| K1C | 81 | TRACKING LOW BOOST FILTER A-H |
| K1D | 44 | TRACKING LOW BOOST FILTER A-L |
| K1E | 7F | TRACKING LOW BOOST FILTER B-H |
| K1F | 5E | TRACKING LOW BOOST FILTER B-L |
| K20 | 82 | TRACKING PHASE COMPENSATE FILTER A |
| K21 | 44 | TRACKING PHASE COMPENSATE FILTER B |
| K22 | 18 | TRACKING OUTPUT GAIN |
| K23 | 30 | TRACKING AUTO GAIN |
| K24 | 7F | FOCUS GAIN DOWN HIGH CUT FILTER A |
| K25 | 46 | FOCUS GAIN DOWN HIGH CUT FILTER B |
| K26 | 81 | FOCUS GAIN DOWN LOW BOOST FILTER A-H |
| K27 | 3A | FOCUS GAIN DOWN LOW BOOST FILTER A-L |
| K28 | 7F | FOCUS GAIN DOWN LOW BOOST FILTER B-H |
| K29 | 66 | FOCUS GAIN DOWN LOW BOOST FILTER B-L |
| K2A | 82 | FOCUS GAIN DOWN PHASE COMPENSATE FILTER A |
| K2B | 44 | FOCUS GAIN DOWN DEFECT HOLD GAIN |
| K2C | 4E | FOCUS GAIN DOWN PHASE COMPENSATE FILTER B |
| K2D | 1B | FOCUS GAIN DOWN OUTPUT GAIN |
| K2E | 00 | NOT USED |
| K2F | 00 | NOT USED |

<Coefficient ROM Preset Value Table (2)>

| ADDRESS | DATA | CONTENTS |
|---------|------|--|
| K30 | 80 | Fix* |
| K31 | 66 | ANTI SHOCK LOW PASS FILTER B |
| K32 | 00 | NOT USED |
| K33 | 7F | ANTI SHOCK HIGH PASS FILTER B-H |
| K34 | 6E | ANTI SHOCK HIGH PASS FILTER B-L |
| K35 | 20 | ANTI SHOCK FILTER COMPARATE GAIN |
| K36 | 7F | TRACKING GAIN UP2 HIGH CUT FILTER A |
| K37 | 3B | TRACKING GAIN UP2 HIGH CUT FILTER B |
| K38 | 80 | TRACKING GAIN UP2 LOW BOOST FILTER A-H |
| K39 | 44 | TRACKING GAIN UP2 LOW BOOST FILTER A-L |
| K3A | 7F | TRACKING GAIN UP2 LOW BOOST FILTER B-H |
| K3B | 77 | TRACKING GAIN UP2 LOW BOOST FILTER B-L |
| K3C | 86 | TRACKING GAIN UP PHASE COMPENSATE FILTER A |
| K3D | 0D | TRACKING GAIN UP PHASE COMPENSATE FILTER B |
| K3E | 57 | TRACKING GAIN UP OUTPUT GAIN |
| K3F | 00 | NOT USED |
| K40 | 04 | TRACKING HOLD FILTER INPUT GAIN |
| K41 | 7F | TRACKING HOLD FILTER A-H |
| K42 | 7F | TRACKING HOLD FILTER A-L |
| K43 | 79 | TRACKING HOLD FILTER B-H |
| K44 | 17 | TRACKING HOLD FILTER B-L |
| K45 | 6D | TRACKING HOLD FILTER OUTPUT GAIN |
| K46 | 00 | NOT USED |
| K47 | 00 | NOT USED |
| K48 | 02 | FOCUS HOLD FILTER INPUT GAIN |
| K49 | 7F | FOCUS HOLD FILTER A-H |
| K4A | 7F | FOCUS HOLD FILTER A-L |
| K4B | 79 | FOCUS HOLD FILTER B-H |
| K4C | 17 | FOCUS HOLD FILTER B-L |
| K4D | 54 | FOCUS HOLD FILTER OUTPUT GAIN |
| K4E | 00 | NOT USED |
| K4F | 00 | NOT USED |

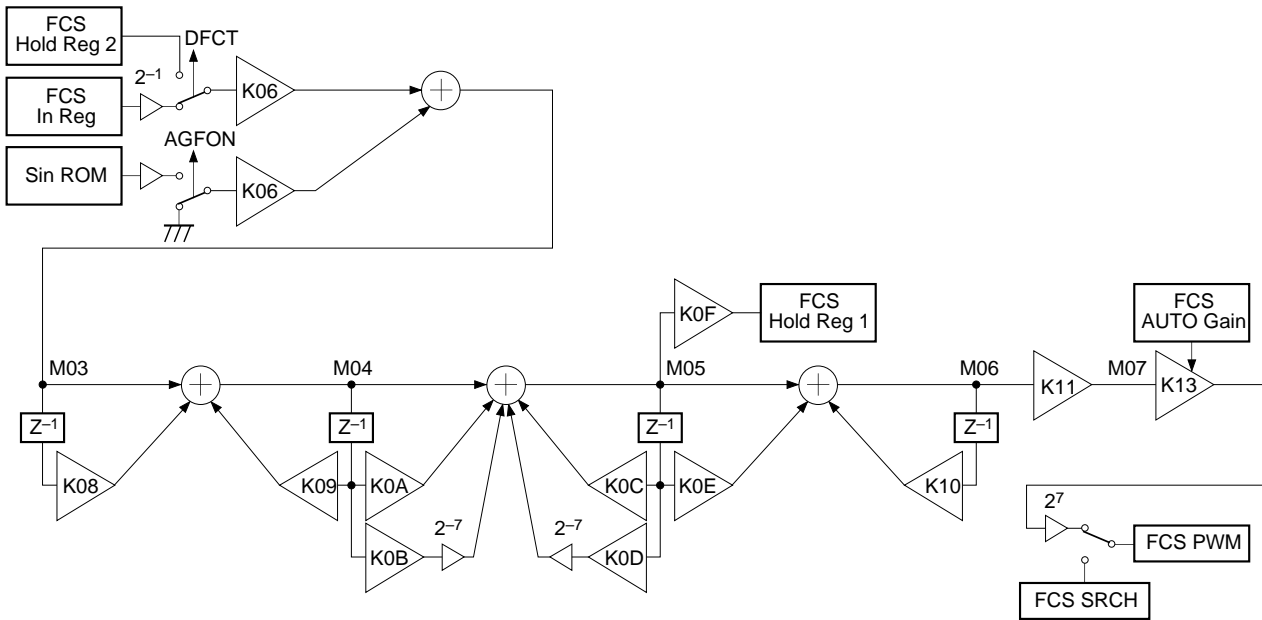
* Fix indicates that normal preset values should be used.

§4-20. FILTER Composition

The internal filter composition is shown below.

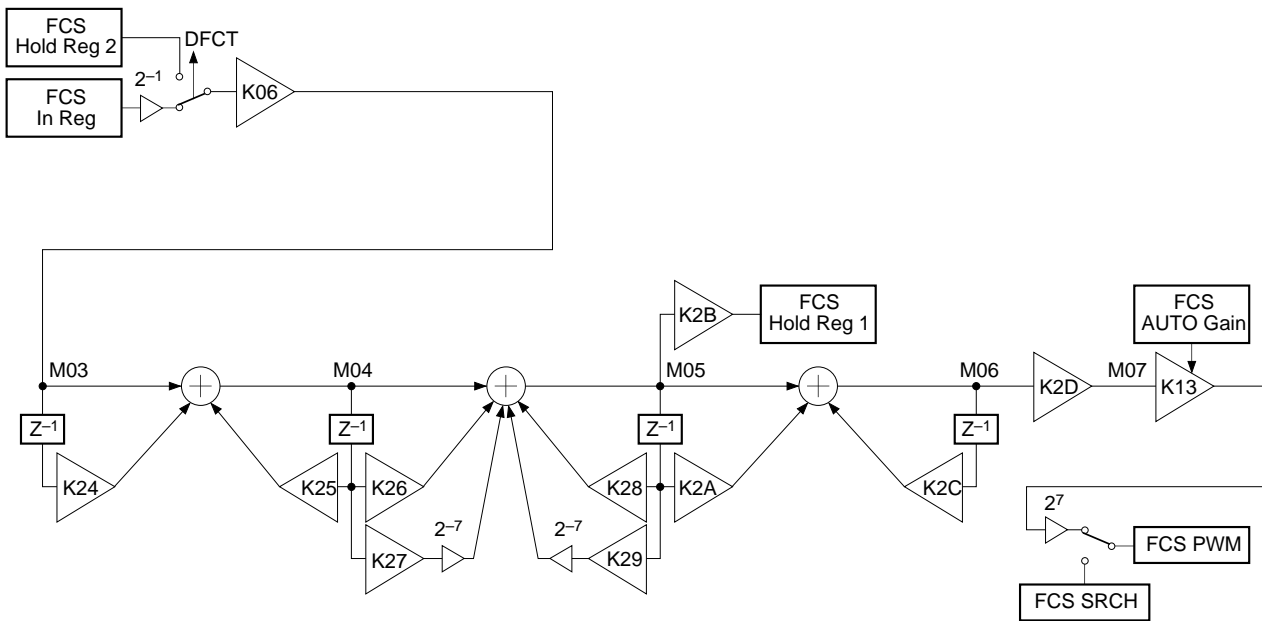
K ** and M ** indicate coefficient RAM and Data RAM address values respectively.

FCS Servo Gain Normal $f_s = 88.2\text{kHz}$



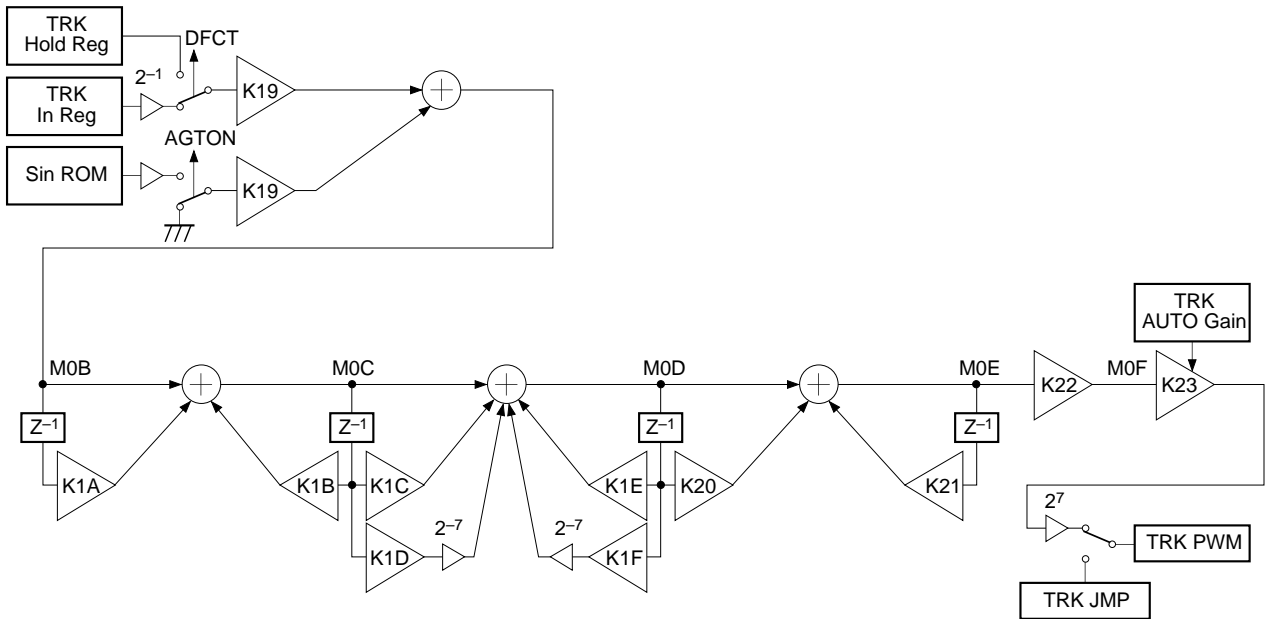
Note) Set the MSB bit of the K0B and K0D coefficients to 0.

FCS Servo Gain Down $f_s = 88.2\text{kHz}$



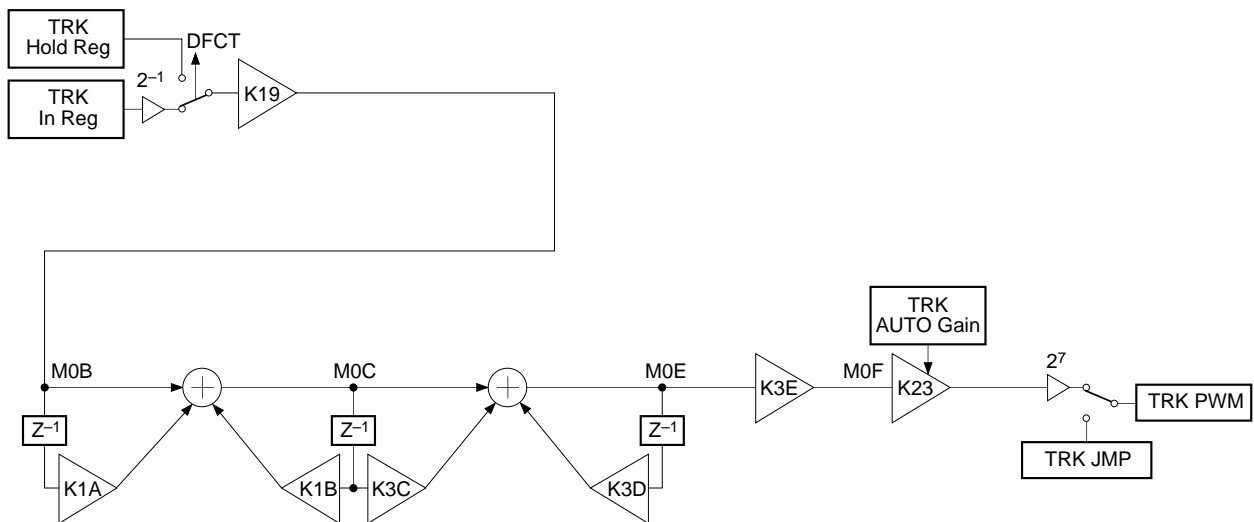
Note) Set the MSB bit of the K27 and K29 coefficients to 0.

TRK Servo Gain Normal $f_s = 88.2\text{kHz}$

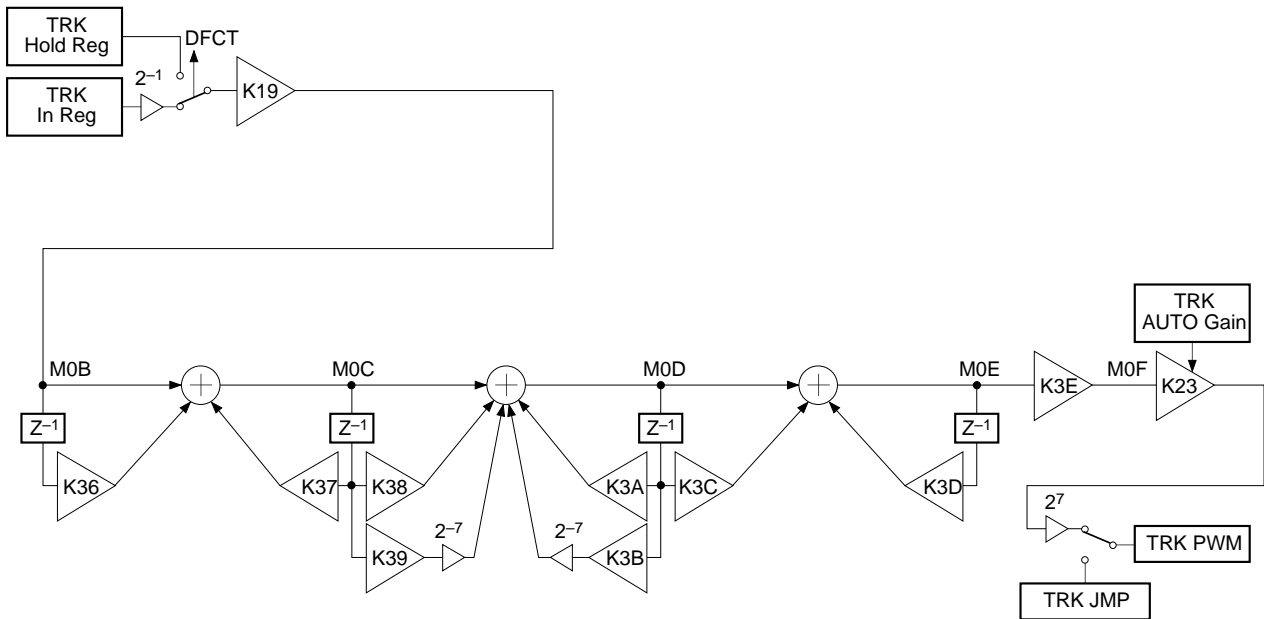


Note) Set the MSB bit of the K1D and K1F coefficients to 0.

TRK Servo Gain Up 1 $f_s = 88.2\text{kHz}$

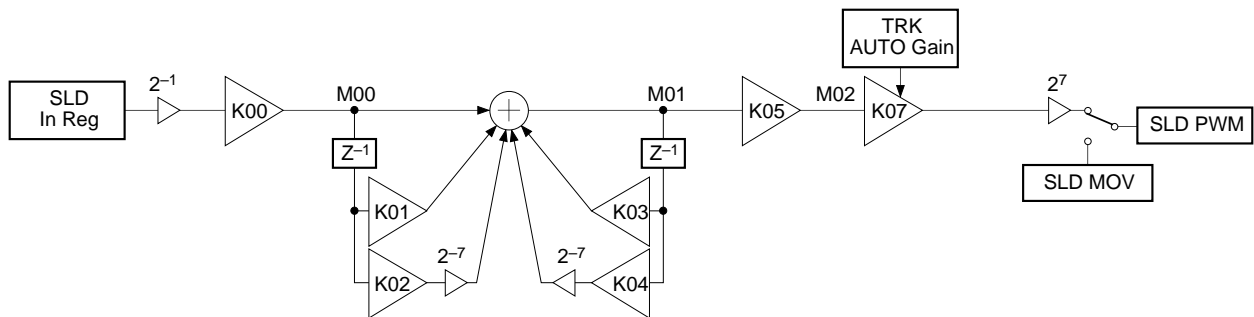


TRK Servo Gain Up 2 fs = 88.2kHz



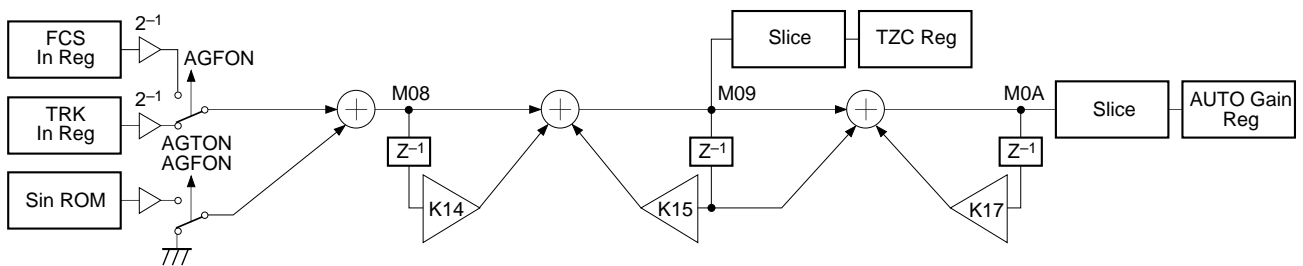
Note) Set the MSB bit of the K39 and K3B coefficients to 0.

SLD Servo fs = 345Hz

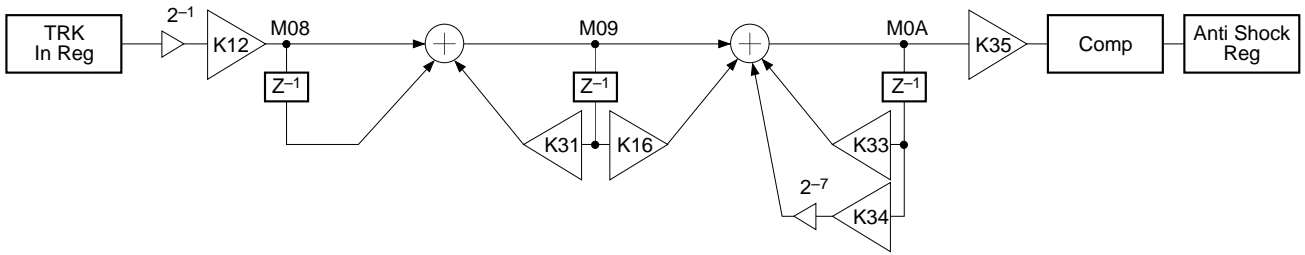


Note) Set the MSB bit of the K02 and K04 coefficients to 0.

HPTZC/Auto Gain fs = 88.2kHz

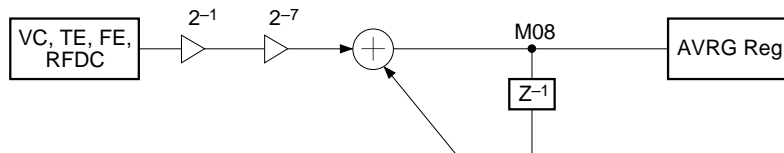


Anti Shock fs = 88.2kHz

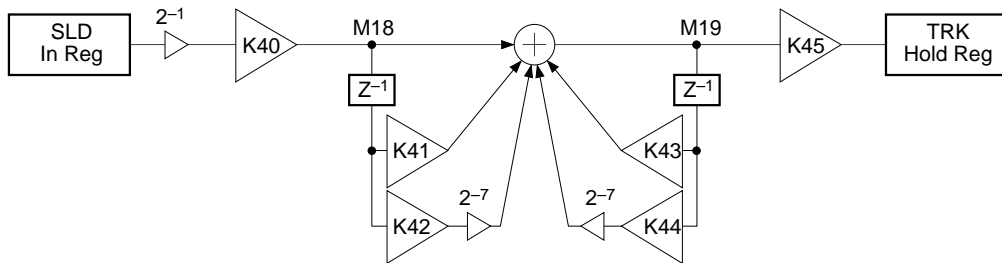


Note) Set the MSB bit of the K34 coefficient to 0.
The comparator level is 1/16 the maximum amplitude of the comparator input.

AVRG fs = 88.2kHz

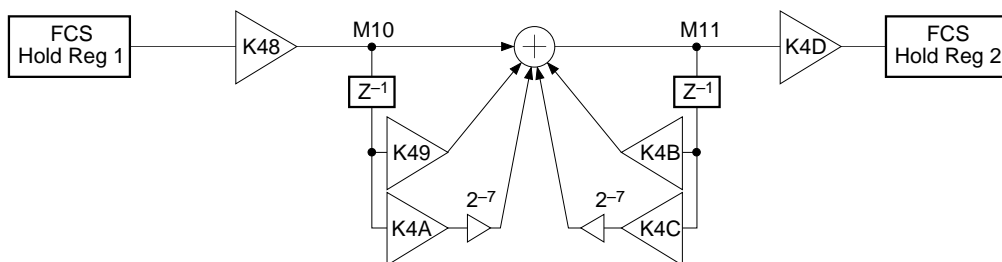


TRK Hold fs = 345Hz



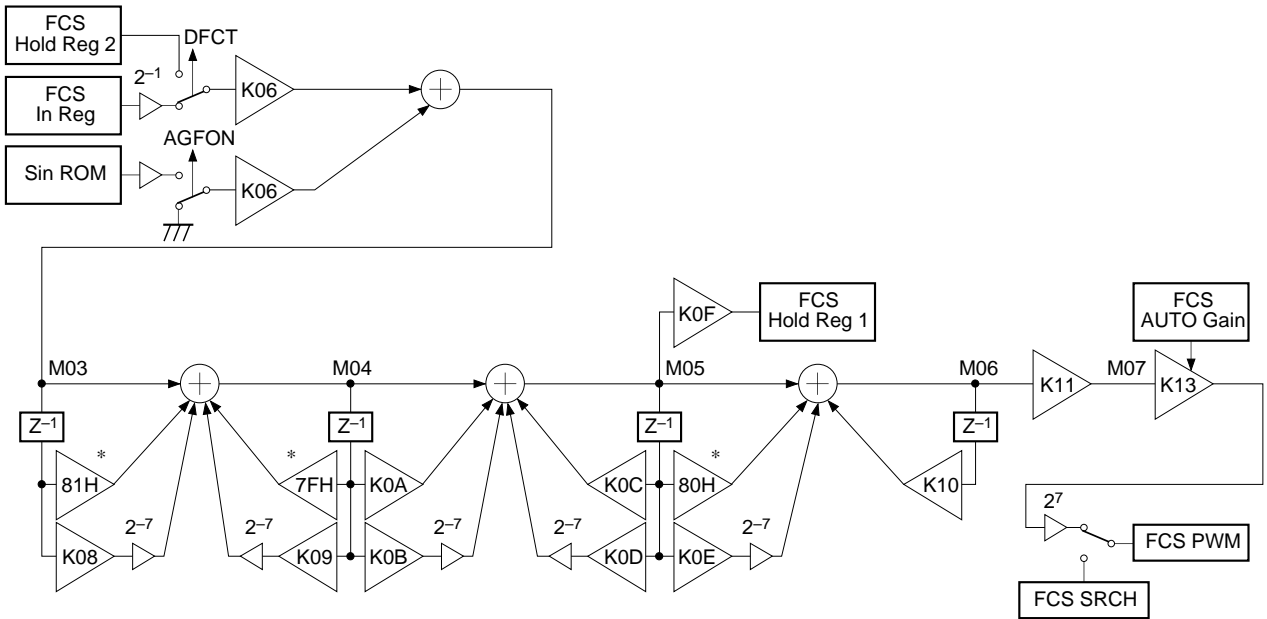
Note) Set the MSB bit of the K42 and K44 coefficients to 0.

FCS Hold fs = 345Hz



Note) Set the MSB bit of the K4A and K4C coefficients to 0.

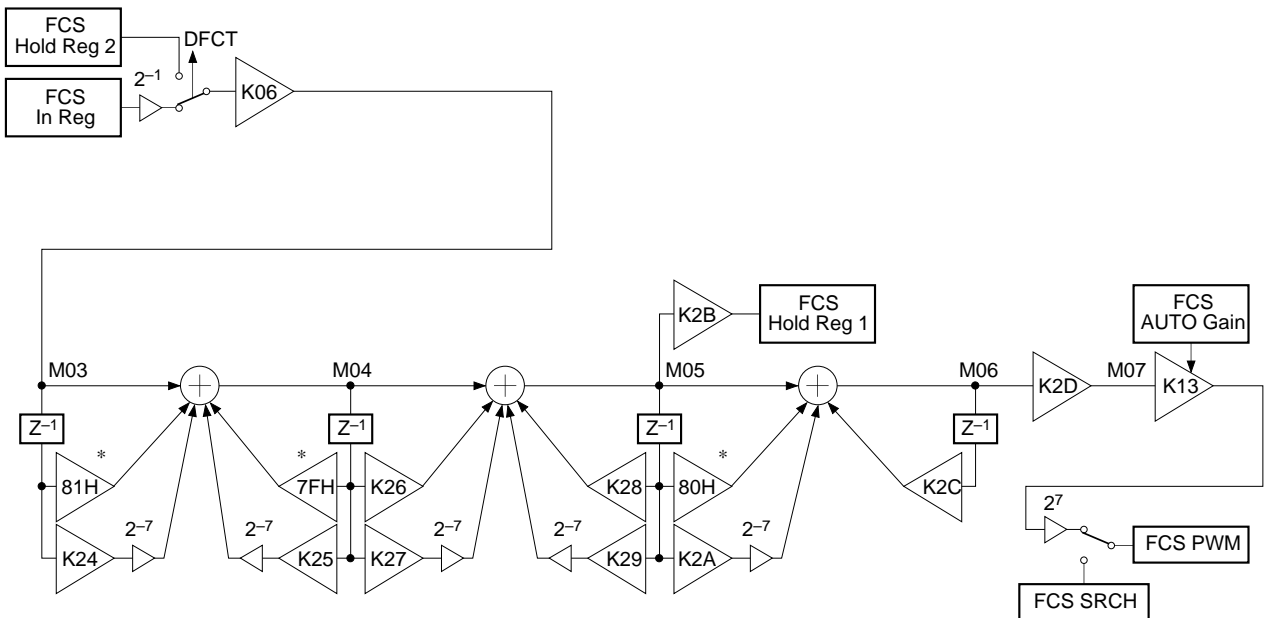
FCS Servo Gain Normal; fs = 88.2kHz, during quasi double accuracy (Ex.: \$3EAXX0)



* 81H, 7FH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.

Note) Set the MSB bit of the K0B and K0D coefficients during normal operation, and of the K08, K09 and K0E coefficients during quasi double accuracy to 0.

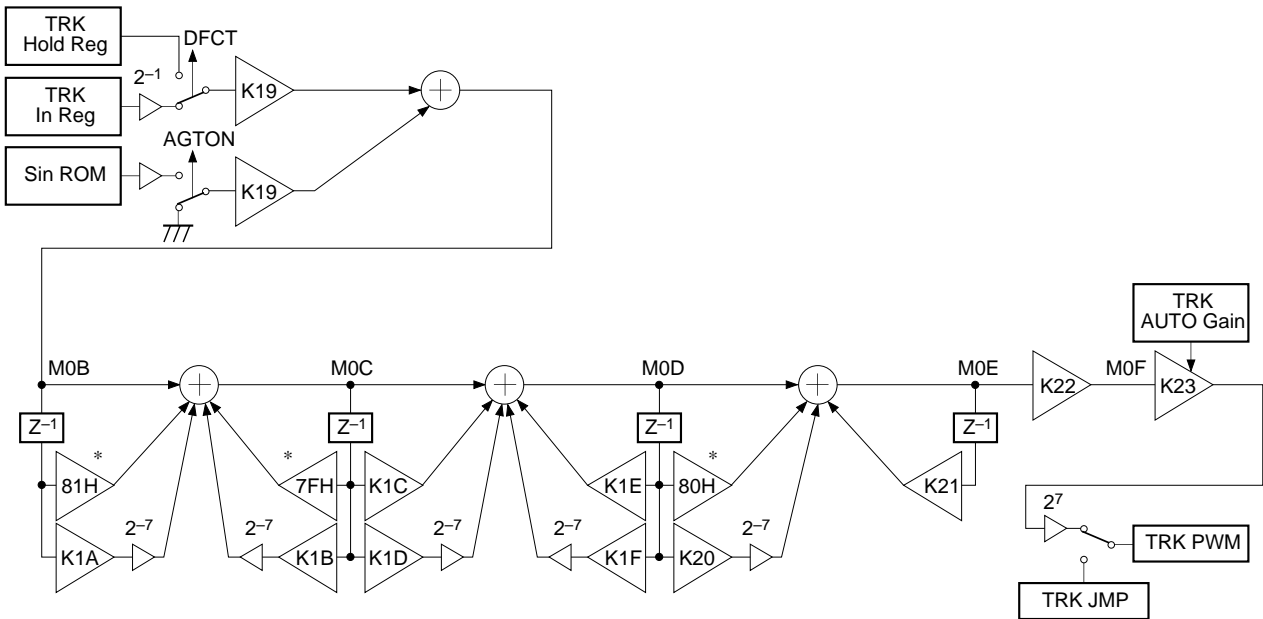
FCS Servo Gain Down; fs = 88.2kHz, during quasi double accuracy (Ex.: \$3E5XX0)



* 81H, 7FH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.

Note) Set the MSB bit of the K27 and K29 coefficients during normal operation, and of the K24, K25 and K2A coefficients during quasi double accuracy to 0.

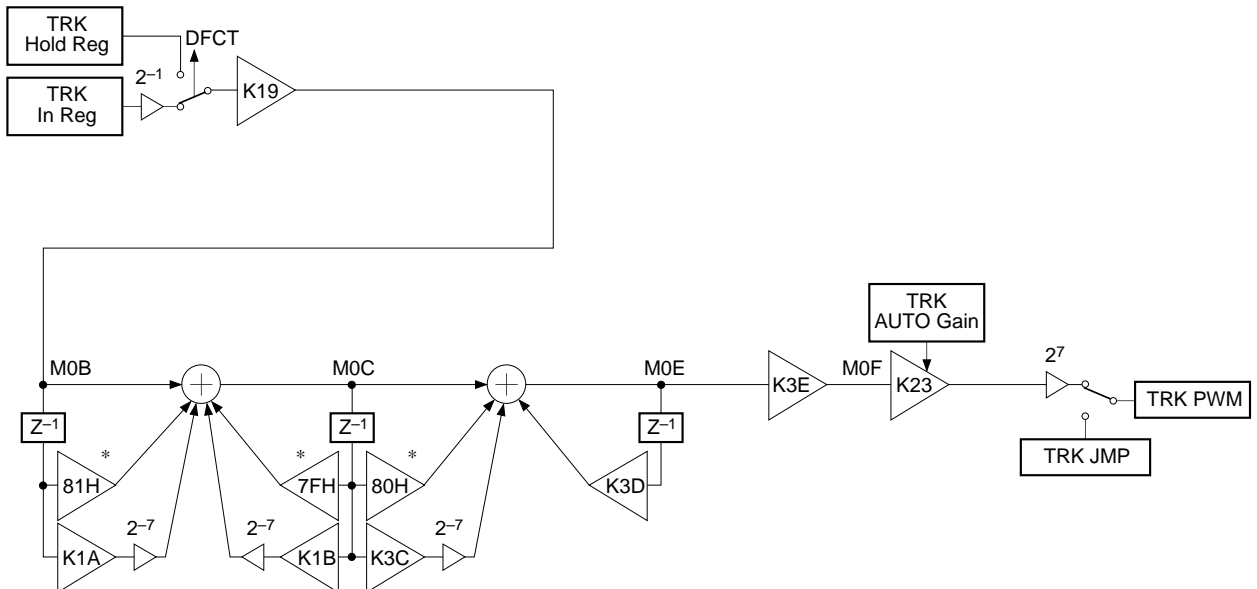
TRK Servo Gain Normal; $f_s = 88.2\text{kHz}$, during quasi double accuracy (Ex.: \$3EXAX0)



* 81H, 7FH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.

Note) Set the MSB bit of the K1D and K1F coefficients during normal operation, and of the K1A, K1B and K20 coefficients during quasi double accuracy to 0.

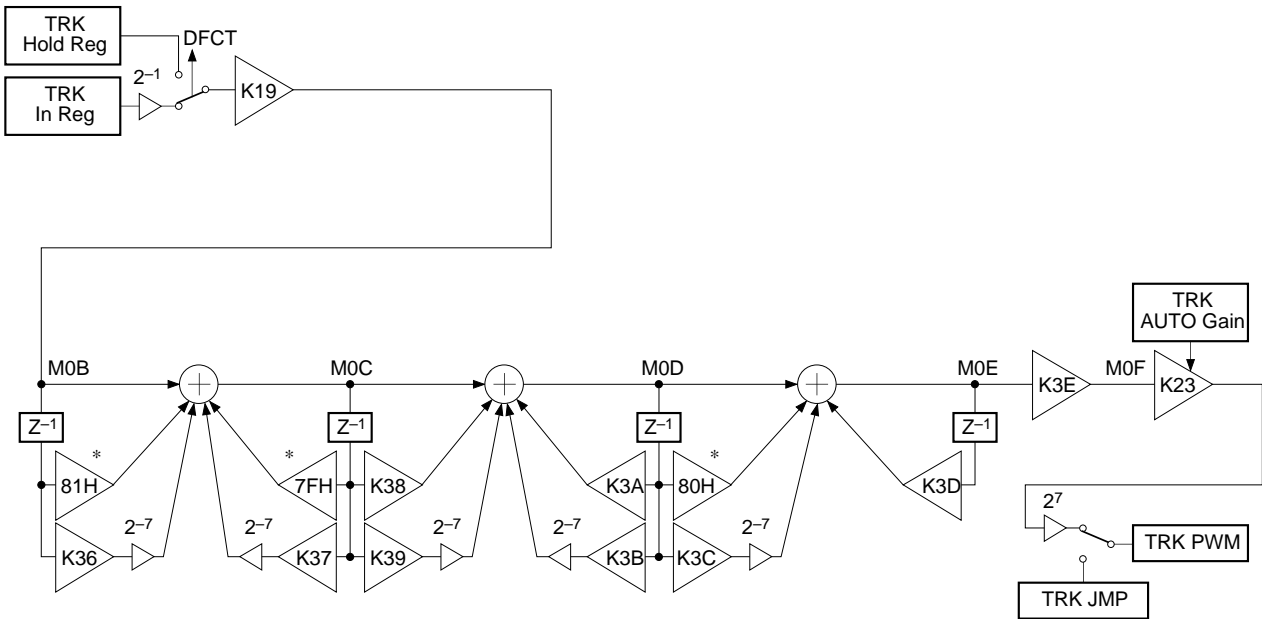
TRK Servo Gain up 1; $f_s = 88.2\text{kHz}$, during quasi double accuracy (Ex.: \$3EX5X0)



* 81H, 7FH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.

Note) Set the MSB bit of the K1A, K1B and K3C coefficients during quasi double accuracy to 0.

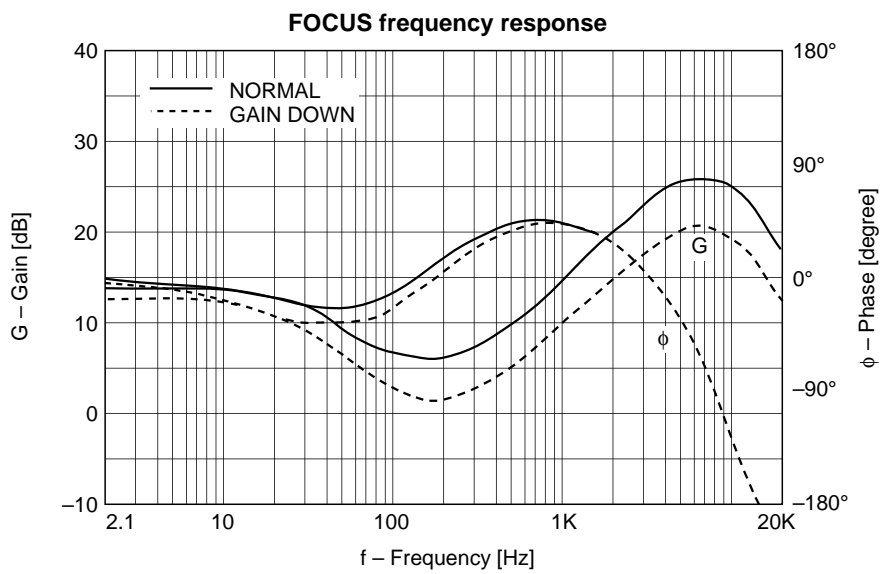
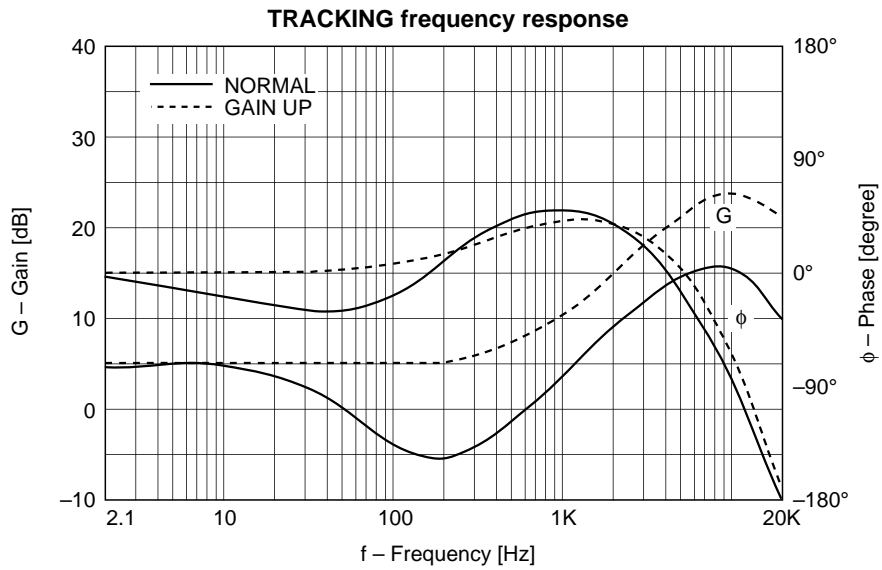
TRK Servo Gain up 2; fs = 88.2kHz, during quasi double accuracy (Ex.: \$3EX5X0)



* 81H, 7FH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.

Note) Set the MSB bit of the K39 and K3B coefficients during normal operation, and the K36, K37 and K3C coefficients during quasi double accuracy to 0.

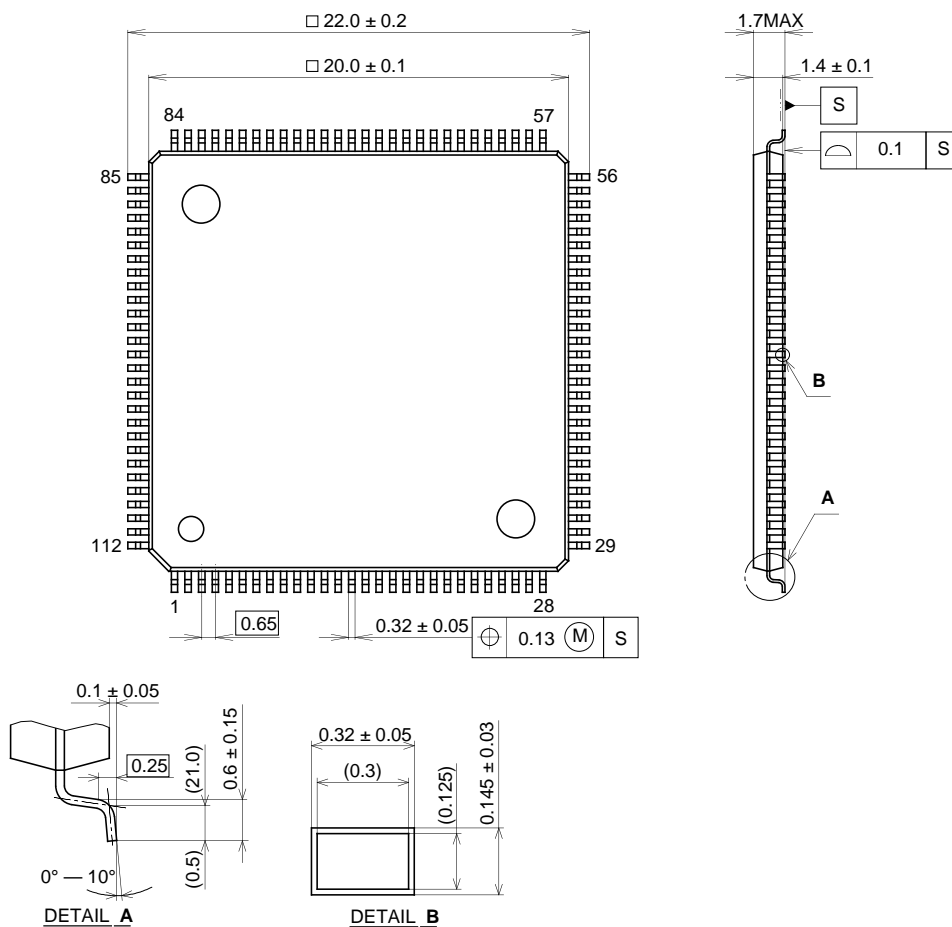
§4-21. TRACKING and FOCUS Frequency Response



Package Outline

Unit: mm

112PIN LQFP(PLASTIC)



| | |
|------------|----------------|
| SONY CODE | LQFP-112P-L01 |
| EIAJ CODE | LQFP112-P-2020 |
| JEDEC CODE | _____ |

PACKAGE STRUCTURE

| | |
|------------------|----------------|
| PACKAGE MATERIAL | EPOXY RESIN |
| LEAD TREATMENT | SOLDER PLATING |
| LEAD MATERIAL | COPPER ALLOY |
| PACKAGE WEIGHT | 1.3g |

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