SONY

CXD2053AM/AS

Auto Wide, EDTV-II ID Detection, ID-1 Detection

Description

The CXD2053AM/AS is an IC which has the three functions of identifying the wide video (auto wide), detecting the EDTV-II ID, and detecting ID-1 (EIAJ, CPX1024) from the video signal.

Features

- Video aspect ratio identification used with wide TVs is realized with a single chip.
- I^2C bus interface.
  This IC can also be used without the bus.
- For auto wide function, 525/60 (NTSC) and 625/50 (PAL, SECAM) can be Supported.

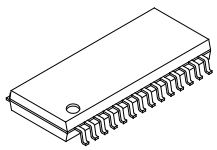
Applications

Wide TV

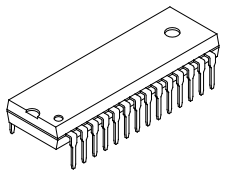
Structure

Silicon gate CMOS IC

CXD2053AM
28 pin SOP (Plastic)



CXD2053AS
28 pin SDIP (Plastic)



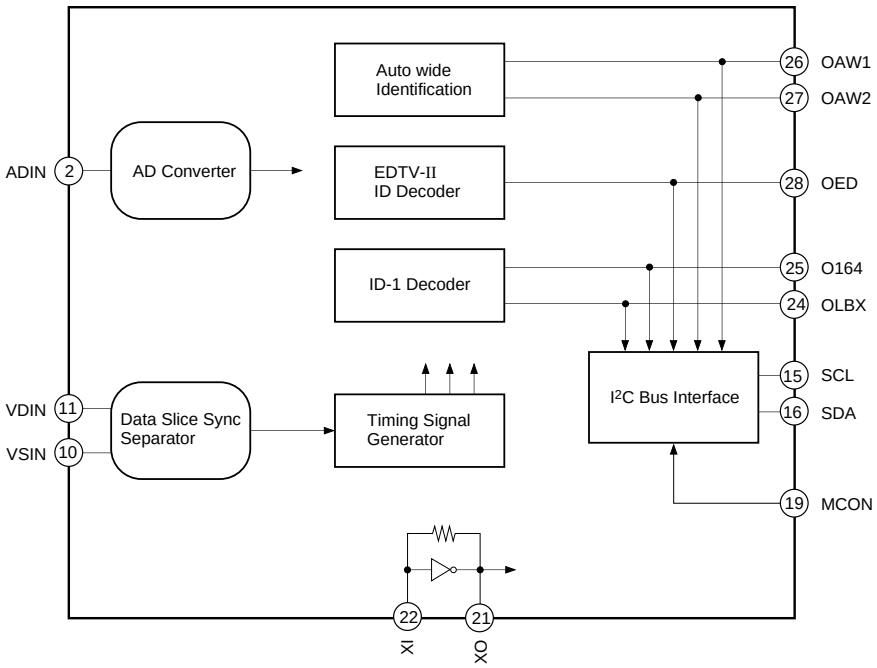
Absolute Maximum Ratings

• Supply voltage	V_{DD}	V_{SS} – 0.5 to +7.0	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Storage temperature			
	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature			
	Topr	–20 to +70	°C

Block Diagram



E96531-ST

Pin Description

Pin No.	Symbol	I/O	I/O level	Description
1	AV_{DD}		ANALOG	Analog power supply.
2	ADIN	I	ANALOG	AD converter input.
3	AV_{SS}		ANALOG	Analog ground.
4	CPV	I	ANALOG	Clamp voltage.
5	VRB	I	ANALOG	AD converter bottom voltage.
6	VRT	I	ANALOG	AD converter top voltage.
7	CCP	I	ANALOG	AD converter clamp integrating capacitor connection.
8	ISET	I	ANALOG	Bias current setting.
9	AV_{DD}			Analog power supply
10	VSIN	I	ANALOG	Sync separation input.
11	VDIN	I	ANALOG	Data slicer input.
12	AV_{SS}			Analog ground.
13	TST1	I	TTL*2	Test input; connect to V_{SS}.
14	TST2	I	TTL*2	Test input; connect to V_{SS}.
15	SCL [EDDEC2]	I	CMOS*1	I^2C bus clock [EDTV-II decoding identification switching]
16	SDA [ED2FSC]	I/O	CMOS*1, 3	I^2C bus data [EDTV-II 3.58 M check existence]
17	V_{SS}			Digital ground.
18	XRST	I	TTL*1	Reset at 0.
19	MCON	I	TTL	I^2C bus-free mode switching; 0 = I^2C-free.
20	V_{DD}			Digital system power supply.
21	XO	O	CMOS	Oscillator connection (14.318MHz).
22	XI	I	CMOS	Oscillator connection or clock input.
23	V_{SS}			Digital ground.
24	OLBX	O	CMOS	VB-ID detection output; 1 = letter-box, 0 = normal.
25	O164	O	CMOS	VB-ID detection output; 1 = full mode.
26	OAW1	O	CMOS	Auto wide identification output; 1 = wide video subtitles not present.
27	OAW2	O	CMOS	Auto wide identification output; 1 = wide video subtitles present.
28	OED	O	CMOS	EDTV-II ID bit 3 detection output.

*1 Schmitt input

*2 With pull-down resistor

*3 Open drain

Note) In I^2C-free mode when Pin 19 (MCON) = 0, Pins 15 and 16 switch to the functions in parentheses [ ].

Electrical Characteristics

DC Characteristics (Logic Section) (V_{DD} = 5.0V, V_{SS} = 0V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Output voltage	V_{OH}	I_{OH} = –2mA	V_{DD} – 0.8			V	Pins 24, 25, 26, 27 and 28
	V_{OL}	I_{OL} = 4mA			0.4	V	
Output voltage	V_{OH}	I_{OH} = –3mA	V_{DD}/2			V	Pin 21 only
	V_{OL}	I_{OL} = 3mA			V_{DD}/2	V	
Output voltage	V_{OL}	I_{OL} = 3mA			0.4	V	Pin 16 only
Input voltage	V_{IH}		2.2			V	Pins 13, 14, 18 and 19
	V_{IL}				0.8	V	
Input voltage	V_{IH}		0.7 × V_{DD}			V	Pin 22 only
	V_{IL}				0.3 × V_{DD}	V	
Input voltage	V_{IH}		0.8 × V_{DD}			V	Pins 15 and 16
	V_{IL}				0.2 × V_{DD}	V	
Input hysteresis width	Vhys		0.05 × V_{DD}			V	Pins 15 and 16
				0.4		V	Pin 18
Input leak current	Ii	V_{IN} = either V_{SS} or V_{DD}	–10		+10	µA	Except for Pins 13, 14 and 22
Output leak current	I_{OZ}	V_{IN} = eother V_{SS} or V_{DD}	–40		+40	µA	Pin 16 only
Input current	Ii	V_{IN} = V_{DD}	40	100	240	µA	Pins 13 and 14
Feedback resistor	Rfbk	XI (Pin 22) = either V_{DD} or V_{SS}	250k	1M	2.5M	Ω	Between Pins 21 and 22
Current consumption	I_{DD}	Clock 14.318MHz		29		mA	Sum of Pins 1, 9 and 20

AC Characteristics (V_{DD} = 5.0V, V_{SS} = 0V, Ta = 25°C)

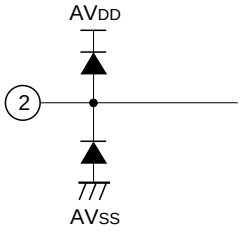
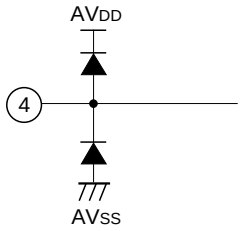
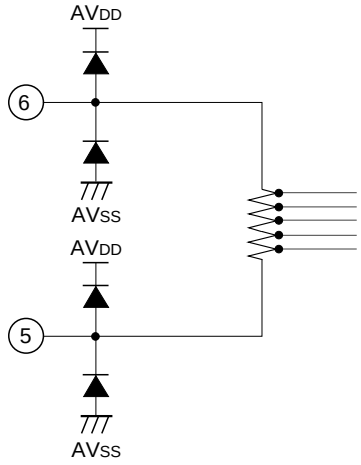
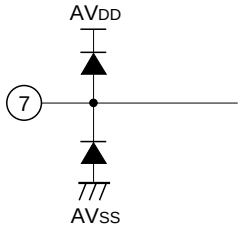
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Clock frequency	fxi			14.318		MHz	Pin 22 input, or oscillator between Pins 21 and 22

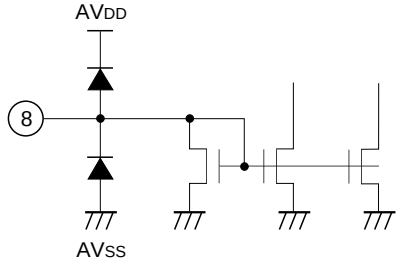
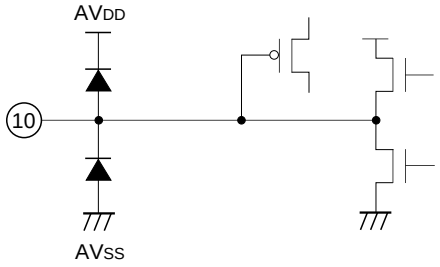
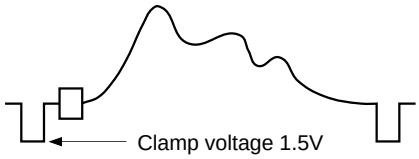
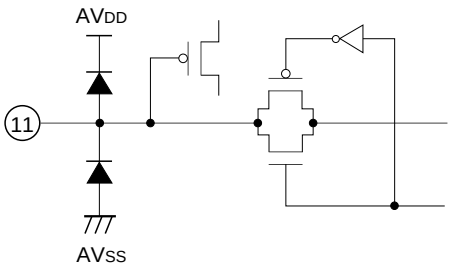
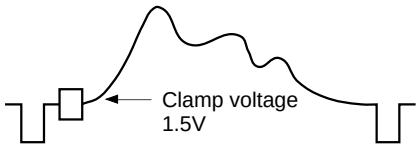
I/O Pin Capacitance

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Input pin capacitance	C_{IN}	V_{DD} = V_I = 0V, f = 1MHz			9	pF	
Output pin capacitance	C_{OUT}	V_{DD} = V_I = 0V, f = 1MHz			11	pF	
Input/output pin capacitance	$C_{I/O}$	V_{DD} = V_I = 0V, f = 1MHz			11	pF	

Pins and Electrical Characteristics

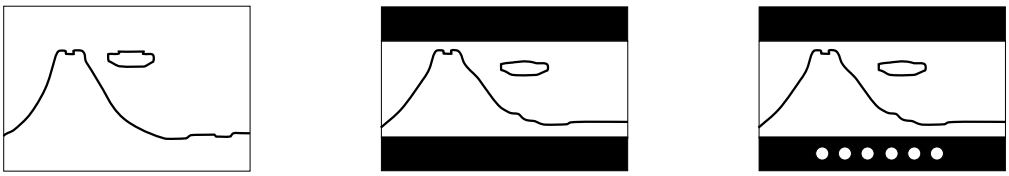
Analog Section (V_{DD} = 5.0V, V_{SS} = 0V, Ta = 25°C)

Pin No.	Symbol	Equivalent circuit	Description
1	AV_{DD}	Not connected to V_{DD} (Pin 20) or AV_{DD} (Pin 9) inside the IC.	AD converter analog power supply. Connect a low-noise power supply from the digital system.
3	AV_{SS}	Not connected to V_{SS} (Pins 17 and 23) or AV_{SS} (Pin 12) inside the IC.	AD converter analog ground. Connect to the same potential as other V_{SS} and AV_{SS}.
2	ADIN		AD converter input. This pin is pedestal clamped to the potential of CPV (Pin 4), so input the video signal with capacitor coupled.
4	CPV		ADIN (Pin 2) pedestal clamp voltage setting.
5	VRB		AD converter input range setting. The resistor between Pins 5 and 6 is 310Ω (Typ.).
6	VRT		
7	CCP		Clamp circuit integrating capacitor connection. Connect 0.022µF between this pin and AV_{SS} (Pin 3).

Pin No.	Symbol	Equivalent circuit	Description
9	AV_{DD}	Not connected to V_{DD} (Pin 20) or AV_{DD} (Pin 1) inside the IC.	Sync separation system analog power supply. Connect a low-noise power supply from the digital system.
12	AV_{SS}	Not connected to AV_{SS} (Pin 3) or V_{SS} (Pins 17 and 23) inside the IC.	Sync separation system analog ground. Connect to the same potential as other V_{SS} and AV_{SS}.
8	ISET		Bias setting. Connect to AV_{DD} (Pin 9) with 33kΩ.
10	VSIN		Chip clamp, sync separation input. Input with capacitor coupled. 
11	VDIN		Pedestal clamp, ID-1 data slicer input. Input with capacitor coupled. 

1. Description of auto wide function

The auto wide function performs wide screen identification from the black bands at the top and bottom of the screen. As shown below, the CXD2053AM/AS identifies the three types of 4:3 normal video, 16:9 wide video, and wide video with subtitles.



4:3 normal video　　16:9 wide video　　Wide video with subtitles

Fig. 1. Wide identification types

The results of this auto wide identification are expressed by 2 bits, and are output through the I^2C bus during bus mode. Also, these results are output directly to the OAW1 (Pin 26) and OAW2 (Pin 27) pins regardless of bus or bus-free mode.

Auto wide identification is provided with a transition time of about 1 to 15 seconds to prevent misoperation. During I^2C bus mode, wide identification can be changed quickly without this transition time by manipulating the INST bit.

2. Description of ID-1 (transmitter method of additional video information, aspect ratio identification)

As shown in the table below, the additional video information consists of 14-bit data, to which a 6-bit CRCC is appended for a total of 20 bits. On an NTSC video signal, this information is carried on lines 20 and 283 of the vertical blanking interval.

		bit-No	Description		
				"1"	"0"
WORD0	A	1 2 3	Transmitter aspect ratio Pictorial representation format Undefined	Full mode (16:9) Letter-box	4:3 Normal
	B	4 5 6	Discrimination information about the video signal and any other signal (audio signal, etc.) incident to the video and transmitted simultaneously.		
WORD1		4-bit width	Word 0 dependent discrimination signal		
WORD2		4-bit width	Word 0 dependent discrimination signal, information, etc.		

(From the Provisional Standard of EIAJ, CPX-1204)

Table 1. Description of ID-1 signal

Of the 14-bit data noted above, only the first 2 bits are handled by the CXD2053AM/AS. These 2 bits are obtained by the I^2C bus during bus mode. Also, these bits are output directly to the OLBX (Pin 24) and O164 (Pin 25) regardless of bus or bus-free mode.

3. Description of EDTV-II ID

As shown in the table below, EDTV-II ID consists of 27-bit data. On an NTSC video signal, this information is carried on lines 22 and 285 of the vertical blanking interval.

Bit No.	Description	0	1	Bit No.	Description	0	1
1	Reference signal	—	1	15	Undefined	—	—
2	Reference signal	0	—	16	Undefined	—	—
3	Letter-box	Full line	Letter-box	17	Undefined	—	—
4	Parity of bits 3 and 5	0	1	18	Error correction signal		
5	Undefined	0	—	19	Error correction signal		
6	Field No.	1	2	20	Error correction signal		
7	Multiphase	A	B	21	Error correction signal		
8	VT	No	Yes	22	Error correction signal		
9	VH	No	Yes	23	Error correction signal		
10	HH	No	Yes	24	0	0	—
11	HH precombing	No	Yes	25	Confirmation sine wave		
12	Broadcasting station operation bit			26	Confirmation sine wave		
13	Broadcasting station operation bit			27	Confirmation sine wave		
14	Broadcasting station operation bit						

Table 2. Description of EDTV-II ID (discrimination control signal) signal

Of the 27 bits noted above, the CXD2053AM/AS outputs only bits 3 and 5. These 2 bits are obtained by the I^2C bus during bus mode. Also, bit 3 only is output directly to the OED (Pin 28) regardless of bus or bus-free mode. Since the CXD2053AM/AS does not perform decode processing for bits 6 to 23, this results in simple identification which does not use the error correction signals.

4. Clock

The CXD2053AM/AS requires a 4fsc clock (14.318MHz). Connect XI (Pin 22) and XO (Pin 21) when using a crystal oscillator.
When inputting the clock from an external source, input to XI (Pin 22).
Clock is 14.318MHz regardless of switching auto wide 525/60 (NTSC) or 625/50 (PAL, SECAM).

5. Settings and data input/output

The CXD2053AM/AS settings and data input/output can be performed by direct setting by pins or with the I^2C bus interface.

5-1. I²C bus

Settings and data can be taken out via the I²C bus when MCON (Pin 19) is set to "1".

This LSI supports the I²C bus slave RECEIVER and slave TRANSMITTER modes. The slave address is 1C (H). Also, in addition to standard mode (Max. 100K bit/s), this LSI also supports high-speed mode (Max. 400K bit/s).

Even when the IC power supply falls to 0V, it does not occupy the bus. However, the Absolute Maximum Ratings should be strictly observed.

The I²C bus transfer sequence is shown in the figure below.
The amount of data transferred by this IC is 2 bytes for the write (RECEIVER) side and 1 byte for the readout (TRANSMITTER) side.

Data write (RECEIVER mode)

	7654321	0	1	76543210	1	76543210	1	
Sm	SLAm	Wm	As	DATAm	As	DATAm	As	P

Data readout (TRANSMITTER mode)

	7654321	0	1	76543210	1	
Sm	SLAm	Rm	As	DATAs	XAm	P

Symbol	Description
*m	from master to slave
*s	from slave to master
S	Start Condition
P	Stop Condition
SLA	Slave Address
DATA	Data
W	0: Write Master→ Slave
R	1: Read Slave → Master
A	Clock pulse for Acknowledgement (SDA: L)
XA	Acknowledgement none (SDA: H)

R/W		Bit	Name	Description
WR	1st byte	bit 7 MSB	ED2FSC	0 when checking the 3.58MHz amplitude during EDTV-II ID decoding; 1 when not checking the amplitude.
		bit 6	ED2RES	EDTV-II ID decoding function reset. 1 = reset.
		bit 5 bit 4	EDDEC1	EDTV-II ID decoding function detection switching. Standard values: bit 5 = 0, bit 4 = 1.
		bit 3 bit 2	EDDEC2	EDTV-II ID decoding function detection switching. Standard values: bit 3 = 0, bit 2 = 1.
		bit 1	VBLNJ1	Decoding not only of line 20 but also of the 1 line before and after line 20 by the ID-1 decoding function. 0 = yes, 1 = line 20 only.
		bit 0 LSB	VBRES	ID-1 decoding function reset. 1 = reset.
	2nd byte	bit 7 MSB	AWRES	Auto wide function reset. 1 = reset to 4:3.
		bit 6	INST	Auto wide switching is performed without the wait time by changing INST from 0 to 1.
		bit 5 bit 4 bit 3 bit 2	No Use and TEST	Not used and LSI test bits. Be sure to set all bits to 0.
		bit 1	UPAREA	Normally. Set the same value as that of PAL bit below. When PAL = 0, UPAREA = 0, etc.
		bit 0 LSB	PAL	Auto wide function switching. 525/60 when PAL = 0 and 625/50 when PAL = 1.
RD	1st byte	bit 7 MSB	ED2ID	EDTV-II ID decoding results. 3rd bit of the EDTV-II ID.
		bit 6		EDTV-II ID decoding results. 5th bit of the EDTV-II ID.
		bit 5	EDVLD	EDTV-II ID decoding results judgment. Becomes 1 when a valid EDTV-II ID exists. The above noted ED2ID is output and held regardless of this judgment.
		bit 4	VBID	ID-1 decoding results. 1st bit: full mode bit.
		bit 3		ID-1 decoding results. 2nd bit: letter-box bit.
		bit 2	VBVLD	VB-ID decoding results judgment. Becomes 1 when a valid VB-ID exists. The above noted VB-ID is output and held regardless of this judgment.
		bit 1	AWS	Auto wide identification results. For 4:3 video, bit 1 = 0 and bit 0 = 0. For 16:9 wide video, bit 1 = 0 and bit 0 = 1. For subtitle video, bit 1 = 1 and bit 0 = 0.
		bit 0 LSB		

Table 3. List of I^2C bus controls

5-2. Bus-free mode

The CXD2053AM/AS can be operated without using the I²C bus when Pin 19 (MCON) is set to 0 and the IC is switched to bus-free mode.

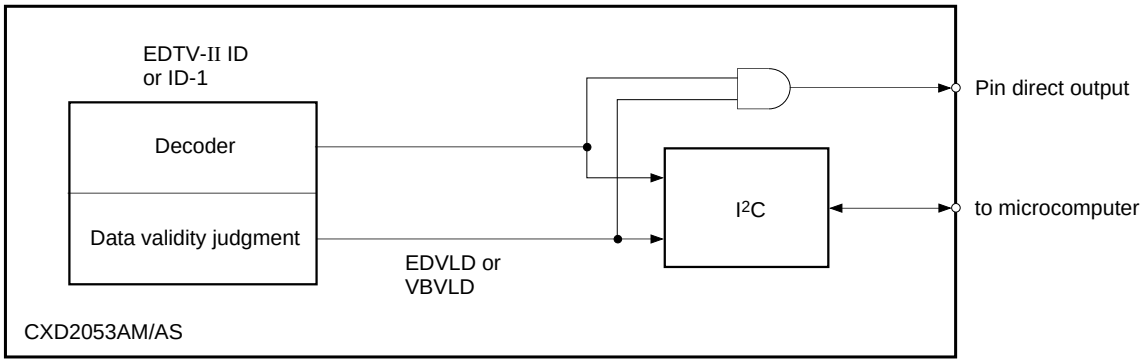
In this case, the contents normally set by the I²C are fixed to the values below.

Also, only the two functions listed in the table below can be switched by Pins 15 (SCL) and 16 (SDA).

		Bit	Name	Description
I²C setting information	1st byte	bit 7 MSB	ED2FSC	Directly controlled by Pin 16 (SDA). The unmodified SDA pin level becomes ED2FSC.
		bit 6	ED2RES	ED2RES = 0
		bit 5 bit 4	EDDEC1	bit5 = 0, bit4 = 1.
		bit 3 bit 2	EDDEC2	Directly controlled by Pin 15 (SCL). When SCL = 0, bit 3 = 0 and bit 2 = 1. When SCL = 1, bit 3 = 1 and bit 2 = 0.
		bit 1	VBLNJ1	VBLNJ1 = 0
		bit 0 LSB	VBRES	VBRES = 0
	2nd byte	bit 7 MSB	AWRES	AWRES = 0
		bit 6	INST	INST = 0
		bit 5 bit 4 bit 3 bit 2	No Use and TEST	All 0
		bit 1	UPAREA	UPAREA = 0
		bit 0 LSB	PAL	PAL = 0 Fixed to 525/60 mode.

Table 4. Setting values during bus-free mode (Pin 19 (MCON) = 0)

6. Processing of EDTV-II ID and ID-1 data from the bus



As shown in the figure above, the data validity judgment and decoding results are obtained independently during EDTV-II ID or ID-1 decoding. When outputting these results directly to pins, the results are output after first taking their logical product (AND). These results are output independently to the I²C bus.
Therefore, processing inside the microcomputer which has acquired the information from the I²C is performed either by simply outputting this data directly to the pins or by taking the logical product (AND) as above.
In addition, performing the processing when the data validity judgment result (EDVLD or VBVLD) is 1 and the decoding result is 0 allows video to be judged as 4:3 video. Even video which has had the top and bottom of the screen blacked out due to picture composition intentions can be viewed as the original 4:3 video by giving this judgment priority over the auto wide function.

7. Setting EDTV-II ID decoding function

The performance of the EDTV-II ID decoding function can be switched directly by pin settings during either I²C bus or bus-free mode.

Setting				
	I²C exists	ED2FSC = 0 EDDEC2 bit3 = 0, bit2 = 1	ED2FSC = 0 EDDEC2 bit3 = 1, bit2 = 0	ED2FSC = 1 EDDEC2 bit3 = 1, bit2 = 0
	I²C -free	SCL (15pin) = Low SDA (16pin) = Low	SCL (15pin) = High SDA (16pin) = Low	SCL (15pin) = High SDA (15pin) = High
Resistance to ghosting		Medium	Strong	Strong
Resistance to weak electric fields		Medium	Medium	Strong

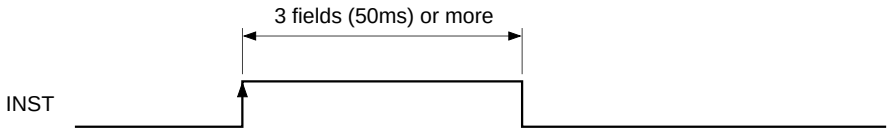
Table 5. EDTV-II ID decoding function switching

ED2FSC is originally a function which stops the 3.58MHz amplitude check for the Y signal input from the S terminal, etc. However, it can also be used in combination with the EDDEC2 setting to increase the resistance to ghosting and weak electric fields as shown in the table above. EDDEC2 is the luminance check level switching during the 3.58MHz or 2.04MHz confirmation signal interval.
Similarly, although EDDEC1 is the 2.04MHz amplitude check level switching, it should be set to bit 5 = 0 and bit 4 = 1.
Since EDTV-II ID identification for this IC is simple identification, increasing the resistance to weak electric fields, etc. results in a tradeoff which increases the possibility of misoperation. Accordingly, the leftmost settings in the table above should be used as the standard settings, and other settings used only when necessary.

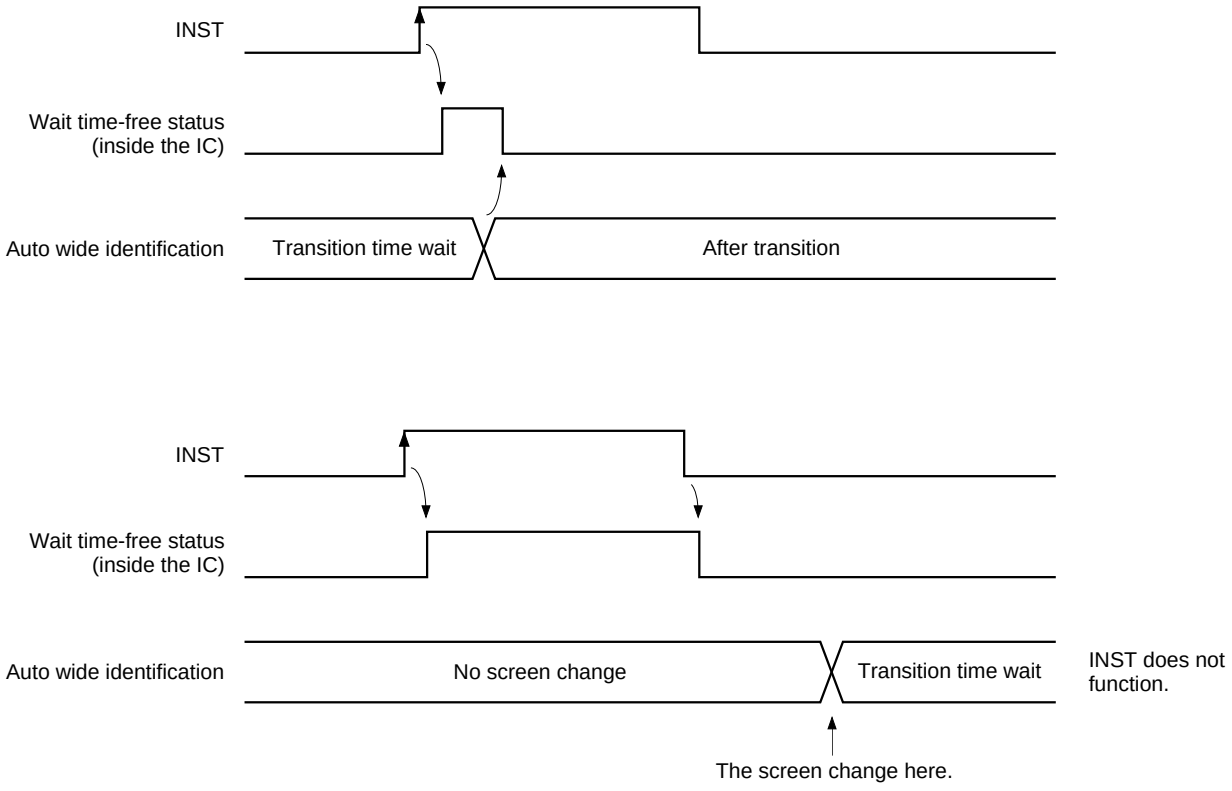
8. Judgment time during auto wide and shortening this time

An appropriate judgment transition wait time is provided during auto wide in order to prevent misjudgments. During I^2C bus mode, this transition time can be shortened as necessary using the INST bit.

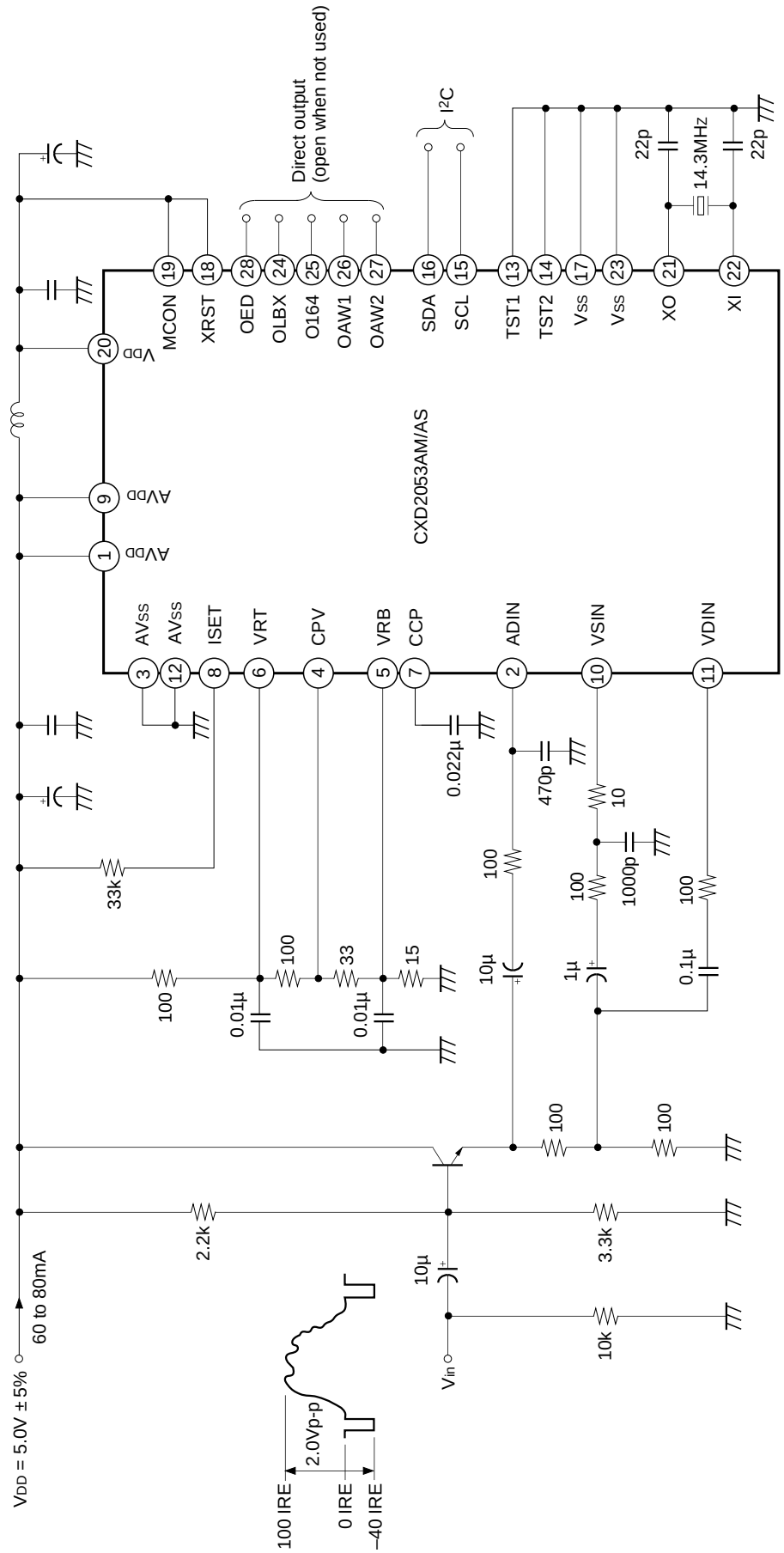
At the rising edge of INST, the screen changes without waiting to the screen being judged at that time.
The INST pulse width should be set to 3 fields or more as shown below.



The wait time-free status ends with the auto wide judgment transition or when INST becomes 0. This situation is illustrated in the figure below.



Application Circuit

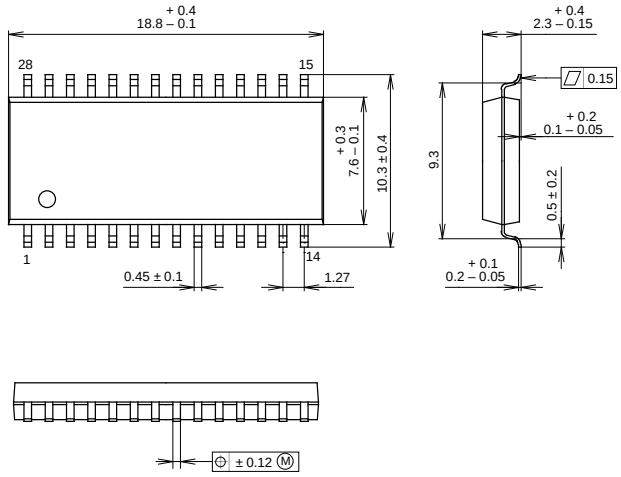


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

CXD2053AM

28PIN SOP (PLASTIC) 375mil



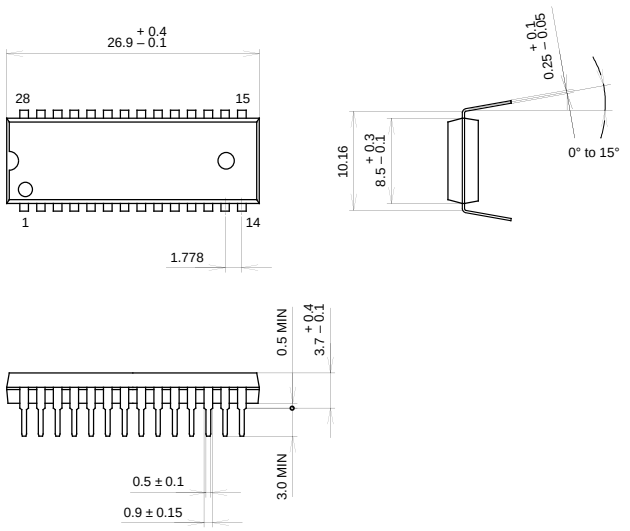
PACKAGE STRUCTURE

SONY CODE	SOP-28P-L04
EIAJ CODE	*SOP028-P-0375-D
JEDEC CODE	————————

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.7g

CXD2053AS

28PIN SDIP (PLASTIC) 400mil



PACKAGE STRUCTURE

SONY CODE	SDIP-28P-01
EIAJ CODE	SDIP028-P-0400-A
JEDEC CODE	————————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.7g

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