

## Digital Video Encoder

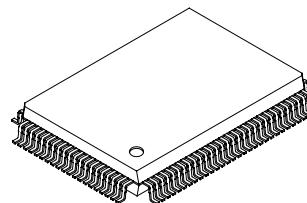
### Description

The CXD1914Q is a digital video encoder designed for DVDs, set top boxes, digital VCRs and other digital video equipment. This device accepts ITU-R601 compatible Y, Cb and Cr data, and the data are encoded to composite video and separate Y/C video (S-video) signals and converted to RGB/YUV signals.

### Features

- NTSC and PAL encoding modes
- Composite video and separate Y/C video (S-video) signal output
- R, G, B/Y, U and V (BetaCam/SMPTE level) signal output
- 8/16-bit pixel data input modes
- 13.5 Mpps pixel rate
- 10-bit 6-channel DAC
- Supports I<sup>2</sup>C bus (400 kHz) and Sony SIO
- Closed Caption (Line 21, Line 284) encoding
- Macrovision Pay-Per-View copy protection system : NTSC Rev. 7.0, PAL Rev. 6.1 (Note 1)
- VBI encoding
- WSS encoding
- Supports non-interlace mode
- Monolithic CMOS single 5.0 V power supply
- 100-pin plastic QFP

100 pin QFP (Plastic)



### Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	V <sub>DD</sub>	-0.3 to +7.0	V
• Input voltage	V <sub>I</sub>	-0.3 to +7.0	V
• Output voltage	V <sub>O</sub>	-0.3 to +7.0	V
• Operating temperature	T <sub>opr</sub>	-20 to +75	°C
• Storage temperature	T <sub>stg</sub>	-40 to +125	°C

(V<sub>SS</sub>=0 V)

### Recommended Operating Conditions

• Supply voltage	V <sub>DD</sub>	4.75 to 5.25	V
• Input voltage	V <sub>IN</sub>	V <sub>SS</sub> to V <sub>DD</sub>	V
• Operating temperature	T <sub>opr</sub>	0 to +70	°C

### I/O Pin Capacitance

• Input pin	C <sub>I</sub>	11 (Max.)	pF
• Output pin	C <sub>O</sub>	11 (Max.)	pF

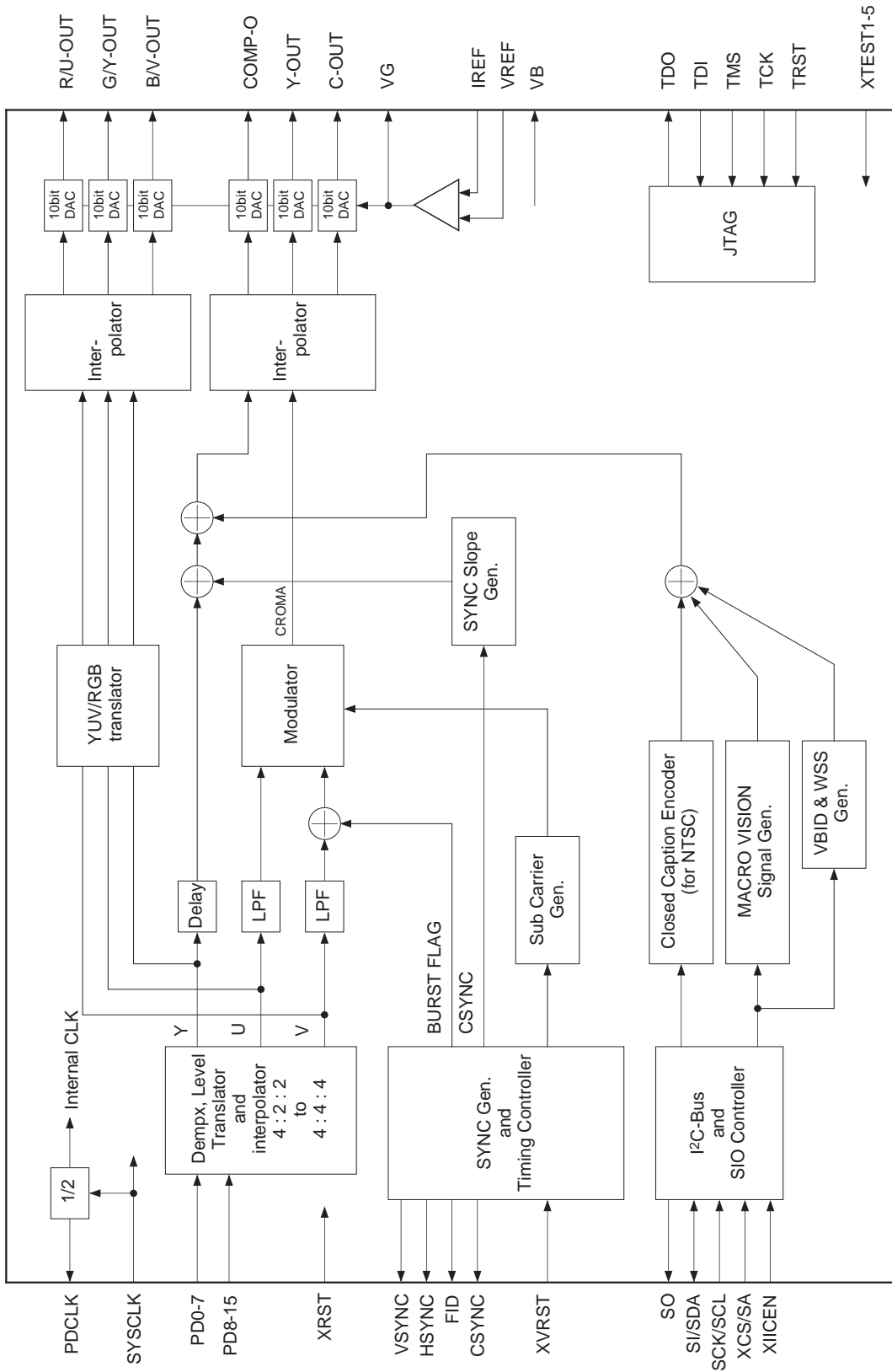
**Note)** Test conditions : V<sub>DD</sub>=V<sub>I</sub>=0 V, f<sub>M</sub>=1 MHz

### (Note 1)

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Block Diagram



## Pin Description

Pin No.	Symbol	I/O	Description
1	F1	I	Field ID input. This signal indicates the field ID when resetting the vertical sync. “H” indicates 1st field. “L” indicates 2nd field.
2	TVSYNC	I	Test pin. Set “L”.
3	OSDSW	I	Test pin. Set “L”.
4	ROSD	I	Test pin. Set “L”.
5	GOSD	I	Test pin. Set “L”.
6	BOSD	I	Test pin. Set “L”.
7	XVRST	I	Vertical sync reset input in active low. This pin is pulled up. This is used for synchronizing the phases of the external and internal vertical sync signals. When XVRST = “L”, the internal digital sync generator is reset according to the F1 status.
8	SYSCLK	I	System clock input. To generate the correct subcarrier frequency, precise 27 MHz is required.
9	Vss1	—	Digital ground.
10	XRST	I	System reset input in active low. Set “L” for 40 clocks (SYSCLK) or more during power-on reset.
11	PDCLK	O	Pixel data clock signal output for 13.5 MHz. A 13.5 MHz signal frequency divided from the system clock (SYSCLK) is output and used as the clock signal when 16-bit pixel data is input.
12	VDD1	—	Digital power supply.
13	NC	—	Not connected inside the IC.
14	FID	O	Field ID output. When control register bit “FIDS” = “1”, “L” indicates 1st field and “H” indicates 2nd field. When control register bit “FIDS” = “0”, “H” indicates 1st field and “L” indicates 2nd field.
15	VSYN	O	Vertical sync signal output.
16	HSYN	O	Horizontal sync signal output.
17	CSYN	O	Composite SYNC output when using RGB output.
18	Vss2	—	Digital ground.
19	PD0	I	8-bit pixel data inputs, or lower 8-bit pixel data inputs when 16-bit pixel data is input. [PD0 to 7] When control register bit “PIF MODE” = “0”, these are multiplexed Y, Cb, and Cr signal inputs. When control register bit “PIF MODE” = “1”, these are Y signal inputs.
20	PD1	I	
21	PD2	I	
22	PD3	I	
23	VDD2	—	Digital power supply.

Pin No.	Symbol	I/O	Description
24	PD4	I	8-bit pixel data inputs, or lower 8-bit pixel data inputs when 16-bit pixel data is input. [PD0 to 7] When control register bit "PIF MODE" = "0", these are multiplexed Y, Cb, and Cr signal inputs. When control register bit "PIF MODE" = "1", these are Y signal inputs.
25	PD5	I	
26	PD6	I	
27	PD7	I	
28	NC	—	Not connected inside the IC.
29	NC	—	Not connected inside the IC.
30	NC	—	Not connected inside the IC.
31	NC	—	Not connected inside the IC.
32	NC	—	Not connected inside the IC.
33	PD8 / TD0	I/O	Upper 8-bit pixel data inputs/test data bus when 16-bit pixel data is input. [PD8 to 15] When control register bit "PIF MODE" = "0", these inputs are not used. When control register bit "PIF MODE" = "1", these are multiplexed Cb and Cr signal inputs. In the test mode, these are used for the internal circuit test data bus. The test data bus is available only for the device vendor.
34	PD9 / TD1	I/O	
35	PD10 / TD2	I/O	
36	PD11 / TD3	I/O	
37	Vss3	—	Digital ground.
38	PD12 / TD4	I/O	Upper 8-bit pixel data inputs/test data bus when 16-bit pixel data is input. [PD8 to 15] When control register bit "PIF MODE" = "0", these inputs are not used. When control register bit "PIF MODE" = "1", these are multiplexed Cb and Cr signal inputs. In the test mode, these are used for the internal circuit test data bus. The test data bus is available only for the device vendor.
39	PD13 / TD5	I/O	
40	PD14 / TD6	I/O	
41	PD15 / TD7	I/O	
42	VDD3	—	Digital power supply.
43	XIICEN	I	Serial interface mode select input. This pin is pulled up. When XIICEN = "L", Pins 44, 45, 47 and 48 are I <sup>2</sup> C bus mode. When XIICEN = "H", Pins 44, 45, 47 and 48 are Sony SIO mode.
44	XCS/SA	I	This pin's function is selected by XIICEN (Pin 43). This pin is pulled up. When XIICEN = "H", this pin is Sony SIO mode ; XCS chip select input. When XIICEN = "L", this pin is I <sup>2</sup> C bus mode ; SA slave address select input which selects the I <sup>2</sup> C bus slave address.
45	SCK/SCL	I	This pin's function is selected by XIICEN (Pin 43). When XIICEN = "H", this pin is Sony SIO mode ; SCK serial clock input. When XIICEN = "L", this pin is I <sup>2</sup> C bus mode ; SCL input.
46	Vss4	—	Digital ground.

Pin No.	Symbol	I/O	Description
47	SI/SDA	I/O	This pin's function is selected by XIICEN (Pin 43). When XIICEN = "H", this pin is Sony SIO mode ; SI serial data input. When XIICEN = "L", this pin is I2C bus mode ; SDA input/output.
48	SO	O	This pin's function is selected by XIICEN (Pin 43). When XIICEN = "H", this pin is Sony SIO mode ; SO serial out output. When XIICEN = "L", this pin is not used and output is high impedance.
49	NC	—	Not connected inside the IC.
50	NC	—	Not connected inside the IC.
51	NC	—	Not connected inside the IC.
52	NC	—	Not connected inside the IC.
53	NC	—	Not connected inside the IC.
54	IREF	I	DAC reference current input. Connect resistance "16R" which is 16 times output resistance "R".
55	VREF	I	DAC reference voltage input. Sets the DAC output full-scale width.
56	CP-OUT	O	10-bit DAC output. This pin outputs the composite signal.
57	AV <sub>DD1</sub>	—	Analog power supply.
58	C-OUT	O	10-bit DAC output. This pin outputs the chroma (C) signal.
59	AV <sub>SS1</sub>	—	Analog ground.
60	NC	—	Not connected inside the IC.
61	VB	O	Connect to ground via a capacitor of approximately 0.1 $\mu$ F.
62	VG	O	Connect to analog power supply via a capacitor of approximately 0.1 $\mu$ F.
63	NC	—	Not connected inside the IC.
64	Y-OUT	O	10-bit DAC output. This pin outputs the luminance (Y) signal.
65	AV <sub>DD2</sub>	—	Analog power supply.
66	B-OUT	O	10-bit DAC output. This pin outputs the B and V signals.
67	AV <sub>SS2</sub>	—	Analog ground.
68	NC	—	Not connected inside the IC.
69	NC	—	Not connected inside the IC.
70	NC	—	Not connected inside the IC.
71	NC	—	Not connected inside the IC.
72	G-OUT	O	10-bit DAC output. This pin outputs the G and Y signals.
73	AV <sub>DD3</sub>	—	Analog power supply.
74	R-OUT	O	10-bit DAC output. This pin outputs the R and U signals.
75	AV <sub>SS3</sub>	—	Analog ground.
76	NC	—	Not connected inside the IC.
77	NC	—	Not connected inside the IC.
78	NC	—	Not connected inside the IC.
79	NC	—	Not connected inside the IC.
80	NC	—	Not connected inside the IC.
81	V <sub>DD4</sub>	—	Digital power supply.

Pin No.	Symbol	I/O	Description
82	TD8	I/O	Test data I/Os. These pins should be open.
83	TD9	I/O	In the test mode, these are used for the internal circuit test data bus. The test data bus is available only for the device vendor.
84	TD10	I/O	
85	XTEST1	I	Test mode control signal inputs. These pins are pulled up. When all these pins are "H", the CXD1914Q is not in the test mode, but is in the normal mode. The test mode is available only for the device vendor.
86	XTEST2	I	
87	XTEST3	I	
88	XTEST4	I	
89	XTEST5	I	
90	Vss5	—	Digital ground.
91	TDI	I	Test pin. Set "H". This pin is pulled up.
92	TMS	I	Test pin. Set "H". This pin is pulled up.
93	TDO	O	Test pin. This pin should be open.
94	TCK	I	Test pin. Set "H".
95	TRST	I	Reset signal input for JTAG in active low. This pin is pulled up.
96	VDD5	—	Digital power supply.
97	NC	—	Not connected inside the IC.
98	NC	—	Not connected inside the IC.
99	NC	—	Not connected inside the IC.
100	NC	—	Not connected inside the IC.

## Electrical Characteristics

## DC Characteristics

(Ta=0 to +70 °C, Vss=0 V)

Item	Symbol	Measurement pins	Measurement conditions	Min.	Typ.	Max.	Unit
Input High voltage	V <sub>IH</sub>	*1	V <sub>DD</sub> =5.0 V ±5 %	2.2			V
Input Low voltage	V <sub>IL</sub>	*1	V <sub>DD</sub> =5.0 V ±5 %			0.8	V
Output High voltage	V <sub>OH1</sub>	*2	I <sub>OH</sub> =-2.4 mA V <sub>DD</sub> =4.75 to 5.25 V	V <sub>DD</sub> -0.8			V
Output Low voltage	V <sub>OL1</sub>	*2	I <sub>OL</sub> =4.8 mA V <sub>DD</sub> =4.75 to 5.25 V			0.4	V
Output High voltage	V <sub>OH2</sub>	*3	I <sub>OH</sub> =-1.2 mA V <sub>DD</sub> =4.75 to 5.25 V	V <sub>DD</sub> -0.8			V
Output Low voltage	V <sub>OL2</sub>	*3	I <sub>OL</sub> =2.4 mA V <sub>DD</sub> =4.75 to 5.25 V			0.4	V
Input leak current	I <sub>IL1</sub>	*4	V <sub>I</sub> =0 to 5.25 V V <sub>DD</sub> =4.75 to 5.25 V	-10		10	μA
Input leak current	I <sub>IL2</sub>	*5	V <sub>I</sub> =0 V V <sub>DD</sub> =5.0 V ±5 %	-40	-100	-240	μA
Supply current	I <sub>DD</sub>		V <sub>DD</sub> =5.0 V ±5 %			85*6	mA

## Note :

- \*1 PD0-15, TD8-10, XTEST1-5, TRST, TDI, TMS, TCK, SI/SDA, SCK/SCL, XCS/SA, XVRST, XRST, SYSCLK, F1, XIICEN, TVSYNC, OSDSW, ROSD, GOSD, BOSD
- \*2 PDCLK, VSYNC, HSYNC, FID, SO, CSYNC
- \*3 TDO, TD0-10
- \*4 PD0-15, TD8-10, TCK, SI/SDA, SCK/SCL, XRST, F1, SYSCLK, TVSYNC, OSDSW, ROSD, GOSD, BOSD
- \*5 XTEST1-5, TRST, TDI, TMS, XCS/SA, XVRST, XIICEN
- \*6 Not including analog supply current

## DAC Characteristics 1

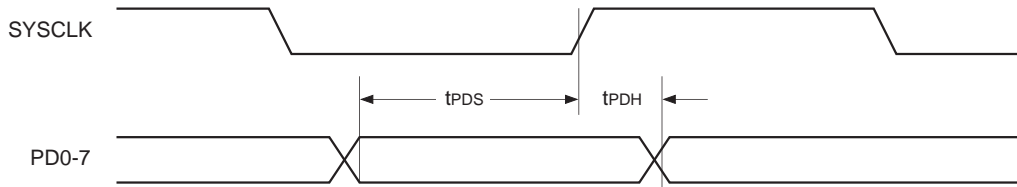
(AV<sub>DD</sub>=5 V, R=200 Ω, VREF=2.00V, Ta=25 °C)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Resolution	n			10		bit
Linearity error	E <sub>L</sub>		-2.0		2.0	LSB
Differential linearity error	E <sub>D</sub>		-1.0		1.0	LSB
Output full-scale current	I <sub>FS</sub>		9.5	10.0	10.5	mA
Output offset voltage	V <sub>OS</sub>				1	mV
Output full-scale voltage	V <sub>FS</sub>		1.9	2.0	2.1	V
Precision guaranteed output voltage range	V <sub>OC</sub>		1.9	2.0	2.1	V

AC Characteristics

1. Pixel data interface

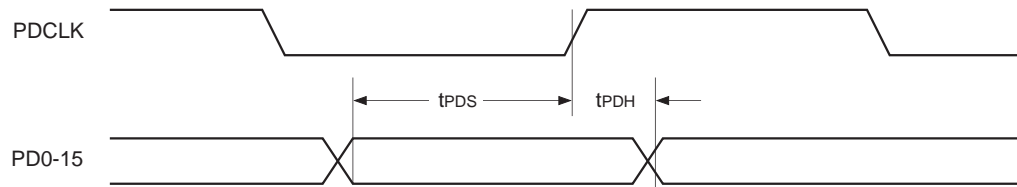
(1) 8-bit mode



(Ta=0 to +70 °C, VDD=4.75 to 5.25 V, VSS=0 V)

Item	Symbol	Min.	Typ.	Max.	Unit
Pixel data setup time to SYSCLK	tPDS	10			ns
Pixel data hold time to SYSCLK	tPDH	3			ns

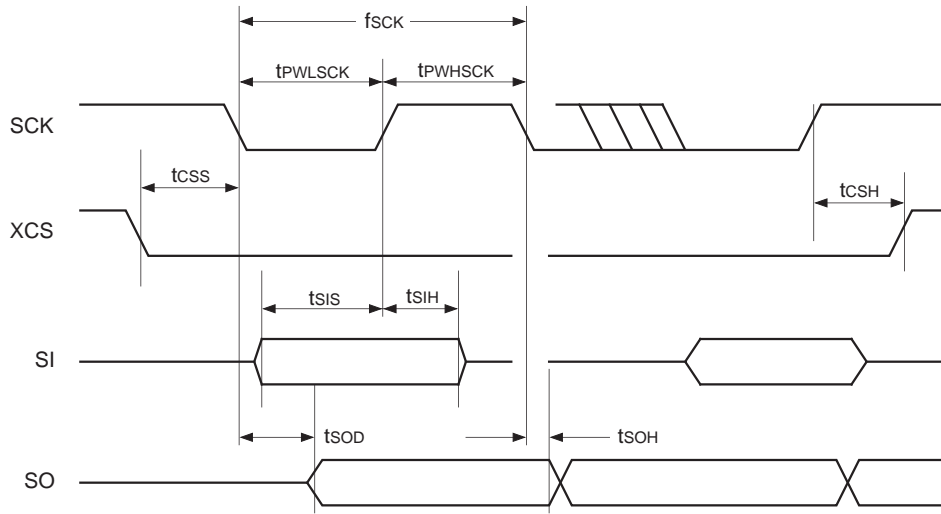
(2) 16-bit mode



(Ta=0 to +70 °C, VDD=4.75 to 5.25 V, VSS=0 V)

Item	Symbol	Min.	Typ.	Max.	Unit
Pixel data setup time to PDCLK	tPDS	20			ns
Pixel data hold time to PDCLK	tPDH	0			ns

2. Serial port interface

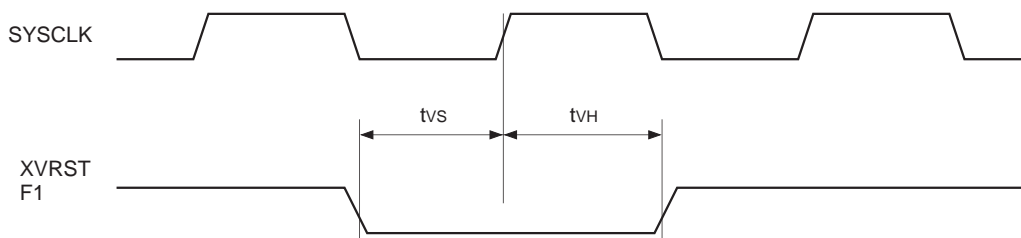


(Ta=0 to +70 °C, VDD=4.75 to 5.25 V, VSS=0 V)

Item	Symbol	Min.	Typ.	Max.	Unit
SCK clock rate	f <sub>SCK</sub>	DC		3	MHz
SCK pulse width Low	t <sub>PWLSCK</sub>	100			ns
SCK pulse width High	t <sub>PWHsCK</sub>	100			ns
Chip select setup time to SCK	t <sub>CSS</sub>	150			ns
Chip select hold time to SCK	t <sub>CsH</sub>	150			ns
Serial input setup time to SCK	t <sub>SI</sub>	50			ns
Serial input hold time to SCK	t <sub>SIH</sub>	10			ns
Serial output delay time from SCK	t <sub>SOD</sub> *			30	ns
Serial output hold time from SCK	t <sub>SOH</sub> *	3			ns

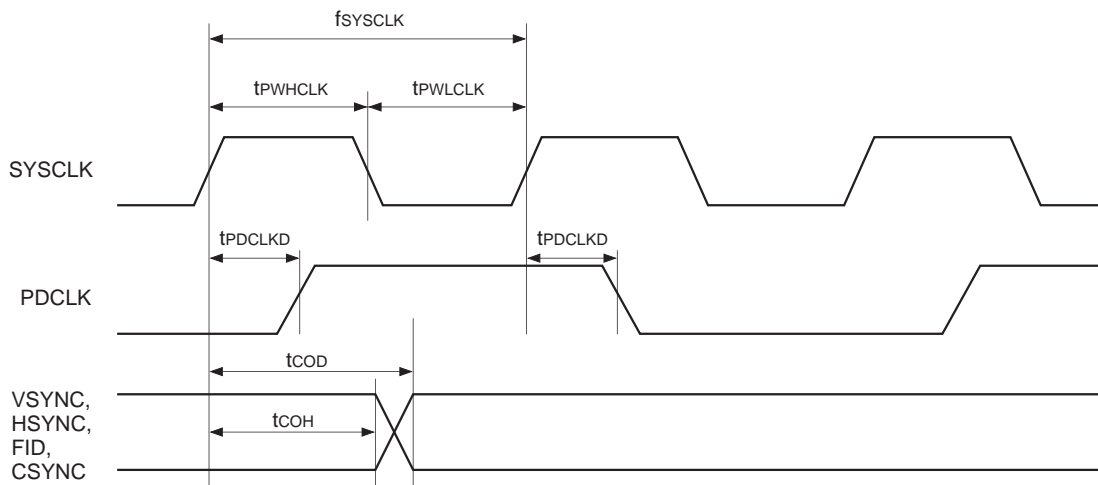
\*CL=35 pF

3. XVRST, F1



Item	Symbol	Min.	Typ.	Max.	Unit
XVRST, F1 setup time to SYSCLK	t <sub>VS</sub>	10			ns
XVRST, F1 hold time to SYSCLK	t <sub>VH</sub>	0			ns

4. SYSCLK, PDCLK, VSYNC, HSYNC, FID, CSYNC



( $T_a=0$  to  $+70$  °C,  $V_{DD}=4.75$  to  $5.25$  V,  $V_{SS}=0$  V)

Item	Symbol	Min.	Typ.	Max.	Unit
SYSCLK clock rate	$f_{SYSCLK}$		27		MHz
SYSCLK pulse width Low	$t_{PWLCLK}$	11			ns
SYSCLK pulse width High	$t_{PWHCLK}$	11			ns
PDCLK delay time from SYSCLK	$t_{PDCLKD}^*$			20	ns
Control output delay time from SYSCLK	$t_{COD}^*$			25	ns
Control output hold time from SYSCLK	$t_{COH}^*$	3			ns

\* $C_L=35$  pF

## Description of Functions

The CXD1914Q converts digital parallel data (ITU-R601 Y, Cb, Cr) into analog TV signals in NTSC (RS170A) or PAL (ITU-R624; B, G, H, I) format.

The CXD1914Q first receives image data in 8-bit parallel form (multiplexed Y, Cb, and Cr data), or in 16-bit parallel form (8-bit Y and 8-bit multiplexed Cb and Cr data). After demultiplexing, it converts the Cb and Cr signals into the U and V signals, respectively, interpolates 4 : 2 : 2 to 4 : 4 : 4, and then modulates the signals with the digital subcarrier inside the CXD1914Q to create the chroma (C) signal.

The Y and chroma (C) signals are oversampled at double speed to reduce  $\sin(X)/X$  roll-off, and then added to become the digital composite signal.

The 10-bit DAC converts the digital composite, Y/C, U, V, and RGB signals into analog signals.

### 1. Pixel input format

The pixel input format is selected according to the value (bit 4 of address 01H) of control register "PIF MODE" as shown in Table 1-1 below.

When "PIF MODE" is "0", the image data (multiplexed Y, Cb, and Cr data) input from PD0 to 7 are sampled at the rising edge of SYSCLK as shown in the chart on the following page. When "PIF MODE" is "1", the image data (PD0 to 7 : Y data, PD8 to 15 : multiplexed Cb and Cr data) input from PD0 to 15 are sampled at the rising edge of PDCLK.

PIF MODE	PD15 to 8	PD7 to 0
0 (8-bit mode)	N/A	Y/Cb/Cr
1 (16-bit mode)	Cb/Cr	Y

**Table 1-1**

Also, the pixel input data timing is determined according to bits 3 and 2 (PIX TIM) of control register address 01H as shown in Table 1-2 below.

When "PIF MODE" is "0", Cb0 of the image data (Cb0, Y0, Cr0 and Y1) input from PD0 to 7 is sampled at the rising edge of SYSCLK after the fall of HSYNC.

(Default : Cb0 is sampled at the rising edge of the second SYSCLK after the fall of HSYNC.)

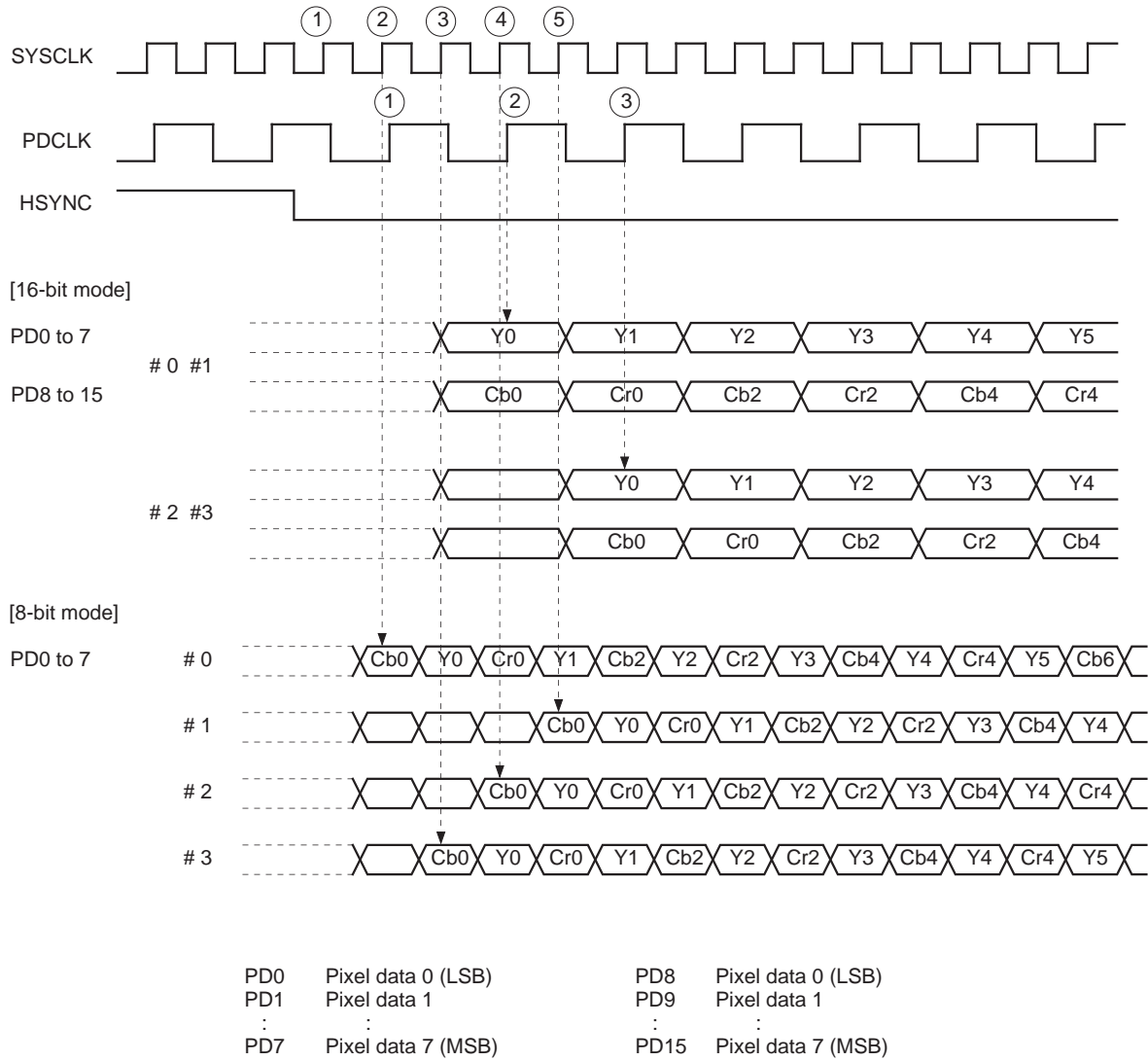
When "PIF MODE" is "1", Y0 and Y1 data are input to PD0 to 7, multiplexed Cb0 and Cr0 data are input to PD8 to 15, and Y0 and Cb0 are sampled at the respective rising edge of PDCLK after the fall of HSYNC.

(Default : Y0 and Cb0 are sampled at the rising edge of the second PDCLK after the fall of HSYNC.)

PIX TIM		Timing phase
0	0	#0 (default)
0	1	#1
1	0	#2
1	1	#3

**Table 1-2**

Pixel Data Input Timing



**2. Serial interface**

The CXD1914Q supports both the I<sup>2</sup>C bus (high-speed mode) and Sony serial interface modes. These modes can be selected by the XIICEN input pin as shown in Table 2-1 below.

XIICEN	H	L
	SONY SIO Mode	I <sup>2</sup> C Mode
SI/SDA	SI	SDA
SCK/SCL	SCK	SCL
XCS/SA	XCS	SA
SO	SO	High-Z

**Table 2-1**

**2-1 I<sup>2</sup>C bus interface**

The CXD1914Q becomes an I<sup>2</sup>C bus slave transceiver, and supports the 7-bit slave address and the high-speed mode (400 Kbits/s).

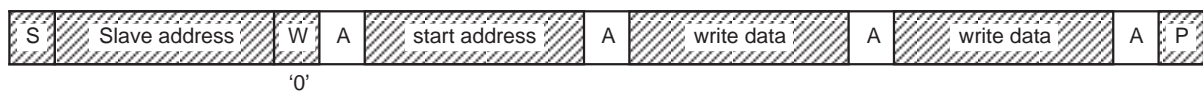
2-1-1. Slave address



Two kinds of slave address (88H, 8CH) can be selected by the SA signal as shown in Table 2-2 below.

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	1	SA	0	X

**Table 2-2**

2-1-2. Write cycle

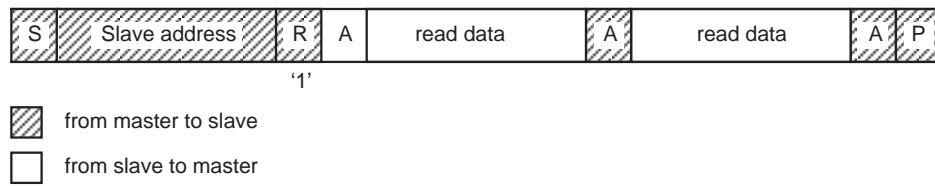


 from master to slave  
 from slave to master



After the slave address is supplied from the master, the data in the next transfer cycle is set up inside the start address register of this IC as the start address of the control register. In subsequent cycles, the data supplied from the master is written in the addresses indicated by the control register address. The set control register address is automatically incremented with the completed transfer of each byte of data.

## 2-1-3. Read cycle



After the slave address is supplied from the master, subsequent cycles change immediately to read cycles and only the ID code (address 0CH, 0DH) is read out. During the read cycle, the start address is automatically set to 0CH.

**(Note)** In the Sony SIO mode, addresses from 00H to 0DH can be read out.

## 2-1-4. Handling of the general call address (00H)

The general call address is ignored and there is no ACK response.

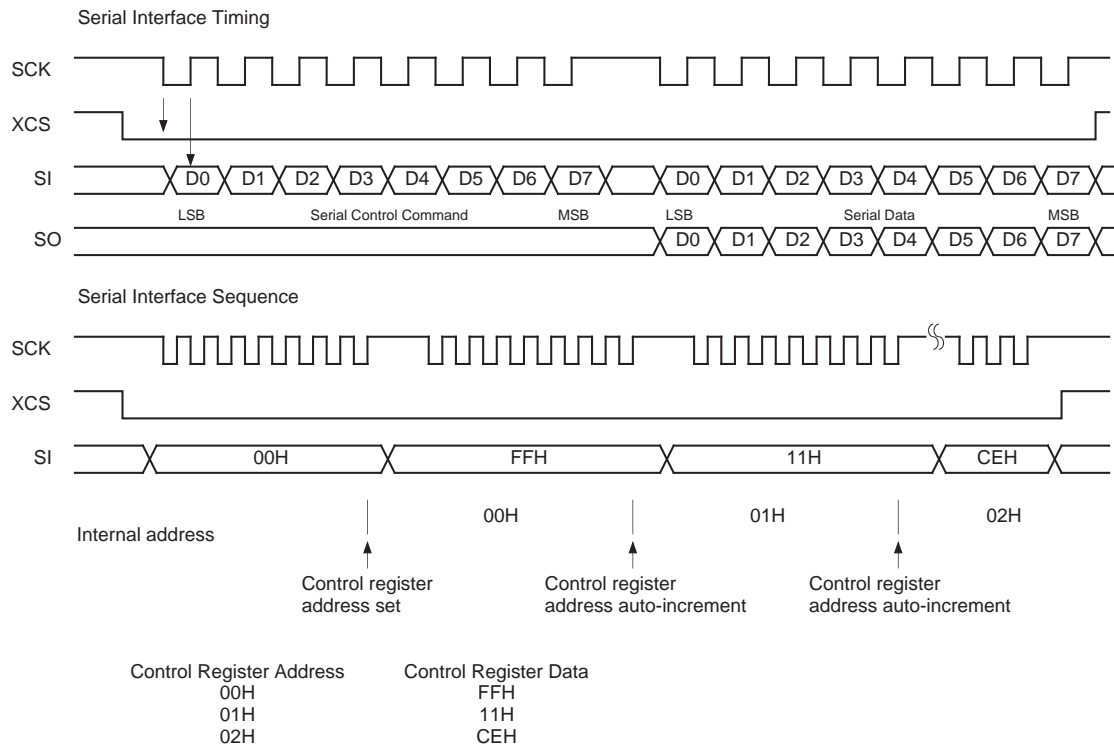
**2-2. Sony serial interface**

The Sony serial interface uses the SCK, XCS, SI and SO signals.

The serial interface is active when the XCS signal is Low and transmits and receives signals to and from the host.

The first byte after the XCS signal becomes Low is set up as a serial control command. Its data includes a control register address and read/write mode information for the interface. (See 2-2-1. Serial control command format.)

The control register address is automatically incremented with the transfer of each byte of data. In the write mode, the SI signal of the serial input data is sampled at the rising edge of the SCK signal. In the read mode, the register value is read out as the SO signal of the serial output data at the falling edge of the SCK signal, and is variable. In this case, the SI signal of the serial input data is ignored.



**2-2-1. Serial control command format**



**WR** : Read/write mode

When this bit is "1" :

The serial interface is write mode, and the SI signal of the serial input data is written in the register.

When this bit is "0" :

The serial interface is read mode, and the register value is read out as the SO signal of the serial output data.

**ADR [4 : 0]** : Control register address setting (Initial value of the address)

**3. XVRST, F1**

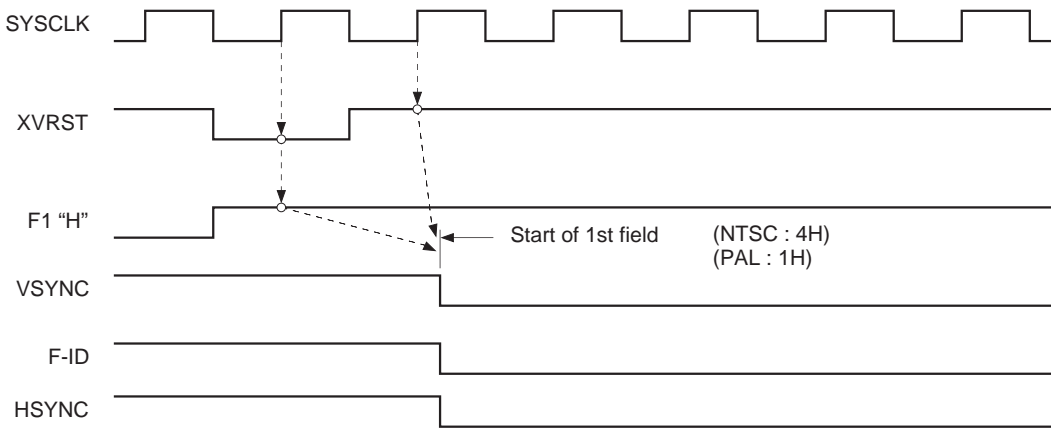
The XVRST and F1 signals are used to synchronize with the external V sync.

The XVRST and F1 signals are sampled at the rising edge of SYSCLK, and the F1 signal is sampled when XVRST is Low. When F1 is High, the internal sync generator is reset to the 1st field, and when F1 is Low, it is reset to the 2nd field. When XVRST is set to High, the digital sync generator starts operation, and the sequence of the 1st or 2nd field starts.

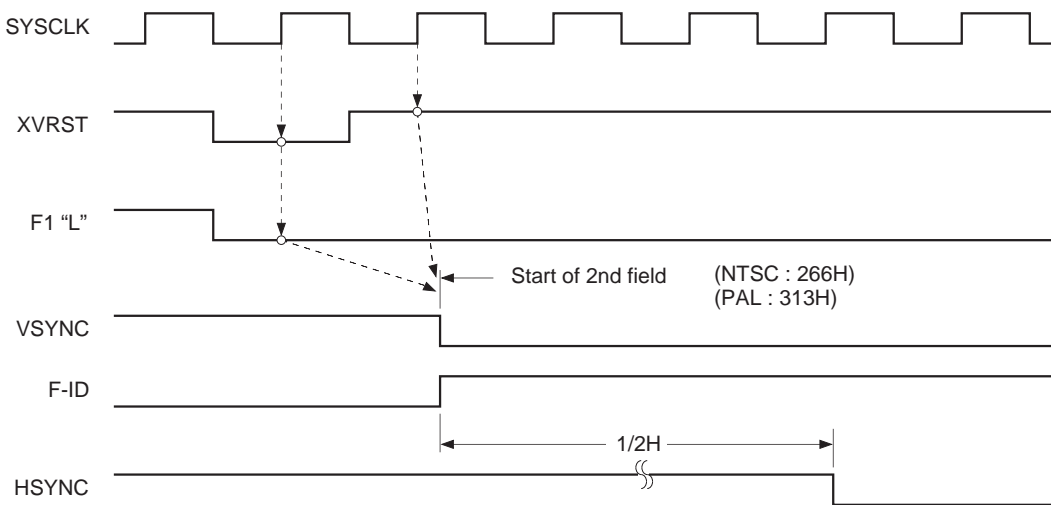
In the 16-bit mode, input XVRST with a width of four SYSCLK pulses at the rise of PDCLK.

[8-bit mode]

XVRST Timing (1st Field)

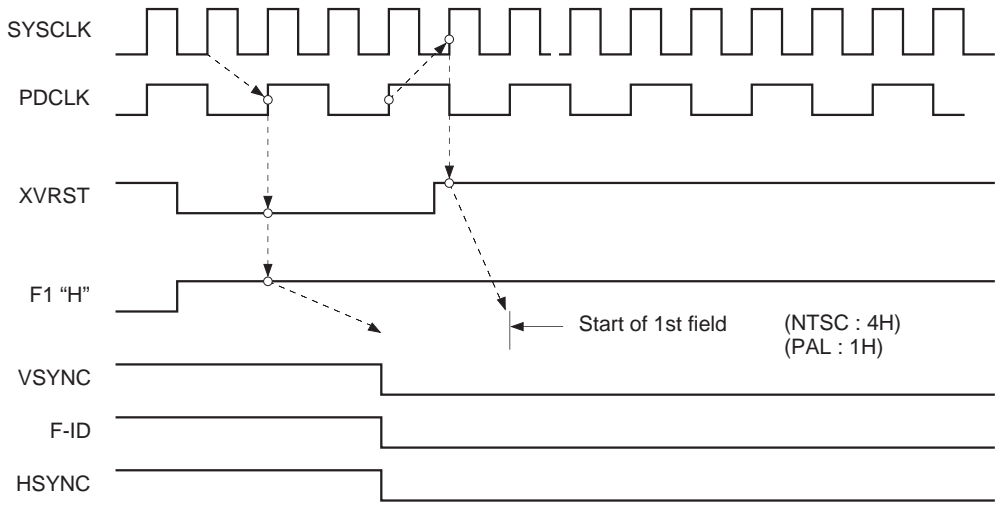


XVRST Timing (2nd Field)

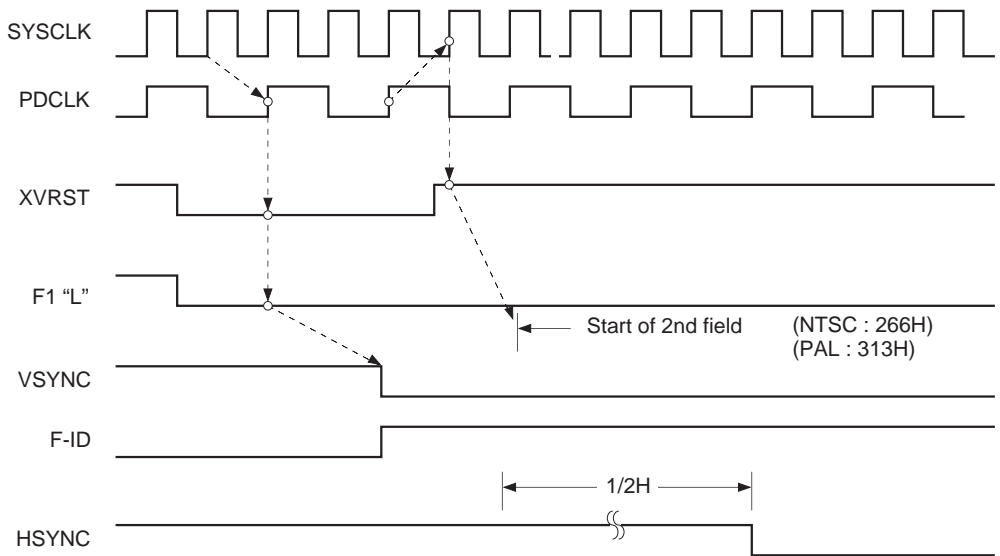


[16-bit mode]

XVRST Timing (1st Field)



XVRST Timing (2nd Field)



**4. Closed caption**

The CXD1914Q supports closed caption encoding.

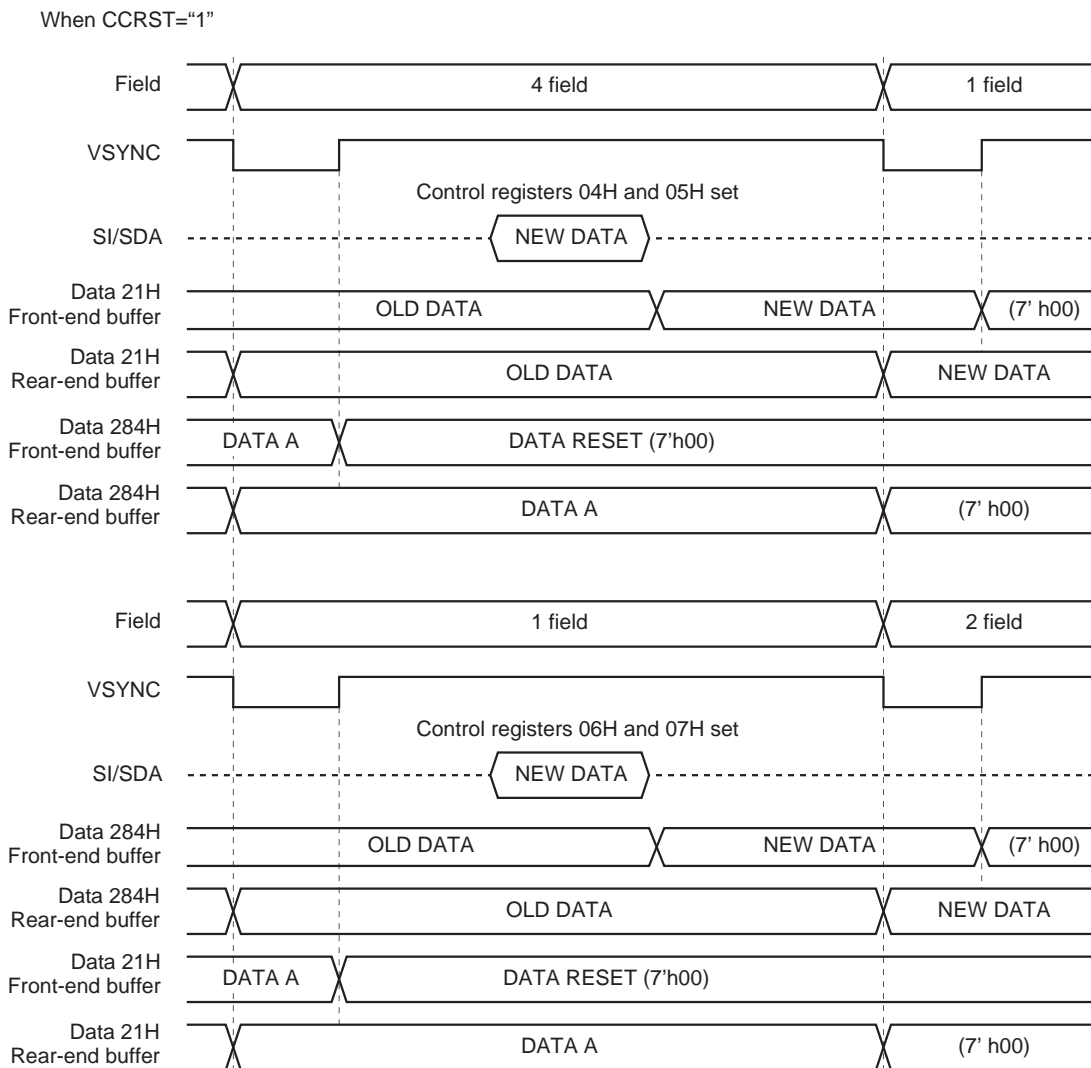
ASCII data for closed captions are encoded in line 21 and line 284 by adding a parity bit to every ASCII data set up in control registers 04H, 05H (data #1 and #2 for line 21) and 06H, 07H (data #1 and #2 for line 284). The control registers (04H to 07H) are double-buffered and ASCII data, which are set up by the serial interface, are synchronized with VSYNC.

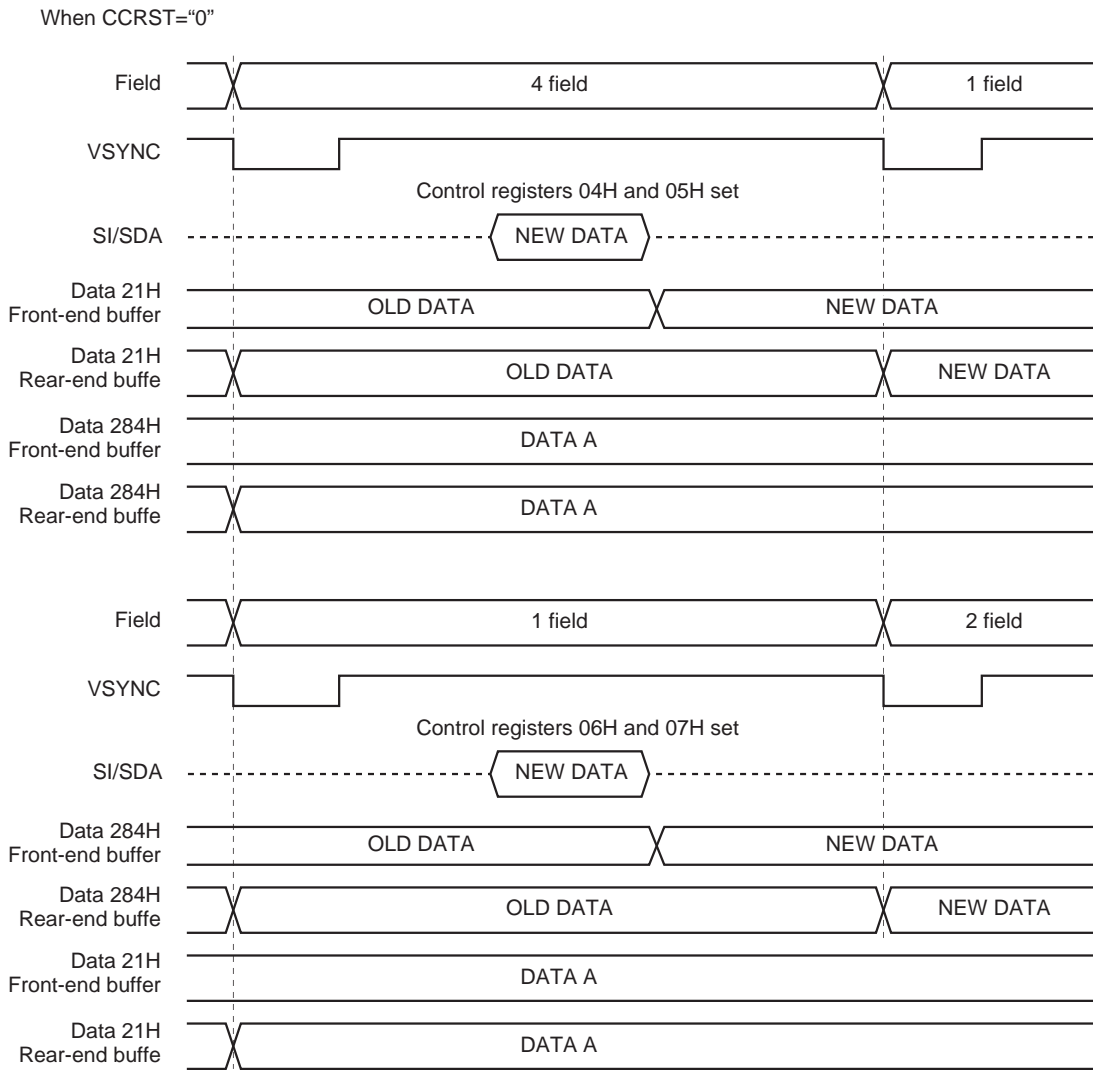
Automatic reset on/off can be selected for ASCII data which has been synchronized with VSYNC by changing the setting of bit 5 (CCRST) of control register address 03H.

When CCRST="1", the control registers (04H, 05H or 06H, 07H) are automatically reset in sync with the rise of the next VSYNC.

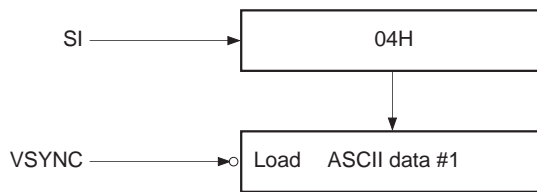
When CCRST="0" (default), the control registers (04H, 05H or 06H, 07H) are not reset, and the data set last is held.

**Closed Caption Data Renewal Timing**

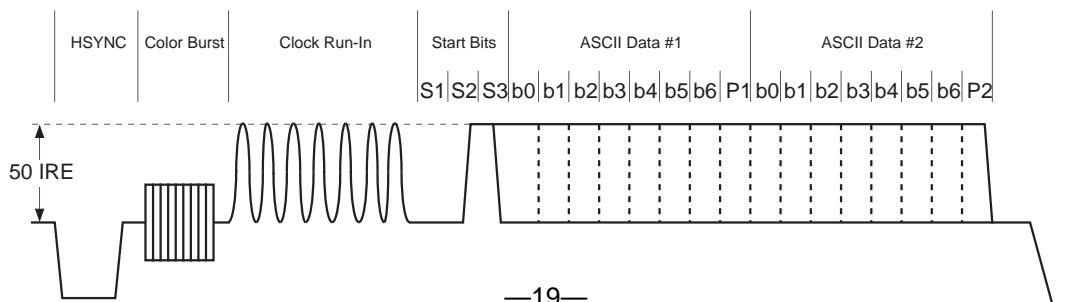




Double Buffer for Closed Caption



Closed Caption Signal Waveform



**5. VBID (Video ID)**

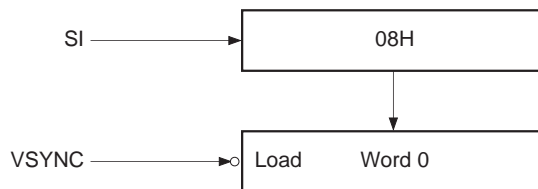
The CXD1914Q supports encoding of Video ID (Provisional Standard EIAJ CPX-1204) to discriminate the aspect ratio. VBID is 14-bit data as shown in Table 5-1, and becomes 20-bit data with the addition of 6-bit CRCC. These data are superimposed and output to lines 20 and 283 during the vertical blanking period of NTSC video signals.

The data setting in Table 5-1 below is done by writing data in control registers (08H and 09H) via the serial interface. These control registers (08H and 09H) are double-buffered, and the VBID data are renewed in sync with the VSYNC signal.

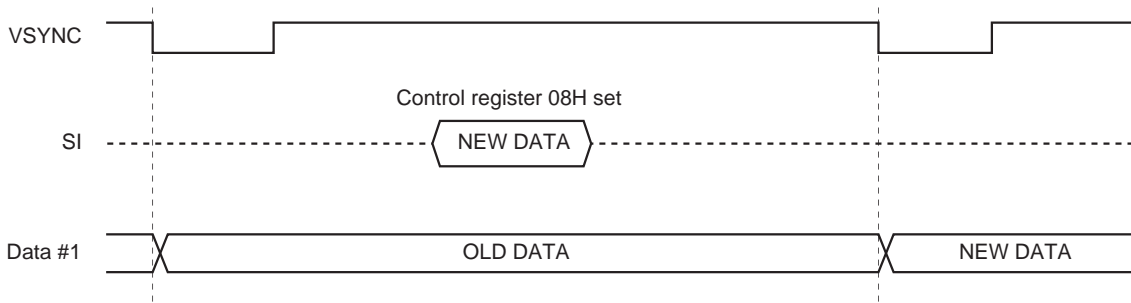
		bit-No.	Contents	"1"	"0"	
Word 0	A	1	Transmission aspect ratio	Full-mode (16 : 9) Letter-box	4 : 3 Normal	
		2	Image display format			
		3	Undefined			
	B	4	Identification information about video and other signals (audio signals, etc.) incidental to image which are transmitted simultaneously			
		5				
		6				
Word 1		4-bit width	Identification signal incidental to Word 0			
Word 2		4-bit width	Identification signal and information incidental to Word 0			

**Table 5-1**

Double Buffer for VBID

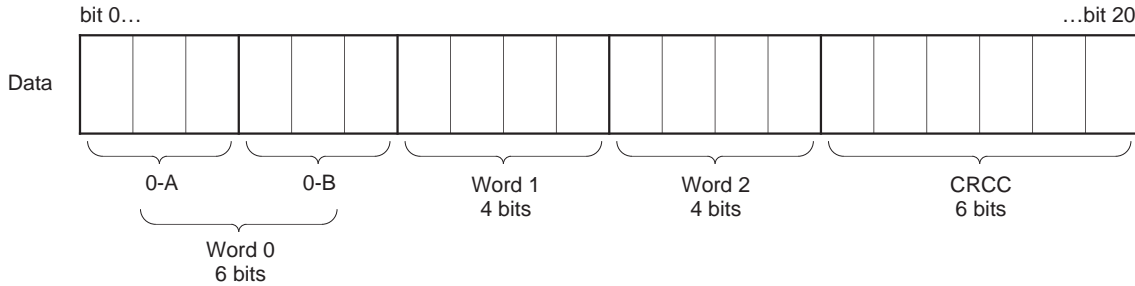


VBID Data Renewal Timing

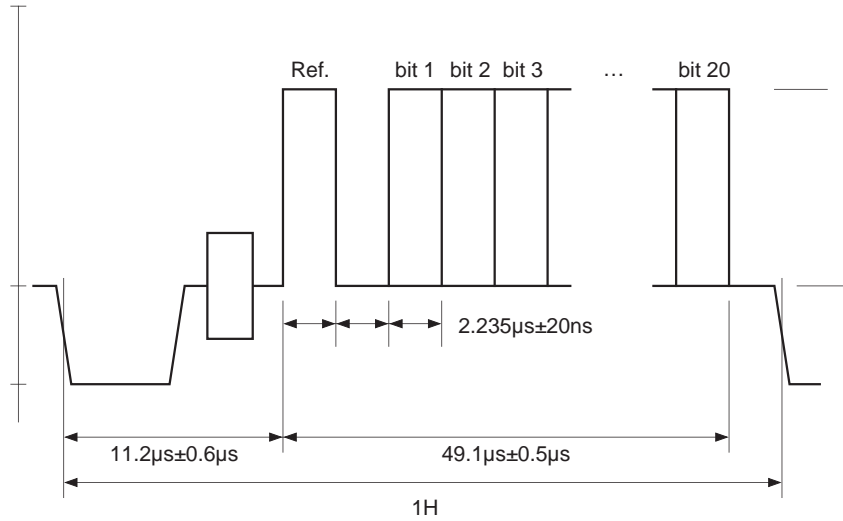


**VBID Code Allocation**

The VBID data are composed of Word 0=6 bits (Word 0-A=3 bits and Word 0-B=3 bits), Word 1=4 bits, Word 2=4 bits, and CRCC=6 bits.



**VBID Signal Waveform**



**6. RGB/YUV output**

The CXD1914Q has an RGB/YUV output function. RGB and YUV can be switched by setting bit 2 (RGB\_UV) of control register address 03H. Also, the UV level can be selected from BetaCam or SMPTE by setting bit 0 (BTCM) of address 03H. During RGB output, when bit 1 (GSYNC) of control register address 03H is “1”, the sync signal is added to the G signal and output ; when bit 1 (GSYNC) is “0”, the sync signal is not added.

**7. Support of interlace/non-interlace modes**

The CXD1914Q can be switched to the interlace and non-interlace modes by varying the setting of bit 1 (INTERLS) of control register address 01H. During the non-interlace mode, the 1st field is repeatedly output.

Register setting value INTERLS	Number of lines/field	
	NTSC	PAL
0 (non-interlace)	262	312
1 (interlace)	262.5	312.5

**8. WSS (Widescreen Signaling)**

The CXD1914Q supports WSS encoding to discriminate the aspect ratio. WSS is 14-bit data as shown in Table 6-1. These data are superimposed and output to line 23 during the vertical blanking period of PAL video signals.

The data setting in Table 6-1 below is done by writing data in control registers (0AH and 0BH) via the serial interface. These control registers (0AH and 0BH) are double-buffered, and the WSS data are renewed in sync with the VSYNC signal.

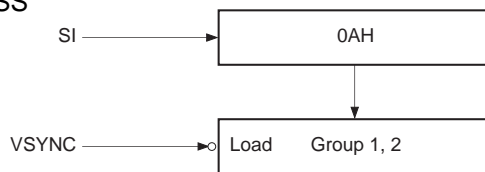
Group 1 Aspect ratio information (4 bits) b0-b3			Group 2 PAL plus related information (4 bits) b4-b7	
0001	Normal		bit4	Camera/Film mode
1000	Letter-box 14 : 9	Center	bit5-7	Reserved
0100	Letter-box 14 : 9	Top		(Color plus)
1101	Letter-box 16 : 9	Center		(Helper)
0010	Letter-box 16 : 9	Top		(Baseband Helper)
1011	Letter-box >16 : 9	Center		
0111	Full-mode 14 : 9			
1110	Full-mode 16 : 9			

\* b3 is odd parity.

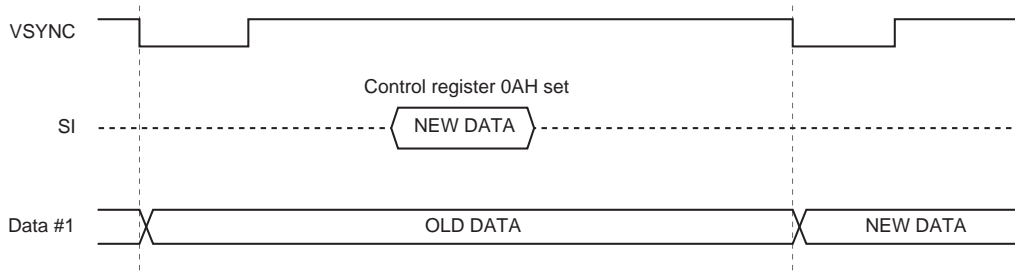
Group 3 Subtitle information (3 bits) b8-b10		Group 4 Undefined (3 bits) b11-b13	
bit8	TeleText subtitle enable/disable	Reserved	
bit9, 10			
00	No subtitle		
10	Subtitle inside screen		
01	Subtitle in black portion		
11	Reserved		

Table 6-1

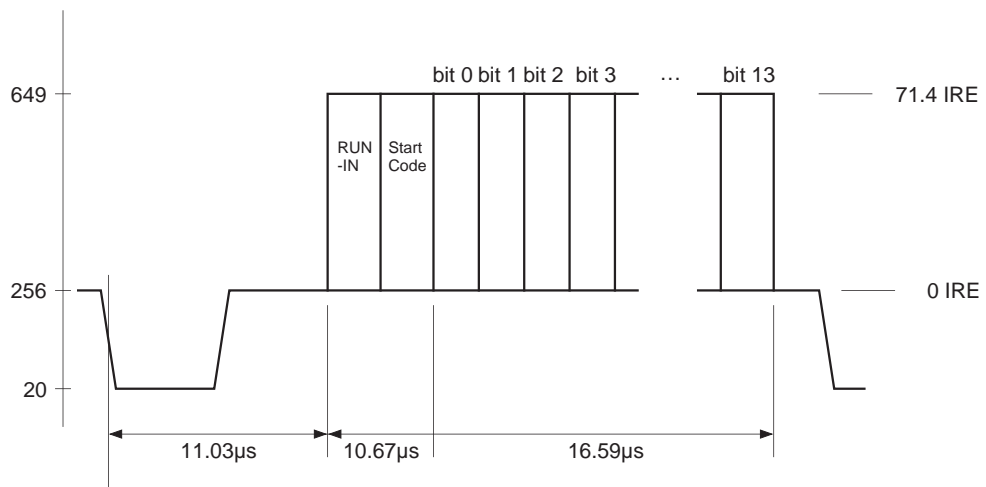
**Double Buffer for WSS**



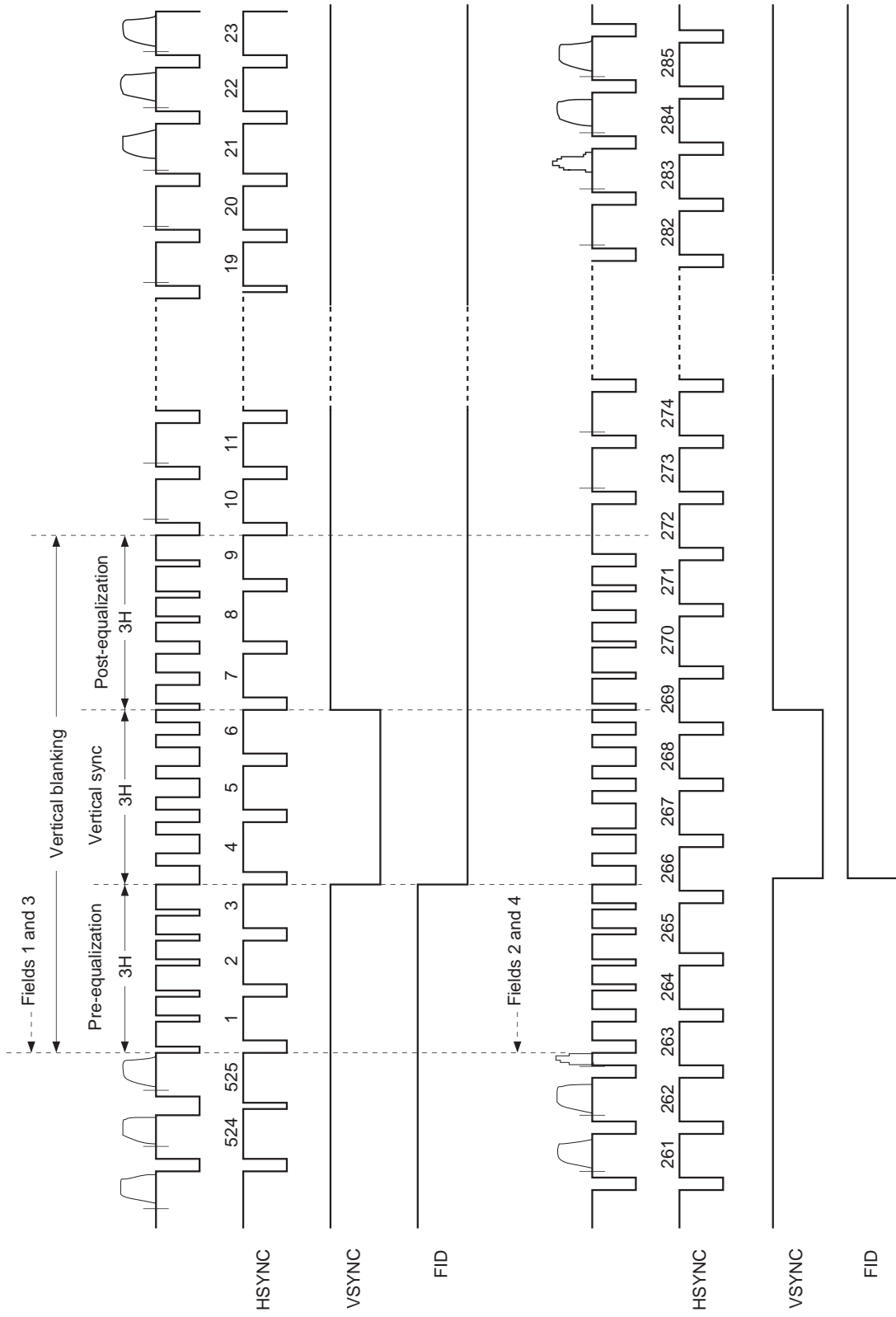
**WSS Data Renewal Timing**



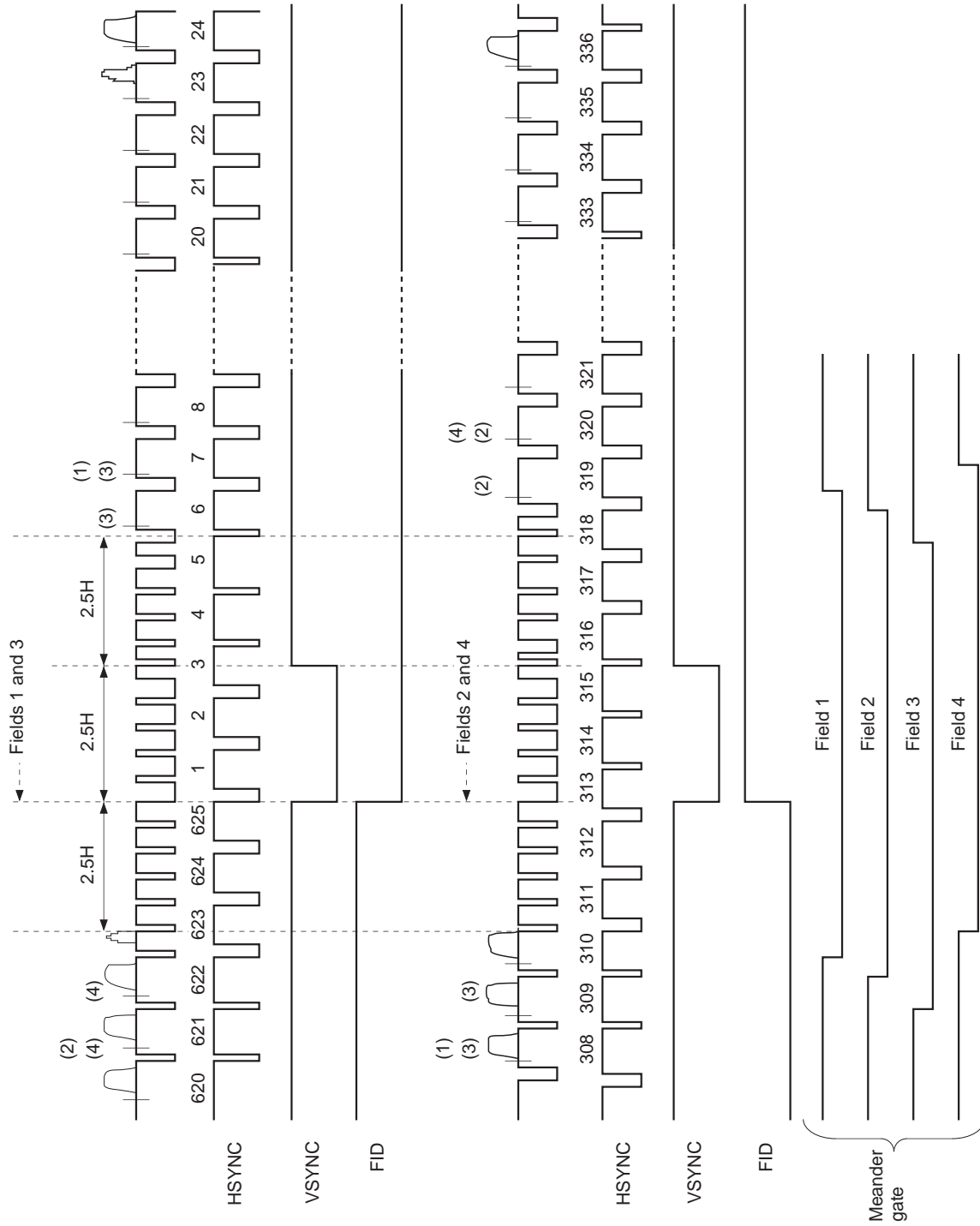
WSS Signal Waveform



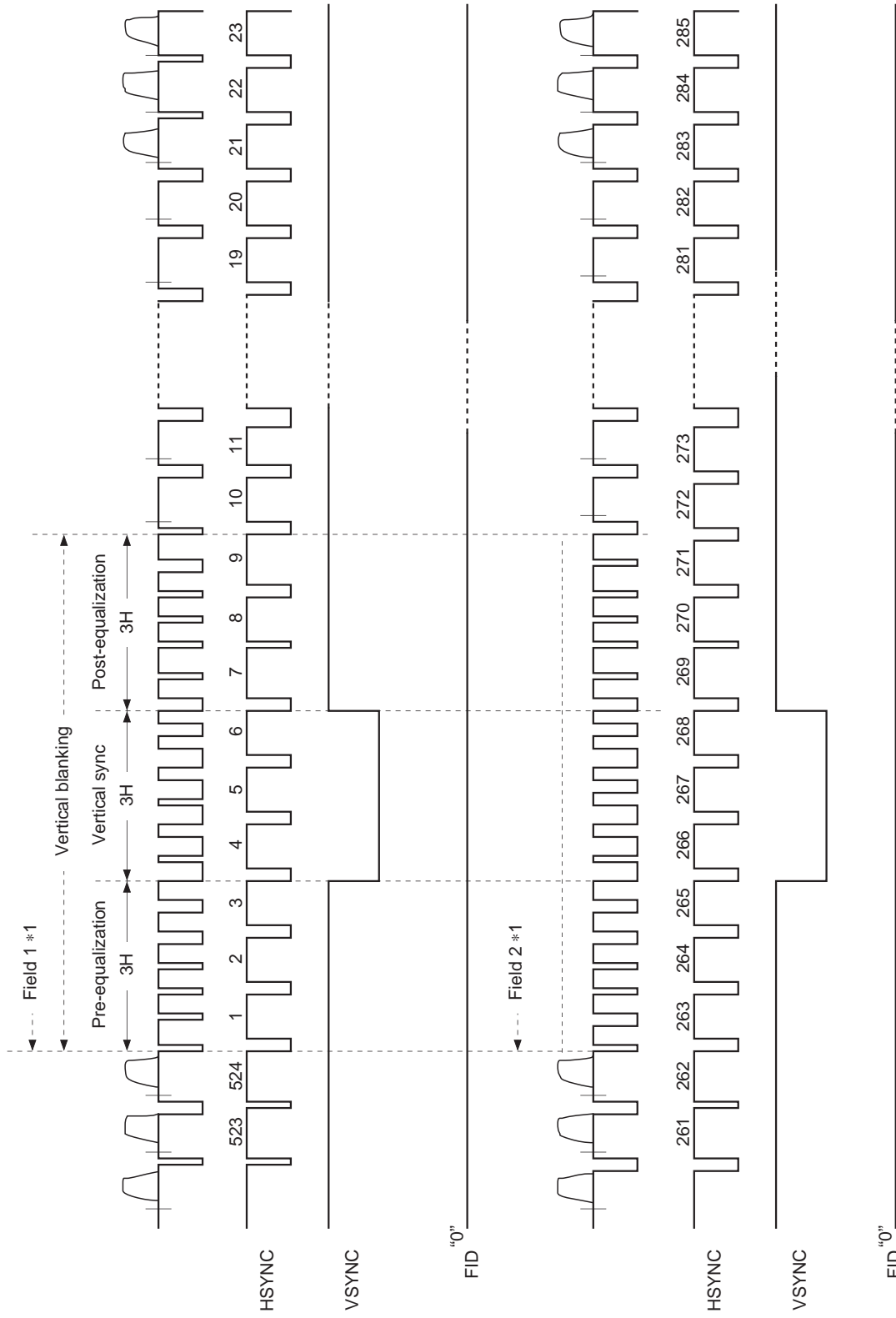
Signal Waveform of NTSC Vertical Blanking Interval (Interlace mode)



Signal Waveform of PAL Vertical Blanking Interval (Interlace mode)

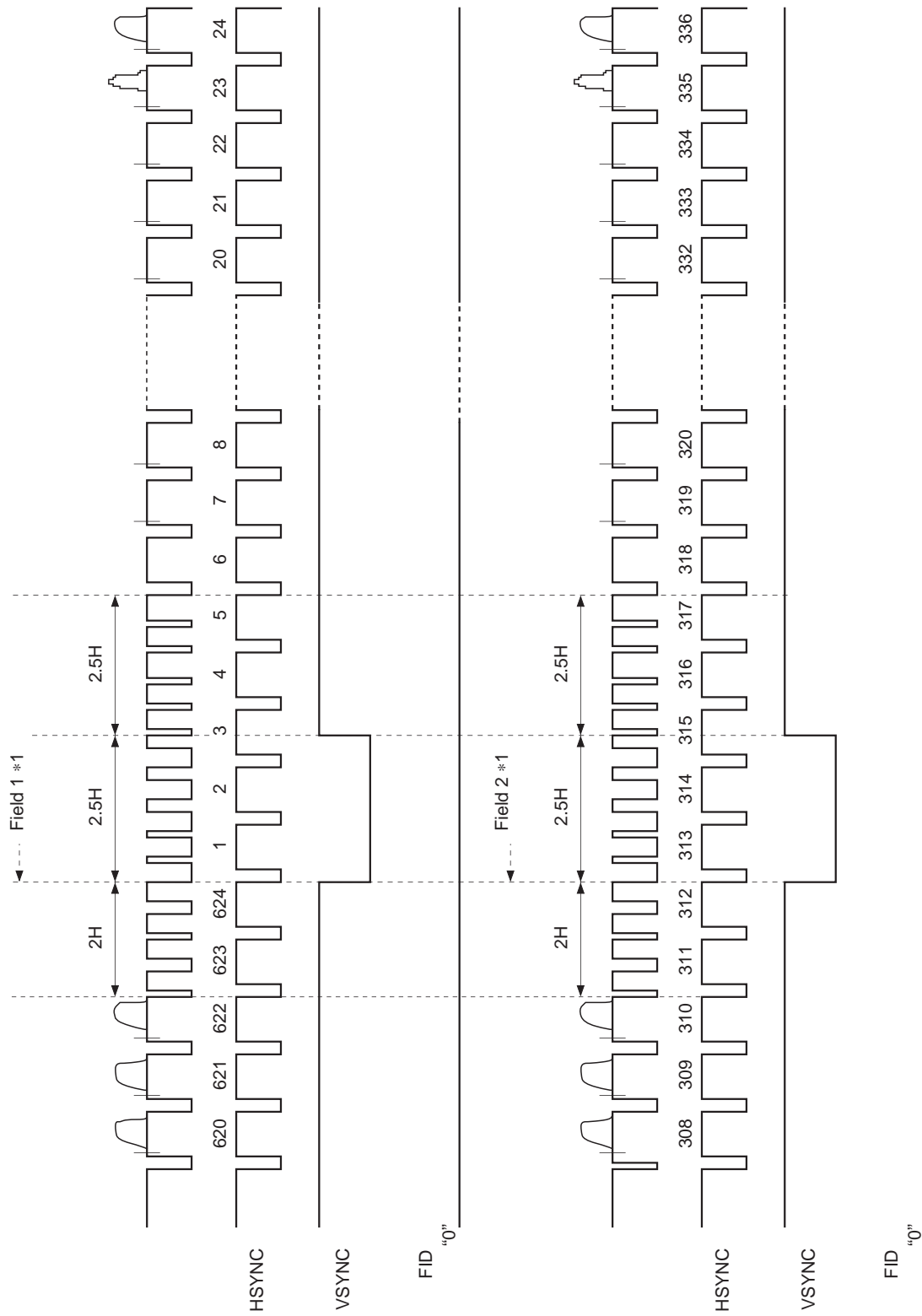


Signal Waveform of NTSC Vertical Blanking Interval (Non-interlace mode)

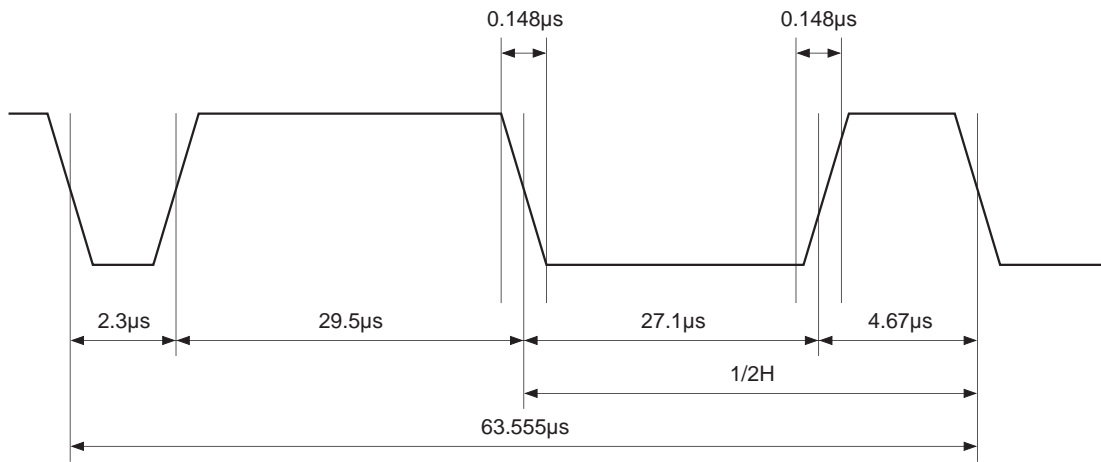


\*1 No differentiation is made between Fields 1 and 2 to facilitate the frame description.

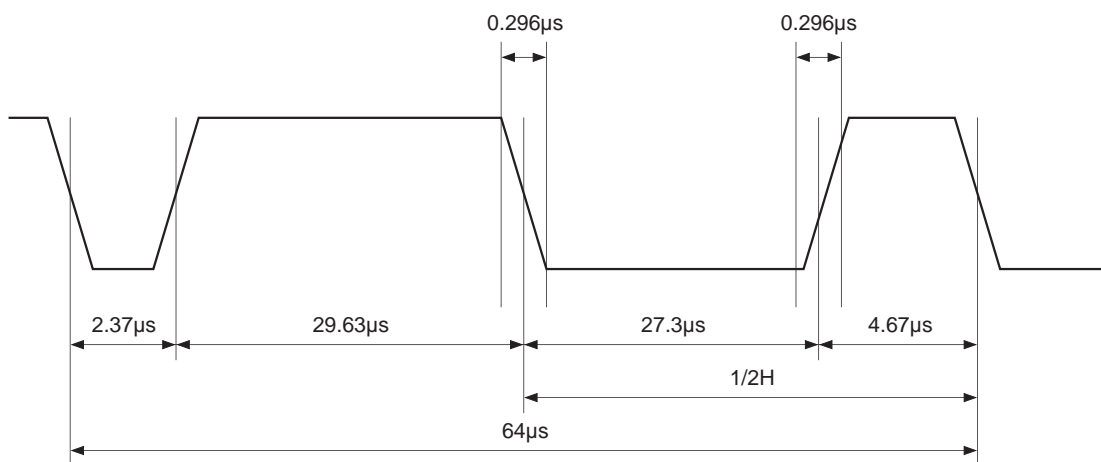
Signal Waveform of PAL Vertical Blanking Interval (Non-interlace mode)



Sync Signal Timing



NTSC Equalizing Pulse and Sync Pulse Signal Waveform



PAL Equalizing Pulse and Sync Pulse Signal Waveform

## Control Register Map

When "0" or "1" is indicated in the map, fix the respective bits to these values.

		BIT								
Function Selection #1		7	6	5	4	3	2	1	0	
Address 00H		FIDS	MASK EN	PIX EN	0	BF	SET UP	0	ENC MODE	R/W

- ENC MODE**      Encoding mode  
 0 : PAL encoding mode  
 1 : NTSC encoding mode (Default)
- SET UP**        Setup enable  
 0 : No setup level, black level=blanking level  
 1 : 7.5 IRE setup level insertion (Default)
- BF**             Burst flag enable  
 0 : Disable burst flag  
 1 : Enable burst flag (Default)
- PIX EN**        Pixel data enable  
 0 : Disable input pixel data  
 1 : Enable input pixel data (Default)
- MASK EN**      Mask enable  
 0 : Pixel data through during vertical blanking  
 1 : Pixel data reject during vertical blanking (Default)
- FIDS**          FID polarity select  
 0 : 1st field "H", 2nd field "L"  
 1 : 1st field "L", 2nd field "H" (Default)

BIT

Function Selection #2

	7	6	5	4	3	2	1	0	
Address 01H	DAC	MODE		PIF MODE	PIX TIM	INTERLS		1	R/W

INTERLS    0 : Non-interlace mode  
              1 : Interlace mode (Default)

PIXTIM     Pixel input timing  
              0 0 : #0 (Default)  
              0 1 : #1  
              1 0 : #2  
              1 1 : #3

PIF MODE   Pixel input format  
              0 : 8-bit mode, multiplexed Y, Cb, Cr (4 : 2 : 2) (Default)  
              1 : 16-bit mode, Y and multiplexed Cb, Cr (4 : 2 : 2)

DAC MODE   DAC output activity  
              0 0 0 : Non-active  
              0 0 1 : Comp-Out active  
              0 1 0 : Inhibit  
              0 1 1 : Video signal (Y, C, Comp) -Out active (Default)  
              1 0 0 : Inhibit  
              1 0 1 : R, G, B-Out and Comp-Out active  
              1 1 0 : Inhibit  
              1 1 1 : All outputs active

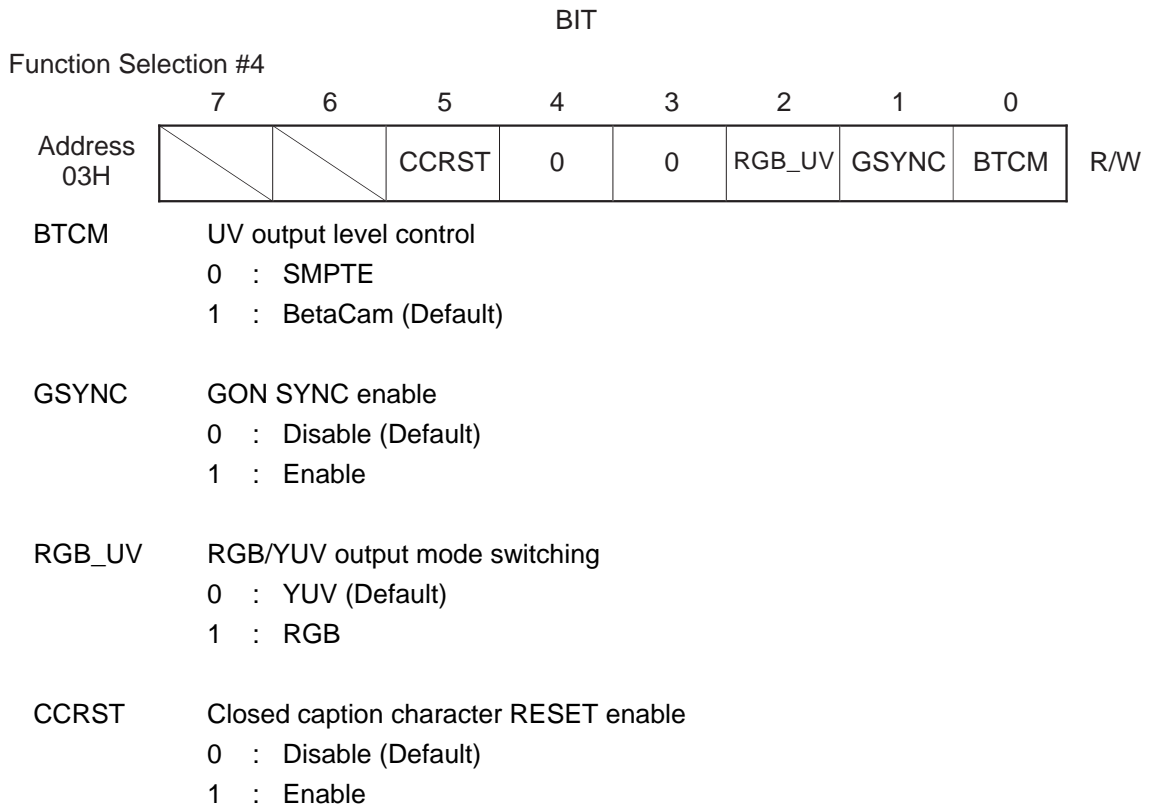
Function Selection #3

	7	6	5	4	3	2	1	0	
Address 02H	0	0	0	0	VBID	WSS		CC Mode	R/W

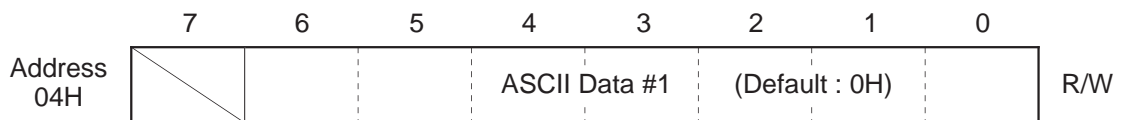
CC MODE    Closed caption encoding mode  
              0 0 : Disable closed caption encoding (Default)  
              0 1 : Enable encoding in 1st field (Line 21)  
              1 0 : Enable encoding in 2nd field (Line 284)  
              1 1 : Enable encoding in both fields

WSS        WSS encoding enable  
              0 : Disable WSS encoding (Default)  
              1 : Enable WSS encoding

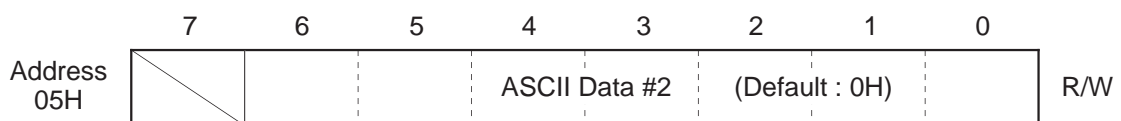
VBID       VBID encoding enable  
              0 : Disable VBID encoding (Default)  
              1 : Enable VBID encoding



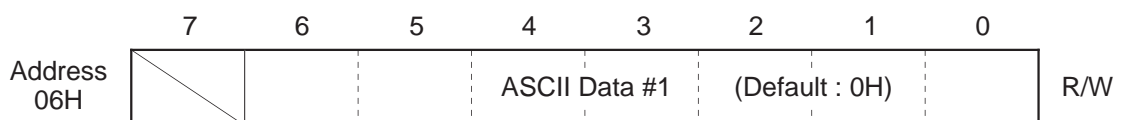
Closed Caption Character #1 (Line 21H)



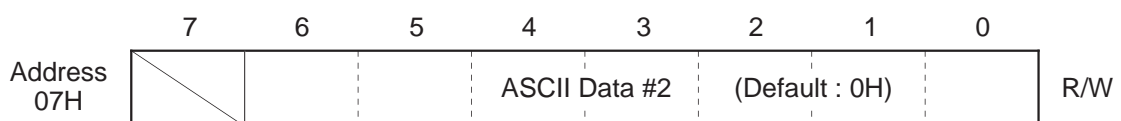
Closed Caption Character #2 (Line 21H)

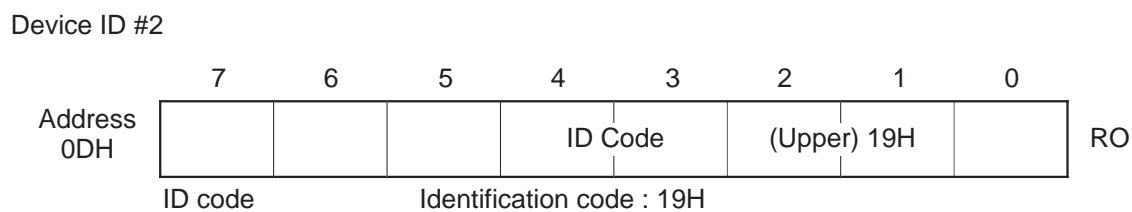
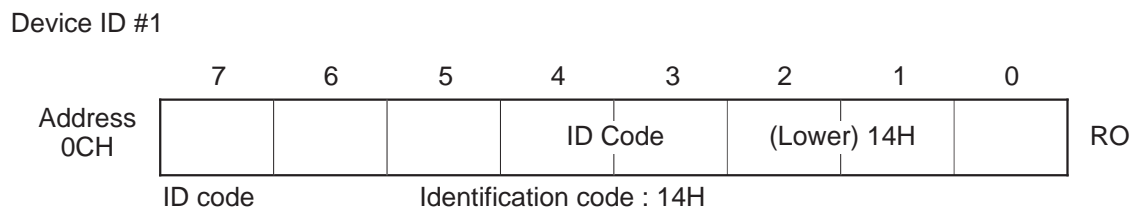
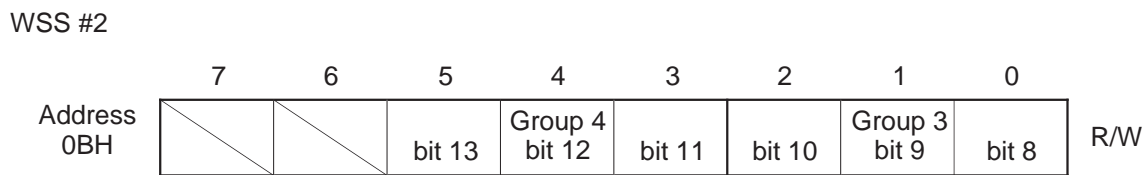
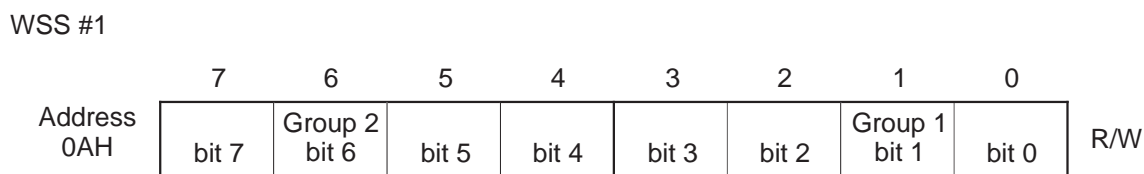
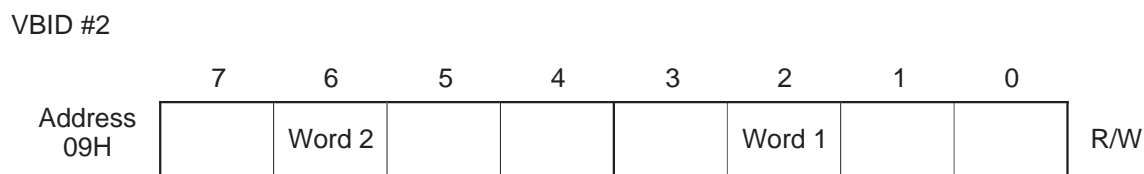
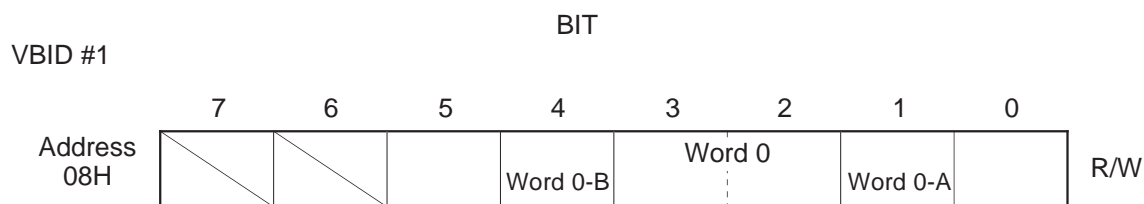


Closed Caption Character #1 (Line 284H)

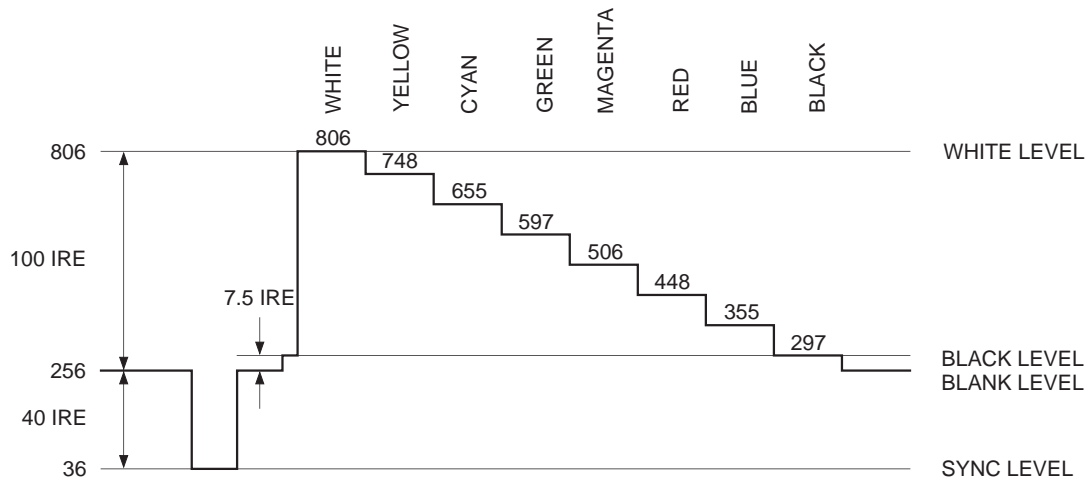


Closed Caption Character #2 (Line 284H)

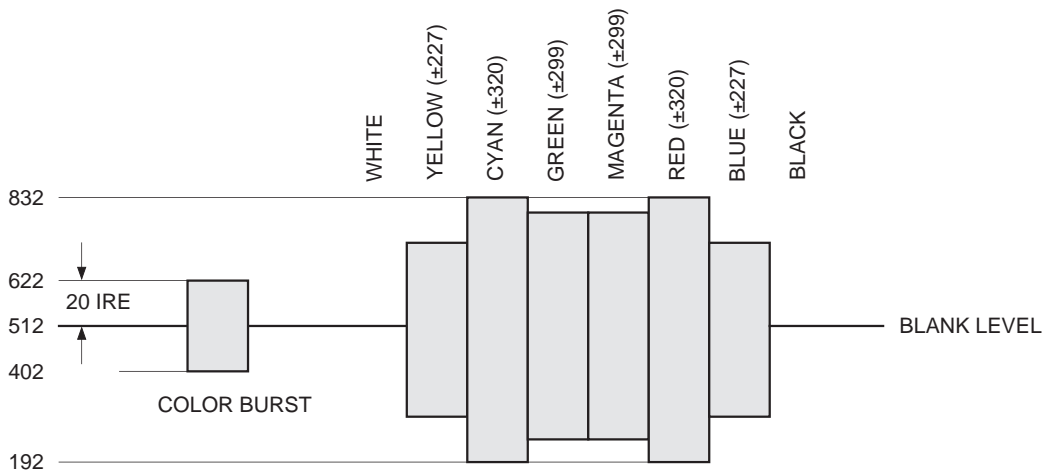




Video Signal Timing (NTSC, 7.5 IRE Setup)

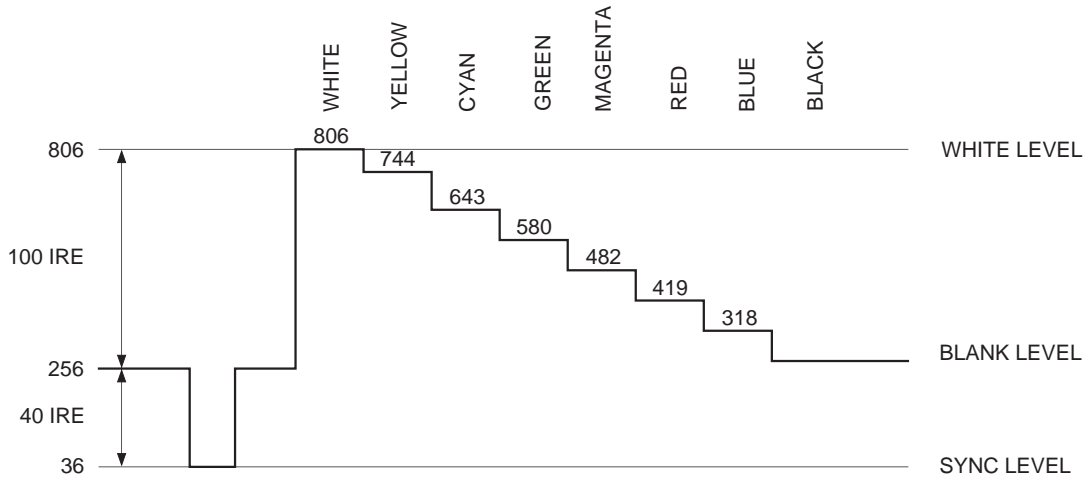


NTSC Y (luminance) signal output waveform  
7.5 IRE setup

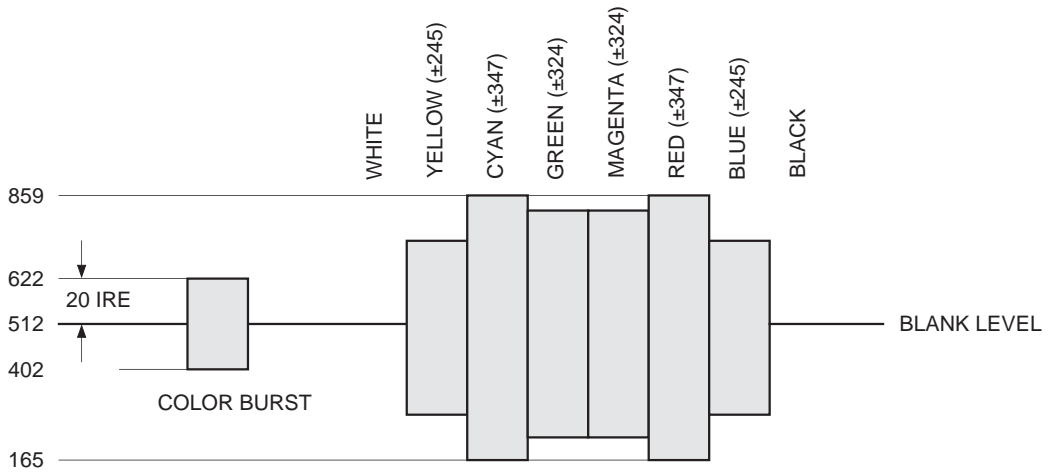


NTSC C (chroma) signal output waveform  
7.5 IRE setup

Video Signal Timing (NTSC, No Setup)

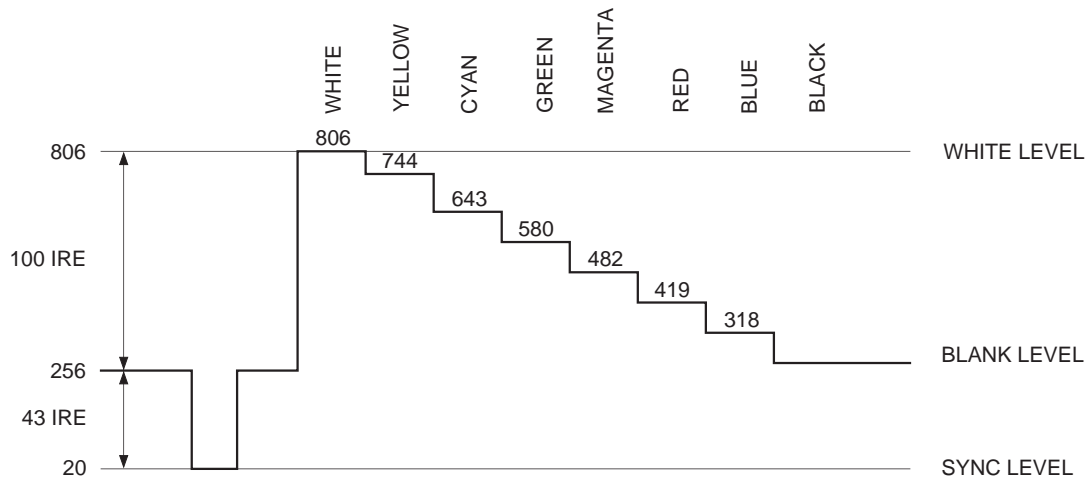


NTSC Y (luminance) signal output waveform

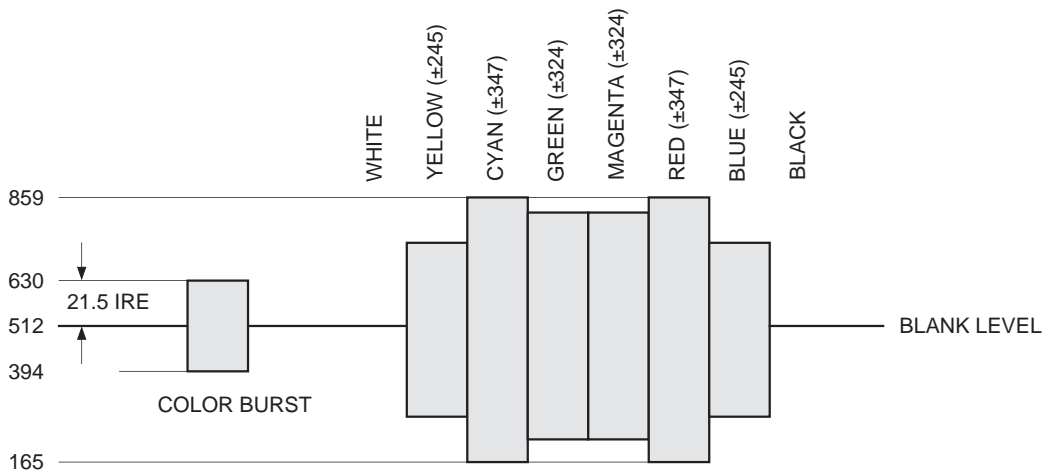


NTSC C (chroma) signal output waveform

Video Signal Timing (PAL)

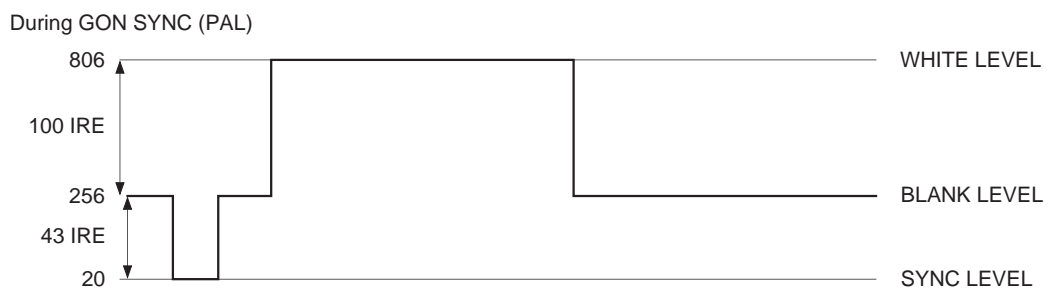
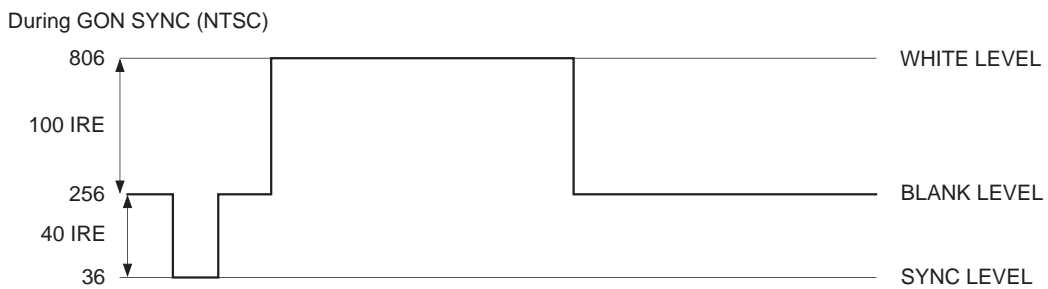
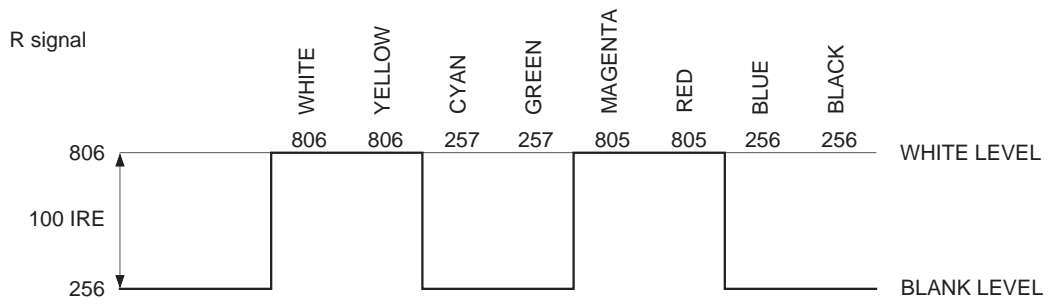


PAL Y (luminance) signal output waveform



PAL C (chroma) signal output waveform

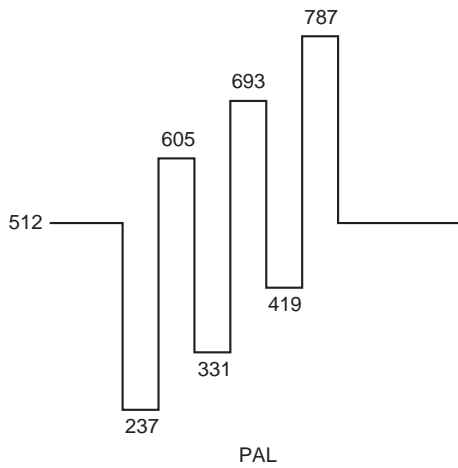
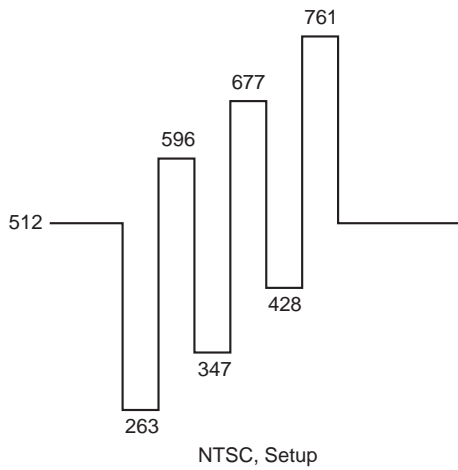
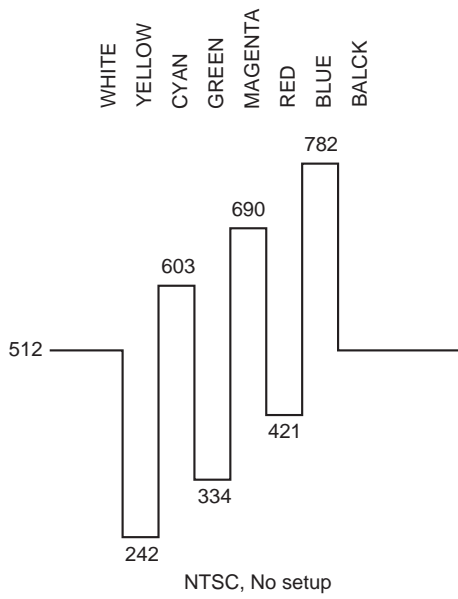
RGB Signal Output Waveform



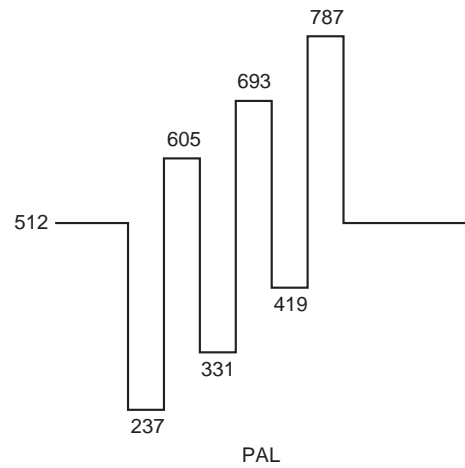
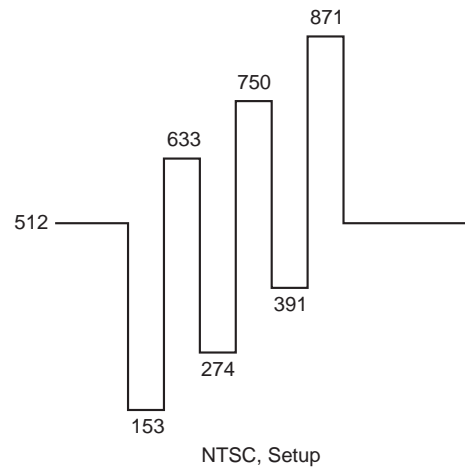
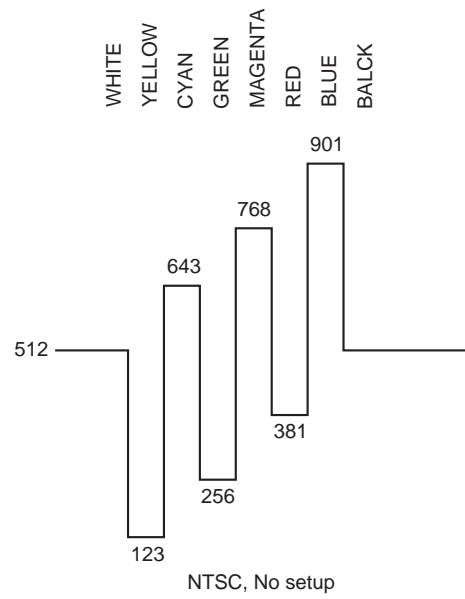
UV Output Level

Color Difference (U) Signal

SMPTE LEVEL

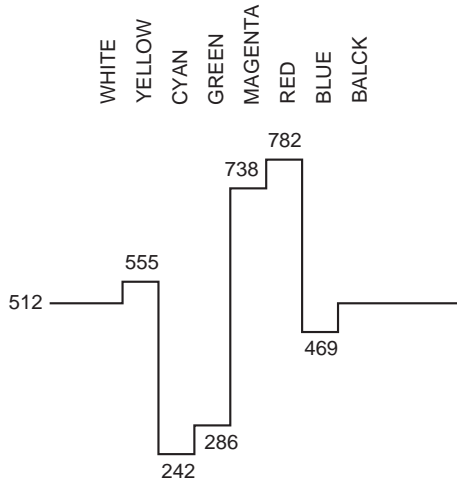


BetaCam LEVEL

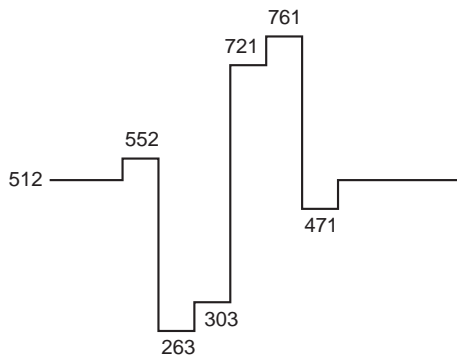


Color Difference (V) Signal

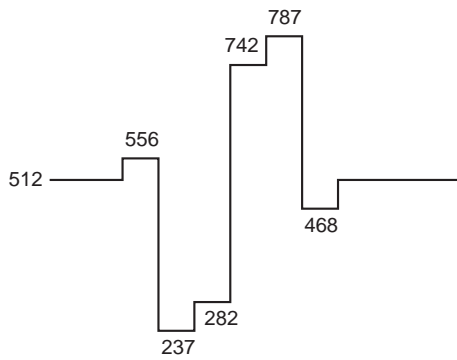
SMPTE LEVEL



NTSC, No setup

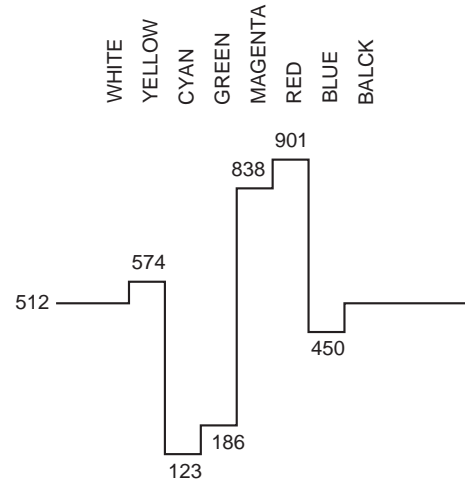


NTSC, Setup

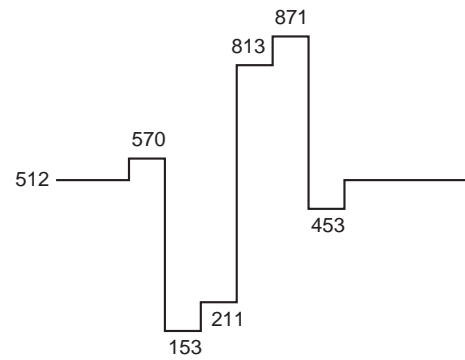


PAL

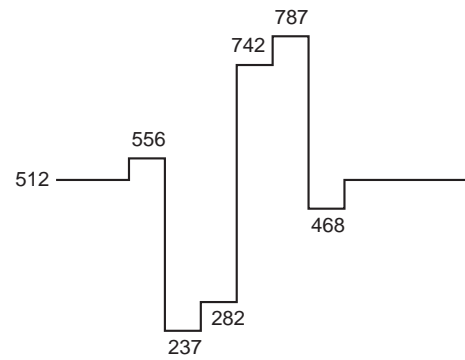
BetaCam LEVEL



NTSC, No setup

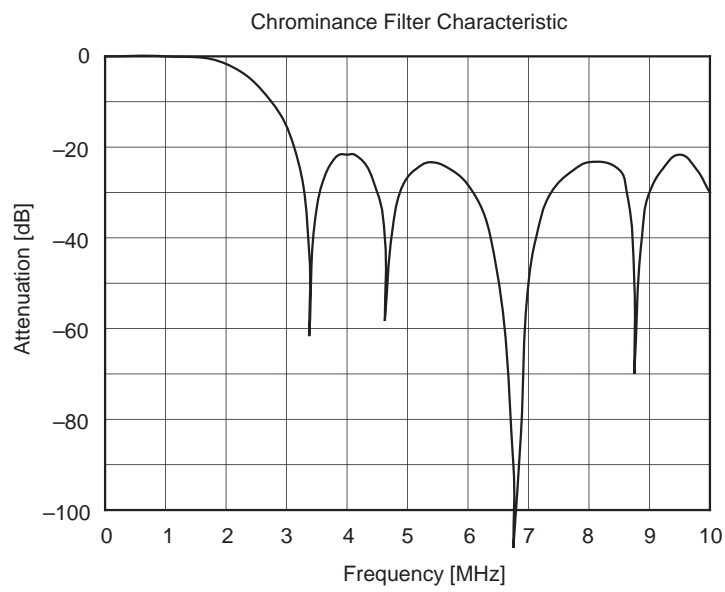
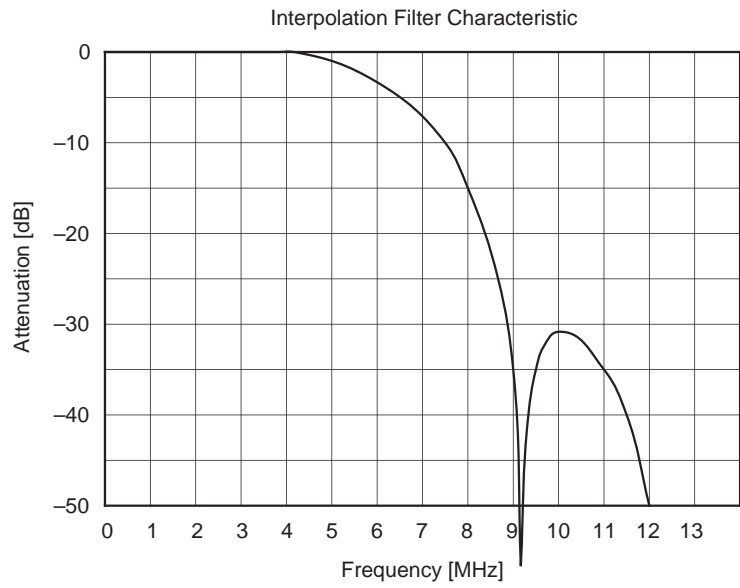


NTSC, Setup

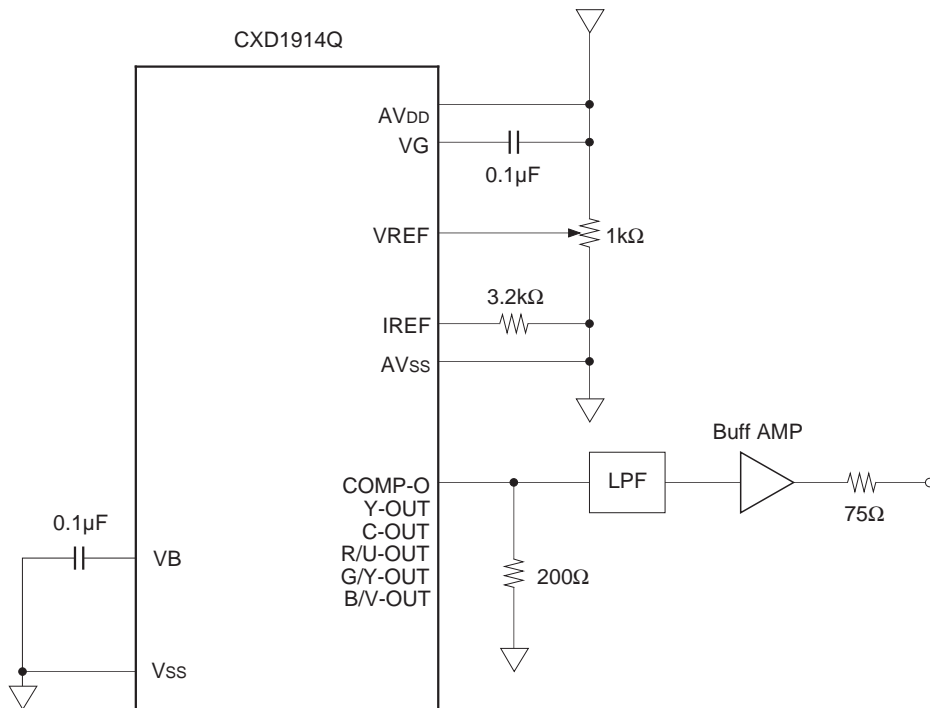


PAL

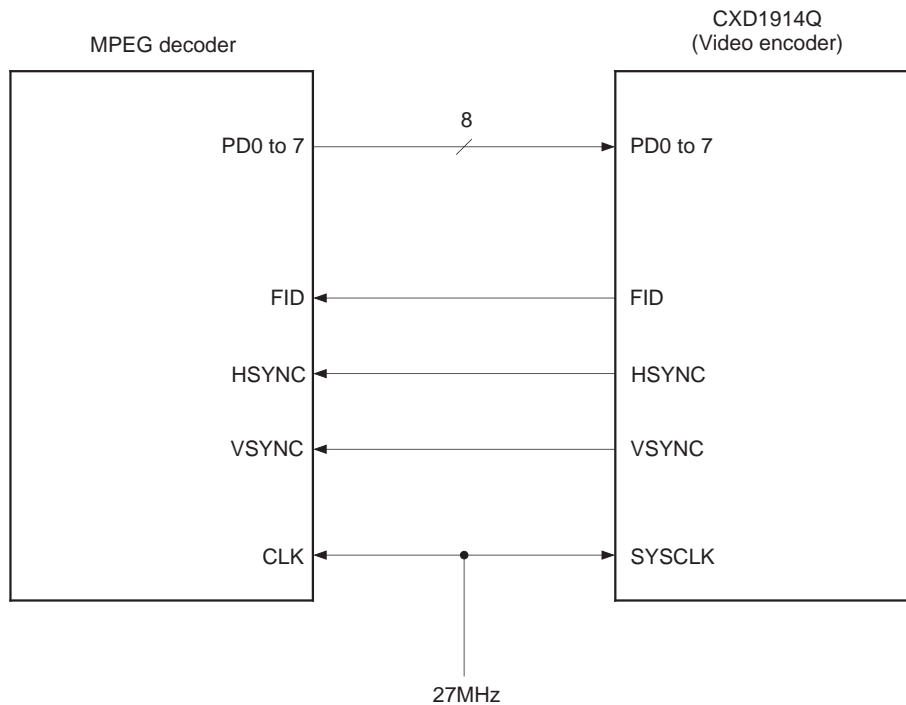
Internal Filter Characteristics



DAC Application Circuit



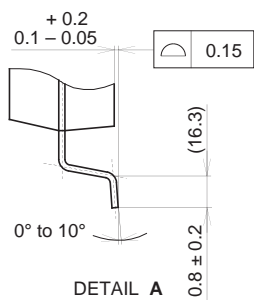
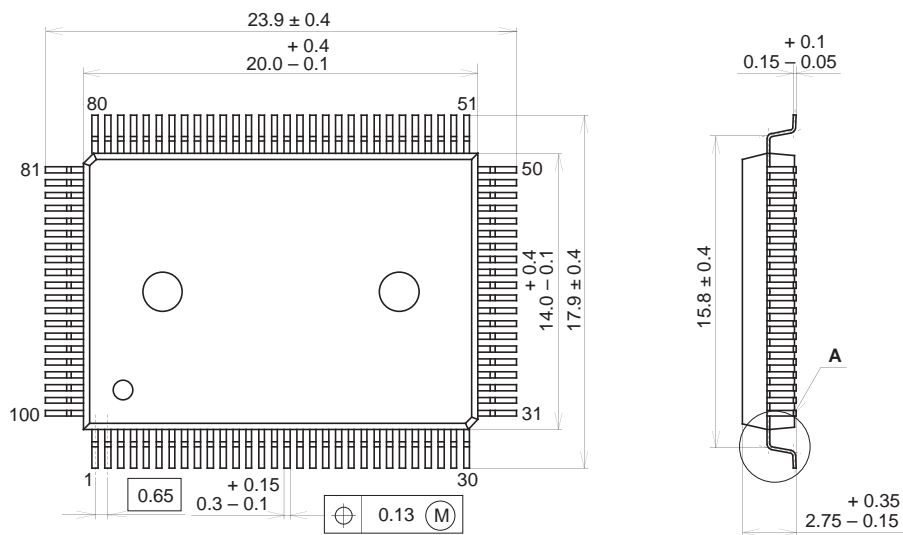
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit : mm

100PIN QFP (PLASTIC)



SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	_____

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g



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