SONY

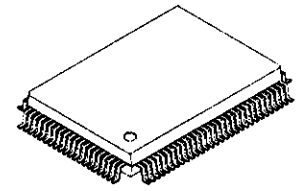
CXD1808AQ

CD-ROM Decoder

Description

The CXD1808AQ is a CD-ROM decoder LSI with a built-in subcode decoder.

100 pin QFP (Plastic)



Features

- Compatible with the CD-ROM, CD-I, and CD-ROM XA formats
- Real-time error correction
- Compatible with up to quadruple-speed playback
- Multiblock automatic transfer function
- The sub CPU can read subcode Q data byte by byte
- Real-time error correction of subcodes (R to W)
- Serial command transfer function to the CD DSP
- 5.6MB/s maximum transfer speed to host when decoding is on (with a clock frequency of 33.8688MHz and 2.4x playback or less)
- 6.7MB/s maximum transfer speed to host when decoding is off (with a clock frequency of 33.8688MHz)
- Permits connection with up to 1M bits (128K bytes) of standard SRAM
- Permits connection with up to 4M bits (512K bytes) of standard DRAM
- Permits connection with up to 1M bits (128K bytes) of standard pseudo-SRAM
- Permits direct connection with Sony's SCSI controller CXD1185CQ
- Intel CPU 80 series interface

Applications

CD-ROM drives

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (Ta = 25℃)

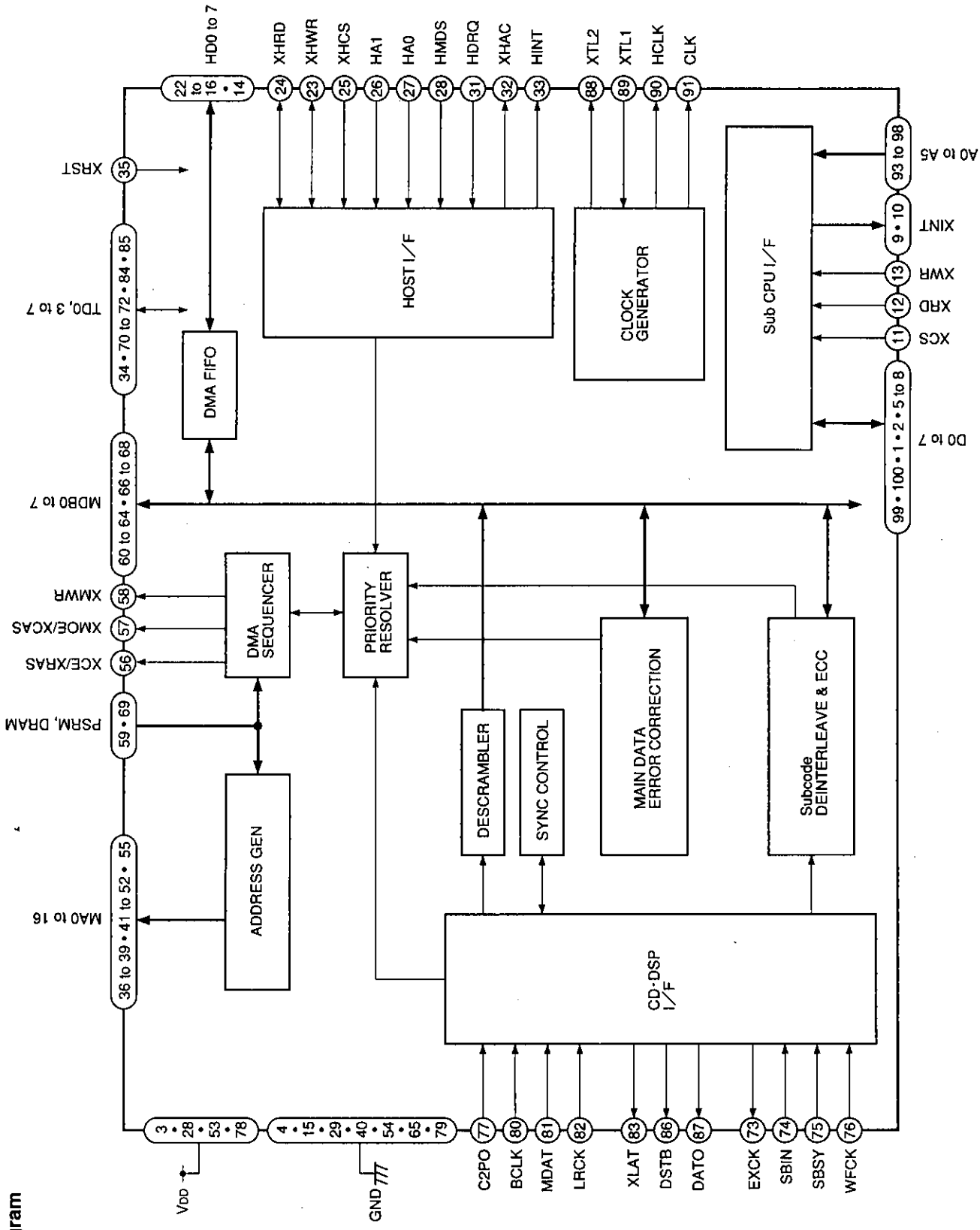
• Supply voltage	V_{DD}	−0.5 to +7.0	V
• Input voltage	V_I	−0.5 to V_{DD}+0.5	V
• Output voltage	V_O	−0.5 to V_{DD}+0.5	V
• Operating temperature	Topr	−20 to +75	℃
• Storage temperature	Tstg	−55 to +150	℃

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature	Topr	−20 to +75	℃

E94Z23A58—ST

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1	D2	I/O	Sub CPU data bus
2	D3	I/O	Sub CPU data bus
3	V_{DD}	—	Power supply (+5V)
4	GND	—	GND
5	D4	I/O	Sub CPU data bus
6	D5	I/O	Sub CPU data bus
7	D6	I/O	Sub CPU data bus
8	D7	I/O	Sub CPU data bus
9	INT0	O	Interrupt request from this IC to sub CPU
10	INT1	O	Interrupt request from this IC to sub CPU
11	XCS	I	IC select negative logic signal from sub CPU
12	XWR	I	Strobe negative logic signal to write this IC's internal registers from sub CPU
13	XRD	I	Strobe negative logic signal to read this IC's internal registers from sub CPU
14	HD7	I/O	Host data bus
15	GND	—	GND
16	HD6	I/O	Host data bus
17	HD5	I/O	Host data bus
18	HD4	I/O	Host data bus
19	HD3	I/O	Host data bus
20	HD2	I/O	Host data bus
21	HD1	I/O	Host data bus
22	HD0	I/O	Host data bus
23	XHWR	I/O	Strobe negative logic signal to write this IC's internal registers from host; or strobe signal to write data to SCSI controller IC
24	XHRD	I/O	Strobe negative logic signal to read this IC's internal registers from host; or strobe signal to read data to SCSI controller IC
25	XHCS	I	IC select negative logic signal from host
26	HA0	I	Host address signal
27	HA1	I	Host address signal
28	V_{DD}	—	Power supply (+5V)
29	GND	—	GND
30	HMDS	I	Host mode select signal
31	HDRQ XSAC	O	Host DMA request positive logic signal DMA acknowledge negative logic signal to SCSI controller IC
32	XHAC SDRQ	I	Host DMA acknowledge negative logic signal DMA data request positive logic signal from SCSI controller IC
33	HINT	O	Interrupt request negative logic signal to host; open drain output

Pin No.	Symbol	I/O	Description
34	TD0	I/O	Test I/O
35	XRST	I	Reset negative logic signal
36	MA0	O	Buffer memory address (LSB)
37	MA1	O	Buffer memory address
38	MA2	O	Buffer memory address
39	MA3	O	Buffer memory address
40	GND	–	GND
41	MA4	O	Buffer memory address
42	MA5	O	Buffer memory address
43	MA6	O	Buffer memory address
44	MA7	O	Buffer memory address
45	MA8	O	Buffer memory address
46	MA9	O	Buffer memory address
47	MA10	O	Buffer memory address
48	MA11	O	Buffer memory address
49	MA12	O	Buffer memory address
50	MA13	O	Buffer memory address
51	MA14	O	Buffer memory address
52	MA15	O	Buffer memory address
53	V_{DD}	–	Power supply (+5V)
54	GND	–	GND
55	MA16	O	Buffer memory address
56	XCE XRAS	O	Buffer memory chip enable (PSRAM); or, row address strobe signal (DRAM)
57	XMOE XCAS	O	Buffer memory output enable negative logic signal (PSRAM); or, column address strobe signal (DRAM)
58	XMWR	O	Buffer memory write enable negative logic signal
59	XPS	I	Buffer memory PSRAM select
60	MDB0	I/O	Buffer memory data bus
61	MDB1	I/O	Buffer memory data bus
62	MDB2	I/O	Buffer memory data bus
63	MDB3	I/O	Buffer memory data bus
64	MDB4	I/O	Buffer memory data bus
65	GND	–	GND
66	MDB5	I/O	Buffer memory data bus
67	MDB6	I/O	Buffer memory data bus
68	MDB7	I/O	Buffer memory data bus

Pin No.	Symbol	I/O	Description
69	DRAM	I	DRAM/SRAM switching input
70	TD3	I/O	Test I/O
71	TD4	I/O	Test I/O
72	TD5	I/O	Test I/O
73	EXCK	O	SBIN signal strobe clock signal
74	SBIN	I	Subcode data serial input signal
75	SCOR	I	Subcode sync signal
76	WFCK	I	Write frame clock input signal
77	C2PO	I	Error flag (C2 pointer) positive logic signal from CD DSP
78	V_{DD}	—	Power supply (+5V)
79	GND	—	GND
80	BCLK	I	DATA signal strobe clock signal (bit clock)
81	MDAT	I	Data signal from CD DSP
82	LRCK	I	LR clock signal from CD DSP (for L and R channel discrimination)
83	XLAT	O	DATO signal latch signal
84	TD6	I/O	Test I/O
85	TD7	I/O	Test I/O
86	DSTB	O	DATO signal transfer clock output
87	DATO	O	Serial data output to CD DSP
88	XTL2	O	Crystal oscillation circuit output
89	XTL1	I	Crystal oscillation circuit input
90	GND	—	GND
91	HCLK	O	Clock output with half the frequency as that input to XTL1
92	CLK	O	Clock output with the same frequency as that input to XTL1
93	A0	I	Sub CPU address
94	A1	I	Sub CPU address
95	A2	I	Sub CPU address
96	A3	I	Sub CPU address
97	A4	I	Sub CPU address
98	A5	I	Sub CPU address
99	D0	I/O	Sub CPU data bus
100	D1	I/O	Sub CPU data bus

Electrical Characteristics

DC characteristics

(V_{DD} = 5V±10%, V_{SS} = 0V, Topr = −20 to +75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
TTL input level pin *1 High level input voltage	V_{IH1}		2.2			V
TTL input level pin *1 Low level input voltage	V_{IL1}				0.8	V
CMOS input level pin *2 High level input voltage	V_{IH2}		0.7V_{DD}			V
CMOS input level pin *2 Low level input voltage	V_{IL2}				0.3V_{DD}	V
CMOS Schmitt input level pin *3 High level input voltage	V_{IH4}		0.8V_{DD}			V
CMOS Schmitt input level pin *3 Low level input voltage	V_{IL4}				0.2V_{DD}	V
CMOS Schmitt input level pin *3 Input voltage hysteresis	V_{IH4}–V_{IL4}			0.6		V
TTL Schmitt input level pin *4 High level input voltage	V_{IH5}		2.2			V
TTL Schmitt input level pin *4 Low level input voltage	V_{IL5}				0.8	V
TTL Schmitt input level pin *4 Input voltage hysteresis	V_{IH5}–V_{IL4}			0.4		V
Bi-directional pin with pull-up resistance value *5 Input current	I_{IL3}	V_{IN} = 0V	−90	−200	−440	µA
Input pin with pull-up resistance *6 Input current	I_{IL4}	V_{IN} = 0V	−40	−100	−240	µA
High level output voltage *7	V_{OH1}	I_{OH} = −2mA	V_{DD}−0.8			V
Low level output voltage *7	V_{OL1}	I_{OL} = 4mA			0.4	V
Input leak current *8	I_{I1}	V_{IN} = V_{SS} or V_{DD}	−10		10	µA
Output leak current *9	I_{OZ}	High-impedance state	−40		40	µA
Oscillation cell *10 high level input voltage	V_{IH4}		0.7V_{DD}			V
Oscillation cell low level input voltage	V_{IL4}				0.3V_{DD}	V
Oscillation cell logic threshold value	LV_{TH}			0.5V_{DD}		V
Oscillation cell feedback resistance	R_{FB}	V_{IN} = V_{SS} or V_{DD}	250K	1M	2.5M	Ω
Oscillation cell High level output voltage	V_{OH2}	I_{OH} = −3mA	0.5V_{DD}			V
Oscillation cell Low level output voltage	V_{OL2}	I_{OL} = 3mA			0.5V_{DD}	V

*1 D7 to 0, HD7 to 0, HA1, HA0, XHCS, MDB7 to 0, TD1, TD0
*2 DATA, LRCK, C2PO, EMP, SBIN, SBSY, WFCK, XPS
*3 BCLK, XRST
*4 A5 to 0, XWR, XRD, XCS, XHWR, XHRD, XHAC, XPS
*5 D7 to 0, MDB7 to 0, HD7 to 0, TD1, TD0
*6 HA1, HA0, XHAC
*7 All output pins except XTL2
*8 All input pins except *5, *6, and XTL1
*9 HINT
*10 Input: XTL1; output: XTL2

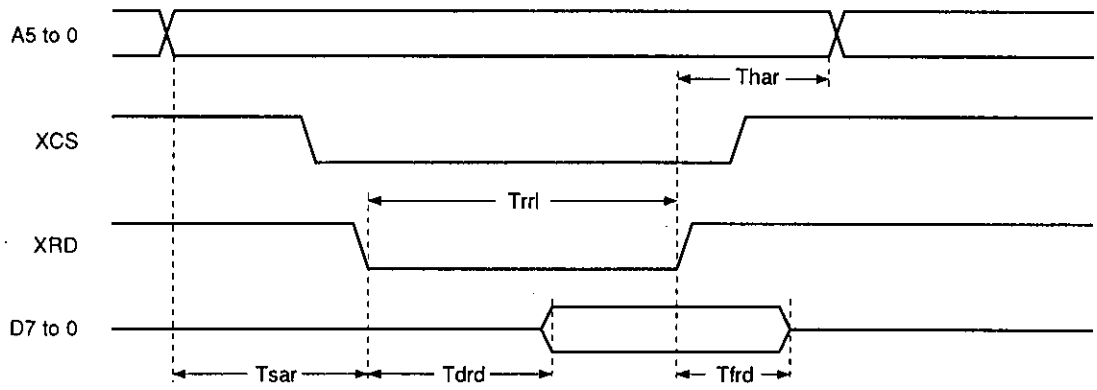
I/O Capacitance (V_{DD} = V_I = 0V, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			9	pF
Output pin	C_{OUT}			11	pF
Input/output pin	$C_{I/O}$			11	pF

AC Characteristics (V_{DD} = 5V±10%, Vss = 0V, Topr = −20 to +75°C)

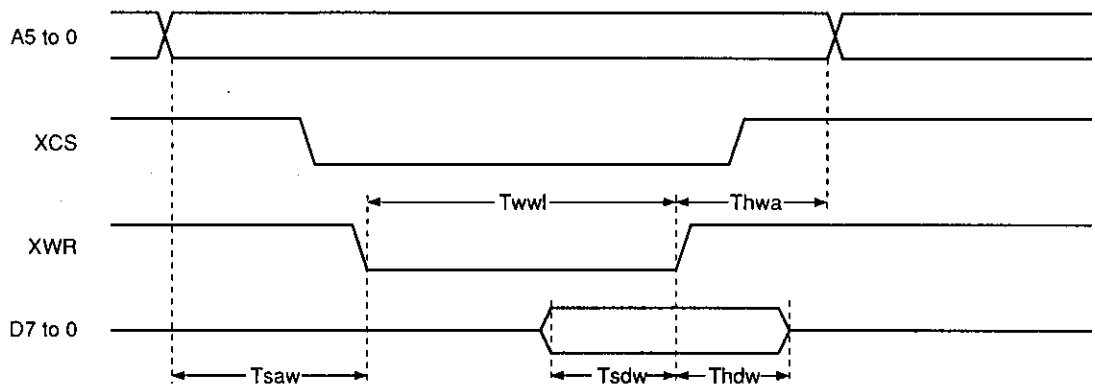
1. Sub CPU interface (Output load = 50pF)

(1) Read



Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (for XCS & XRD ↓)	Tsar	10			ns
Address hold time (for XCS & XRD ↑)	Thar	10			ns
Data delay time (for XCS & XRD ↓)	Tdrd			35	ns
Data float time (for XCS & XRD ↑)	Tfrd	0		15	ns

(2) Write

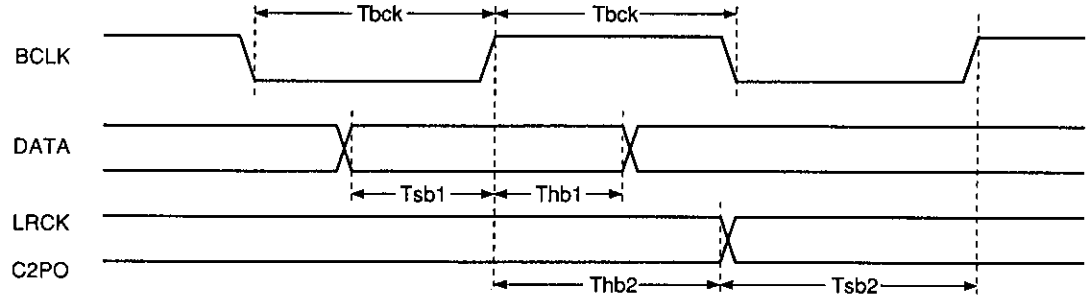


Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (for XCS & XWR ↓)	Tsaw	20			ns
Address hold time (for XCS & XWR ↑)	Thaw	10			ns
Data setup time (for XCS & XWR ↓)	Tsdw	20			ns
Data hold time (for XCS & XWR ↑)	Thdw	10			ns
Low level XWR pulse width	Twwl	30			ns

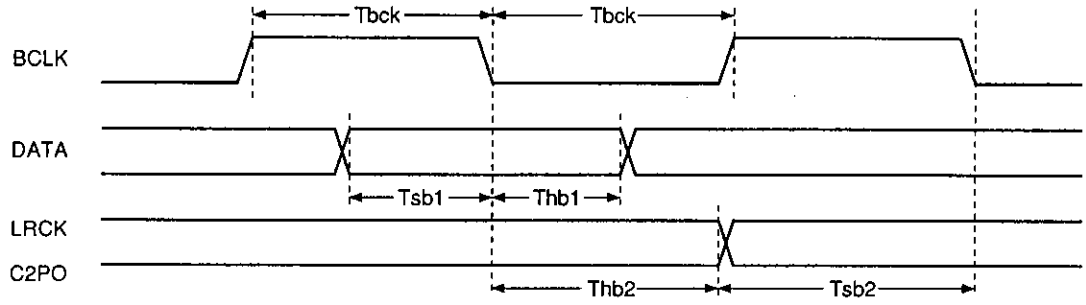
The "&" symbol in the tables indicates "logical product".

2. CD DSP interface

BCKRED = "H"



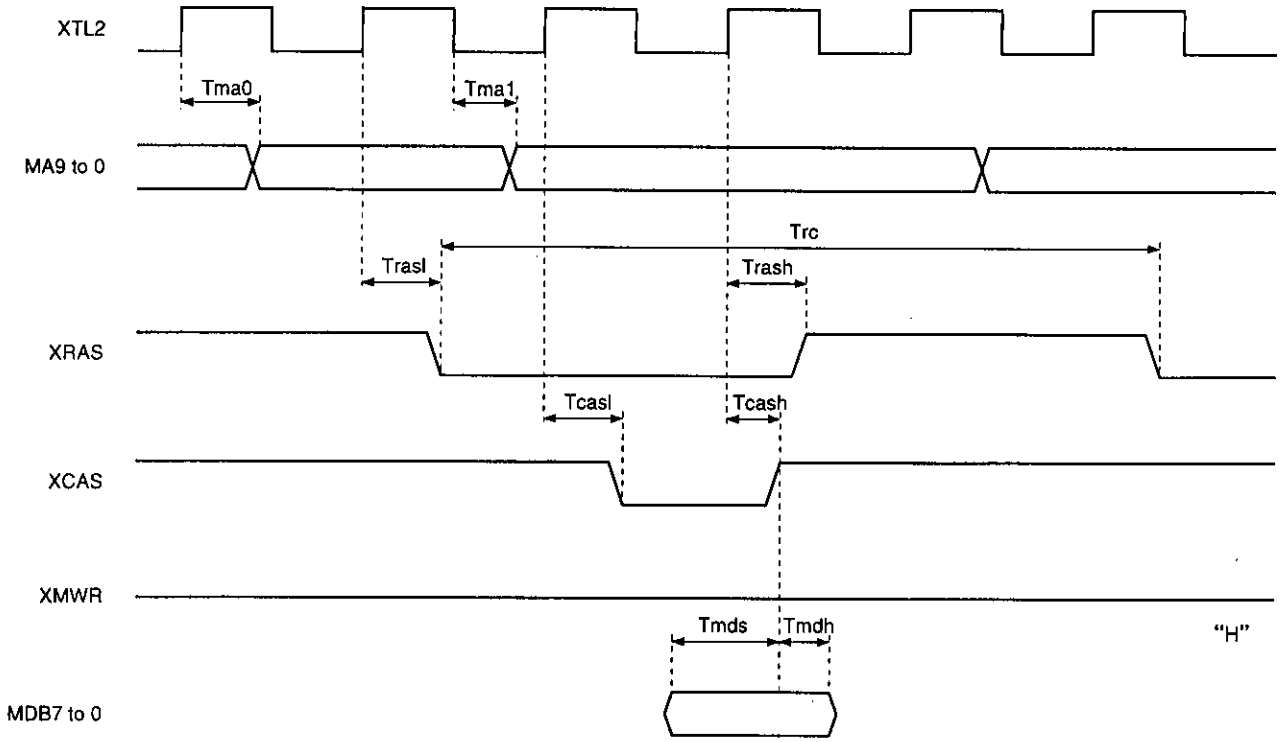
BCKRED = "L"



Item	Symbol	Min.	Typ.	Max.	Unit
BCLK frequency	Fbck			26	MHz
BCLK pulse width	Tbck	19			ns
DATA setup time (for BCLK)	Tsb1	12			ns
DATA hold time (for BCLK)	Thb1	12			ns
LRCK, C2PO setup time (for BCLK)	Tsb2	12			ns
LRCK, C2PO hold time (for BCLK)	Thb2	12			ns

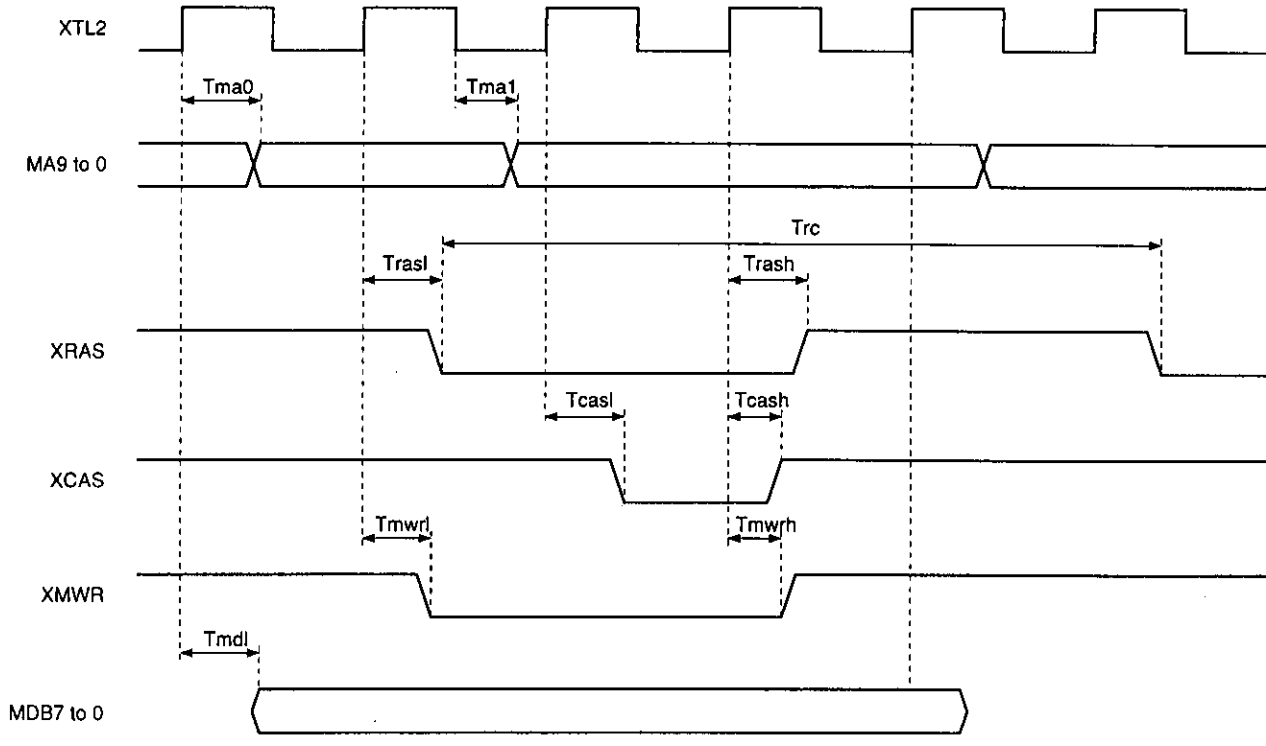
3. DRAM interface (Output load = 30pF)

(1) Read



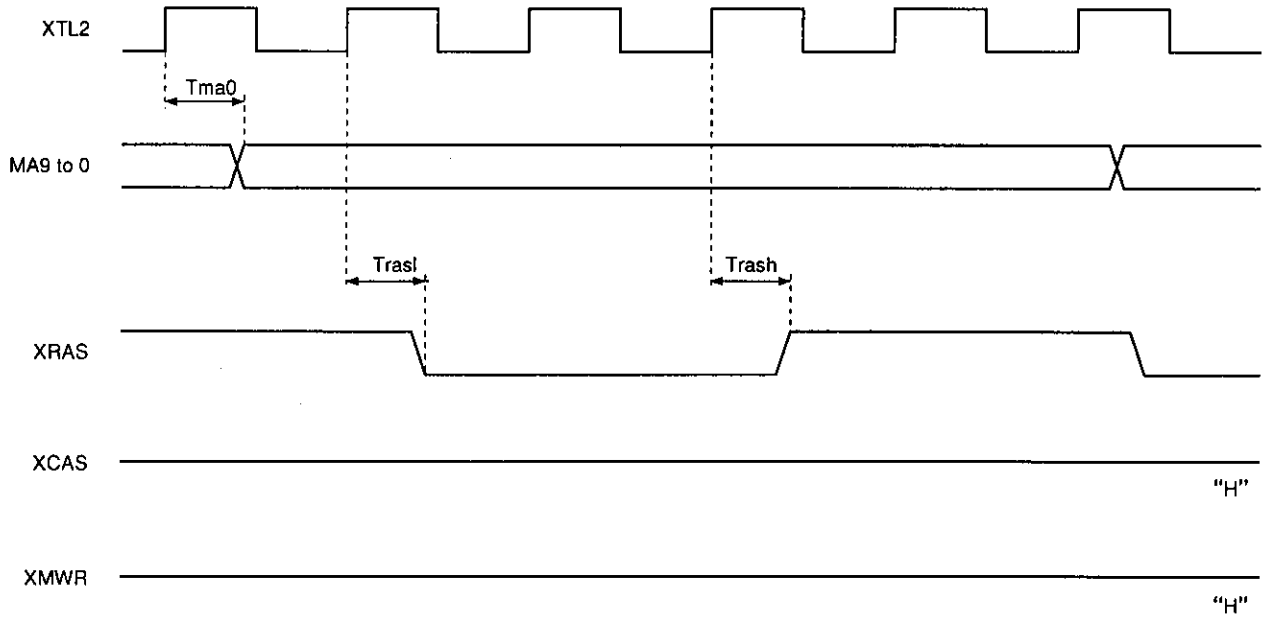
Item	Symbol	Min.	Typ.	Max.	Unit
Random read/write cycle time	Trc	4Tw			ns
Address delay time (for XTL2 ↑)	Tma0		17	29	ns
Address delay time (for XTL2 ↓)	Tma1		15	25	ns
XRAS ↓ delay time (for XTL2 ↑)	Trasl		10	17	ns
XRAS ↑ delay time (for XTL2 ↑)	Trash		11	19	ns
XCAS ↓ delay time (for XTL2 ↑)	Tcasl		9	15	ns
XCAS ↑ delay time (for XTL2 ↑)	Tcash		10	17	ns
Data setup time (for XCAS ↑)	Tmds		9	14	ns
Data hold time (for XCAS ↓)	Tmdh	0			ns

(2) Write



Item	Symbol	Min.	Typ.	Max.	Unit
Random read/write cycle time	Trc	4Tw			ns
Address delay time (for XTL2 ↑)	Tma0		17	29	ns
Address delay time (for XTL2 ↓)	Tma1		15	25	ns
XRAS ↓ delay time (for XTL2 ↑)	Trasl		10	17	ns
XRAS ↑ delay time (for XTL2 ↑)	Trash		11	19	ns
XCAS ↓ delay time (for XTL2 ↑)	Tcasl		9	15	ns
XCAS ↑ delay time (for XTL2 ↑)	Tcash		10	17	ns
XMWR ↓ delay time (for XTL2 ↑)	Tmwrl		9	15	ns
XMWR ↑ delay time (for XTL2 ↑)	Tmwrh		10	17	ns
Data delay time (for XTL2 ↑)	Tmds		19	32	ns

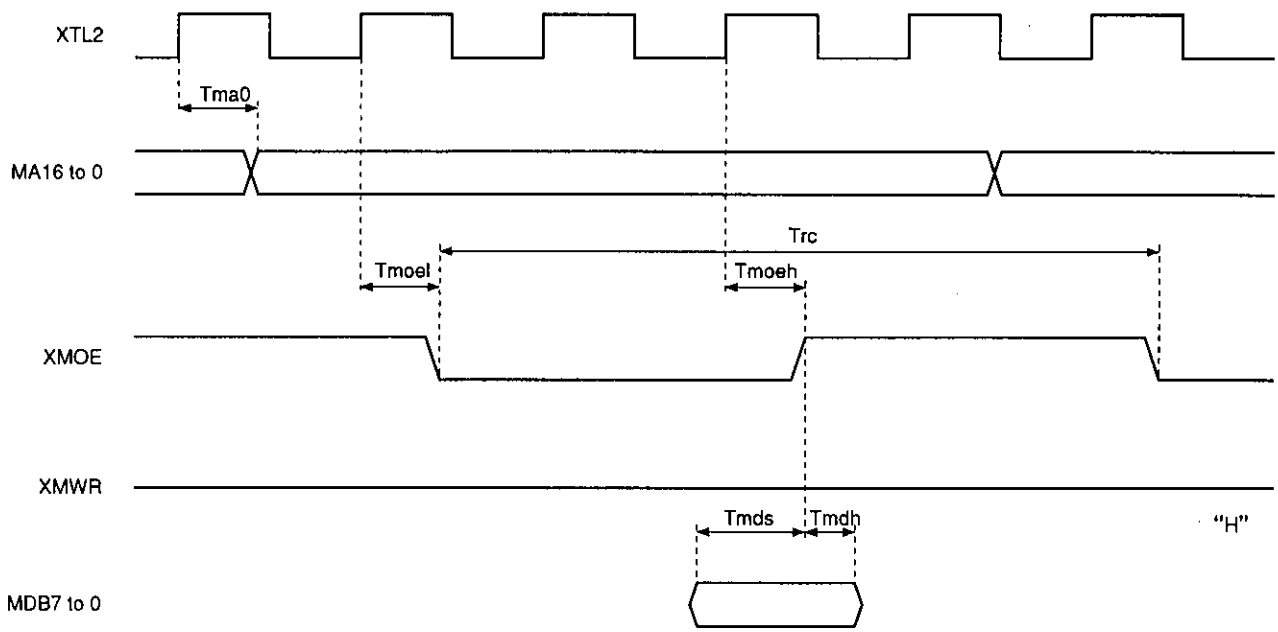
(3) Refresh (RAS-only refresh)



Item	Symbol	Min.	Typ.	Max.	Unit
Random read/write cycle time	Trc	4Tw			ns
Address delay time (for XTL2 ↑)	Tma0		17	29	ns
XRAS ↓ delay time (for XTL2 ↑)	Trasl		10	17	ns
XRAS ↑ delay time (for XTL2 ↑)	Trash		11	19	ns

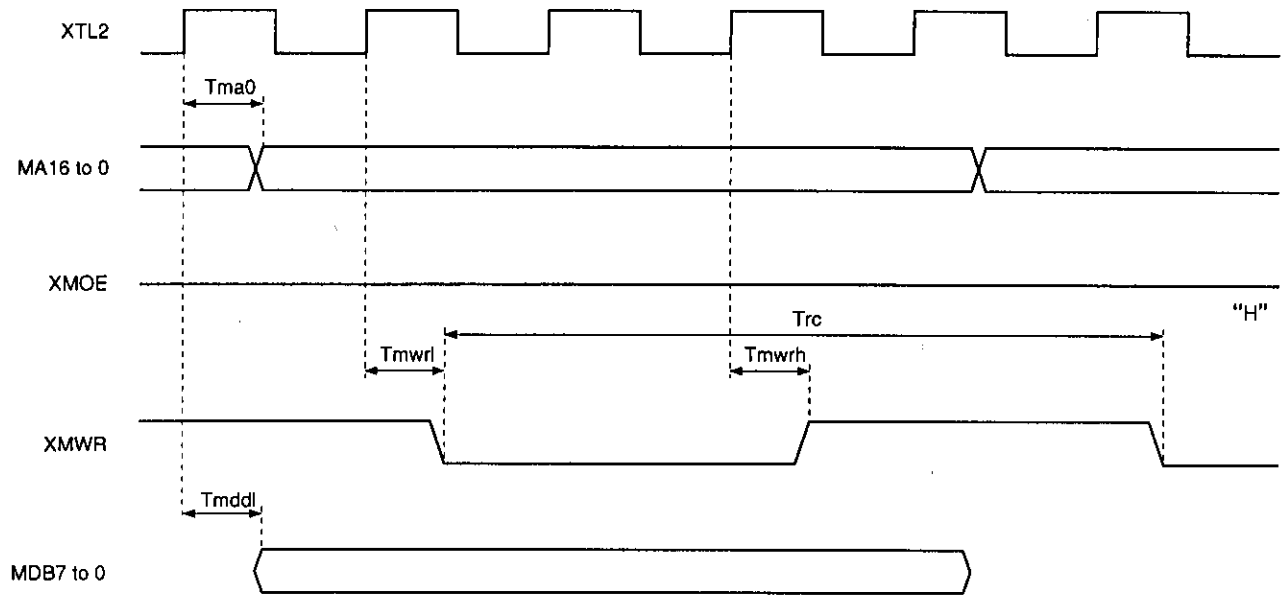
4. SRAM interface (Output load = 30pF)

(1) Read



Item	Symobl	Min.	Typ.	Max.	Unit
Random read/write cycle time	Trc	4Tw			ns
Address delay time (for XTL2 ↑)	Tma0		19	32	ns
XMOE ↓ delay time (for XTL2 ↑)	Tmoel		10	17	ns
XMOE ↑ delay time (for XTL2 ↑)	Tmoeh		10	17	ns
Data setup time (for XMOE ↑)	Tmds		9	15	ns
Data hold time (for XMOE ↓)	Tmdh	0			ns

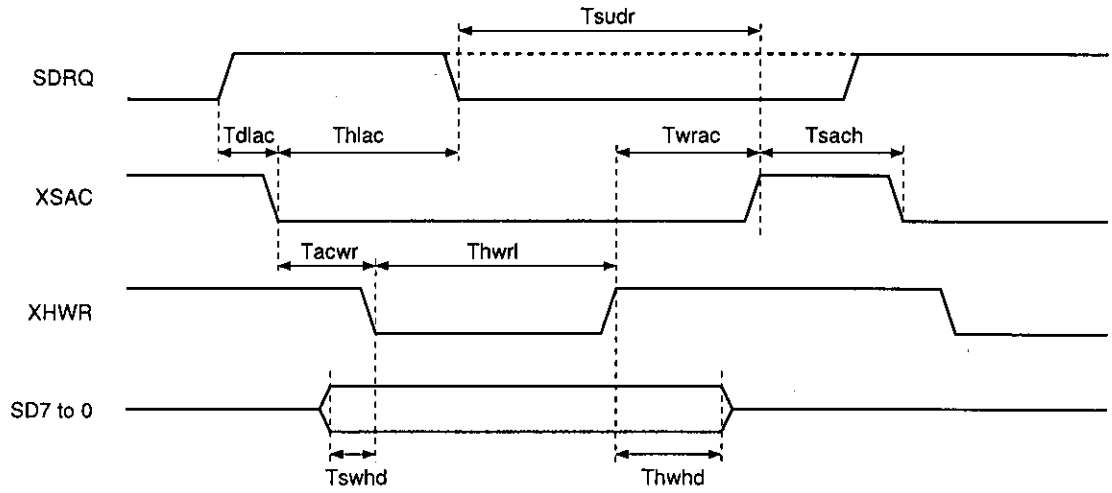
(2) Write



Item	Symbol	Min.	Typ.	Max.	Unit
Random read/write cycle time	Trc	4Tw			ns
Address delay time (for XTL2 ↑)	Tma0		19	32	ns
XMWR ↓ delay time (for XTL2 ↑)	Tmwrl		10	17	ns
XMWR ↑ delay time (for XTL2 ↑)	Tmwrh		10	17	ns
Data delay time (for XTL2 ↑)	Tmddl		20	34	ns

5. SCSI IC interface (Output load = 30pF)

(1) to SCSI IC



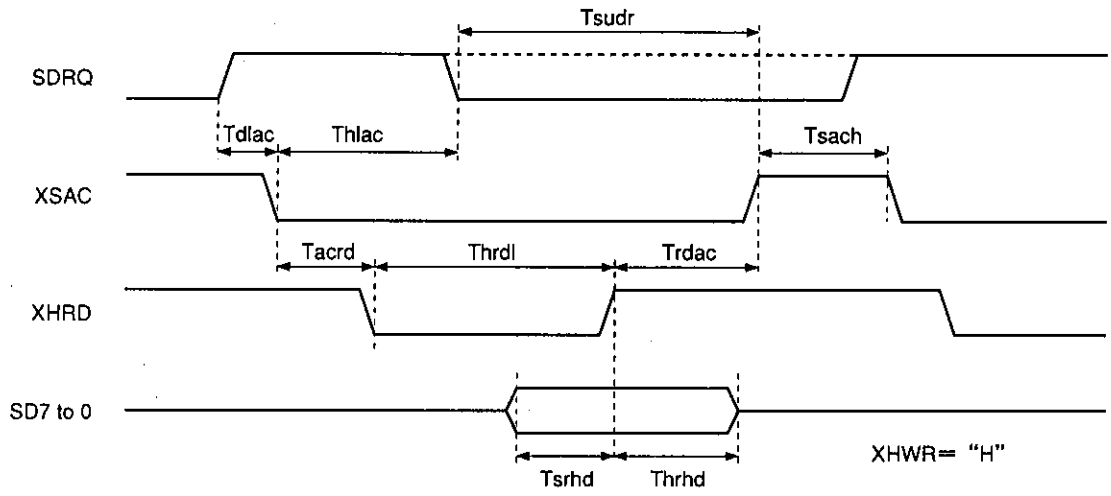
Item	Symbol	Min.	Typ.	Max.	Unit
XSAC fall delay time (for SDRQ ↑)	Tdlac	0			ns
XSAC setup time (for XSWR ↓)	Tacwr	Tw			ns
XSAC hold time (for XSWR ↑)	Twrac	Tw–9			ns
Data setup time (for XSWR ↓)	Tswhd	Tw–14			ns
Data hold time (for XSWR ↑)	Thwhd	Tw–11			ns
XHWR low pulse width	Thwrl	(m–2) x Tw			ns
XSAC high pulse width	Tsach	T_1–1			ns
SDRQ fall hold time (for XSAC ↑)	Thlac	0			ns
SDRQ fall setup time (for XSAC ↑)	Tsudr	0			ns

$$T_1 = \begin{cases} \text{Tw (XFRRATE1, 0 = "L", "L")} \\ \text{(n–m) x Tw} \end{cases}$$

m: Number of cycles determined by SXFRCYC1, 0

n: Number of cycles determined by XFRRATE1, 0

(2) from SCSI IC



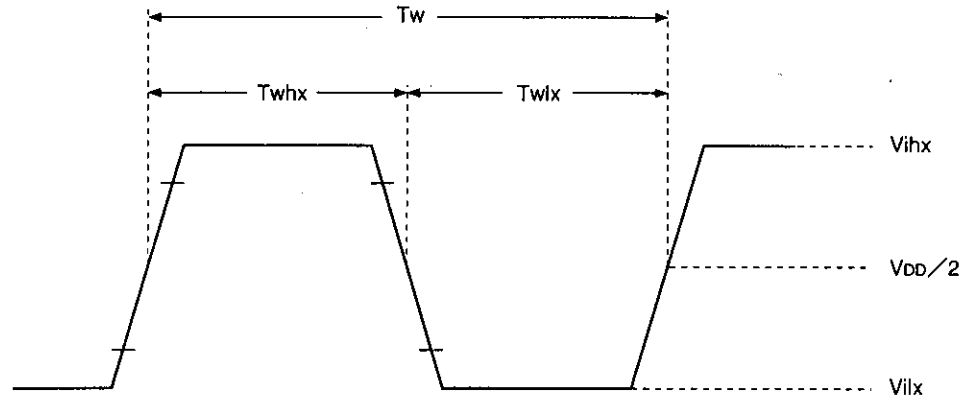
Item	Symbol	Min.	Typ.	Max.	Unit
XSAC fall delay time (for SDRQ ↑)	Tdlac	0			ns
XSAC setup time (for XHRD ↓)	Tacrd	0			ns
XSAC hold time (for XHRD ↑)	Trdac	Tw–9			ns
Data setup time (for XHRD ↑)	Tsrhd	18			ns
Data hold time (for XHRD ↑)	Thrhd	0			ns
XHRD low pulse width	Thwrl	(m–1) x Tw			ns
XSAC high pulse width	Thwrh	T_1–1			ns
SDRQ fall hold time (vs. XSAC ↓)	Thlac	0			ns
SDRQ fall setup time (vs. XSAC ↑)	Tsudr	0			ns

7. XTL1 pin, XTL2 pin

(1) For self-excited oscillation

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency	Fmax			40.0	MHz

(2) When a pulse is input to XTL1 pin



Item	Symbol	Min.	Typ.	Max.	Unit
High level pulse width	Twhx	10			ns
Low level pulse width	Twlx	10			ns
Pulse cycle	Tw	25			ns

1. Pin Description

The pin descriptions by function are given below.

1-1. CD player interface (11pins)

This interface enables direct connection with Sony's digital signal processor LSI for CD players. Digital signal processor LSI for CD players is hereafter called "CD DSP".

(1) MDAT (medium DATA: input)
Serial data stream from the CD DSP.

(2) BCLK (bit clock: input)
Bit clock signal; MDAT signal strobe.

(3) LRCK (LR clock: input)
LR clock signal; indicates the left or right channel for the MDAT signal.

(4) C2PO (C2 pointer: input)
C2 pointer signal; indicates that the MDAT input contains an error.

(5) WFCK (write frame clock: input)
Write frame clock input signal; connect to the WFCK pin (Pin 62) of the CXD2500.

(6) SCOR (subcode sync OR: input)
Subcode sync signal; connect to the SCOR pin (Pin 63) of the CXD2500.

(7) SBIN (subcode serial input: input)
Subcode serial signal; connect to the SBSO pin (Pin 64) of the CXD2500.

(8) EXCK (external clock: output)
Clock output used to read the SBIN signal; connect to EXCK pin (Pin 65) of the CXD2500.

(9) DATO (DATA output: output)
Serial data output from the sub CPU to the CD DSP.

(10) DSTB (data strobe: output)
DATO transfer clock output.

(11) XLAT (latch: output)
DATO latch signal; DATO is latched at the falling edge of XLAT.

1-2. Buffer memory interface (28 pins)

The table below shows the types of the buffer memory that can be connected to this IC.

Size	SRAM	DRAM	PSRAM
32KB (256Kbit)	$32K^{w} \times 8^{b}$	Not permitted	$32K^{w} \times 8^{b}$
64KB (512Kbit)	Not permitted	Not permitted	$64K^{w} \times 8^{b}$
128KB (1Mbit)	$128K^{w} \times 8^{b}$	$128K^{w} \times 8^{b}$ *1	$128K^{w} \times 8^{b}$
256KB (2Mbit)	Not permitted	$256K^{w} \times 4^{b} \times 2$ or $256K^{w} \times 8^{b}$	Not permitted
512KB (4Mbit)	Not permitted	$512K^{w} \times 8^{b}$	Not permitted

*1 CXD1808AQ can be connected to $128K^{w} \times 8^{b}$ DRAM which has 8 row addresses and 9 column addresses.

(1) DRAM (buffer memory DRAM: input)
Input a low signal when SRAM or PSRAM is connected as buffer memory.
Input a high signal when DRAM is connected as buffer memory.

(2) XPS (/buffer memory PSRAM: input)
Input a high signal or leave open when SRAM or DRAM is connected as buffer memory.
Input a low signal when PSRAM is connected as buffer memory.

(3) XMWR (buffer memory write: output)
Strobe negative logic output signal for writing data to buffer memory.

(4) XMOE/XCAS (buffer memory output enable/column address strobe: output)
Strobe negative logic output signal for reading data to buffer memory when connected to SRAM or PSRAM. When connected to DRAM, serves as the XCAS (column address strobe, negative logic) signal.

(5) MA0 to 16 (buffer memory address: output)
Address signals for buffer memory; when connected to DRAM, only MA0 to 9 are valid.

(6) XRAS/XCE (row address strobe/chip enable: output)
When connected to DRAM, serves as the XRAS (row address strobe, negative logic) signal. When connected to PSRAM, serves as chip enable negative logic signal.

(7) MDB0 to 7 (buffer memory data bus: input/output)
Buffer memory data bus signals; pulled up by standard 25KΩ resistance.

1-3. Sub CPU interface (19pins)

(1) XWR (sub CPU write: input)
Strobe negative logic signal for writing to the IC's internal registers.

(2) XRD (sub CPU read: input)
Strobe negative logic signal for reading the status information in the IC's internal registers.

(3) D0 to 7 (sub CPU data bus: input/output)
8-bit data bus.

(4) A0 to 5 (sub CPU address: input)
Address signals for selecting IC's internal registers from the sub CPU.

(5) INT0, 1 (sub CPU interrupt: output)
Interrupt request signal to the sub-CPU; open drain. Polarity can be controlled by the sub CPU.

(6) XCS (chip select: input)
IC select negative logic signal from the sub CPU.

1-4. Host interface (17pins)

(1) HMDS (host mode select: input)
Input a low signal when connected to an 80 series host.
Input a high signal when connected to the SCSI controller.

(2) HDRQ/XSAC (host DMA request/SCSI DMA acknowledge: output)
DMA data request positive logic signal to host when HMDS is low; DMA acknowledge negative logic signal to the SCSI controller IC when HMDS is high.

(3) XHAC/SDRQ (host DMA acknowledge/SCSI data request: input)
DMA acknowledge negative logic signal from host when HMDS is low; DMA data request positive logic signal from the SCSI controller IC when HMDS is high.

(4) XHWR (host write: input/output)
Data write strobe input from host when HMDS is low; data write strobe output to the SCSI controller IC when HMDS is high.

(5) XHRD (host read: input/output)
Data read strobe input from host when HMDS is low; data read strobe output to the SCSI controller IC when HMDS is high.

(6) XHCS (host chip select: input)
IC select negative logic signal from host when HMDS is low; not used when HMDS is high.

(7) HA0, 1 (host address: input)
Address signals used by host to select the IC's internal registers when HMDS is low; not used when HMDS is high.

(8) HD0 to 7 (host data bus: input/output)
Host data bus signals.

(9) HINT (host interrupt: output)
Interrupt request output signal for host when HMDS is low; open drain. The polarity can be controlled by the sub CPU.
Not used when HMDS is high.

1-5. Others (5pins)

(1) XRST (reset: input)
Chip reset negative logic input signal.

(2) XTL1 (crystal 1: input)

(3) XTL2 (crystal 2: output)
Connect a crystal oscillator between XTL1 and XTL2. (The capacitor value depends on the crystal oscillator.)
Alternatively, input a clock signal to the XTL1 pin.

(4) CLK (clock: output)
Outputs a clock with the same frequency as that input to XTL1.
If this clock is not used, the CLK pin output can be fixed low.

(5) HCLK (half clock: output)
Outputs a clock with half the frequency as that input to XTL1.
If this clock is not used, the HCLK pin output can be fixed low.

1-6. Test pins (8pins)

(1) TD0 to 7
These are test pins used during the manufacture of the IC. Normally, they are left open.

2. Sub CPU Write Registers

2-1. CONFIG0 (configuration 0) register (address 00HEX)

bit 7: CINTPOL (sub CPU interrupt polarity)

High: The INT1 and 0 pins are active high. When inactive, they are low.

Low: The INT1 and 0 pins are active low. When inactive, they are high impedance.

bit 6: HINTPOL (host interrupt polarity)

High: The HINT pin is active high. When inactive, it is high impedance.

Low: The HINT pin is active low. When inactive, it is high impedance.

bits 5, 4: SXFRCY1, 0

These bits determine the number of cycles needed for data transfers between this IC and the SCSI controller IC. The sub CPU sets these bits according to the clock frequency and the AC characteristics of the SCSI controller IC.

SXFRSCY1	SXFRCY0	Number of transfer cycles
"L"	"L"	3
"L"	"H"	4
"H"	"L"	5
"H"	"H"	RESERVED

bit 3: EXCKSL (EXCK select)

This bit determines the EXCK clock frequency used to get the subcode from the CD DSP. The sub CPU sets this bit according to the XTL1 clock frequency and the playback speed. (The maximum frequency for EXCK is 1MHz.)

High: Sets the EXCK frequency to 1/48 that of the clock input to XTL1. Set this bit high when the frequency of XTL1 is greater than 32MHz.

Low: Sets the EXCK frequency to 1/32 that of the clock input to XTL1. Set this bit low when the frequency of XTL1 is 32MHz or less.

bit 2: DISCLK (disable CLK output)

High: The CLK pin is fixed low.

Low: The CLK pin outputs a clock with the same frequency as that input to XTL1.

bit 1: DISHCLK (disable HCLK output)

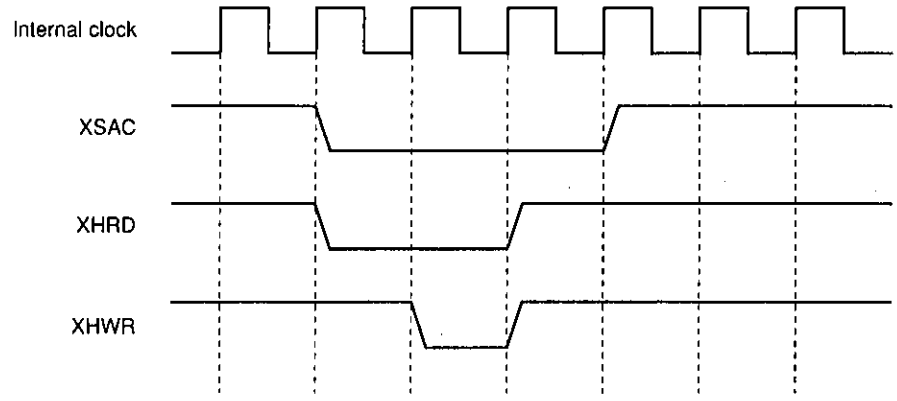
High: The HCLK pin is fixed low.

Low: The HCLK pin outputs a clock with half the frequency as that input to XTL1.

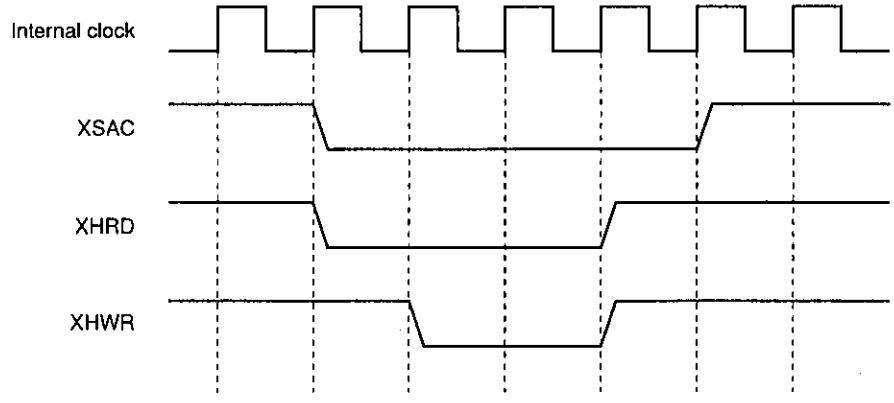
bit 0: RAMSIZE (RAM size)

Set this bit as shown below, according to the type of buffer memory connected:

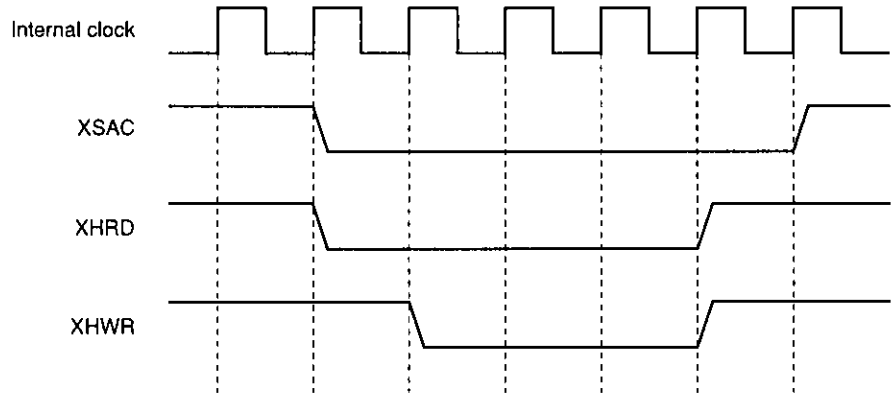
Size	Type	DRAM pin	RAMSIZE pin
32KB (256Kbit)	SRAM	"L"	"L"
128KB (1Mbit)	SRAM	"L"	"L"
256KB (2Mbit)	DRAM	"H"	"L"
512KB (4Mbit)	DRAM	"H"	"H"



Three-cycle Mode Transfer SXFRCYC [1:0] = 0



Four-cycle Mode Transfer SXFRCYC [1:0] = 1



Five-cycle Mode Transfer SXFRCYC [1:0] = 2

2-2. CONFIG1 (configuration 1) register (address 01HEX)

bit 7: SWOPEN (sync window open)

High: The sync mark detection window opens. In this case, the IC's internal sync protection circuit is disabled.

Low: The sync mark detection window is controlled by the IC's internal sync protection circuit.

bits 6 to 4: SYCNGC2 to 0 (SYNC NG count 2 to 0)

Once a sync mark is inserted only for the number of times specified by these bits, the sync mark detection window opens. Setting a value of 1HEX or less here is prohibited. (When reset, the value of 2HEX is set here.)

bits 3, 2: Reserved

Normally set low.

bits 1, 0: SBCECC1, 0 (subcode ECC)

These two bits specify the error correction method used when decoding subcodes.

SBECC1	SBECC0	Mode
"X"	"L"	No error correction
"L"	"H"	Single error correction
"H"	"H"	Double error correction

2-3. LSTARA (last area)/LHADR (last HADRC) register (address 02HEX)

This register specifies the highest area.

Alternatively, this register specifies the upper limit (upper 8 bits) for HADRC when automatic transfer mode to the host is disabled, and specifies the upper limit (upper 8 bits) for the address for the subcode buffering command. The lower 11 bits are 7FFHEX.

Note that when making full use of the buffer memory, the setting for LSTARA is as shown in the following table.

BFBYTEF	RAM size	LSTARAHEX
"L"	32KB	0C
"H"		0A
"L"	64KB	19
"H"		16
"L"	128KB	34
"H"		2E
"L"	256KB	69
"H"		5E
"L"	512KB	D3
"H"		BD

2-4. DRVIF (drive interface) register (address 03HEX)

This register controls the CD DSP connection mode. After this IC is reset, the sub CPU sets this register according to the CD DSP connected to the IC.

bit 7: C2PL1ST (C2PO lower byte first)

High: C2PO is input in the sequence "lower byte, upper byte" for 2-byte DATA input.

Low: C2PO is input in the sequence "upper byte, lower byte" for 2-byte DATA input.

"Upper byte" means the upper 8 bits including the MSB from the CD DSP, and "lower byte" means the lower 8 bits including the LSB from the CD DSP. For instance, the header minute byte is the lower byte and the second byte is the upper byte.

bit 6: LCHLOW (LCH low)

High: When LRCK is low, determined to be the left channel data.

Low: When LRCK is high, determined to be the left channel data.

bit 5: BCKRED (BCLK rising edge)

High: Data is strobed at the rising edge of BCLK.

Low: Data is strobed at the falling edge of BCLK.

bits 4 and 3: BCKMD1, 0 (BCLK mode 1, 0)

These bits are set according to the number of BCLK clock pulses output during one WCLK cycle by the CD DSP.

BCKMD1	BCKMD0	
"L"	"L"	16BCLKs/WCLK
"L"	"H"	24BCLKs/WCLK
"H"	"X"	32BCLKs/WCLK

bit 2: LSB1ST (LSB first)

High: Connects with the CD DSP that outputs data with LSB first.

Low: Connects with the CD DSP that outputs data with MSB first.

bit 1: SONY30 (Sony CDL30 series)

High: Connects with the Sony 30 series CD DSP.

Low: Connects with the CD DSP that is not a Sony 30 series CD DSP.

bit 0: Reserved

Normally set low.

Any change of each bit value in this register must be made in the decoder disable status. (After being reset, the register is set to 28HEX.)

Table 2-1-1 shows the settings for bits 7 to 2 when this IC is connected to a Sony CD DSP.

Fig. 2-4-1. (1) to (3) are input timing charts.

Sony CD DSP	DRVIF register						Timing chart
	bit7	bit6	bit5	bit4	bit3	bit2	
	c2po	lrck	bedg	bck1	bck0	lsb	
CDL30 series CDL35 series	L	L	L	L	H	L	Fig. 2-4-1. (1)
CDL40 series (48-bit strobe mode)	L	L	H	L	H	L	Fig. 2-4-1. (2)
CDL40 series (64-bit strobe mode)	L	H	L	H	X	H	Fig. 2-4-1. (3)

Table 2-1-1. DRVIF Register Settings

Note 1:

CDL30 series	CXD1125Q/QZ, CXD1130Q/QZ, CXD1135Q/QZ CXD1241Q/QZ, CXD1245Q, CXD1246Q/QZ CXD1247Q/QZ/R etc.
CDL35 series	CXD1165Q, CXD1167Q/QZ/R etc.
CDL40 series	CXD2500Q/QZ etc.

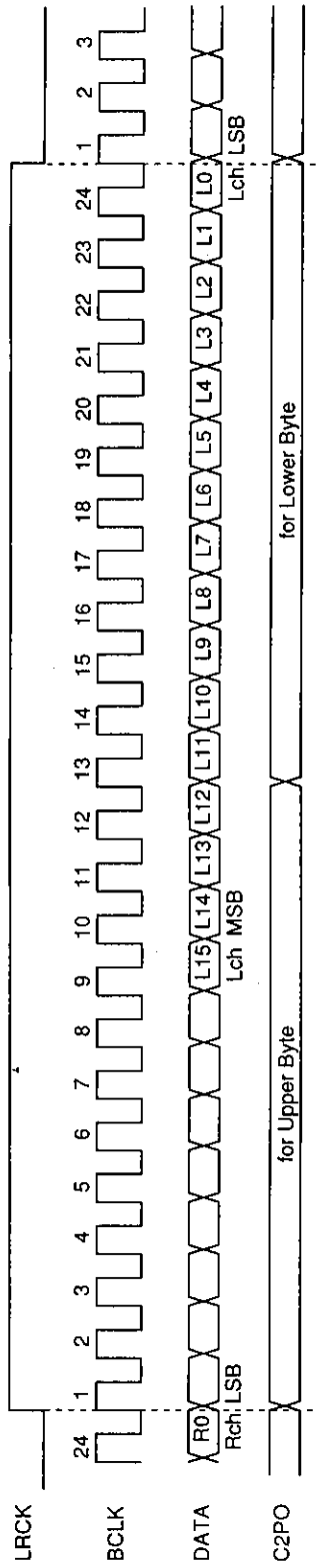


Fig. 2-4-1 (1). CDL30/CDL50 Series Timing Chart

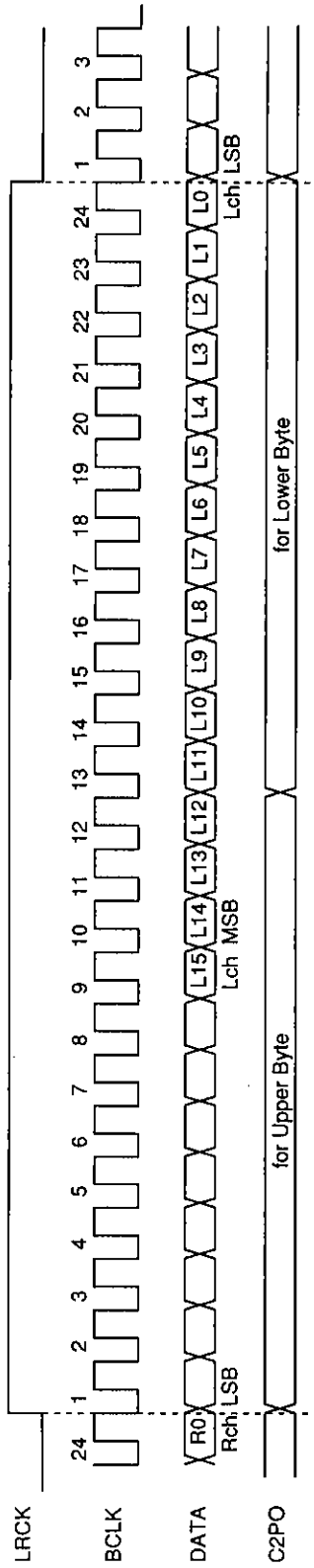


Fig. 2-4-1 (2). CDL40 Series 48-bit Slot Mode Timing Chart

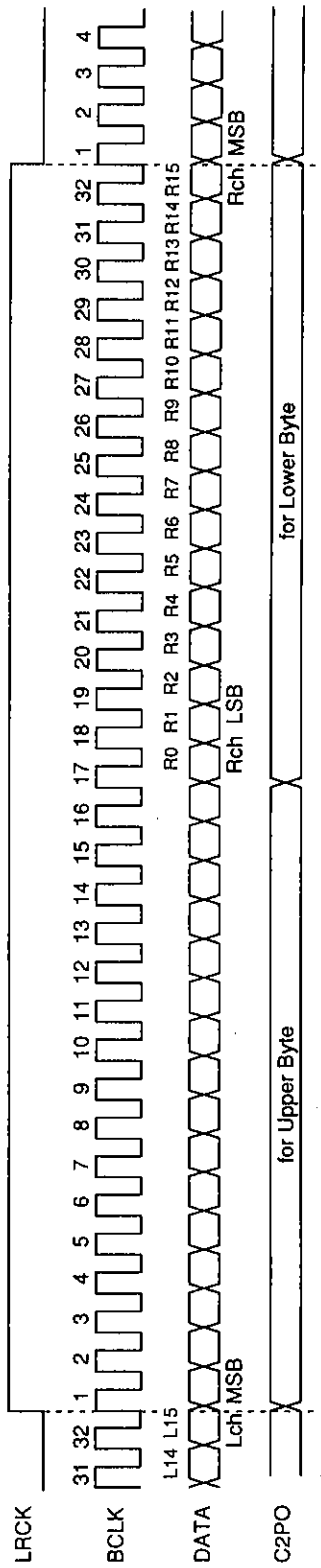


Fig. 2-4-1 (3). CDL40 Series 64-bit Slot Mode Timing Chart

2-5. XFRMT0 (transfer format 0) register (address 04HEX)

This register determines the transfer format for automatic transfers. Before starting the transfer of each sector, this IC reads the value of the SCTINF register written in buffer memory. The data in buffer memory is transferred to the host according to the value read from the SCTINF register and the XFRFMT1 and 0 registers. The MODEs and FORMs mentioned in the explanations concerning bits 3 to 1 are determined by bits 2 and 1 of the SCTINF register.

For MODE2 of the Yellow Book, FORM2 (bit 2) in the SCTINF register is "don't care." In order to send 2336 bytes of user data, set bits 3 to 1 of the XFRFMT0 register high.

bit 7: 1024XFR

When this bit is set high, the user data (2048 bytes) is sent 1024 bytes at a time. In this case, the values of bits 5 to 1 in the XFRFMT0 register and the value of the XFRFMT1 register are invalid. In other words, the sync mark, header, subheader, parity byte, block error flag, byte error flag and subcode cannot be sent to the host. This transfer mode is not supported for MODE2/FORM2 sectors.

bit 6: 512XFR (512-byte transfer mode)

When this bit is set high, the user data (2048 bytes) is sent 512 bytes at a time. In this case, the values of bits 5 to 1 in the XFRFMT0 register and the value of the XFRFMT1 register are invalid. In other words, the sync mark, header, subheader, parity byte, block error flag, byte error flag and subcode cannot be sent to the host. This transfer mode is not supported for MODE2/FORM2 sectors.

Setting both 1024XFR and 512XFR high at the same time is prohibited.

bit 5: SYNC

High: The sync mark is transferred to the host.

Low: The sync mark is not transferred to the host.

bit 4: HEADER

High: The 4 header bytes are transferred to the host.

Low: The 4 header bytes are not transferred to the host.

bit 3: SUBHEADER

High: MODE1: No meaning.
MODE2: The 8 subheader bytes are transferred to the host.

Low: The bytes described above are not transferred to the host.

bit 2: USERDATA (user data)

High: MODE1 and MODE2/FORM1: The user data (2048 bytes) is transferred to the host.
MODE2/FORM2: The user data (2324 bytes) is transferred to the host.

Low: The bytes described above are not transferred to the host.

bit 1: PARITY

High: MODE1: The EDC and ECC parity bytes and 8 zero bytes between them are transferred to the host, for a total of 288 bytes.
MODE2/FORM1: 280 EDC and ECC parity bytes are transferred to the host.
MODE2/FORM2: 4 reserved bytes (at the end of the sector) are transferred to the host.

Low: The bytes described above are not transferred to the host.

bit 0: RESERVED

Normally set low.

Note that the value 3EHEX should be set in this register for CD-DA data.

2-6. XFRFMT1 (transfer format 1) register (address 05HEX)

bit 7: ENBLKEFL (enable block error flag)

High: The block error flag (one byte) is transferred to the host.

Low: The byte described above is not transferred to the host.

bit 6: BLKEFLSL (block error flag select)

This bit is valid only when ENBLKEFL is high.

High: The value that the sub CPU wrote to the BLEFLG register (one byte) is transferred to the host as the block error flag.

Low: The data which is transferred as the block error flag is the "OR" of all byte error flag bits.

bit 5: ENBYTFBT (enable byte error flag buffering and transfer)

The following operations are performed when this bit is set high, and are not performed when this bit is set low.

(1) The byte error flag is buffered when executing write-only, real-time correction, and the CD-DA command.

(2) When automatic transfer mode to the host is enabled (the AUTOXFR bit (bit 7) of the XFRCTL register is high), the byte error flag is transferred to the host.

The ENBYTFBT bit and the BYTEFLSL bit are valid only when the USERDATA bit (bit 2) of the XFRFMT0 register is high.

bit 4: BYTEFLSL (byte error flag select)

This bit is valid only when ENBYTFBT is high. When this bit is high, the value in BYTERSTS (byte error status register, described later) is written to the byte error flag area in buffer memory. BLKEFLSL = low and BYTEFLSL = high cannot both be set at the same time.

When this bit is set low, the value written in the byte error flag area is either C2PO from the CD DSP.

bit 3: ENSBCBT (enable subcode buffering and transfer)

The following operations are performed when this bit is set high, and are not performed when this bit is set low.

(1) All subcodes or subcode Q is buffered when the decoder is executing the CD-DA command.

(2) When automatic transfer mode to the host is enabled (the AUTOXFR bit (bit 7) of the XFRCTL register is high), all subcodes or subcode Q is transferred to the host.

Note that buffering subcode or subcode Q data along with CD-ROM data is not supported.

bit 2: ALLSBC (all subcodes/subcode Q)

When ENSBCBT is high, this bit determines whether all subcodes or subcode Q is to be buffered and transferred to the host.

High: All subcodes

Low: Subcode Q

bit 1: SBCESTS (subcode error status)

This bit is valid only when ENSBCBT is high.

High: The sub CPU transfers the value (one byte) written in the SBCESTS register to the host.

Low: The byte described above is not transferred to the host.

bit 0: ZASQEF (zero after sub Q error flag)

This bit is valid only when ENSBCBT = SBCFLAG = high and ALLSBC =low. (Valid only when subcode Q and the subcode error flag are transferred to the host.)

High: 5 zero (00HEX) bytes are appended after the sub Q error flag and are then transferred to the host.

Low: 5 zero (00HEX) bytes are not appended after the sub Q error flag.

2-7. DECCTL0 (decoder control 0) register (address 06HEX)

bit 7: AUTODIST (auto distinction)

High: Error correction is performed according to the MODE byte and FORM bit read from the drive.

Low: Error correction is performed according to bits 6 and 5, the MODESEL and FORMSEL bits.

bit 6: MODESEL (mode select)

bit 5: FORMSEL (form select)

When AUTODIST is low, sectors are corrected in the MODE or FORM as indicated below.

MODESEL	FORMSEL	
"L"	"L"	MODE1
"H"	"L"	MODE2, FORM1
"H"	"H"	MODE2, FORM2

bit 4: Reserved

Normally set low.

bit 3: ENFM2EDC (enable FORM2 EDC check)

High: Enables EDC checks for FORM2.

Low: Disables EDC checks for FORM2. The EDCNG bit of the DECSTS0 register goes low.

bit 2: MDBYTCTL (mode byte control)

High: Even if the upper 6 bits of the MODE byte in the header are not all zeros, the data is not treated as an error. Set this bit high when playing back a CD-R or similar disc.

Low: If the upper 6 bits of the MODE byte in the header are not "000000", the data is treated as an error.

bit 1: ENDLA (enable drive last area (address))

High: Enables DLAR (drive last area). When buffering in the buffer memory area is completed while the decoder is executing a write-only command, a real-time correction command, or a CD-DA command, the DRVOVRN (drive overrun) status results. Writing of subsequent sectors to the buffer is halted.

Low: When this bit is low, DLAR (drive last area) is disabled.

bit 0: ATDLRNEW (auto DLARA renewal)

High: After one sector of data is transferred to the host, DLARA is updated to the area in which that sector was written.

Low: The sub CPU updates DLARA.

2-8. DECCTL1 (decoder control 1) register (address 07HEX)

bit 7: ENSBQRD (enable subcode Q read)

Gets subcodes from the DSP and performs a CRC check on subcode Q. The sub-CPU can read subcode Q from the SUBQ register. Decodes the subcodes (de-interleaving, error correction).

bit 6: Reserved

Normally set low.

bits 5 to 3: DECCMD2 to 0 (decoder command 2 to 0)

DECCMD2	DECCMD1	DECCMD0	Decoder command
"L"	"L"	"L"	DECODER Disable
"L"	"L"	"H"	RESERVED
"L"	"H"	"L"	Write only
"L"	"H"	"H"	Real-time correction
"H"	"L"	"H"	Subcode buffering
"H"	"H"	"H"	CD-DA

bits 2 to 0: Reserved

Normally set low.

2-9. XFRCTL0 (transfer control 0) register (address 08HEX)

bit 7: AUTOXFR (auto transfer)

High: Automatic transfer to host mode (described later) is enabled.

Low: Automatic transfer to host mode is disabled. Transfers to the host are performed using HADRC and HXFRC.

bit 6: Reserved

Set high when HMDS is low.

bits 5, 4, 1: Reserved

Normally set low.

bit 3: CPUDMAEN (sub CPU DMA enable)

When this bit is set high, sub CPU buffer memory access is enabled. The sub CPU sets this bit high after setting the head address for the buffer access in CADRC.

bit 2: CPUSRC (sub CPU source)

High: Data is transferred from the sub CPU to the buffer memory.

Low: Data is transferred from buffer memory to the sub CPU.

bit 0: HSTSRC (host source)

High: Data is transferred from the host to buffer memory.

Low: Data is transferred from buffer memory to the host.

This bit is valid when auto transfer to host mode is disabled (when the AUTOXFR bit (bit 7) of the XFRCTL register is low).

2-10. XFRCTL1 (transfer control 0) register (address 09HEX)

bits 7 to 5: Reserved

Normally set low.

bit 4: HSTXFREN (host transfer enable)

When this bit is set high, a transfer between the host and buffer memory starts. After the transfer is completed, this bit is automatically set low again.

bits 3 to 0: Reserved

Normally set low.

2-11. HIFCTL (host interface control) register (address 0AHEX)

bit 7: CLRBUSY (clear busy)

When this bit is set high, the BUSY status is cleared.

bits 6 to 3: Reserved

Normally set low.

bits 2 to 0: ACTHINT#2 to 0 (active host interrupt #2 to 0)

The values of these bits become those of corresponding HINTSTS#2 (ap0) bits in the STATUS register in the host. Once these bits are set high, they remain high until either they are cleared by the host or the chip is reset. In other words, the sub CPU cannot change these bits from high to low. Therefore, when the sub CPU sets these bits, there is no need to take the values of other bits into consideration.

2-12. DSPCTL (DSP control) register (address 0BHEX)

bits 7 and 6: DSTBSL1, 0

These bits determine the frequency of the DSTB and XLAT clocks that are used to pass data (DATO) to the CD DSP. The sub CPU sets these bits on the basis of the XTL1 pin clock frequency. (The maximum frequency for DSTB is 1 MHz.)

DSTBDL1	DSTBDL0	Frequency
0	0	1/24 of XTL1
0	1	1/32 of XTL1
1	0	1/48 of XTL1
1	1	1/64 of XTL1

bit 5: DISXLAT (disable XLAT output)

High: After the contents of the DSPCMD register are transferred to the DSP, a latch pulse is not output from the XLAT pin. In this case, the sub CPU outputs a latch pulse from the XLAT pin at a correct time, using DSPCMDLT (bit 0 of the CHPCTL0 register).

Low: After the contents of the DSPCMD register are transferred to the DSP, a latch pulse is output from the XLAT pin.

bits 4 and 3: XFRBYT1, 0 (transfer command byte length)

These bits determine the number of bytes of command data (DSPCMD register) transferred to the CD DSP. The relationship between the settings and the number of bytes is shown in the following table.

XFRBYT1	XFRBYT0	Number of bytes
"L"	"L"	Prohibited
"L"	"H"	1
"H"	"L"	2
"H"	"H"	3

bits 2 to 0: Reserved

Normally set low.

2-13. CHPCTL0 (chip control 0) register (address 0C$_{HEX}$)

bit 7: CHIPRST (chip reset)

Setting this bit high resets the IC.

bit 6: TGTMET (target met)

(1) The sub CPU sets TGTMET high when the target sector is found when executing a write-only, real-time correction command.

(2) TGTMET is sampled for 3/4 of a sector after the decoder interrupt (the time changes with the playback speed). Therefore, if the target sector is found, the sub CPU must set TGTMET high before this time elapses after the decoder interrupt.

(3) Once TGTMET is set high, it remains high until DECODER is disabled in the IC.

(4) When TGTMET is sampled and it is low while executing a write-only, real-time correction command:

- The main data and subcode buffer areas are not updated.
- Main data error correction is not executed.

bit 5: INCTGT (increment target register)

When this bit is set high, the target registers (TGTMIN, TGTSEC, and TGTBLK) are incremented. The target registers use BCD code.

TGTMIN, TGTSEC, and TGTBLK are connected in cascade fashion, and are incremented in the following manner:

(1) The TGTBLK register is always incremented by this bit; when this register reaches 74, it returns to 0 the next time it is incremented.

(2) The TGTSEC register is incremented when this bit goes high and the TGTBLK register is 74. When this register reaches 59, it returns to 0 the next time it is incremented.

(3) The TGTMIN register is incremented when this bit goes high, the TGTBLK register is 74 and the TGTBLK register is 59. When this register reaches 99, it returns to 0 the next time it is incremented.

bit 4: RPCORTRG (repeat correction trigger)

When this bit is set high while the decoder is disabled, CD-ROM sector error correction begins. The sector that error correction is performed on is specified by the BFARA# register.

bit 3: CLRRSLT (clear result)

Setting this bit high clears the RESULT register.

bit 2: CLDSPCMD (clear DSP DATA register)

Setting this bit high clears the DSPCMD register.

bit 1: DSPCMDXF (DSP command transfer)

Setting this bit high initiates serial transfer of the contents of the DSPCMD register to the CD DSP.

bit 0: DSPCMDLT (DSP command latch)

Setting this bit high outputs a pulse from the XLAT pin.

2-14. CPUBWDT (CPU buffer write data) register (address 0D$_{HEX}$)

The sub-CPU writes the data to be written to buffer memory in this register.

2-15. DSPCMD (DSP command) register (address 0E$_{HEX}$)

The serial transfer data for the CD DSP is written to this register. The data consists of 3 bytes written on a LIFO (last in, first out) basis.

2-16. RESULT (result) register (address 0F$_{HEX}$)

This register returns the command execution results to the host. The results consist of 10 bytes written on a FIFO (first in, first out) basis.

2-17. SCTINF (sector information) register (address 10HEX)

During a DECINT, the current sector information is written to this register. When performing automatic transfers to the host, be sure to always set this register for each DECINT. The value of this register is written to the top address in the buffer memory area.

bit 2: MODE2

High: The current sector is a MODE2 sector.

Low: The current sector is a MODE1 or CD-DA sector.

bit 1: FORM2

This bit is valid only when the MODE2 bit is high.

High: The current sector is a FORM2 sector.

Low: The current sector is a FORM1 sector.

This bit can be either low or high for MODE2 of the Yellow Book.

MODE2	FORM2	
"L"	"L"	MODE1
"L"	"H"	RESERVED
"H"	"L"	MODE2/FORM1
"H"	"H"	MODE2/FORM2

bit 0: XFRSCT (transfer sector)

High: The data in the current sector is transferred to the host.

Low: The data in the current sector is not transferred to the host. In this case, bits 2 and 1 have no meaning.

2-18. BLKESTS (block error status) register (address 11HEX)

The data to be transferred to the host as the block error status is written in this register. Set this register before setting the SCTINF register.

2-19. SBCESTS (subcode error status) register (address 12HEX)

The data to be transferred to the host as the subcode error status is written in this register. Set this register before setting the SCTINF register.

2-20. INCBLKS (increment blocks) register (address 13HEX)

bits 7 to 3: Reserved

Normally set low.

bits 2 to 0: INCBLKS2 to 0

This register specifies the increment step (+1 to 4) for the BFBLKC (buffer block count) register. Setting the value as 0 or 5 or greater is prohibited. After a reset, the value is set to "1".

2-21. BYTERSTS (byte error status) register (address 14HEX)

When ENBYTFBT and ENBYTEFG of the XFRFMT1 register are both high, the data to be transferred to the host as the byte error status is written in this register. Set this register before setting the SCTINF register.

2-22. CHPCTL1 (chip control 1) register (address 15HEX)

bit 7: BURSTXFR (burst transfer)

High: Data transfers with the SCSI controller IC are performed in burst mode. In burst mode, SDRQ and XSAC are kept active while the transfer is in progress.

Low: Data transfers with the SCSI controller IC are performed in single mode. In single mode, either: (1) handshaking is performed with SDRQ and XSAC, or (2) SDRQ is maintained high, but XSAC goes inactive with the transfer of each byte. There is no distinction between (1) and (2) in this IC.

bits 6 and 5: XFRRATE1, 0 (transfer rate 1, 0)

These bits are used to limit the data transfer speed during data transfers with the SCSI controller IC.

XFRRATE1	XFRRATE0	
"H"	"H"	Limits the SDRQ acceptance interval to 8 x the XTL1 period, or more.
"H"	"L"	Limits the SDRQ acceptance interval to 7 x the XTL1 period, or more.
"L"	"H"	Limits the SDRQ acceptance interval to 6 x the XTL1 period, or more.
"L"	"L"	No limit on the SDRQ acceptance interval.

bits 4 and 3: RFRSCTL1, 0 (refresh control 1, 0)

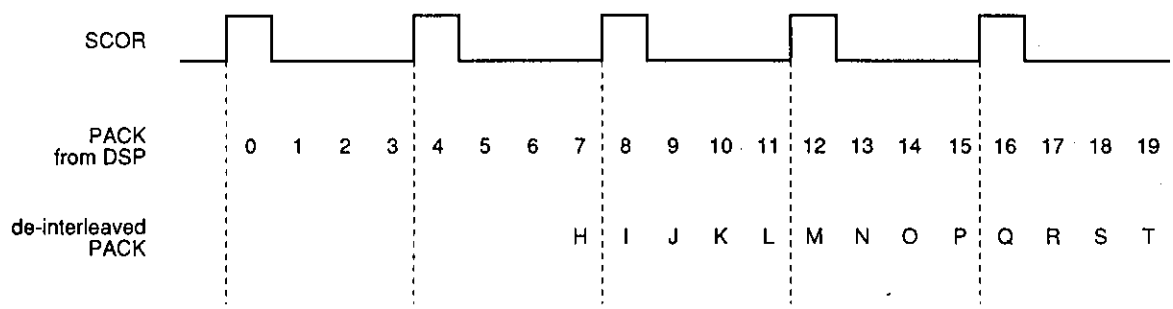
These bits are used to control the refresh interval when the IC is connected to DRAM. Set these bits according to the XTL1 clock frequency. The refresh interval is designed to be 8ms. In addition, this IC performs RAS-only refresh. Note that when this IC is connected to SRAM, the settings of these bits are "don't care".

RFRSCTL1	RFRSCTL0	
"L"	"L"	XTL1 frequency is less than 24MHz.
"L"	"H"	XTL1 frequency is 24MHz or more.
"H"	"L"	XTL1 frequency is 32MHz or more.
"H"	"H"	XTL1 frequency is 33.8688MHz or more.

bit 2: PACKMODE (pack mode)

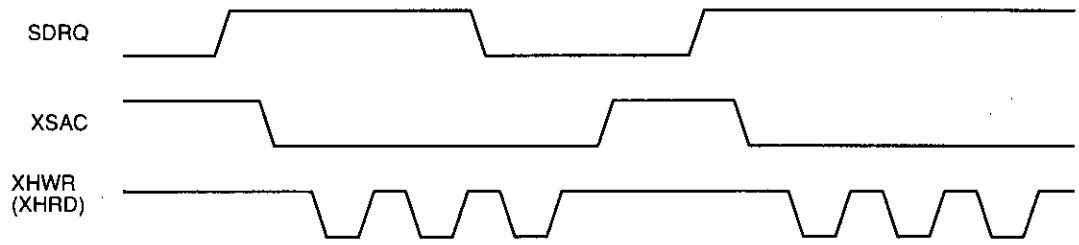
High: The four packs of data starting from the five packs before the subcode sync signal are written to the buffer as one group of data. In the illustration below, H to K are treated as one group.

Low: The four packs of data before the subcode sync signal are written to the buffer as one group of data. In the illustration below, I to L are treated as one group.

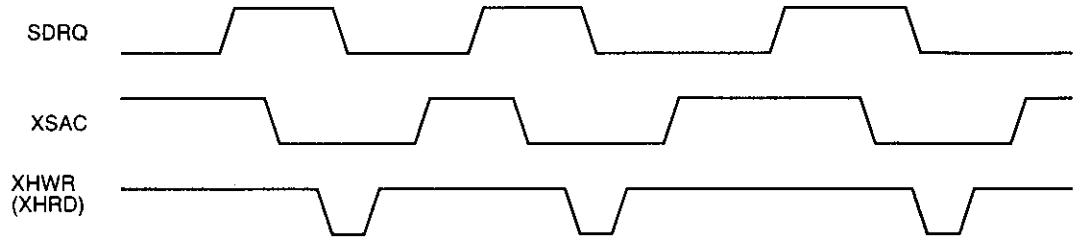


PACKMODE

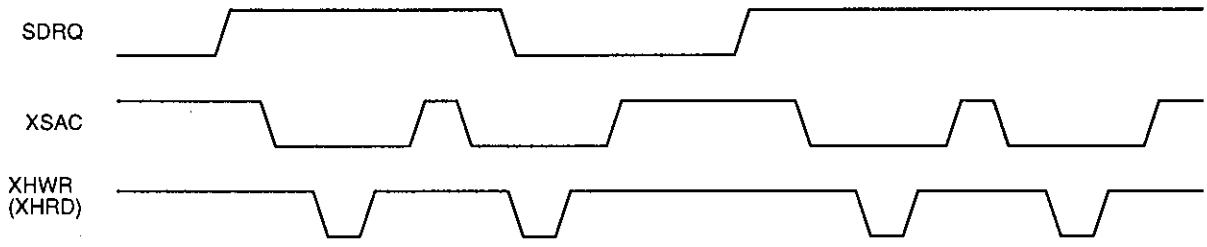
H: pack using 0 to 7
I: pack using 1 to 8
J: pack using 2 to 9



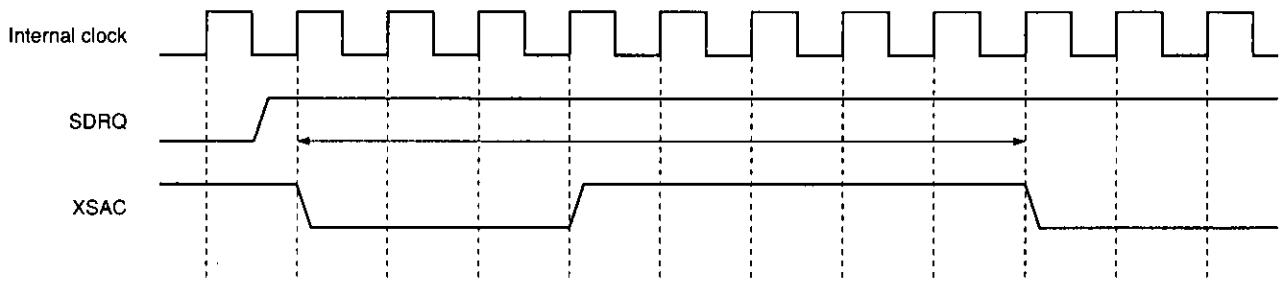
Burst mode transfer



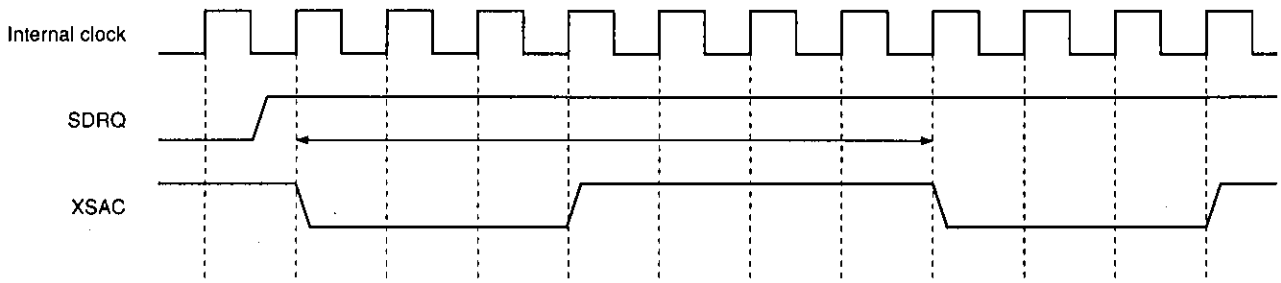
Single mode transfer (1)



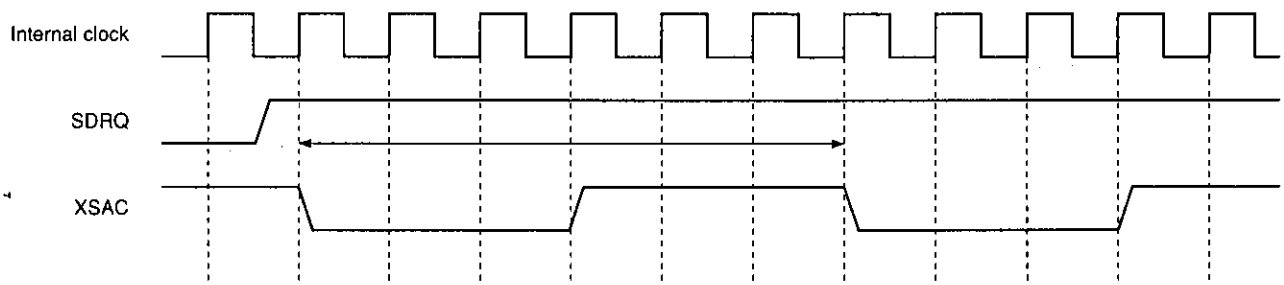
Single mode transfer (2)



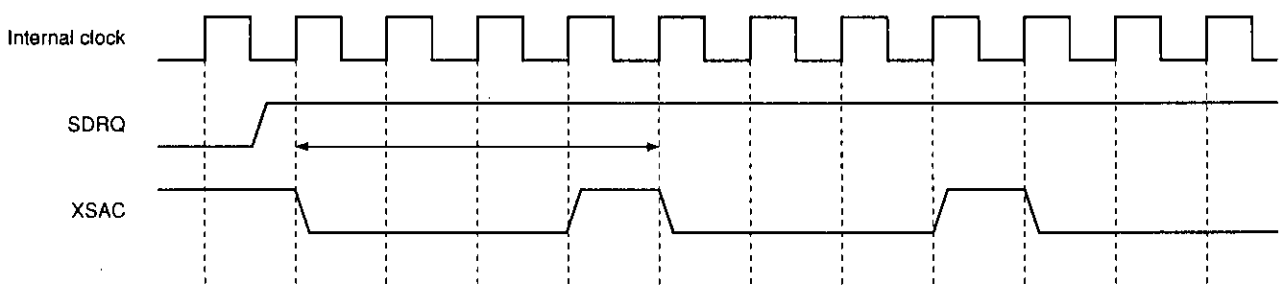
XFRRATE [1:0] = 3



XFRRATE [1:0] = 2



XFRRATE [1:0] = 1



XFRRATE [1:0] = 0

bits 1 and 0: Reserved
Normally set low.

2-23. TGTMIN (target minute) register (address 17HEX)

0 to 99

2-24. TGTSEC (target second) register (address 18HEX)

0 to 59

2-25. TGTBLK (target block) register (address 19HEX)

0 to 74

During the execution of a monitor-only, write-only, or real-time correction command, the address of the target sector is set in these three registers. This address is compared with the address of the current sector, and the results are reflected in TGTNTMT (target not met) status (bit 0 of the DECSTS0 register).

2-26. XFRCNT-H, M, L (transfer block counter - high, middle, low) register (address 1B to 1DHEX)

This is a 24-bit register that shows the number of blocks remaining to be transferred. Before starting a transfer, the sub CPU sets the total number of blocks to be transferred in this register.

Each time the transfer of one block is completed, this register is decremented.

The sub CPU can read the value stored in XFRCNT at any time. Note that there is an error of ±1 between the value that is read and the actual value because the sub CPU's reads and the changes in the value of XFRCNT are not synchronized.

The sub CPU can read the value stored in XFRARA, XFRPOS, BFBLKC, and XFRCNT at any time. However, Note that there is an error of ±1 between the value that is read and the actual value
because the sub CPU's reads and the changes in the value of BFBLKC are not synchronized.

2-27. BFARA# (buffer area number) register (address 1EHEX)

This register indicates the buffer area when executing a write-only, real-time correction, or CD-DA command. Before executing any of these commands, the sub CPU specifies the first area where buffering is to start. As each sector is buffered, this register is incremented.

When executing a subcode buffering command, buffering starts at address 0.

2-28. DLARA (drive last area) register (address 1FHEX)

This register indicates the final buffer area when the decoder is executing a write-only, real-time correction, or CD-DA command. If ENDLA (bit 1) in the DECCTL0 register is set high and the decoder writes data from the drive (CD DSP) to the area specified by DLARA while one of the above commands is being executed, subsequent buffering is prohibited.

2-29. XFRARA (transfer area) register (address 20HEX)

In automatic transfer mode, this register specifies the first area where the transfer is to start from. After each block is transferred, this register is incremented.

2-30. XFRPOS (first transfer position) register (address 21HEX)

bits 1 and 0: XFRPOS1, 0

In 512-byte or 1024-byte transfer mode (automatic transfer mode), this register specifies the first block position where the transfer is to start from. In 1024-byte mode, XFRPOS1 is invalid. After each block is transferred, this register is incremented. This register is invalid in manual transfer mode and in automatic transfer modes other than 512-byte or 1024-byte transfer mode.

2-31. HXFRC-H, M, L (host transfer counter-high, middle, low) register (address 23 to 25HEX)

This register specifies the total number of bytes to be transferred in manual transfer mode. (20 bits)

2-32. HADRC-H, M, L (host address counter-high, middle, low) register (address 27 to 29HEX)

This register specifies the head address from which the transfer is to start in manual transfer mode.

2-33. SLADR-H, M, L (subcode last address-high, middle, low) register (address 2B to 2DHEX)

This register specifies the final buffering address for the subcode buffering command. When ENDLA (bit 1) in the DECCTL0 register is set high and the decoder writes data to the buffer address specified by SLADR while the subcode buffering command is being executed, subsequent buffering is prohibited. Always set these registers in the sequence H - M - L.

2-34. CADRC-H, M, L (sub CPU address counter-high, middle, low) register (address 2F to 31HEX)

The address is set here when the sub CPU accesses buffer memory. When data is read from buffer memory or written to buffer memory, this register is incremented.

2-35. CLRINT0 (clear interrupt status 0) register (address 32HEX)

When any bit of this register is set high, the corresponding interrupt status is cleared. After the interrupt status is cleared, the corresponding bit automatically goes low. Accordingly, there is no need for the sub CPU to set these bits low.

bit 7: DECINT (decoder interrupt)
bit 6: DECTOUT (decoder timeout)
bit 5: DRVOVRN (drive overrun)
bit 4: SUBCSYNC (subcode sync)
bits 3 to 0: Reserved
Normally set low.

2-36. CLRINT1 (clear interrupt status 1) register (address 33HEX)

When any bit of this register is set high, the corresponding interrupt status is cleared. After the interrupt status is cleared, the corresponding bit automatically goes low. Accordingly, there is no need for the sub CPU to set these bits low.

bit 7: HCRISD (host chip reset issued)
bits 6 to 4: Reserved
Normally set low.
bit 3: HSTCMD (host command)
bit 2: RSLTEMPT (result empty)
bit 1: XFRSTOP (transfer stop)
bit 0: BLXFRCMP (block transfer complete)

2-37. INTEN0 (interrupt enable 0) register (address 34HEX)

When any bit of this register is set high, interrupt requests are enabled to the sub CPU from this IC as a result of the corresponding interrupt status. (In other words, if that interrupt status occurs, the INT0 pin goes active.) The value of each bit in this register has no effect on the corresponding interrupt status.

bit 7: DECINT (decoder interrupt)
bit 6: DECTOUT (decoder timeout)
bit 5: DRVOVRN (drive overrun)
bit 4: SUBCSYNC (subcode sync)
bits 3 to 0: Reserved
Normally set low.

2-38. INTEN1 (interrupt enable 1) register (address 35HEX)

When any bit of this register is set high, interrupt requests are enabled to the sub CPU from this IC as a result of the corresponding interrupt status. (In other words, if that interrupt status occurs, the INT0 pin goes active.) The value of each bit in this register has no effect on the corresponding interrupt status.

bit 7: HCRISD (host chip reset issued)
bits 6 to 4: Reserved
Normally set low.
bit 3: HSTCMD (host command)
bit 2: RSLTEMPT (result empty)
bit 1: XFRSTOP (transfer stop)
bit 0: BLXFRCMP (block transfer complete)

2-39. BFBLKC-H, L (buffer block counter - high, low) register (address 36, 37HEX)

This is a 10-bit counter that indicates the number of transferable blocks in the buffer. The sub CPU sets the number of transferable blocks before starting up the decoder.

When a transferable block is created (when a sector with XFRSCT (bit 0) of the SCTINF register high is written to the buffer), the value of BFBLKC is incremented (by + 1 to 4). The increment step is specified by the INCBLKS register.

In addition, when the transfer of one block is completed, the register is decremented (–1).

Initial Register Values

The values after a reset for the following registers are as shown:

Register name	Address (HEX)	Value after reset (HEX)	
CONFIG1	01	0010 0000	20
DRVIF	03	0010 1000	28
DECCTL0	06	1000 0101	85
XFRCTL0	08	1100 0000	C0
DSPCTL	0B	0001 1000	18
INCBLKS	13	0000 0001	01
Other than the above		0000 0000	00

Note that the CONFIG1 and DRVIF registers are not affected by software resets.

3. Sub CPU Read Registers

The explanations are omitted for the same registers as those of the write registers.

3-1. RAWHDR (raw header) register (address 00HEX)

During a DECINT, the header byte of the sector being sent from the CD DSP can be read from this register.

3-2. BFHDR (buffer header) register (address 02HEX)

The header byte of the current sector can be read from this register when executing a write-only or real-time correction command, and when executing a repeated correction. This register is invalid when the decoder is disabled or the monitor-only command or CD-DA command is being executed.

3-3. BFSHDR (buffer subheader) register (address 03HEX)

The subheader byte of the current sector can be read from this register when executing a write-only or real-time correction command, and when executing a repeated correction. This register is invalid when the decoder is disabled or the monitor-only command or CD-DA command is being executed.

3-4. RAWHDRFLG (raw header flag) register (address 04HEX)

This register shows the C2PO value for the RAWHDR register.

bit 7: Minute
bit 6: Second
bit 5: Block
bit 4: Mode
bits 3 to 0: Reserved

3-5. BFHDRFLG (buffer header flag) register (address 05HEX)

This register shows the error status for each byte of the BFHDR and BFSHDR registers. A bit that is set high indicates an error.

bit 7: Minute
bit 6: Second
bit 5: Block
bit 4: Mode
bit 3: File
bit 2: Channel
bit 1: Submode
bit 0: Data type

3-6. DECSTS0 (decoder status 0) register (address 06HEX)

bit 7: SHRTSCT (short sector)

Indicates that since the previous DECINT, a sector with a SYNC mark interval of 2351 bytes or less was found. This sector does not remain in buffer memory.

bit 6: NOSYNC

Indicates that a sync mark was not detected in the prescribed position in the current sector and that a sync mark was inserted as a result.

bit 5: CORINH (correction inhibit)

This bit goes high when the AUTODIST bit of the DECCTL register is high and the MODE and FORM of the current sector could not be decided. ECC and EDC are not executed for this sector. When AUTODIST is low, this bit is invalid. If the AUTODIST bit is high, CORINH goes high in any of the following instances:

(1) There was an error in the MODE byte.
(2) The MODE byte had a value other than 01HEX or 02HEX.
(3) The value of the MODE byte was 02HEX, and the C2 pointer in the submode byte was high.

bit 4: ERINBLK (erasure in block)

Indicates that when the decoder was executing in write-only and real-time mode, at least one error flag (C2PO) for one byte had been set in the data, excluding the SYNC mark from the CD DSP in the current sector.

bit 3: CORDONE (correction done)

Indicates that there is a byte for which error correction was performed in the current sector.

bit 2: EDCNG

Indicates that the EDC check indicates an error in the current sector.

bit 1: ECCNG

Indicates that an uncorrectable error is found somewhere between the header byte and the P parity byte in the current sector. (For a MODE2, FORM2 sector, this bit is "don't care".)

bit 0: TGTNTMET (target not met)

Indicates that the address in the TGTMNT, TGTSEC, and TGTBLK registers does not match the address of the current sector. The error pointer is not referenced in this instance.

3-7. DECSTS1 (decoder status 1) register (address 07HEX)

bits 7 to 4: Reserved

bit 3: SBCNTRDY (subcode not ready)

Indicates that when executing a write-only or real-time correction command, the subcode was not ready by the time the target sector was found (when the sub CPU set the TGTMET bit (bit 6 of the CHPCTL register)). In this case, the subcode buffered in the same area as the target sector is not correct.

bit 2: EDCALL0 (EDC ALL 0)

This bit goes high if there are no errors in all 4 EDC parity bytes for the current sector and the value of all 4 bytes was 00HEX.

bit 1: CMODE (correction mode)

bit 0: CFORM (correction form)

When the decoder is executing in either real-time correction or repeated correction mode, these bits indicate what the MODE and FORM of the current sector were determined to be when error correction was performed.

CFORM	CMODE	
"X"	"L"	MODE1
"L"	"H"	MODE2, FORM1
"H"	"H"	MODE2, FORM2

3-8. XFRSTS (data transfer status) register (address 08HEX)

bits 7 to 2: Reserved

bit 1: CBFWRRDY (sub CPU buffer write ready)
When this bit is high, the sub CPU can write to the CPUBWDT register.

bit 0: CBFRDRDY (sub CPU buffer read ready)
When this bit is high, the sub CPU can read the CPUBRDT register.

3-9. HIFSTS (host interface status) register (address 0AHEX)

bit 7: BUSYSTS (BUSY status)
This bit has the same value as the BUSYSTS bit (bit 7) of the HSTS register on the host side. This bit goes high when the host writes a command to the command register, and goes low when the sub CPU sets CLRBUSY in the HIFCTL register.

bit 6: RSLTEMPT (result empty)
When this bit is high, the RESULT register is empty. This indicates that the status (RESULT register) previously sent from the sub CPU to the host has been completely read by the host.

bit 5: RSLTWRDY (RESULT write ready)
When this bit is high, the RESULT register is not full. In this case, the sub CPU can write command execution results in the RESULT register.

bit 4: PRMFULL (parameter full)
When this bit is high, the HSTPRM register is full.

bit 3 PRMRRDY (parameter read ready)
When this bit is high, the HSTPRM register is not empty. In this case, the sub CPU can read the command parameters from the HSTPRM register.

bit 2: HINTSTS#2 (host interrupt status #2)
This bit goes high when the sub CPU writes data to HINT#2 (bit 2 of the HIFCTL register). This bit goes low when the host sets CLRINT#2 (bit 2 of the HCLRCTL register) high. This bit is used to monitor interrupts to the host.

bit 1: HINTSTS#1 (host interrupt status #1)
This bit goes high when the sub CPU writes data to HINT#1 (bit 1 of the HIFCTL register). This bit goes low when the host sets CLRINT#1 (bit 1 of the HCLRCTL register) high. This bit is used to monitor interrupts to the host.

bit 0: HINTSTS#0 (host interrupt status #0)
This bit goes high when the sub CPU writes data to HINT#0 (bit 0 of the HIFCTL register). This bit goes low when the host sets CLRINT#0 (bit 0 of the HCLRCTL register) high. This bit is used to monitor interrupts to the host.

3-10. DSPSTS (DSP status) register (address 0BHEX)

bits 7 to 5: REV#2 (revision number bits 2 to 0)
REV#2 to 0=001. The sub CPU identifies the type of LSI from these bits.

bits 4 to 1: Reserved

bit 0: CMDOBUSY (command output busy)
This bit goes high when DSPCMDXFR is set. This bit goes low when the transfer of the contents of the DSPCMD register to the CD DSP is completed.

3-11. CPUBRDT (CPU buffer read data) register (address 0DHEX)

The sub CPU reads the buffer memory data through this register.

3-12. COMMAND (host command) register (address 0EHEX)

The command from the host can be read from this register.

3-13. PARAM (parameter) register (address 0FHEX)

The parameters needed for command execution are read from this register. The 10 bytes of data are handled on a FIFO basis.

3-14. SBCSTS (subcode status) register (address 10HEX)

This register indicates the error status of the subcodes written to the buffer when executing a write-only, real-time correction, or CD-DA command. This register is valid between DECINTs.

bit 7: SBCOVRN (subcode overrun)
The SBCOVRN status is set if ENSBCBT (bit 5) of the XFRFMT1 register is set high and subcode buffering in the area specified by DLARA is completed when the decoder is executing or CD-DA command.
There are no stipulations governing the timing relationship between subcode SYNC and the CD-ROM data SYNC mark. There is a time lag in the generation of DRVOVRN and SBCOVRN.

bit 6: OVERFLOW
Indicates that the SBSSTS FIFO overflowed because of frequent generation of subcode short syncs. When an overflow occurs, subcode buffering is halted. Subcodes are not buffered for sectors subsequently obtained by decoder interrupts.

bit 5: BFNTVAL (buffer not valid)
Indicates that valid data was not written to the buffer from a short subcode sector.

bit 4: NOSYNC0
Indicates that a subcode sync was not detected in the prescribed position and that a sync mark was inserted as a result.

bits 3 to 1: SBCERR3 to 1 (subcode pack error 3 to 1)
Indicate that the pack contains an uncorrectable error as a results of subcode error correction. These bits are valid only when ALLSBC (bit 4) of the XFRFMT register is high.

bit 0: SBCERR0 (subcode pack error 0)/SUBQERR0 (subcode Q error 0)
When ALLSBC of XFRFMT1 register is high, this bit shows the PACK0 error status.
When ALLSBC of XFRFMT1 register is low, subcode Q was determined to be in error as a result of the subcode Q CRC check.

3-15. SBQSTS (subcode Q status) register (address 11HEX)

This register shows the error status of the subcode Q gotten from the CD DSP. This register is valid between SBCSYNCs.

bits 7 to 3: Reserved

bit 2: SHTSBCS1 (short subcode sector 1)
Indicates that there was a subcode sync interval of less than 98 WFCK pulses since the SBCSYNC interrupt.

bit 1: NOSYNC1
Indicates that a subcode sync was not detected in the prescribed position and that a sync mark was inserted as a result.

bit 0: SUBQERR1 (subcode Q error 1)
Subcode Q was determined to contain an error as a result of the CRC check.

3-16. SBQDT (subcode Q data) register (address 12HEX)

The subcode Q value can be read by reading this register 10 times. The subcode Q that is read is the data immediately preceding the SBCSYNC interrupt.

3-17. CSCTARA (current sector area) register (address 13HEX)

This register indicates the AREA# to which the current sector is being written.

3-18. CHPCTL1 (chip control 1) register (address 15HEX)

The values written in the write register CHPCTL1 can be read as is in bits 7 to 2.

bit 7: BURSTXFR (burst transfer)

bits 6 and 5: XFRRATE1, 0 (transfer rate 1, 0)

bits 4 and 3: RFRSCTL1, 0 (refresh control 1, 0)

bit 2: BURSTXFR (burst transfer) CKMODE (pack mode)

3-19. TGTMNT (target minute) register (address 17HEX)

3-20. TGTSEC (target second) register (address 18HEX)

3-21. TGTBLK (target block) register (address 19HEX)

3-22. XFRCNT-H, M, L (transfer block counter-high, middle, low) register (address 1B to 1DHEX)

3-23. BFARA# (buffer area number) register (address 1EHEX)

Permits reading of the AREA# where the main data is being buffered.

3-24. DLADR (drive last address) register (address 1FHEX)

3-25. XFRARA (transfer area) register (address 20HEX)

3-26. XFRPOS (first transfer position) register (address 21HEX)

3-27. HXFRC-H, M, L (host transfer counter-high, middle, low) register (address 23 to 25HEX)

3-28. HADRC-H, M, L (host address counter-high, middle, low) register (address 27 to 29HEX)

3-29. SLDR-H, M, L (subcode last address-high, middle, low) register (address 2B to 2DHEX)

3-30. SADRC-H, M, L (subcode address counter-high, middle, low) register (address 2F to 31HEX)

Permits reading of the buffering address in the subcode buffering command.

3-31. INTSTS0 (interrupt status 0) register (address 32HEX)

The value of each bit in this register indicates the value of the corresponding interrupt status. The values of these bits are not affected by the values of the INTEN0 register bits.

bit 7: DECINT (decoder interrupt)

This interrupt is generated when the decoder executes a command.

(1) During execution of a write-only or real-time correction command
When a header byte in which a SYNC mark was detected or inserted is received from the CD DSP, the DECINT status is set. However, when the SYNC mark detection window is open, the DECINT status does not result if the SYNC mark interval is less than 2352 bytes.

(2) During execution of repeated correction
The DECINT status is set each time one correction is completed.

(3) During CD-DA command execution
The DECINT status is set each time the data of 2352 bytes are written.

(4) During subcode buffering execution
The DECINT status is set when the subcode for one sector is written to the buffer.

bit 6: DECTOUT (decoder timeout)

After the decoder is set to the write-only and real-time correction modes, the DECTOUT status is set if a SYNC mark is not detected even after three sector's worth of time elapses (40.6ms at normal playback speed).

bit 5: DRVOVRN (drive overrun)

When the decoder is executing a write-only, real-time correction, or CD-DA command, the DRVOVRN status is set if buffering is completed in the area specified by DLARA.

bit 4: SUBCSYNC (subcode sync)

If a subcode sync mark is detected or inserted when subcode fetches are enabled, the SUBCSYNC status is set. Note that if the SUBCSYNC interrupt is not cleared within 95 WFCK pulses, the SUBCSYNC status does not result the next time subcode sync mark is detected or inserted. In this case, the subcode Q read from the SBQDT register is also not updated.

bits 3 to 0: Reserved

3-32. INTSTS1 (interrupt status 1) register (address 33HEX)

The value of each bit in this register indicates the value of the corresponding interrupt status. The values of these bits are not affected by the values of the INTEN1 register bits.

bit 7: HCRISD (host chip reset issued)

The HCRISD status is set when the host clears this chip.

bits 6 to 4: Reserved

bit 3: HSTCMD (host command)

The HSTCMND status is set when the host writes to the command register.

bit 2: RSLTEMPT (result empty)

The RSLTEMP status is set when the host reads the RESULT register and the RESULT register becomes empty. (This bit is used when the number of RESULT bytes to be sent to the host is 11 or more.)

bit 1: XFRSTOP (transfer stop)

When automatic transfer to host mode is enabled, the XFRSTOP status is set if the transfer to the host is stopped because the BFBLKC register or the XFRCNT register was set to 0.

bit 0: BLXFRCMP (block transfer complete)

When automatic transfer to host mode is enabled, the BLXFRCMP status is set if the transfer of one block is completed. The BLXFRCMP status is not set when the block transfer is completed and the XFRSTOP status was set. When automatic transfer to host mode is disabled, the BLXFRCMP status is set if the transfer to the host is completed by HXFRC.

3-33. INTEN0 (interrupt enable 0) register (address 34HEX)

The value written in the INTEN0 register can be read as is from this register.

3-34. INTEN1 (interrupt enable 1) register (address 35HEX)

The value written in the INTEN1 register can be read as is from this register.

3-35. BFBLKC-H, L (buffer block counter - high, low) register (address 36 to 37HEX)

REG	ADR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
CONFIG0	00	CINT POL	HINT POL	SXFR CYC1	SXFR CYC0	EXCK SL	DIS CLK	DIS HCLK	RAM SIZE
CONFIG1	01	SW OPEN	SYC NGC2	SYC NGC1	SYC NGC0	"L"	"L"	SBC ECC1	SBC ECC0
LSTARA LHADR	02	b7	b6	b5	b4	b3	b2	b1	b0
DRVIF	03	C2PO L 1st	LCH LOW	BCK RED	BCKL MD1	BCKL MD0	LSB 1st	"L"	"L"
XFRFMT0	04	1024 XFR	512 XFR	SYNC	HEAD ER	SBHE ADER	USER DATA	PARI TY	"L"
XFRFMT1	05	BLKE FLAG	BLKE FLSL	ENBY TFBT	BYTE FLSL	ENSB CBT	ALL SBC	SBCE STS	ZA SQEF
DECCTL0	06	AUTO DIST	MODE SEL	FORM SEL	"L"	ENFM 2EDC	MDBY TCTL	EN DLA	ATDL RNEW
DECCTL1	07	ENSB QRD	ENSB CDEC	DEC CMD2	DEC CMD1	DEC CMD0	"L"	"L"	"L"
XFRCTL0	08	AUTO XFR	"H"	"L"	"L"	CPUD MAEN	CPU SRC	"L"	HST SRC
XFRCTL1	09	"L"	"L"	"L"	HSTX FREN	"L"	"L"	"L"	"L"
HIFCTL	0A	CLR BUSY	"L"	"L"	"L"	"L"	ACTH INT2	ACTH INT1	ACTH INT0
DSPCTL	0B	DSTB SL1	DSTB SL0	DIS XLAT	XFR BYT1	XFR BYT0	"L"	"L"	"L"
CHPCTL0	0C	CHIP RST	TGT MET	INC TGT	RPCO RTRG	CLR RSLT	CLDS PCMD	DSPC MDXF	DSPC MDLT
CPUBW DT	0D	b7	b6	b5	b4	b3	b2	b1	b0
DSPCMD	0E	b7	b6	b5	b4	b3	b2	b1	b0
RESULT	0F	b7	b6	b5	b4	b3	b2	b1	b0
SCTINF	10	"L"	"L"	"L"	"L"	"L"	MODE 2	FORM 2	XFR SCT
BLKE STS	11	b7	b6	b5	b4	b3	b2	b1	b0
SBCE STS	12	b7	b6	b5	b4	b3	b2	b1	b0
INC BLKS	13	"L"	"L"	"L"	"L"	"L"	INCB LKS2	INCB LKS1	INCB LKS0
BYTER STS	14	b7	b6	b5	b4	b3	b2	b1	b0
CHPCTL1	15	BURS TXFR	XFRR ATE1	XFRR ATE0	RFRS CTL1	RFRS CTL0	PACK MODE	"L"	"L"
	16	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"

Sub CPU Write Registers (1)

REG	ADR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
TGTMNT	17	b7	b6	b5	b4	b3	b2	b1	b0
TGTSEC	18	b7	b6	b5	b4	b3	b2	b1	b0
TGTBLK	19	b7	b6	b5	b4	b3	b2	b1	b0
	1A	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
XFRCNT -H	1B	b23	b22	b21	b20	b19	b18	b17	b16
XFRCNT -M	1C	b15	b14	b13	b12	b11	b10	b9	b8
XFRCNT -L	1D	b7	b6	b5	b4	b3	b2	b1	b0
BFARA#	1E	b7	b6	b5	b4	b3	b2	b1	b0
DLARA	1F	b7	b6	b5	b4	b3	b2	b1	b0
XFRARA	20	b7	b6	b5	b4	b3	b2	b1	b0
XFRPOS	21	"L"	"L"	"L"	"L"	"L"	"L"	XFR POS1	XFR POS0
	22	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
HXFRC -H	23	"L"	"L"	"L"	"L"	b19	b18	b17	b16
HXFRC -M	24	b15	b14	b13	b12	b11	b10	b9	b8
HXFRC -L	25	b7	b6	b5	b4	b3	b2	b1	b0
	26	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
HADRC -H	27	"L"	"L"	"L"	"L"	"L"	b18	b17	b16
HADRC -M	28	b15	b14	b13	b12	b11	b10	b9	b8
HADRC -L	29	b7	b6	b5	b4	b3	b2	b1	b0
	2A	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
SLADR -H	2B	"L"	"L"	"L"	"L"	"L"	b18	b17	b16
SLADR -M	2C	b15	b14	b13	b12	b11	b10	b9	b8
SLADR -L	2D	b7	b6	b5	b4	b3	b2	b1	b0

Sub-CPU Write Registers (2)

REG	ADR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	2E	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"
CADRC -H	2F	"L"	"L"	"L"	"L"	"L"	b18	b17	b16
CADRC -M	30	b15	b14	b13	b12	b11	b10	b9	b8
CADRC -L	31	b7	b6	b5	b4	b3	b2	b1	b0
CLRINT0	32	DEC INT	DEC TOUT	DRV OVRN	SUBC SYNC	"L"	"L"	"L"	"L"
CLRINT1	33	HCR ISD	"L"	"L"	"L"	HST CMD	RSLT EMPT	XFR STOP	BLXF RCMP
INTEN0	34	DEC INT	DEC TOUT	DRV OVRN	SUBC SYNC	"L"	"L"	"L"	"L"
INTEN1	35	HCR ISD	"L"	"L"	"L"	HST CMD	RSLT EMPT	XFR STOP	BLXF RCMP
BFBLKC -H	36	"L"	"L"	"L"	"L"	"L"	"L"	b9	b8
BFBLKC -L	37	b7	b6	b5	b4	b3	b2	b1	b0

Sub-CPU Write Registers (3)

REG	ADR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
RAWHDR	00	b7	b6	b5	b4	b3	b2	b1	b0
	01								
BFHDR	02	b7	b6	b5	b4	b3	b2	b1	b0
BFSHDR	03	b7	b6	b5	b4	b3	b2	b1	b0
RAWHDR FLG	04	MIN UTE	SEC OND	BLO CK	MODE				
BFHDR FLG	05	MIN UTE	SEC OND	BLO CK	MODE	FILE	CHAN NEL	SUB MODE	DATA TYPE
DECSTS0	06	SHRT SCT	NO SYNC	COR INH	ERIN BLK	COR DONE	EDC NG	ECC NG	TGTN TMET
DECSTS1	07					SBCN TRDY	EDC ALL0	C MODE	C FORM
XFRSTS	08							CBFW RRDY	CBFR DRDY
	09								
HIFSTS	0A	BUSY STS	RSLT EMPT	RSLT WRDY	PRM FULL	PRM RRDY	HINT STS2	HINT STS1	HINT STS0
DSPSTS	0B	REV# "L"	REV# "L"	REV# "H"					CMDO BUSY
	0C								
CPUBR DT	0D	b7	b6	b5	b4	b3	b2	b1	b0
COMM AND	0E	b7	b6	b5	b4	b3	b2	b1	b0
PARAM	0F	b7	b6	b5	b4	b3	b2	b1	b0
SBCSTS	10	SBC OVRN	OVER FLOW	BFNT VAL	NO SYNC	SBC ERR2	SBC ERR1	SBC ERR0	SBC
SBQSTS	11						SHTS BCS1	NOSY NC1	SUBQ ERR1
SUBQDT	12	b7	b6	b5	b4	b3	b2	b1	b0
CSCT ARA	13	b7	b6	b5	b4	b3	b2	b1	b0
	14								
CHPCTL1	15	BURS TXFR	XFRR ATE1	XFRR ATE0	RFRS CTL1	RFRS CTL0	PACK MODE		
	16								

Sub-CPU Read Registers (1)

REG	ADR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
TGTMNT	17	b7	b6	b5	b4	b3	b2	b1	b0
TGTSEC	18	b7	b6	b5	b4	b3	b2	b1	b0
TGTBLK	19	b7	b6	b5	b4	b3	b2	b1	b0
	1A								
XFRCNT -H	1B	b23	b22	b21	b20	b19	b18	b17	b16
XFRCNT -M	1C	b15	b14	b13	b12	b11	b10	b9	b8
XFRCNT -L	1D	b7	b6	b5	b4	b3	b2	b1	b0
BFARA#	1E	b7	b6	b5	b4	b3	b2	b1	b0
DLADR	1F	b7	b6	b5	b4	b3	b2	b1	b0
XFRARA	20	b7	b6	b5	b4	b3	b2	b1	b0
XFRPOS	21							XFR POS1	XFR POS0
	22								
HXFRC -H	23					b19	b18	b17	b16
HXFRC -M	24	b15	b14	b13	b12	b11	b10	b9	b8
HXFRC -L	25	b7	b6	b5	b4	b3	b2	b1	b0
	26								
HADRC -H	27						b18	b17	b16
HADRC -M	28	b15	b14	b13	b12	b11	b10	b9	b8
HADRC -L	29	b7	b6	b5	b4	b3	b2	b1	b0
	2A								
SLADR -H	2B						b18	b17	b16
SLADR -M	2C	b15	b14	b13	b12	b11	b10	b9	b8
SLADR -L	2D	b7	b6	b5	b4	b3	b2	b1	b0

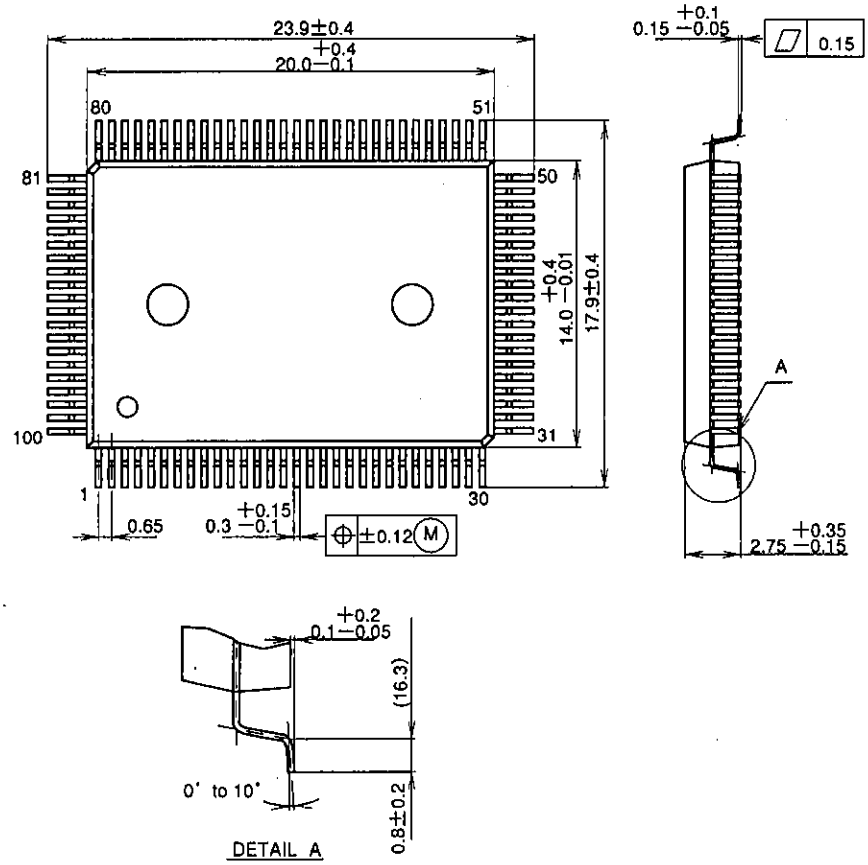
Sub-CPU Read Registers (2)

REG	ADR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	2E								
SADRC -H	2F						b18	b17	b16
SADRC -M	30	b15	b14	b13	b12	b11	b10	b9	b8
SADRC -L	31	b7	b6	b5	b4	b3	b2	b1	b0
INTSTS0	32	DEC INT	DEC TOUT	DRV OVRN	SUBC SYNC				
INTSTS1	33	HCR ISD				HST CMD	RSLT EMPT	XFR STOP	BLXF RCMP
INTEN0	34	DEC INT	DEC TOUT	DRV OVRN	SUBC SYNC				
INTEN1	35	HCR ISD				HST CMD	RSLT EMPT	XFR STOP	BLXF RCMP
BFBLKC -H	36							b9	b8
BFBLKC -L	37	b7	b6	b5	b4	b3	b2	b1	b0

Sub-CPU Read Registers (3)

Package Outline Unit : mm

100PIN QFP(PLASTIC)



PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	1.7 g

SONY CODE	QFP-100P-L01
EIAJ CODE	*QFP100-P-1420-A
JEDEC CODE	————

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