SONY

CXD1804AR

CD-ROM Decoder

Description

The CXD1804AR is a CD-ROM decoder LSI with a built-in Fast SCSI controller.

Features

- Fast SCSI controller (Target mode)
- Maximum transfer speed of 10MB/s (when using Fast SCSI synchronous transfer)
- SCSI overhead reduced by executing multiple SCSI sequences
- Supports SCAM Level 2
- Compatible with CD-ROM, CD-I and CD-ROM XA formats
- Real-time error correction
- Capable of handling up to twelvefold-speed playback
- Multiblock auto-transfer function
- Can read subcode-Q data for each byte from the sub CPU
- Real-time subcode (R to W) error correction
- Serial transfer of commands to CD DSP
- Connectable with standard DRAM of up to 8M bits (1024K bytes)
- DRAM bit width selectable for 8 bits or 16 bits

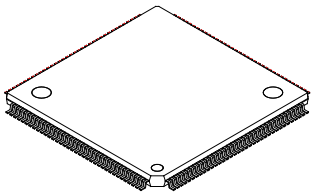
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	–0.5 to +7.0	V
• Input voltage	V_I	–0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	–0.5 to V_{DD} + 0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5 (5.0 typ.)	V
• Operating temperature	Topr	–20 to +75	°C

144 pin LQFP (Plastic)



Applications

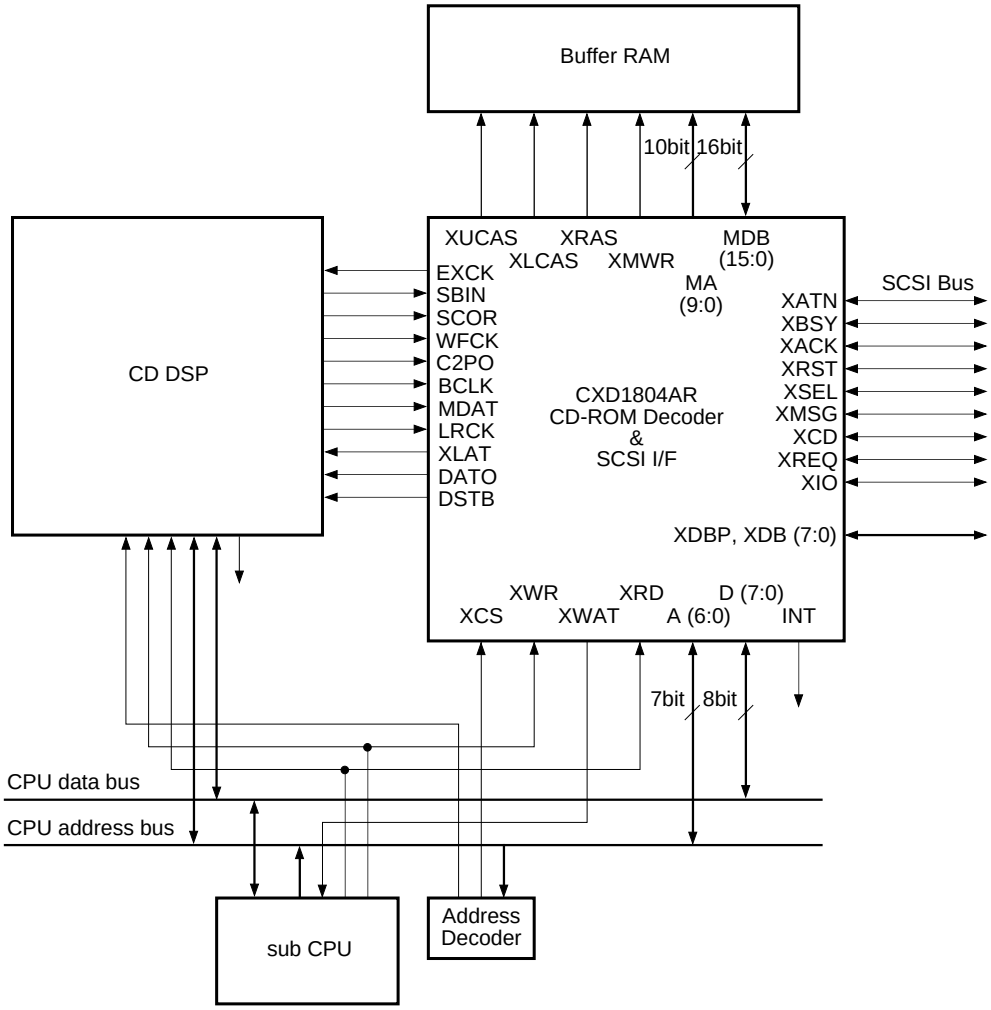
CD-ROM drives

Structure

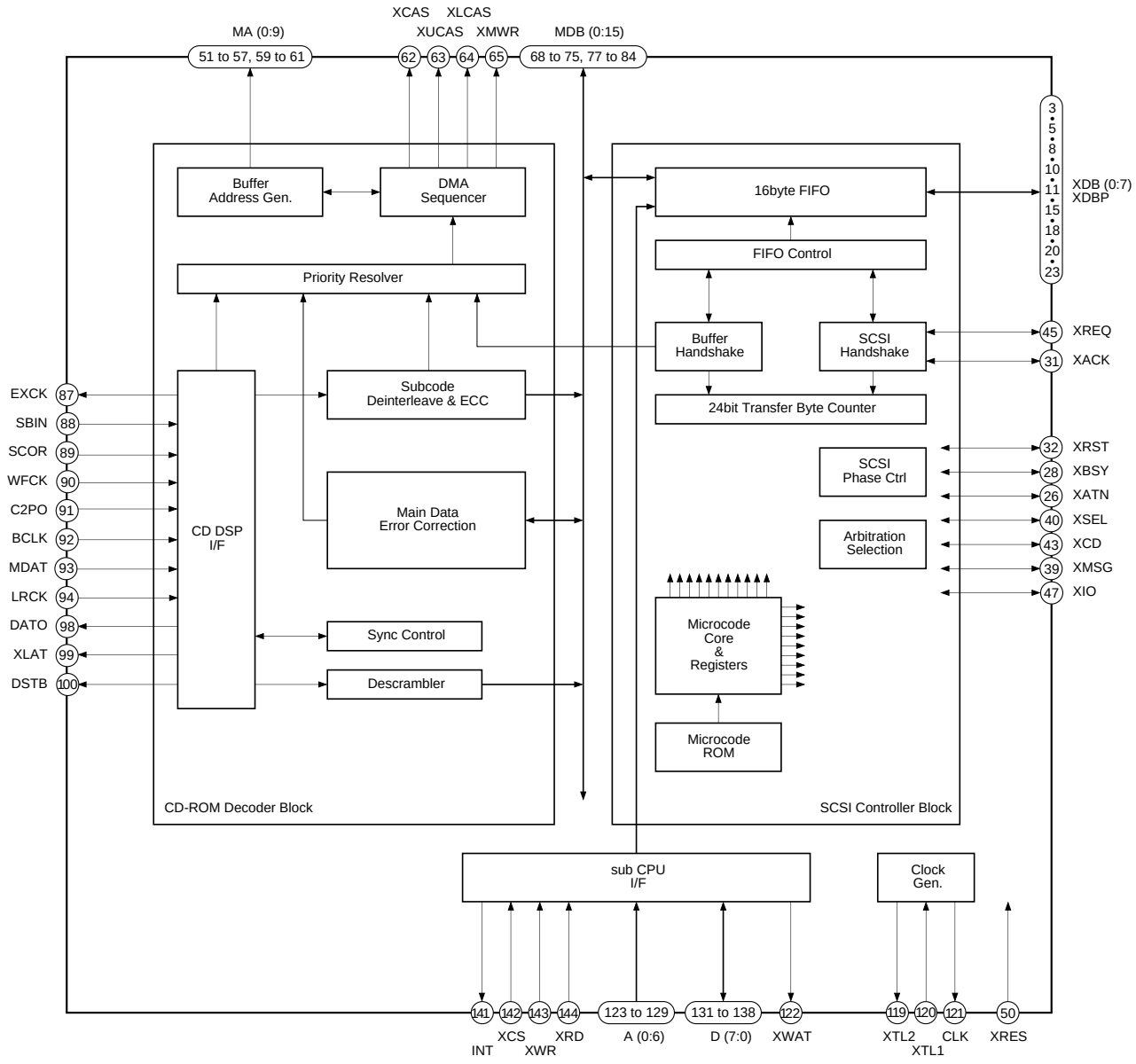
Silicon gate CMOS IC

E96658-PS

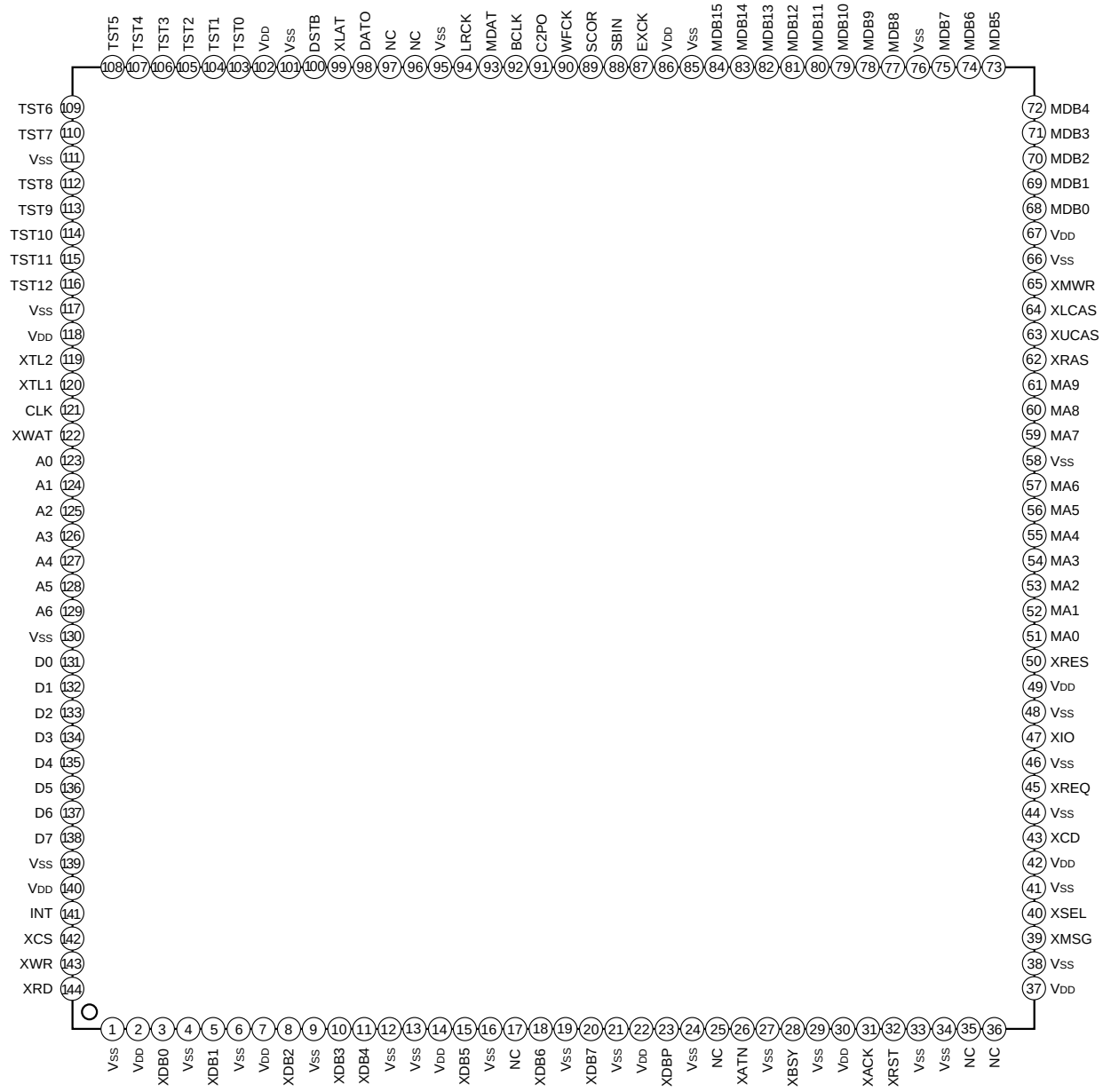
Connection Example



Block Diagram



Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Logic	Classification	Description
1	V_{SS}	—	—	Power	V_{SS}
2	V_{DD}	—	—	Power	V_{DD}
3	XDB0	I/O	Negative	SCSI I/F	SCSI data bus bit 0
4	V_{SS}	—	—	Power	V_{SS}
5	XDB1	I/O	Negative	SCSI I/F	SCSI data bus bit 1
6	V_{SS}	—	—	Power	V_{SS}
7	V_{DD}	—	—	Power	V_{DD}
8	XDB2	I/O	Negative	SCSI I/F	SCSI data bus bit 2
9	V_{SS}	—	—	Power	V_{SS}
10	XDB3	I/O	Negative	SCSI I/F	SCSI data bus bit 3
11	XDB4	I/O	Negative	SCSI I/F	SCSI data bus bit 4
12	V_{SS}	—	—	Power	V_{SS}
13	V_{SS}	—	—	Power	V_{SS}
14	V_{DD}	—	—	Power	V_{DD}
15	XDB5	I/O	Negative	SCSI I/F	SCSI data bus bit 5
16	V_{SS}	—	—	Power	V_{SS}
17	NC	—	—	NC	NC
18	XDB6	I/O	Negative	SCSI I/F	SCSI data bus bit 6
19	V_{SS}	—	—	Power	V_{SS}
20	XDB7	I/O	Negative	SCSI I/F	SCSI data bus bit 7
21	V_{SS}	—	—	Power	V_{SS}
22	V_{DD}	—	—	Power	V_{DD}
23	XDBP	I/O	Negative	SCSI I/F	SCSI data bus parity
24	V_{SS}	—	—	Power	V_{SS}
25	NC	—	—	NC	NC
26	XATN	I/O	Negative	SCSI I/F	SCSI control bus XATN signal
27	V_{SS}	—	—	Power	V_{SS}
28	XBSY	I/O	Negative	SCSI I/F	SCSI control bus XBSY signal
29	V_{SS}	—	—	Power	V_{SS}
30	V_{DD}	—	—	Power	V_{DD}
31	XACK	I/O	Negative	SCSI I/F	SCSI control bus XACK signal
32	XRST	I/O	Negative	SCSI I/F	SCSI control bus XRST signal
33	V_{SS}	—	—	Power	V_{SS}
34	V_{SS}	—	—	Power	V_{SS}
35	NC	—	—	NC	NC
36	NC	—	—	NC	NC

Pin No.	Symbol	I/O	Logic	Classification	Description
37	V_{DD}	—	—	Power	V_{DD}
38	V_{SS}	—	—	Power	V_{SS}
39	XMSG	I/O	Negative	SCSI I/F	SCSI control bus XMSG signal
40	XSEL	I/O	Negative	SCSI I/F	SCSI data bus XSEL signal
41	V_{SS}	—	—	Power	V_{SS}
42	V_{DD}	—	—	Power	V_{DD}
43	XCD	I/O	Negative	SCSI I/F	SCSI control bus XCD signal
44	V_{SS}	—	—	Power	V_{SS}
45	XREQ	I/O	Negative	SCSI I/F	SCSI control bus XREQ signal
46	V_{SS}	—	—	Power	V_{SS}
47	XIO	I/O	Negative	SCSI I/F	SCSI control bus XIO signal
48	V_{SS}	—	—	Power	V_{SS}
49	V_{DD}	—	—	Power	V_{DD}
50	XRES	I	Negative	System I/F	CXD1804AR reset signal
51	MA0	O		BufMem I/F	Address bus output bit 0 to buffer memory
52	MA1	O		BufMem I/F	Address bus output bit 1 to buffer memory
53	MA2	O		BufMem I/F	Address bus output bit 2 to buffer memory
54	MA3	O		BufMem I/F	Address bus output bit 3 to buffer memory
55	MA4	O		BufMem I/F	Address bus output bit 4 to buffer memory
56	MA5	O		BufMem I/F	Address bus output bit 5 to buffer memory
57	MA6	O		BufMem I/F	Address bus output bit 6 to buffer memory
58	V_{SS}	—	—	Power	V_{SS}
59	MA7	O		BufMem I/F	Address bus output bit 7 to buffer memory
60	MA8	O		BufMem I/F	Address bus output bit 8 to buffer memory
61	MA9	O		BufMem I/F	Address bus output bit 9 to buffer memory
62	XRAS	O	Negative	BufMem I/F	Buffer memory RAS (Row Address Strobe) signal
63	XUCAS	O	Negative	BufMem I/F	Buffer memory CAS (Column Address Strobe) signal
64	XLCAS	O	Negative	BufMem I/F	Buffer memory CAS (Column Address Strobe) signal
65	XMWR	O	Negative	BufMem I/F	Data write strobe signal to buffer memory
66	V_{SS}	—	—	Power	V_{SS}
67	V_{DD}	—	—	BufMem I/F	V_{DD}
68	MDB0	I/O		BufMem I/F	Buffer memory data bus bit 0
69	MDB1	I/O		BufMem I/F	Buffer memory data bus bit 1
70	MDB2	I/O		BufMem I/F	Buffer memory data bus bit 2
71	MDB3	I/O		BufMem I/F	Buffer memory data bus bit 3
72	MDB4	I/O		BufMem I/F	Buffer memory data bus bit 4
73	MDB5	I/O		BufMem I/F	Buffer memory data bus bit 5

Pin No.	Symbol	I/O	Logic	Classification	Description
74	MDB6	I/O		BufMem I/F	Buffer memory data bus bit 6
75	MDB7	I/O	—	BufMem I/F	Buffer memory data bus bit 7
76	V_{SS}	—		Power	V_{SS}
77	MDB8	I/O		BufMem I/F	Buffer memory data bus bit 8
78	MDB9	I/O		BufMem I/F	Buffer memory data bus bit 9
79	MDB10	I/O		BufMem I/F	Buffer memory data bus bit 10
80	MDB11	I/O		BufMem I/F	Buffer memory data bus bit 11
81	MDB12	I/O		BufMem I/F	Buffer memory data bus bit 12
82	MDB13	I/O		BufMem I/F	Buffer memory data bus bit 13
83	MDB14	I/O		BufMem I/F	Buffer memory data bus bit 14
84	MDB15	I/O		BufMem I/F	Buffer memory data bus bit 15
85	V_{SS}	—	—	Power	V_{SS}
86	V_{DD}	—	—	Power	V_{DD}
87	EXCK	O		CD DSP I/F	SBIN read clock (connected to the EXCK pin (Pin 65) of the CXD2500)
88	SBIN	I		CD DSP I/F	Subcode serial signal (connected to the SBSO pin (Pin 64) of the CXD2500)
89	SCOR	I		CD DSP I/F	Subcode sync signal (connected to the SCOR pin (Pin 63) of the CXD2500)
90	WFCK	I		CD DSP I/F	Write frame clock (connected to the WFCK pin (Pin 62) of the CXD2500)
91	C2PO	I		CD DSP I/F	Indicates that an error exists in C2 pointer signal MDAT.
92	BCLK	I		CD DSP I/F	Bit clock. MDAT strobe signal.
93	MDAT	I		CD DSP I/F	Serial data stream from CD DSP
94	LRCK	I		CD DSP I/F	LR signal. Indicates MDAT L or R channel.
95	V_{SS}	—	—	Power	V_{SS}
96	NC	—	—	NC	NC
97	NC	—	—	NC	NC
98	DATO	O		CD DSP I/F	Serial data output from sub CPU to CD DSP
99	XLAT	O		CD DSP I/F	DATO latch signal. Latches at the rising edge.
100	DSTB	O		CD DSP I/F	DATO transfer clock
101	V_{SS}	—	—	Power	V_{SS}
102	V_{DD}	—	—	Power	V_{DD}
103	TST0	I		Test I/F	Test pin 0
104	TST1	I		Test I/F	Test pin 1
105	TST2	I		Test I/F	Test pin 2
106	TST3	I		Test I/F	Test pin 3
107	TST4	I		Test I/F	Test pin 4

Pin No.	Symbol	I/O	Logic	Classification	Description
108	TST5	I		Test I/F	Test pin 5
109	TST6	I		Test I/F	Test pin 6
110	TST7	I		Test I/F	Test pin 7
111	V_{SS}	—	—	Power	V_{SS}
112	TST8	I		Test I/F	Test pin 8
113	TST9	I		Test I/F	Test pin 9
114	TST10	I		Test I/F	Test pin 10
115	TST11	I		Test I/F	Test pin 11
116	TST12	I		Test I/F	Test pin 12
117	V_{SS}	—	—	Power	V_{SS}
118	V_{DD}	—	—	Power	V_{DD}
119	XTL2	O		System I/F	Crystal oscillation circuit output
120	XTL1	I		System I/F	Crystal oscillation circuit input
121	CLK	O		System I/F	Clock output
122	XWAT	O	Negative	sub CPU I/F	Wait signal for sub CPU buffer memory access
123	A0	I		sub CPU I/F	CXD1804AR built-in register address bus bit 0
124	A1	I		sub CPU I/F	CXD1804AR built-in register address bus bit 1
125	A2	I		sub CPU I/F	CXD1804AR built-in register address bus bit 2
126	A3	I		sub CPU I/F	CXD1804AR built-in register address bus bit 3
127	A4	I		sub CPU I/F	CXD1804AR built-in register address bus bit 4
128	A5	I		sub CPU I/F	CXD1804AR built-in register address bus bit 5
129	A6	I		sub CPU I/F	CXD1804AR built-in register address bus bit 6
130	V_{SS}	—	—	Power	V_{SS}
131	D0	I/O		sub CPU I/F	Sub CPU data bus bit 0
132	D1	I/O		sub CPU I/F	Sub CPU data bus bit 1
133	D2	I/O		sub CPU I/F	Sub CPU data bus bit 2
134	D3	I/O		sub CPU I/F	Sub CPU data bus bit 3
135	D4	I/O		sub CPU I/F	Sub CPU data bus bit 4
136	D5	I/O		sub CPU I/F	Sub CPU data bus bit 5
137	D6	I/O		sub CPU I/F	Sub CPU data bus bit 6
138	D7	I/O		sub CPU I/F	Sub CPU data bus bit 7
139	V_{SS}	—	—	Power	V_{SS}
140	V_{DD}	—	—	Power	V_{DD}
141	INT	O	Selectable	sub CPU I/F	Interrupt to sub CPU
142	XCS	I	Negative	sub CPU I/F	CXD1804AR chip select signal
143	XWR	I	Negative	sub CPU I/F	CXD1804AR built-in register write signal
144	XRD	I	Negative	sub CPU I/F	CXD1804AR built-in register read signal

Electrical Characteristics (V_{DD} = 5V ± 10%, V_{SS} = 0V, Topr = –20 to +75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable pins
TTL input level pin High level input voltage	V_{IH1}		2.2			V	*1
TTL input level pin Low level input voltage	V_{IL1}				0.8	V	*1
CMOS input level pin High level input voltage	V_{IH2}		0.7V_{DD}			V	*2
CMOS input level pin Low level input voltage	V_{IL2}				0.3V_{DD}	V	*2
CMOS Schmitt input level pin High level input voltage	V_{IH4}		0.8V_{DD}			V	*3
CMOS Schmitt input level pin Low level input voltage	V_{IL4}				0.2V_{DD}	V	*3
CMOS Schmitt input level pin Input voltage hysteresis	$V_{IH4} – V_{IL4}$			0.6		V	*3
TTL Schmitt input level pin High level input voltage	V_{IH5}		2.2V			V	*4
TTL Schmitt input level pin Low level input voltage	V_{IL5}				0.8V	V	*4
TTL Schmitt input level pin Input voltage hysteresis	$V_{IH5} – V_{IL4}$			0.4		V	*4
SCSI Schmitt input level pin High level input voltage	V_{IHS}		2.2V			V	*11
SCSI Schmitt input level pin Low level input voltage	V_{ILS}				0.8V	V	*11
SCSI Schmitt input level pin Input voltage hysteresis	$V_{IHTS} – V_{ILTS}$			0.4		V	*11
Bidirectional pin with pull-up resistor Input current	I_{IL3}	V_{IN} = 0V	–90	–200	–440	µA	*5
High level output voltage	V_{OH1}	I_{OH} = –2mA	V_{DD} – 0.8			V	*6
High level output voltage	V_{OH2}	I_{OH} = –6mA	V_{DD} – 0.8			V	*7
SCSI high level output voltage	V_{OHS}		2.5		3.7	V	*12
Low level output voltage	V_{OL1}	I_{OL} = 4mA			0.4	V	*8
SCSI low level output voltage	V_{OLS}	I_{OL} = 48mA			0.5	V	*11
Input leakage current	I_{I1}	V_{IN} = V_{SS} or V_{DD}	–10		10	µA	*9
Oscillation cell high level input voltage	V_{IH4}		0.7V_{DD}			V	*10
Oscillation cell low level input voltage	V_{IL4}				0.3V_{DD}	V	
Oscillation cell logic threshold value	LV_{TH}			0.5V_{DD}		V	
Oscillation cell feedback resistance value	R_{FB}	V_{IN} = V_{SS} or V_{DD}	250k	1M	2.5M	Ω	
Oscillation cell high level output voltage	V_{OH3}	I_{OH} = –12mA	0.5V_{DD}			V	
Oscillation cell low level output voltage	V_{OL3}	I_{OL} = 12mA			0.5V_{DD}	V	

*1 D7 to 0, MDBF to 0
*2 MDAT, LRCK, C2PO, SBIN, SCOR, TD12 to 0
*3 BLCK, WFCK, XRES
*4 A6 to 0, XWR, XRD, XCS
*5 D7 to 0, MDBF to 0
*6 All output pins except XTL2, XRAS, XUCAS, XLCAS, XMWR and CLK
*7 XRAS, XUCAS, XLCAS, XMWR, CLK
*8 All output pins except XTL2
*9 All input pins except *5 and XTL1
*10 Input: XTL1, Output: XTL2
*11 XRST, XBSY, XSEL, XATN, XMSG, XCD, XIO, XREQ, XACK, XDBP, XDB7 to 0
*12 XREQ, XACK, XDBP and XDB7 to 0 when active negation is ON

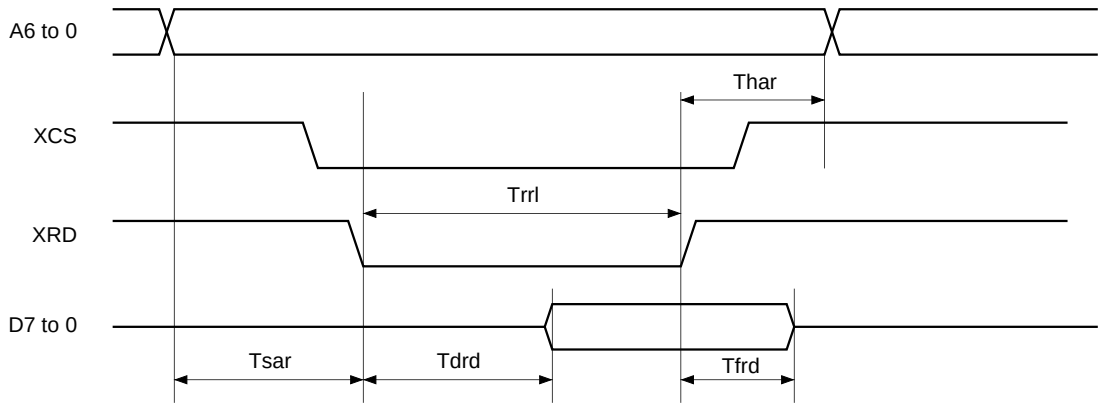
I/O Capacitance (V_{DD} = V_I = 0V, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}			9	pF
Output capacitance	C_{OUT}			11	pF
I/O capacitance	$C_{I/O}$			11	pF

AC Characteristics

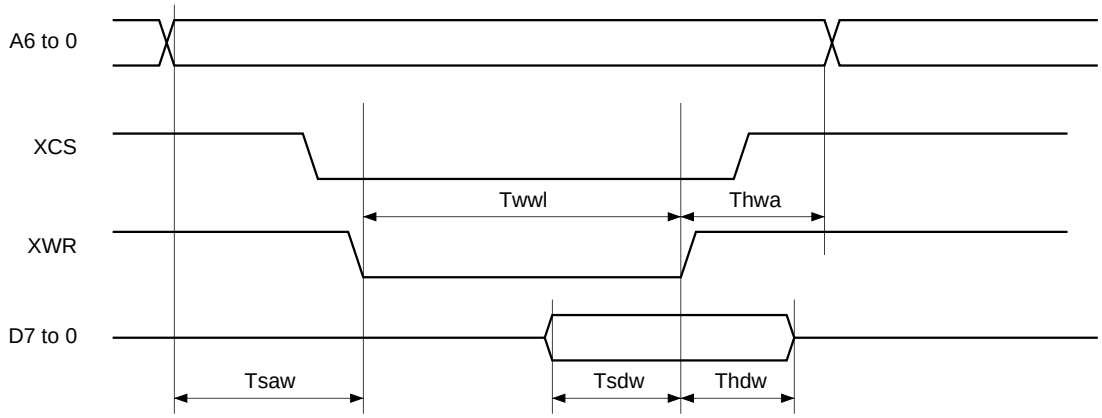
1. Sub CPU Interface (Output Load = 50pF)

(1) Read



Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (for XCS & XRD ↓)	Tsar	10			ns
Address hold time (for XCS & XRD ↑)	Thar	10			ns
Data delay time (for XCS & XRD ↓)	Tdrd			35	ns
Data float time (for XCS & XRD ↑)	Tfrd	0		15	ns

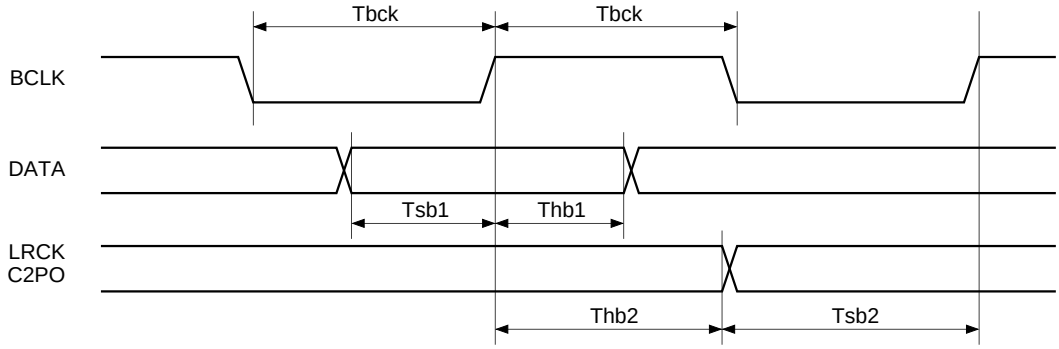
(2) Write



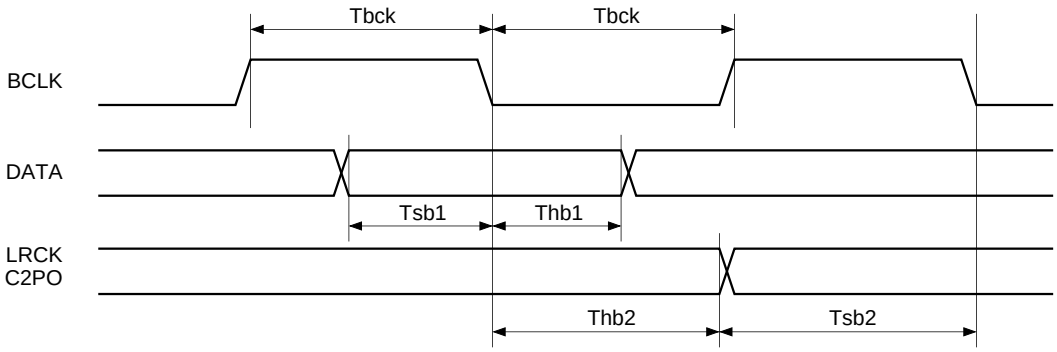
Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (for XCS & XWR ↓)	Tsaw	20			ns
Address hold time (for XCS & XWR ↑)	Thaw	10			ns
Data setup time (for XCS & XWR ↓)	Tsdw	20			ns
Data hold time (for XCS & XWR ↑)	Thdw	10			ns
Low level XWR pulse width	Twwl	30			ns

2. CD DSP Interface

BCKRED = "H"



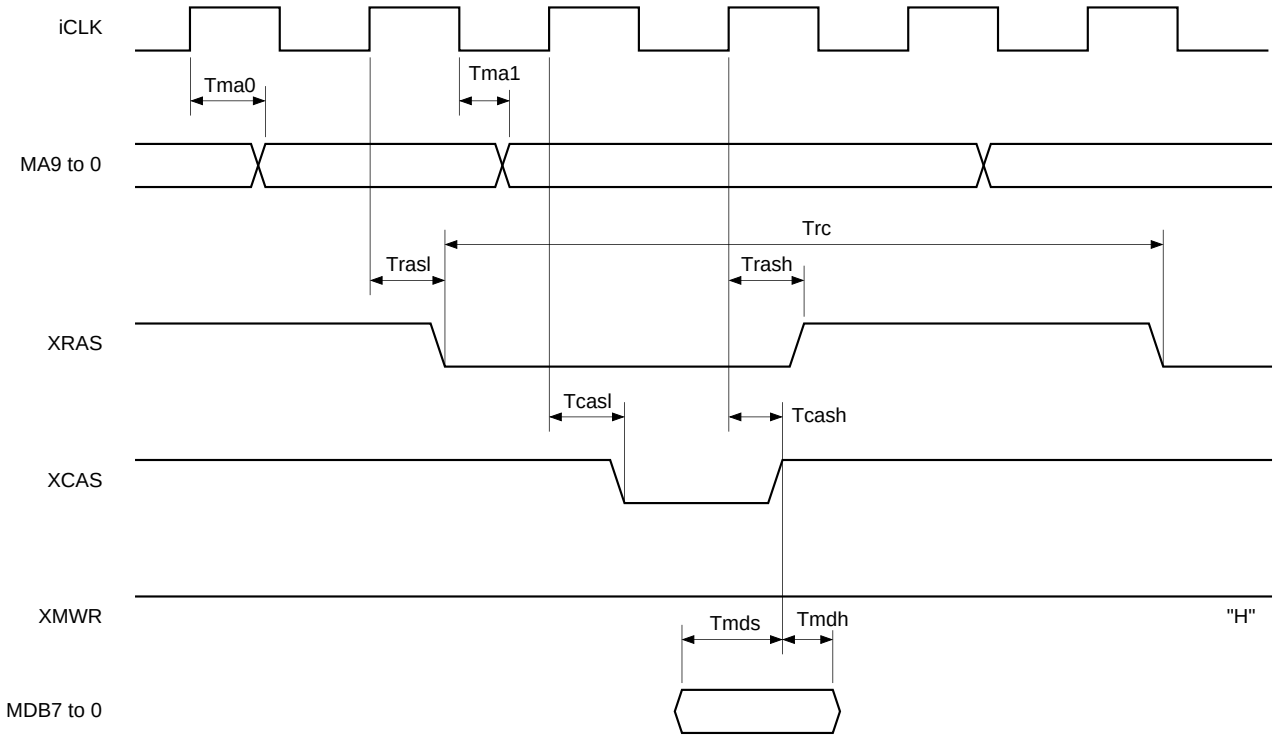
BCKRED = "L"



Item	Symbol	Min.	Typ.	Max.	Unit
BCLK frequency	Fbck			26	ns
BCLK pulse width	Tbck	19			ns
DATA setup time (for BCLK)	Tsb1	10			ns
DATA hold time (for BCLK)	Thb1	10			ns
LRCK, C2PO setup time (for BCLK)	Tsb2	10			ns
LRCK, C2PO hold time (for BCLK)	Thb2	10			ns

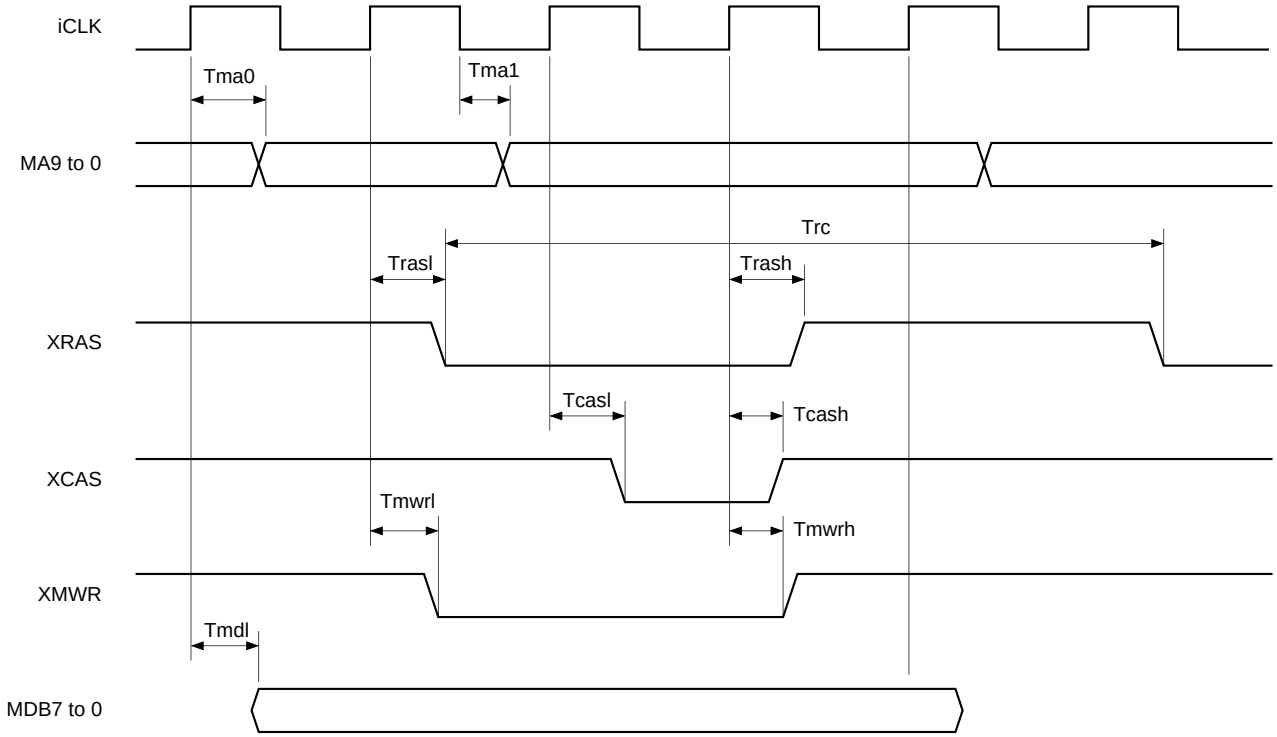
3. DRAM Interface

(1) Read



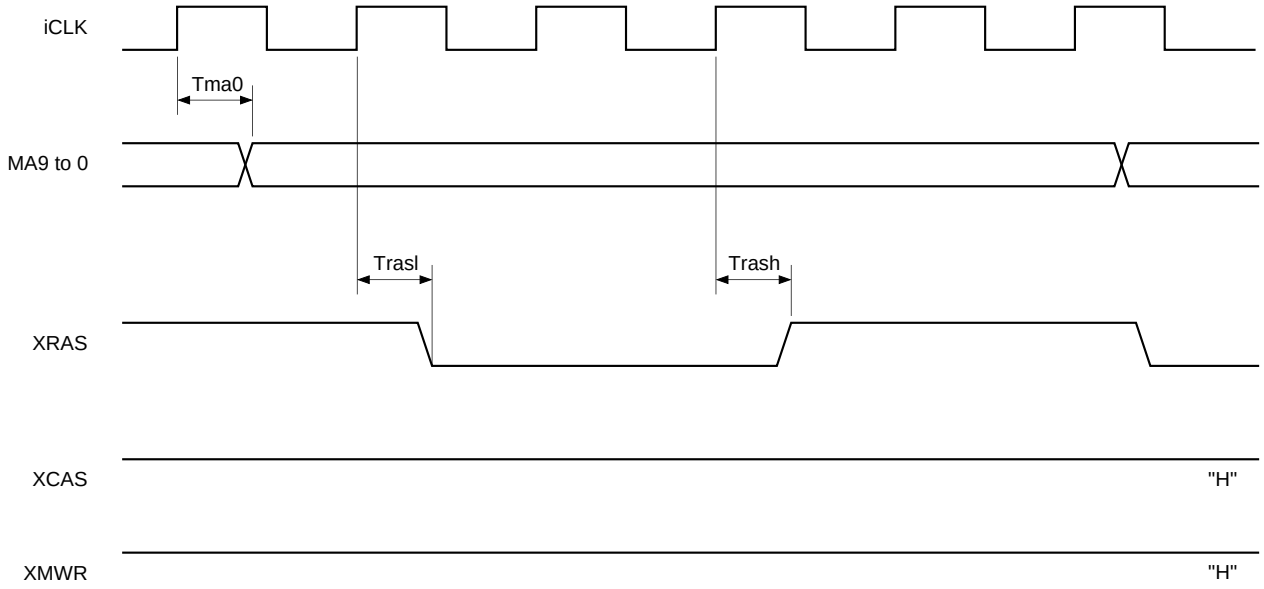
Item	Symbol	Min.	Typ.	Max.	Unit
Random read/write cycle time	Trc	5Tw			ns
Address delay time (for XTL2 ↑)	Tma0	13	24	45	ns
Address delay time (for XTL2 ↓)	Tma1	11	22	41	ns
XRAS ↓ delay time (for XTL2 ↑)	Trasl	6	12	23	ns
XRAS ↑ delay time (for XTL2 ↑)	Trash	6	11	20	ns
XCAS ↓ delay time (for XTL2 ↑)	Tcasl	7	14	25	ns
XCAS ↑ delay time (for XTL2 ↑)	Tcash	6	12	22	ns
Data setup time (for XCAS ↑)	Tmds	2	4	6	ns
Data hold time (for XCAS ↓)	Tmdh	0			ns

(2) Write



Item	Symbol	Min.	Typ.	Max.	Unit
Random read/write cycle time	Trc	5Tw			ns
Address delay time (for XTL2 ↑)	Tma0	13	24	45	ns
Address delay time (for XTL2 ↓)	Tma1	11	22	41	ns
XRAS ↓ delay time (for XTL2 ↑)	Trasl	6	12	23	ns
XRAS ↑ delay time (for XTL2 ↑)	Trash	6	11	20	ns
XCAS ↓ delay time (for XTL2 ↑)	Tcasl	7	14	25	ns
XCAS ↑ delay time (for XTL2 ↑)	Tcash	6	12	22	ns
XMWR ↓ delay time (for XTL2 ↑)	Tmwrl	7	14	25	ns
XMWR ↑ delay time (for XTL2 ↑)	Tmwrh	6	11	21	ns
Data setup time (for XTL2 ↑)	Tmdws	14	28	51	ns
Data hold time (for XTL2 ↑)	Tmdwh	7	14	26	ns

(3) Refresh (RAS only refresh)

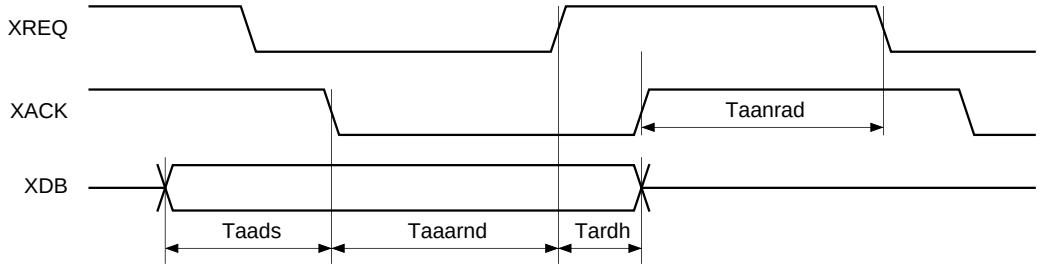


Item	Symbol	Min.	Typ.	Max.	Unit
Random read/write cycle time	Trc	5Tw			ns
Address delay time (for XTL2 ↑)	Tma0	12	24	43	ns
XRAS ↓ delay time (for XTL2 ↑)	Tras1	6	12	23	ns
XRAS ↑ delay time (for XTL2 ↑)	Trash	6	11	20	ns

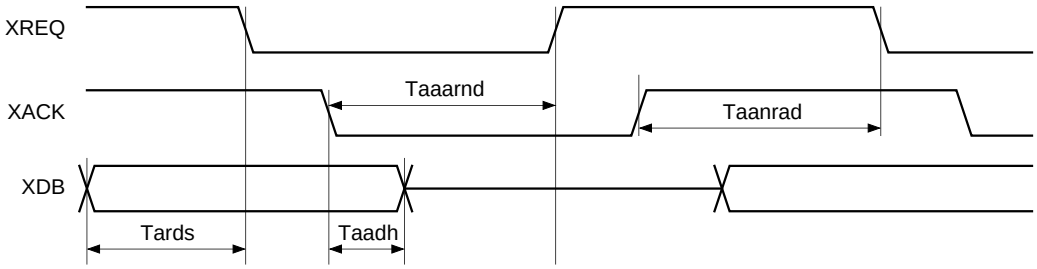
4. SCSI Interface

(1) SCSI asynchronous transfer timing

When receiving: Initiator → Target



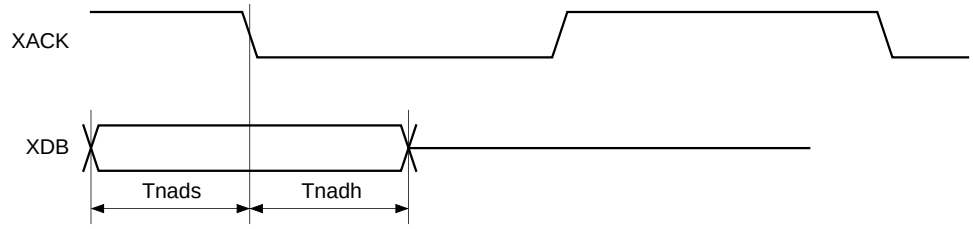
When transmitting: Target → Initiator



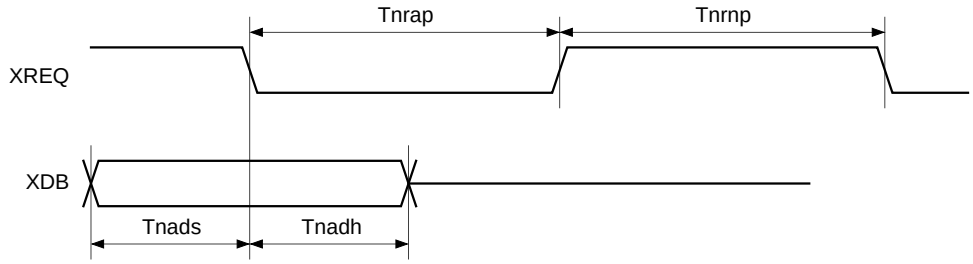
Item	Symbol	Min.	Typ.	Max.	Unit
XDB setup time (for XACK ↓)	Taads	15			ns
XDB hold time (for XREQ ↑)	Tardh	0			ns
XDB setup time (for XREQ ↓)	Tards	30			ns
XDB hold time (for XREQ ↓)	Taadh	60			ns
XREQ rise delay time (for XACK ↓)	Taaarnd	30		70	ns
XREQ fall time (for XACK ↑)	Taanrad	30		85	ns

(2) SCSI synchronous transfer timing

When receiving: Initiator → Target



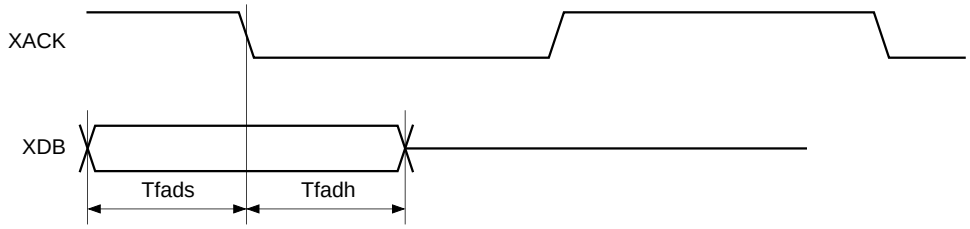
When transmitting: Target → Initiator



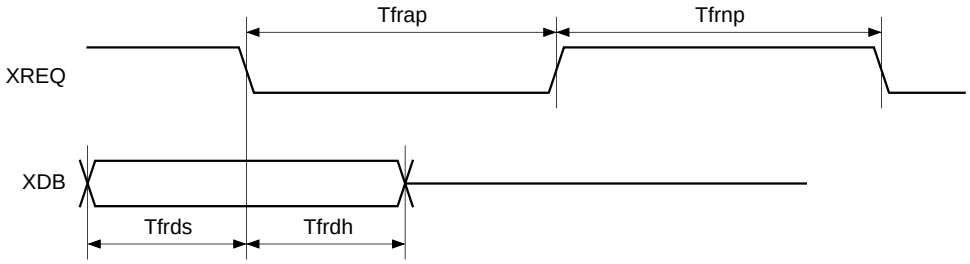
Item	Symbol	Min.	Typ.	Max.	Unit
XDB setup time (for XACK ↓)	Tnads	15			ns
XDB hold time (for XACK ↓)	Tnadh	10			ns
XDB setup time (for XREQ ↓)	Tnrds	80			ns
XDB hold time (for XREQ ↓)	Tnrdh	105			ns
XREQ assert time	Tnrap			110	ns
XREQ negate time	Tnrnp	90			ns

(3) Fast SCSI synchronous transfer timing

When receiving: Initiator → Target



When transmitting: Target → Initiator



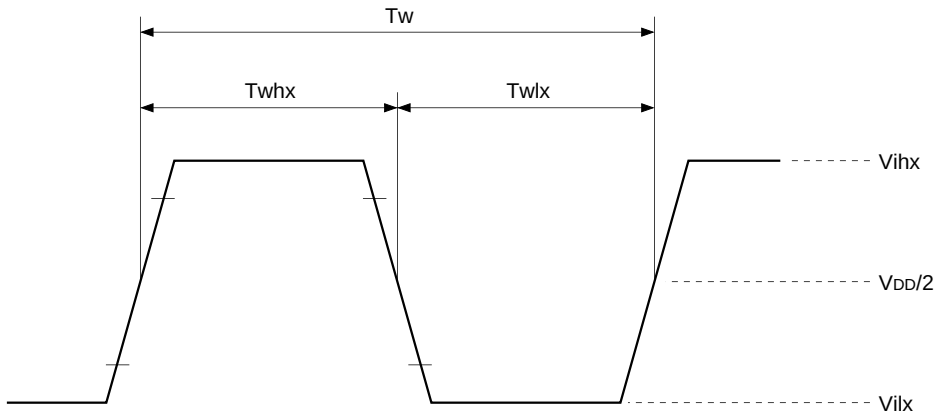
Item	Symbol	Min.	Typ.	Max.	Unit
XDB setup time (for XACK ↓)	Tfads	15			ns
XDB hold time (for XACK ↓)	Tfadh	10			ns
XDB setup time (for XREQ ↓)	Tfrds	55			ns
XDB hold time (for XREQ ↓)	Tfrdh	55			ns
XREQ assert time	Tfrap			60	ns
XREQ negate time	Tfrnp	40			ns

5. XTL1 and XTL2 Pins

(1) When using self-excited oscillation

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency	Fmax			40.0	MHz

(2) When inputting a pulse to the XTL1 pin



Item	Symbol	Min.	Typ.	Max.	Unit
High level pulse width	Twhx	10			ns
Low level pulse width	Twhx	10			ns
Pulse cycle	Tw	25			ns

Contents

[1] Description of Registers

The CXD1804AR's register address area is allotted as shown in the table below.

Address		Description
00h to 4Fh	0xx xxxx 100 xxxx	CD-ROM decoder block
50h to 6Fh	101 xxxx 110 xxxx	SCSI2 interface block
70h to 7Fh	111 xxxx	CD-ROM decoder/SCSI2 interface common block

1-1. Description of Decoder Block Registers

1-1-1. 00h

(1) RAWMIN (raw minute) register (read)

RAWMIN (raw minute) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
00h (R)									REWMIN

The Header Minute byte for the sector being sent from the CD DSP while DECINT is active can be read from this register. A difference of two sectors exists between the RAWxxx and BFxxx registers during the write-only and real-time correction modes.

(2) CONFIG0 (configuration 0) register (write)

CONFIG0 (configuration 0) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
00h (W)	CINT POL	RAM SIZE1	RAM SIZE0	RAM8 BITW	RAM2 CAS	EXCK SEL	CLK SEL1	CLK SEL0	CONFIG0

bit 7: CINTPOL (sub CPU interrupt polarity)

High: The INT pin becomes active high. When the register is inactive, it goes low.

Low: The INT pin becomes active low. When the register is inactive, it goes to high impedance.

bits 6, 5: RAMSIZE1, 0 (DRAM size 1, 0)

Set these bits according to the total size of the DRAM connected to this IC.

RAMSIZE1	RAMSIZE0	DRAM total size
"L"	"L"	1M bits
"L"	"H"	2M bits
"H"	"L"	4M bits
"H"	"H"	8M bits

bit 4: RAM8BITW (DRAM 8-bit wide)

This bit is set according to the bit width of the DRAM data bus to be connected.

High: Set this bit high when the DRAM to be connected has the 8-bit width.

Low: Set this bit low when the DRAM to be connected has the 16-bit width.
(Set low when two 8-bit width DRAMs are connected in parallel.)

bit 3: RAM2CAS (DRAM 2 CAS)

When the DRAM bus width is 16 bits, set this bit according to the number of CAS and WE signals. When the DRAM bus width is 8 bits, this bit has no meaning.

High: Set this bit high when the IC is connected to a DRAM with 2 CAS signals and 1 WE signal.

Low: Set this bit low when the IC is connected to a DRAM with 1 CAS signal and 2 WE signals.

bit 2: EXCKSEL (EXCK select)

This bit determines the frequency of the EXCK clock that is used to get the subcode from the CD DSP. This bit is set by the sub CPU on the basis of the playback speed and the clock frequency on the XTL1 pin. (The maximum frequency for EXCK is 1MHz.)

High: The EXCK frequency is 1/48 the frequency of the XTL1 pin. Set this bit high when the XTL1 frequency is greater than 32MHz.

Low: The EXCK frequency is 1/32 the frequency of the XTL1 pin. Set this bit low when the XTL1 frequency is less than 32MHz.

bits 1, 0: CLKSEL1, 0 (CLK select 1, 0)

These bits determine the clock frequency output from the CLK pin.

CLKSEL1	CLKSEL0	Clock frequency
"L"	"L"	Fixed to high
"L"	"H"	1/2 of XTL1
"H"	"L"	Same frequency as XTL1
"H"	"H"	RESERVED

1-1-2. 01h

(1) RAWSEC (raw second) register (read)

RAWSEC (raw second) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
00h (R)									RAWSEC

The Header Second byte for the sector being sent from the CD DSP while DECINT is active can be read from this register.

(2) CONFIG1 (configuration 1) register (write)

CONFIG1 (configuration 1) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
00h (W)	SW OPEN	SYC NGC2	SYC NGC1	SYC NGC0	HWKR QDIS	"L"	SBC ECC1	SBC ECC0	CONFIG1

bit 7: SWOPEN (sync window open)

High: The Sync mark detection window opens. In this case, the IC's internal Sync protection circuit is disabled.

Low: The Sync mark detection window is controlled by the IC's internal Sync protection circuit.

bits 6 to 4: SYCNGC2 to 0 (sync NG count 2 to 0)

The Sync mark detection window opens once the number of Sync marks specified by these bits is inserted. Setting a value of 1h or less for these bits is prohibited. (After a reset, these bits are set to 2h.)

bit 3 HWKRQDIS (host DMA weak request disable)

High: (For the send system command passed through a buffer)
When the FIFO does not have eight empty bytes or more, the DMA does not start to the FIFO from the buffer.
(For the receive system command passed through a buffer)
When the data of eight bytes or more are written (or the last data is written) in the FIFO, the DMA starts to the buffer from the FIFO.

Low: (For the send system command passed through a buffer)
When the FIFO is not filled with data, the DMA starts to the FIFO from the buffer.
(For the receive system command passed through a buffer)
The DMA starts to the buffer from the FIFO immediately after the data are written in the FIFO.

The number of times of the DMA execution for the host is reduced by setting this bit high.
(Because the page mode is always used.)

bit 2: RESERVED
Normally set low.

bits 1, 0: SBCECC1, 0 (subcode ECC 1, 0)
These two bits specify the error correction method when decoding the subcode.

SBECC1	SBECC0	Subcode error correction
"X"	"L"	Error correction not performed.
"L"	"H"	Single error correction performed.
"H"	"H"	Double error correction performed.

1-1-3. 02h

(1) RAWBLK (raw block) register (read)

RAWBLK (raw block) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
02h (R)									RAWBLK

The Header Block byte for the sector being sent from the CD DSP while DECINT is active can be read from this register.

(2) DSPIF (DSP interface) register (write)

DSPIF (DSP interface) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
02h (W)	C2PO L1st	LCH LOW	BCK RED	BCKL MD1	BCKL MD0	LSB 1st	"L"	BFSH DFSL	DSPIF

This register controls the connection mode with the CD DSP. After the IC is reset, the sub CPU sets this register according to the CD DSP to be connected.

bit 7: C2PL1ST (C2PO lower byte first)

High: When two bytes of data are input, C2PO inputs the lower byte first followed by the upper byte.

Low: When two bytes of data are input, C2PO inputs the upper byte first followed by the lower byte.
Here, "upper byte" means the upper 8 bits including MSB from the CD DSP and "lower byte" means the lower 8 bits including LSB from the CD DSP. For example, the Header minute byte is the lower byte and the second byte, the upper byte.

bit 6: LCHLOW (Lch low)
High: When LRCK is low, determined to be the left channel data.
Low: When LRCK is high, determined to be the right channel data.

bit 5: BCKRED (BLCK rising edge)
High: Data is strobed at the rising edge of BCLK.
Low: Data is strobed at the falling edge of BCLK.

bits 4, 3: BCKMD1, 0 (BCLK mode 1, 0)
These bits are set according to the number of clocks output for BCLK during 1/2 LCLK cycle by the CD digital signal processing LSI (CD DSP).

BCKMD1	BCKMD0	
"L"	"L"	16BCLKs/WCLK
"L"	"H"	24BCLKs/WCLK
"H"	"X"	32BCLKs/WCLK

bit 2: LSB1ST (LSB first)
High: Connected with the CD DSP which outputs data with LSB first.
Low: Connected with the CD DSP which outputs data with MSB first.

bit 1: RESERVED
Normally set low.
Any change to the bits in this register must be made in the decoder disable status. (After the IC is reset, the address is 28h.)

bit 0 BFSHDFSL (buffering subheader flag select)
High: The Sub Headers written two times are compared and, if they do not match, the result reports an error to bits 3 to 0 of BFHDRFLG.
Low: When the C2PO of the Sub Headers written two times are both high, that reports an error to the bits 3 to 0 of BFHDRFLG.

1-1-4. 03h

(1) RAWMD (raw mode) register (read)

RAWMD (raw mode) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
03h (R)									RAWMD

The Header Mode byte for the sector being sent from the CD DSP while DECINT is active can be read from this register.

(2) RFINTVL (refresh interval) register (write)

RFINTVL (refresh interval) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
03h (W)	b7	b6	b5	b4	b3	b2	b1	b0	RFINTVL

This register determines the refresh interval. The refresh interval is RFINTVL $\times$ 4 $\times$ TW. Here, TW represents the XTL1 clock frequency. Note that this IC performs RAS only refresh.

1-1-5. 04h

(1) BFMIN (buffer minute) register (read)

BFMIN (buffer minute) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
04h (R)									BFMIN

During the execution of a write-only or real-time error correction command and after execution of a repeat correction command, the Header Minute byte of the current sector can be read from this register. This register is invalid when the decoder is disabled or a monitor-only command is being executed.

(2) DSPCTL (DSP control) register (write)

DSPCTL (DSP control) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
04h (W)	DSTB SL1	DSTB SL0	DIS XLAT	XFR BYT1	XFR BYT0	"L"	SBAI TMSL	FAST EXCK	DSPCTL

bits 7, 6: DSTBSL1, 0

These bits determine the frequency of the DSTB and XLAT clocks used for passing data (DATO) to the CD DSP. The sub CPU sets these bits according to the frequency of the clock on the XTL1 pin. (The maximum frequency for DSTB is 1MHz.)

DSTBDL1	DSTBDL0	Frequency
0	0	1/24 of XTL1
0	1	1/32 of XTL1
1	0	1/48 of XTL1
1	1	1/64 of XTL1

bit 5: DISXLAT (disable XLAT output)

High: After the contents of the DSPCMD register are transferred to the DSP, a latch pulse is not output from the XLAT pin. In this case, the sub CPU uses DSPCMDLT (bit 0 of the CHPCTL0 register) to output a latch pulse from the XLAT pin at the appropriate time.

Low: After the contents of the DSPCMD register are transferred to the DSP, a latch pulse is output from the XLAT pin.

bits 4, 3: XFRBYT1, 0 (transfer command byte length 1,0)

These bits determine the number of bytes in the command data (DSPCMD register) to be transferred to the CD DSP. The relationship between the settings and the number of transferred bytes is shown in the following table.

XFRBYT1	XFRBYT0	Number of transferred bytes
"L"	"L"	Prohibited
"L"	"H"	1
"H"	"L"	2
"H"	"H"	3

bits 2: RESERVED

Normally set low.

bit 1 SBAITMSL (subcode buffering area increment timing select)
High: The internal subcode buffering area is incremented when the first pack of data is retrieved and de-interleaving is performed.
Low: The internal subcode buffering are is incremented when the subcode Sync mark is detected and inserted.

bit 0 FASTEXCK (fast EXCK)
High: The EXCK frequency is 1/8 the frequency of the XTL1 pin.
Low: The EXCK frequency depends on the settings of EXCKSEL (CONFIG0 bit 2)

1-1-6. 05h

(1) BFSEC (buffer second) register (read)

BFSEC (buffer second) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
05h (R)									BFSEC

During the execution of a write-only or real-time error correction command and after execution of a repeat correction command, the Header Second byte of the current sector can be read from this register. This register is invalid when the decoder is disabled or a monitor-only command is being executed.

(2) DSPCMD (DSP command) register (write)

DSPCMD (DSP command) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
05h (W)	b7	b6	b5	b4	b3	b2	b1	b0	DSPCMD

The data to be serially transferred to the CD DSP is written in this register. This register is a three-byte LIFO (last-in, first-out) register.

1-1-7. 06h

(1) BFHDRBLK (buffer header block) register (read)

BFHDRBLK (buffer block) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
06h (R)									BFHDRBLK

During the execution of a write-only or real-time error correction command and after execution of a repeat correction command, the Header Block byte of the current sector can be read from this register. This register is invalid when the decoder is disabled or a monitor-only command is being executed.

1-1-8. 07h

(1) BFMD (buffer mode) register (read)

BFMD (buffer mode) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
07h (R)									BFMD

During the execution of a write-only or real-time error correction command and after execution of a repeat correction command, the Header Mode byte of the current sector can be read from this register. This register is invalid when the decoder is disabled or a monitor-only command is being executed.

1-1-9. 08h

(1) BFFILE (buffer file) register (read)

BFFILE (buffer file) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
08h (R)									BFFILE

During the execution of a write-only or real-time error correction command and after execution of a repeat correction command, the Sub Header File byte of the current sector can be read from this register. This register is invalid when the decoder is disabled or a monitor-only command is being executed.

1-1-10. 09h

(1) BFCHAN (buffer channel) register (read)

BFCHAN (buffer channel) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
09h (R)									BFCHAN

During the execution of a write-only or real-time error correction command and after execution of a repeat correction command, the Sub Header Channel byte of the current sector can be read from this register. This register is invalid when the decoder is disabled or a monitor-only command is being executed.

1-1-11. 0Ah

(1) BFSUBM (buffer sub mode) register (read)

BFSUBM (buffer sub mode) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
0Ah (R)									BFSUBM

During the execution of a write-only or real-time error correction command and after execution of a repeat correction command, the Sub Header Sub Mode byte of the current sector can be read from this register. This register is invalid when the decoder is disabled or a monitor-only command is being executed.

1-1-12. 0Bh

(1) BFDTYP (buffer data type) register (read)

BFDTYP (buffer data type) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
0Bh (R)									BFDTYP

During the execution of a write-only or real-time error correction command and after execution of a repeat correction command, the Sub Header Data Type byte of the current sector can be read from this register. This register is invalid when the decoder is disabled or a monitor-only command is being executed.

1-1-13. 0Ch

(1) RAWHDRFLG (raw header flag) register (read)

RAWHDRFLG (raw header flag) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
0Ch (R)	MIN	SEC	BLOCK	MODE				CDRDTEN	RAWHDR

This register indicates the C2PO value for the RAWHDR register.

bit 7 Minute
bit 6 Second
bit 5 Block
bit 4 Mode
bit 3 to 1 RESERVED
bit 0 CD-R Mode Detect Enable

(2) CDRMOD (CD-R mode) register (write)

CDRMOD (CD-R mode) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
0Ch (W)								CDRDTEN	CDRMODE

bit 0 CDRDTEN (CD-R mode detect enable)

High: The CDRINT status results when the decoder is operating in the monitor-only, write-only, real-time correction or asynchronous correction mode if either of the conditions below is met.

(1) Bits 7 to 5 of the Raw Mode byte are not "000".

(2) The error flag of the Raw Mode byte is not established. (Values after processing by setting of MDBYTCTL (DECCTL0 bit 2))

Low: The CD-R Mode byte is not detected.

1-1-14. 0Dh

(1) BFHDRFLG (buffer header flag) register (read)

BFHDRFLG (buffer header flag) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
0Dh (R)	MIN	SEC	BLOCK	MODE	FILE	CHAN	SUBMODE	DATATYPE	HDRFLG

This register shows the error status of each byte in the BFHDR and BFSHDR registers. High means an error.

bit7 Minute
bit6 Second
bit5 Block
bit4 Mode
bit3 File
bit2 Channel
bit1 Submode
bit0 Data Type

1-1-15. 0Eh

(1) DECSTS0 (decoder status 0) register (read)

DECSTS0 (decoder status 0) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
0Eh (R)									DECSTS0

bit 7: SHRTSCT (short sector)
Indicates that the Sync mark interval was less than 2351 bytes since the previous DECINT. This sector does not remain in the buffer memory.

bit 6: NOSYNC
Indicates that the Sync mark was inserted because one was not detected in the prescribed position for the current sector.

bit 5: CORINH (correction inhibit)
This is high if the current sector Mode and Form could not be determined when the AUTODIST bit of the DECCTL register is set high. ECC or EDC is not executed in this sector. The CORINH bit is invalid when AUTODIST is set low. It is high in any of the conditions below when the AUTODIST bit is set high.
(1) When an error was found in the Mode byte.
(2) When the Mode byte is a value other than 01h or 02h.
(3) When the Mode byte is 02h and the C2 pointer is high in the Submode byte.

bit 4: ERINBLK (erasure in block)
When the decoder is operating in the monitor-only, write-only or real-time mode which prohibits erasure correction, this indicates that at least a 1-byte error flag (C2PO) has been raised in the data excluding the Sync mark from the current sector CD DSP.

bit 3: CORDONE (correction done)
Indicates that there is an error corrected byte in the current sector.

bit 2: EDCNG
Indicates that an error was found in the current sector through an EDC check.

bit 1: ECCNG
Indicates that an uncorrectable error was found somewhere between the Header byte and the Parity byte in the current sector. (Bit 1 = don't care in the Mode2, Form2 sectors.)

bit 0: TGTNTMET (target not met)
Indicates that the current sector address and the target address in the TGTMNT, TGTSEC, and TGTBLK registers do not match. The error pointer is not referenced in this instance.

1-1-16. 0Fh

(1) DECSTS1 (decoder status 1) register (read)

DECSTS1 (decoder status 1) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
0Fh (R)									DECSTS1

bits 7 to 3: RESERVED

bit 2: EDCALL0 (EDC all 0)

This is high when there are no error flags in all the 4 EDC parity bytes of the current sector and their values are all 00h.

bit 1: CMODE (correction mode)

bit 0: CFORM (correction form)

These bits indicate the Mode and Form of the current sector the decoder has discriminated to correct errors when the decoder is operating in the real-time correction or repeat correction mode.

CFORM	CMODE	
"X"	"L"	MODE1
"L"	"H"	MODE2, FORM1
"H"	"H"	MODE2, FORM2

1-1-17. 10h, 11h

(1) LSTARA-H, L (last area-high, low) register (read/write)

LSTARA-H, L (last area-high, low) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
10h (R/W)								b8	LSTARA-H
11h (R/W)	b7	b6	b5	b4	b3	b2	b1	b0	LSTARA-L

This register specifies the last order area. Set bits 7 to 1 of the LSTARA-H register low when writing in this register.

1-1-18. 12h, 13h

(1) LHADR-H, L (last HADR-high, low) register (read/write)

LHADR-H, L (last HADR-high, low) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
12h (R/W)								b8	LHADR-H
13h (R/W)	b7	b6	b5	b4	b3	b2	b1	b0	LHADR-L

When host automatic transfer mode is disabled, this register specifies the upper limit for HADRC (the upper 9 bits); for the subcode buffering command, this register specifies the upper limit for the address (upper 9 bits). The lower 11 bits are 7FFh. Set bits 7 to 1 of the LHADR-H register low when writing in this register.

1-1-19. 14h

(1) XFRFMT0 (transfer format 0) register (read/write)

XFRFMT0 (transfer format 0) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
14h (R/W)	1024 XFR	512 XFR	SYNC	HEAD ER	SBHE ADER	USER DATA	PARI TY	AUTO XFR	XFRFMT0

The transfer format for automatic data transfer is determined by this register. Before starting to transfer each sector, this IC reads the value of the SCTINF register written in the buffer memory. The buffer memory data is transferred to the host according to the read values and those in the XFRFMT1 and 0 registers. The Mode/Form of bits 3 to 1 depends on the values of bits 2 and 1 in the SCTINF register.

Regarding Mode2 in the Yellow Book, don't care the Form2 (bit 2) of the SCTINF register. Set bits 3 to 1 of the XFRFMT0 register high to transfer 2336 bytes of user data.

bit 7: 1024XFR

When this bit is set high, the user data (2048 bytes) is divided into 1024-byte blocks for transmission. In this case, set bits 6 to 1 in the XFRFMT0 register and bits 7 to 0 in the XFRFMT1 register low. In other words, the Sync mark, Header, Sub Header, and Parity bytes, as well as the block error flag, byte error flag, and subcode cannot be sent to the host. This transfer mode is not supported for Mode2/Form2 sectors.

bit 6: 512XFR (512 bytes transfer mode)

When this bit is set high, the user data (2048 bytes) is divided into 512-byte blocks for transmission. In this case, set bit 7 and bits 5 to 1 in the XFRFMT0 register and bits 7 to 0 in the XFRFMT1 register low. In other words, the Sync mark, Header, Sub Header, and Parity bytes, as well as the block error flag, byte error flag, and subcode cannot be sent to the host. This transfer mode is not supported for Mode2/Form2 sectors.

bit 5: SYNC

High: Sync marks are transferred to the host.

Low: Sync marks are not transferred to the host.

bit 4: HEADER

High: The four Header bytes are transferred to the host.

Low: The four Header bytes are not transferred to the host.

bit 3: SBHEADER

High: Mode1: This bit has no meaning.

Mode2: The eight Sub Header bytes are transferred to the host.

Low: The bytes indicated above are not transferred to the host.

bit 2: USERDATA (user data)

High: Mode1 and Mode2/Form1: User data (2048 bytes) is transferred to the host.

Mode2/Form2: User data (2324 bytes) is transferred to the host.

Low: The bytes indicated above are not transferred to the host.

bit 1: PARITY

High: Mode1: The EDC, ECC parity bytes and the eight 00h bytes, for a total of 288 bytes, are transferred to the host.

Mode2/Form1: The 280 EDC and ECC parity bytes are transferred to the host.

Mode2/Form2: The four reserved bytes (at the end of the sector) are transferred to the host.

Low: The bytes indicated above are not transferred to the host.

bit 0: AUTOXFR

Set this bit high when operating in automatic transfer mode. Set this bit low when operating in manual transfer mode. For CD-DA data, set 3Fh in this register when operating in automatic transfer mode.

1-1-20. 15h

(1) XFRFMT1 (transfer format 1) register (read/write)

XFRFMT1 (transfer format 1) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
15h (R/W)	ENBL KEFL	BLKE FLSL	ENBY TFBT	BYTE FLSL	ENSB CBT	ALL SBC	SBCE STS	ZA SQEF	XFRFMT1

bit 7: ENBLKEFL (enable block error flag)

High: The block error flag (1 byte) is transferred to the host.

Low: The byte indicated above is not transferred to the host.

bit 6: BLKEFLSL (block error flag select)

This bit is valid only when ENBLKEFL is high.

High: The value (one byte) written in the BLKESTS register by the sub CPU is transferred to the host as the block error flag.

Low: The OR value of each bit in the byte error flag is transferred to the host as the block error flag.

bit 5: ENBYTFBT (enable byte error flag buffering & transfer)

If this bit is set high, the operations described below are performed. If this bit is set low, the operations described below are not performed.

(1) The byte error flag is buffered during execution of a write-only, real-time error correction, and CD-DA command.

(2) When host automatic transfer mode is enabled (the AUTOXFR bit (bit 0) of the XFRFMT0 register is high), the byte error flag is transferred to the host.

The ENBYTFBT and BYTEFLSL bits are valid only when the USERDATA bit (bit 2) of the XFRFMT0 register is high.

bit 4: BYTEFLSL (byte error flag select)

This bit is valid only when ENBYTFBT is high. When this bit is set high, the value of BYTERSTS (the byte error status register, described later) is written in the byte error flag area of the buffer memory. Setting the BLKEFLSL bit low and the BYTEFLSL bit high at the same time is prohibited.

If this bit is set low, the value of C2PO from the CD DSP is written in the byte error flag area.

bit 3: ENSBCBT (enable subcode buffering & transfer)

If this bit is set high, the operations described below are performed. If this bit is set low, the operations described below are not performed.

(1) All subcodes or subcode-Q is buffered while the decoder executes CD-DA commands.

(2) When host automatic transfer mode is enabled (the AUTOXFR bit (bit 0) of the XFRFMT0 register is high), all subcodes or subcode-Q is transferred to the host.

Note that buffering the CD-ROM data and the subcodes or subcode-Q at the same time is not supported.

bit 2: ALLSBC (all subcode/subcode-Q)

This determines whether to buffer and transfer all subcodes or subcode-Q to the host when ENSBCBT is high.

High: All subcodes

Low: Subcode-Q

bit 1: SBCESTS (subcode error status)

This bit is valid only when ENSBCBT is high.

High: The value (one byte) written in the SBCESTS register by the sub CPU is transferred to the host.

Low: The byte indicated above is not transferred to the host.

bit 0: ZASQEF (zero after subcode-Q error flag)

This bit is valid only when ENSBCBT and SBCESTS are both high. (This bit is valid only when subcode-Q and the subcode error flag are transferred to the host.)

High: Five 00h bytes in addition to the subcode-Q error flag are transferred to the host.

Low: Five 00h bytes are not added to the subcode-Q error flag.

1-1-21. 16h

(1) DECCTL0 (decoder control 0) register (read/write)

DECCTL0 (decoder control 0) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
16h (R/W)	AUTO DIST	MODE SEL	FORM SEL		ENFM 2EDC	MDBY TCTL	EN DLA	ATDL RNEW	DECCTL0

bit 7: AUTODIST (auto distinction)

High: Errors are corrected according to the Mode byte and the Form bit read from the drive.

Low: Errors are corrected according to the MODESEL and FORMSEL bits (bits 6 and 5).

bit 6: MODESEL (mode select)

bit 5: FORMSEL (form select)

When AUTODIST is low, the sector is corrected in the Mode or Form indicated in the table below.

MODESEL	FORMSEL	
"L"	"L"	MODE1
"H"	"L"	MODE2, FORM1
"H"	"H"	MODE2, FORM2

bit 4: RESERVED

Always set low.

bit 3: ENFM2EDC (enable Form2 EDC check)

High: EDC check for Form2 is enabled.Low: EDC check for Form2 is disabled. The EDCNG bit of the DECSTS0 register goes low.

bit 2: MDBYTCTL (mode byte control)

High: Even if there are data other than "0" in the upper six bits of the Mode byte in the Header, an error does not result. Set this bit high when playing back discs such as CD-ROM.

Low: If the upper six bits of the Mode byte in the Header are not "000000", an error results.

bit 1: ENDLA (enable drive last area (address))

High: DLAR (Drive Last Area) is enabled. While the decoder is executing a write-only command, real-time error correction command, or CD-DA command, if buffering of the buffer memory area specified by DLAR is completed, the DRVOVRN (drive overrun) status results. Buffer-write of subsequent sectors is then interrupted.

Also, while the decoder is executing a subcode buffering command, if data is written in the buffer memory address specified by SLADR, the DRVOVRN (Drive Overrun) status results. Buffer-write of subsequent sectors is then interrupted.

Low: DLAR (Drive Last Area) and SLADR are disabled when this is set low.

bit 0: ATDLRNEW (auto DLARA renewal)

High: When the data transfer to the host is completed for one sector, DLARA is renewed in the written area of the sector.

Low: DLARA is renewed by the sub CPU.

1-1-22. 17h

(1) DECCTL1 (decoder control 1) register (read/write)

DECCTL1 (decoder control 1) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
17h (R/W)	ENSB QRD		DEC CMD2	DEC CMD1	DEC CMD0	NTCR CT2	NTCR CT1	NTCR CT0	DECCTL1

bit 7: ENSBQRD (enable subcode-Q read)

The subcode is fetched from the DSP and the subcode-Q CRC check is performed. The sub CPU can read the subcode-Q from the SUBQ register. Subcode decoding (de-interleave, error correction) is performed.

bit 6: RESERVED

Normally set low.

bits 5 to 3: DECCMD2 to 0 (decoder commands 2 to 0)

DECCMD2	DECCMD1	DECCMD0	Decoder command
"L"	"L"	"L"	DECODER Disable
"L"	"L"	"H"	Monitor-only
"L"	"H"	"L"	Write-only
"L"	"H"	"H"	Real-time correction
"H"	"L"	"L"	Asynchronous correction
"H"	"L"	"H"	Subcode buffering
"H"	"H"	"H"	CD-DA

bits 2 to 0: NTCRCT2 to 0 (number of times of correction)

This determines the number of times where error correction is performed when operating in asynchronous correction mode. (1 to 4 times)

1-1-23. 18h

(1) XFRSTS (data transfer status) register (read)

XFRSTS (data transfer status) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
18h (R)	REV#2	REV#1	REV#0		CMDOBUSY		CBFWRRDY	CBFRDRDY	XFRSTS

bits 7 to 5: REV#2 to 0 (revision number bits 2 to 0)
"000" is read out. This can be used to recognize the version.

bit 4: CMDOBUSY (command output busy)
This bit goes high if DSPCMDXFR is set. Once the transfer of contents of the DSPCMD register to the CD DSP is completed, this bit goes low.

bit 1: CBFWRRDY (CPU buffer write ready)
The sub CPU can write in the CPUBWDT register when this bit is high.

bit 0: CBFRDRDY (sub CPU buffer read ready)
The sub CPU can read the CPUBRDT register when this bit is high.

(2) CHPCTL0 (chip control 0) register (write)

CHPCTL0 (chip control 0) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
18h (W)	CHIPRST	TGTMET	INCTGT	RPCORTRG	"L"	CLDSPCMD	DSPCMDXF	DSPCMDLT	CHPCTL0

bit 7: CHIPRST (chip reset)
This IC is reset when this bit is set high.

bit 6: TGTMET (target met)

(1) During execution of a write-only or real-time error correction command, if the target sector is found, the sub CPU sets TGTMET high.
(2) TGTMET is sampled for 3/4 sectors (depends on the playback speed) after the decoder interrupt. Accordingly, if the target sector is found, the sub CPU must set TGTMET high within this interval after DECINT.
(3) Once TGTMET is set high, it remains high internally until the decoder is disabled.
(4) If TGTMET is sampled and found to be low during execution of a write-only or real-time error correction command:
• The main data and subcode buffering areas are not renewed.
• Main data error correction is not performed.

bit 5: INCTGT (increment target register)
If this bit is set high, the target registers (TGTMIN, TGTSEC, and TGTBLK) are incremented. The target registers use BCD code.
TGTMIN, TGTSEC, and TGTBLK are connected in cascading fashion and are incremented as shown below.

(1) The TGTBLK register is always incremented by this bit. When the TGTBLK register is incremented after reaching "74", it returns to "0".
(2) The TGTSEC register is incremented when the TGTBLK register is "74" and this bit goes high. When the TGTSEC register is incremented after reaching "59", it returns to "0".
(3) The TGTMIN register is incremented when the TGTBLK register is "74", the TGTSEC register is "59", and this bit goes high. When the TGTMIN register is incremented after reaching "99", it returns to "0".

bit 4: RPCORTRG (repeat correction trigger)
If this bit is set high while the decoder is disabled, the CD-ROM sector error correction begins. The sector that is corrected is specified by the BFARA# register.
bit 3: RESERVED
Always set low.
bit 2: CLDSPCMD (clear DSP data register)
Setting this bit high clears the DSPCMD register.
bit 1: DSPCMDXF (DSP command transfer)
Setting this bit high starts serial transfer of the contents of the DSPCMD register to the CD DSP.
bit 0: DSPCMDLT (DSP command latch)
Setting this bit high outputs a pulse from the XLAT pin.

1-1-24. 19h

(1) CPUBRDT (CPU buffer read data) register (read)

CPUBRDT (CPU buffer read data) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
19h (R)									CPUBRDT

The sub CPU reads the Data In the buffer memory through this register.

(2) CPUBWDT (CPU buffer write data) register (write)

CPUBWDT (CPU buffer write data) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
19h (W)	b7	b6	b5	b4	b3	b2	b1	b0	CPUBWDT

The sub CPU writes the data to be written in the buffer memory in this register.

1-1-25. 1Ah

(1) SCTINF (sector information) register (read/write)

SCTINF (sector information) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
1Ah (R/W)	SUBQ FMSL					MODE2	FORM2	XFR SCT	SCTINF

While DECINT is active, the current sector information is written in this register. When making transfers to the host automatically, be sure to set the information in this register each time DECINT is active. The value in this register is written in the last address in the buffer memory area.

bit 7: SUBQFMSL (subcode-Q format select)
High: When ENSBCBT is high and ALLSBC is low, the decoder does not write the subcode error flag or 00h after subcode-Q in the buffer. When transferring the subcode error flag and 00h after subcode-Q address data to the host, the sub CPU must write Data In the above address before setting the SCTINF register.
Set this bit high only when ENSBCBT is high and ALLSBC is low is prohibited.
Low: When ENSBCBT is high and ALLSBC is low, the decoder writes the subcode error flag and 00h after subcode-Q in the buffer.

bits 6 to 3: RESERVED
Always set low.

bit 2: Mode2
High: This sector is a Mode2 sector.
Low: This sector is a Mode1 or CD-DA sector.

bit 1: Form2
This bit is valid only when the Mode2 bit is high.
High: This sector is a Form2 sector.
Low: This sector is a Form1 sector.
This bit can either be high or low in the Mode2 for the Yellow Book.

MODE2	FORM2	
"L"	"L"	MODE1
"L"	"H"	RESERVED
"H"	"L"	MODE2/FORM1
"H"	"H"	MODE2/FORM2

bit 0: XFRSCT (transfer sector)
High: The Data In this sector is transferred to the host.
Low: The Data In this sector is not transferred to the host. In this case, bits 2 and 1 have no meaning.

1-1-26. 1Bh

(1) SBCSTS (subcode status) register (read)

SBCSTS (subcode status) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
1Bh (R)									SBCSTS

During execution of a CD-DA command or a subcode buffering command, this register indicates the error status of the subcode written to the buffer. The Data In this register is valid from DECINT to DECINT.

bit 7: SBCOVRN (subcode overrun)
If the ENSBCBT bit (bit 5) of the XFRFMT1 register is set high, if subcode buffering to the area specified by DLARA is completed while the decoder is executing a CD-DA command or a subcode buffering command, the SBCOVRN status results. There are no stipulations regarding the time relationship between the subcode and CD-ROM data Sync marks. Accordingly, a time difference exists between the occurrence of DRVOVRN and SBCOVRN.

bit 6: OVERFLOW
Indicates that the SBCSTS FIFO has overflowed due to multiple subcode short sync. When overflow occurs, subcode buffering is stopped. Subcodes are not buffered in subsequent sectors obtained by decoder interrupt.

bit 5: BFNTVAL (buffer not valid)
Indicates that valid data is not written in the buffer due to a short subcode sector.

bit 4: NOSYNC
Indicates that the Sync mark was inserted because a subcode Sync mark was not detected in the prescribed position.

bits 3 to 1: SBCERR3 to 1 (subcode pack error 3 to 1)
Indicates that an uncorrectable error was found in that pack as the result of subcode error correction. These bits are valid only when the ALLSBC bit (bit 4) of the XFRFMT1 register is high.

bit 0: SBCERR0 (subcode pack error 0)/SUBQERR0 (subcode-Q error 0)
When ALLSBC is high, this bit is the PACK0 error status.
When ALLSBC is low, an error was detected in the subcode-Q as the result of the CRC check.

(2) BLKESTS (block error status) register (write)

BLKESTS (block error status) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
1Bh (W)	b7	b6	b5	b4	b3	b2	b1	b0	BLKESTS

The data to be transferred to the host as the block error status byte is written in this register. Set this register before writing the SCTINF register.

1-1-27. 1Ch

(1) SBQSTS (subcode-Q status) register (read)

SBQSTS (subcode-Q status) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
1Ch (R)									SBQSTS

This register indicates the error status of the subcode-Q fetched from the CD DSP. Except for bit 7, the Data In this register is valid from SBCSYNC to SBCSYNC.

bit 7: SBQERR (subcode-Q error)
This bit is the status which is normally to be written in the SBCSTS register. This bit is valid for the same period as the SBCSTS register. This bit indicates that an error was detected in the subcode-Q as a result of the CRC check. The sub CPU should read this bit before reading the SBCSTS register. When ALLSBC is high, bit 0 of SBCESTS becomes SBCERR0. Therefore, the subcode-Q error information is obtained from this bit. When ALLSBC is low, SUBQERR0 and SBQERR are the same. Accordingly, there is no need to read this bit.

bits 6 to 3: RESERVED

bit 2: SHTSBCS (short subcode sector)
Indicates that the subcode Sync mark interval since the previous SBCSYNC interrupt was less than 98 WFCK.

bit 1: NOSYNC (no subcode Sync)
Indicates that since a subcode Sync mark could not be detected at the prescribed position, a Sync mark was inserted.

bit 0: SUBQERR (subcode-Q error)
An error was detected in the subcode-Q as a result of the CRC check.

(2) SBCESTS (subcode error status) register (write)

SBCESTS (subcode error status) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
1Ch (W)	b7	b6	b5	b4	b3	b2	b1	b0	SBCESTS

The data to be transferred to the host as the subcode error status byte is written in this register. Set this register before writing in the SCTINF register.

1-1-28. 1Dh

(1) INCBLKS (increment blocks) register (read/write)

INCBLKS (increment blocks) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
1Dh (R/W)						INCB LKS2	INCB LKS1	INCB LKS0	INCBLKS

bits 7 to 3: RESERVED
Always set low.

bits 2 to 0: INCBLKS2 to 0
This register specifies the increment value (+1 to 4) of the BFBLKC (buffer block count) register. Setting "0" or a value of "5" or greater is prohibited. After a reset, the increment value is set to "1".

1-1-29. 1Eh

(1) SBQDT (subcode-Q data) register (read)

SBQDT (subcode-Q data) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
1Eh (R)									SBQDT

The subcode-Q value can be read by reading this register ten times. The subcode-Q that is read is the data immediately prior to the SBCSYNC interrupt.

(2) BYTERSTS (byte error status) register (write)

BYTERSTS (byte error status) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
1Eh (W)	b7	b6	b5	b4	b3	b2	b1	b0	BYTERSTS

When ENBYTFBT and ENBYTEFG in the XFRFMT1 register are both high, the data to be transferred to the host as the byte error status byte is written in this register. Set this register before writing in the SCTINF register.

1-1-30. 1Fh

(1) CHPCTL1 (chip control 1) register (read/write)

CHPCTL1 (chip control 1) register

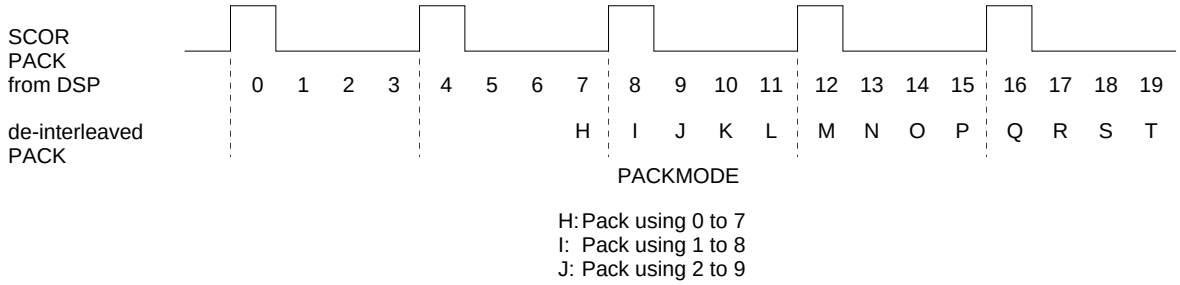
Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
15h (R/W)						PACK MODE			CHPCTL1

bits 7 to 3, 1, 0: RESERVED
Always set low.

bit 2: PACKMODE (pack mode)

High: The four packs of data starting from the five packs before the subcode sync signal are written in the buffer as one group of data. In the illustration below, H to K are treated as one group.

Low: The four packs of data before the subcode sync signal are written in the buffer as one group of data. In the illustration below, I to L are treated as one group.



1-1-31. 20h, 21h

(1) BFARA#-H, L (buffering area number-high, low) (read/write)

BFARA#-H, L (buffering area number-high, low)

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
20h (R/W)								b8	BFARA#-H
21h (R/W)	b7	b6	b5	b4	b3	b2	b1	b0	BFARA#-L

The area is read where the data from the CD DSP is buffered.

This register indicates the buffering area when executing a write-only, real-time error correction, or CD-DA command. Before executing one of these commands, the sub CPU specifies the area where buffering is to start initially. When the buffering of a sector is completed, this register is incremented.

When executing a subcode buffering command, buffering starts from address 0.

1-1-32. 22h, 23h

(1) CSCTARA-H, L (current sector area-high, low) register (read)

CSCTARA-H, L (current sector area-high, low) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
22h (R)								b8	CSCTARA-H
23h (R)	b7	b6	b5	b4	b3	b2	b1	b0	CSCTARA-L

This register indicates the area number where the current sector is being written.

1-1-33. 24h, 25h

(1) DLARA-H, L (drive last area-high, low) register (read/write)

DLARA-H, L (drive last area-high, low) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
24h (R/W)								b8	DLARA-H
25h (R/W)	b7	b6	b5	b4	b3	b2	b1	b0	DLARA-L

This register specifies the last buffering area while the decoder is executing a write-only, real-time error correction, or CD-DA command. If the ENDLA bit (bit 1) of the DECCTL0 register is set high and the data from the drive (CD DSP) is written in the area specified by DLARA while the decoder is executing one of the above commands, subsequent buffering is prohibited.

1-1-34. 27h

(1) TGTMIN (target minute) register (read/write)

TGTMIN (target minute) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
27h (R/W)	b7	b6	b5	b4	b3	b2	b1	b0	TGTMNT

0 to 99 (BCD)

1-1-35. 28h

(1) TGTSEC (target second) register (read/write)

TGTSEC (target second) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
28h (R/W)	b7	b6	b5	b4	b3	b2	b1	b0	TGTSEC

0 to 59 (BCD)

1-1-36. 29h

(1) TGTBLK (target block) register (read/write)

TGTBLK (target block) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
29h (R/W)	b7	b6	b5	b4	b3	b2	b1	b0	TGTBLK

0 to 74 (BCD)

Set the target sector address in these three registers when executing a monitor-only, write-only, or real-time error correction command. This address is compared with the current sector address, and if they do not match, TGTNTMT (target not met) status (bit 0 of the DECSTS0 register) is established.

1-1-37. 2B to 2Dh

(1) XFRCNT-H, M, L (transfer block counter-high, middle, low) register (read/write)

XFRCNT-H, M, L (transfer block counter-high, middle, low) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
2Bh (R/W)	b23	b22	b21	b20	b19	b18	b17	b16	XFRCNT-H
2Ch (R/W)	b15	b14	b13	b12	b11	b10	b9	b8	XFRCNT-M
2Dh (R/W)	b7	b6	b5	b4	b3	b2	b1	b0	XFRCNT-L

This is a 24-bit register that shows the number of blocks remaining to be transferred. Before the start of the transfer the sub CPU sets the total number of blocks to be transferred in this register.
This register is decremented as the transfer of each block is completed.

1-1-38. 2Eh, 2Fh

(1) XFRARA-L, H (transfer area-low, high) register (read/write)

XFRARA-L, H (transfer area-low, high) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
2Eh (R/W)								b8	XFRARA-H
2Fh (R/W)	b7	b6	b5	b4	b3	b2	b1	b0	XFRARA-L

During an automatic transfer, this register specifies the initial area from which the transfer is to start. This register is incremented after a block is transferred. Note that bits 7 to 1 of the XFRCNT-H register should normally be set low.

1-1-39. 31h

(1) XFRPOS (first transfer position) register (read/write)

XFRPOS (transfer position) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
31h (R/W)							XFR POS1	XFR POS0	XFRPOS

bits 7 to 2: RESERVED
Always set low.

bits 1, 0: XFRPOS1, 0
These bits specify the initial block position from which transfer is to start when in 512- or 1024-byte transfer mode (automatic transfer mode). In 1024-byte transfer mode, XFRPOS1 is invalid. This register is incremented after a block is transferred. This register is invalid in manual transfer mode and automatic transfer modes other than 512- and 1024-byte mode.
The sub CPU can read the values of XFRARA, XFRPOS, BFBLKC and XFRCNT at any time. However, because the reads by the sub CPU are not synchronized with the variation of BFBLKC, note that there is a possibility of an error of ±1 between the value that is read and the actual value.

1-1-40. 33h to 35h

(1) HXFRC-H, M, L (host transfer byte counter-high, middle, low) register (read/write)

HXFRC-H, M, L (host transfer byte counter-high, middle, low) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
33h (R/W)					b19	b18	b17	b16	HXFRC-H
34h (R/W)	b15	b14	b13	b12	b11	b10	b9	b8	HXFRC-M
35h (R/W)	b7	b6	b5	b4	b3	b2	b1	b0	HXFRC-L

In manual transfer mode, these registers set the number of bytes to be transferred. (20 bits) The number of bytes remaining to be transferred can also be read from this register. Note that bits 7 to 4 of HXFRC-H should normally be set low.

Note) Send Data (A1h), Send Status (A5h) and Send Message (A7h), which were passed via the buffer, should not be executed if HADRC-H, M, L are odd addresses and HXFRC-H, M, L are 3 bytes for setting conditions.

1-1-41. 37h to 39h

(1) HADRC-H, M, L (host address counter-high, middle, low) register (read/write)

HADRC-H, M, L (host address counter-high, middle, low) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
37h (R/W)					b19	b18	b17	b16	HADRC-H
38h (R/W)	b15	b14	b13	b12	b11	b10	b9	b8	HADRC-M
39h (R/W)	b7	b6	b5	b4	b3	b2	b1	b0	HADRC-L

In manual transfer mode, these registers set the head address from which the transfer begins. Note that bits 7 to 4 of HADRC-H should normally be set low.

Note) Send Data (A1h), Send Status (A5h) and Send Message (A7h), which were passed via the buffer, should not be executed if HADRC-H, M, L are odd addresses and HXFRC-H, M, L are 3 bytes for setting conditions.

1-1-42. 3Bh to 3Dh

(1) SLADR-H, M, L (subcode last address-high, middle, low) register (read/write)

SLADR-H, M, L (subcode last address-high, middle, low) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
3Bh (R/W)					b19	b18	b17	b16	SLADR-H
3Ch (R/W)	b15	b14	b13	b12	b11	b10	b9	b8	SLADR-M
3Dh (R/W)	b7	b6	b5	b4	b3	b2	b1	b0	SLADR-L

These registers specify the last buffering address for subcode buffering commands. If the ENDLA bit (bit 1) of the DECCTL0 register is set high and the data is written in the buffer address specified by SLADR while the decoder is executing a subcode buffering command, subsequent buffering is prohibited. Be sure to set these registers in the order of H $\rightarrow$ M $\rightarrow$ L. Note that bits 7 to 4 of SLADR-H should normally be set low.

1-1-43. 3Fh to 41h

(1) CWADRC-H, M, L (CPU write address counter-high, middle, low) register (read/write)

CWADRC-H, M, L (CPU write address counter-high, middle, low) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
3Fh (R/W)					b19	b18	b17	b16	CWADRC-H
40h (R/W)	b15	b14	b13	b12	b11	b10	b9	b8	CWADRC-M
41h (R/W)	b7	b6	b5	b4	b3	b2	b1	b0	CWADRC-L

The sub CPU sets this address when writing Data In the buffer memory. The register is incremented when data is written in the buffer memory. The sub CPU should set these registers in the order of CWADRC-H, M, L. Note that bits 7 to 4 of CWADRC-H should normally be set low.

1-1-44. 43h to 45h

(1) CRADRC-H, M, L (CPU read address counter-high, middle, low) register (read/write)

CRADRC-H, M, L (CPU read address counter-high, middle, low) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
43h (R/W)					b19	b18	b17	b16	CRADRC-H
44h (R/W)	b15	b14	b13	b12	b11	b10	b9	b8	CRADRC-M
45h (R/W)	b7	b6	b5	b4	b3	b2	b1	b0	CRADRC-L

The sub CPU sets this address when reading data from the buffer memory. The register is incremented when data is read from the buffer memory. The sub CPU should set these registers in the order of CRADRC-H, M, L. Note that bits 7 to 4 of CRADRC-H should normally be set low.

1-1-45. 46h, 47h

(1) BFBLKC-H, L (buffer block count-high, low) register (read/write)

BFBLKC-H, L (buffer block count-high, low) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
46h (R/W)						b10	b9	b8	BFBLKC-H
47h (R/W)	b7	b6	b5	b4	b3	b2	b1	b0	BFBLKC-L

This register is a 10-bit counter that indicates the number of blocks in the buffer that can be transferred. Before activating the decoder, the sub CPU sets the number of blocks that can be transferred.

Once the number of transferable blocks is reached (once the buffer is written with XFRSCT (bit 0) of the SCTINF register high), the value of BFBLKC is incremented (+1 to 4). The increment value is specified by the INCBLKS register.

When the transfer of one block is completed, this register is decremented (–1).

Note that bits 7 to 3 of BFBLKC-H should normally be set low.

1-1-46. 48h, 49h

(1) BFFLRT-H, L (buffer full ratio-high, low) register (read/write)

BFFLRT-H, L (buffer full ratio-high, low) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
48h (R/W)						b10	b9	b8	BFFLRT-H
49h (R/W)	b7	b6	b5	b4	b3	b2	b1	b0	BFFLRT-L

These registers indicate the buffer full ratio.

Note that bits 7 to 3 of BFFLRT-H should normally be set low.

1-1-47. 4Ah, 4Bh

(1) TIMER-H, L (timer-high, low) register (read/write)

TIMER-H, L (timer-high, low) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
4Ah (R/W)	b15	b14	b13	b12	b11	b10	b9	b8	TIMER-H
4Bh (R/W)	b7	b6	b5	b4	b3	b2	b1	b0	TIMER-L

These are the timer settings. The sub CPU should set these registers in the order of TIMER-H, L. After a value is set in TIMER-L, a timer interrupt occurs when the time specified by (TIMER-H, L) ∗TIMRRSL passes.

1-1-48. 4Ch

(1) TMRRSL (timer resolution) register (read/write)

TMRRSL (timer resolution) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
4Ch (R/W)	b7	b6	b5	b4	b3	b2	b1	b0	TMRRSL

This register determines the timer resolution. Assuming the XTL1 clock cycle to be Tw, the timer resolution is TIMRRSL $\times$ 16 $\times$ Tw.

[Example] Setting a resolution of 100µs

(1) XTL1 = 40MHz (Tw = 25ns)
100 $\times$ 1000 / (16 $\times$ 25) = 250 (FAh)
Set FAh in this register. The resolution becomes 100µs.

(2) XTL1 = 33.8688 MHz (Tw = 29.5ns)
100 $\times$ 1000 / (16 $\times$ 29.5) = 211.68
Set D3 or D4h in this register. The resolution becomes 96.7µs or 100.2µs, respectively.

1-1-49. 4Eh, 4Fh

(1) STARTARA-H, L (start area-high, low) register (read)

STARTARA-H, L (start area-high, low) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
4Eh (R)								b8	STARTARA-H
4Fh (R)	b7	b6	b5	b4	b3	b2	b1	b0	STARTARA-L

These registers indicate the area from which transfer starts when executing stream processing.

1-2. Description of SCSI2 Controller Block Registers

1-2-1. 50h

(1) SCSTS (SCSI module status) register (read)

SCSTS (SCSI module status) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
50h (R)	MON RST	MON DBP			TRAG MODE	TBC ZERO		CMDI NPRG	SCSTS
	*	*			0	1		0	Initial value

This register monitors the various states of the CXD1804AR/SCSI2 controller block.

bit 7: MONRST (monitor RST)
Monitors the SCSI bus XRST signal (positive logic).

bit 6: MONDBP (monitor DBP)
Monitors the SCSI bus XDBP signal (positive logic).

bit 3: TARGMODE (target mode indicator)
This bit goes high when the CXD1804AR/SCSI2 controller block is in the target status.

bit 2: TBCZERO (transfer byte counter zero)
This bit goes high while the value of the transfer byte counter (set by the SCSXFRC register) used to transfer data between the sub CPU and the SCSI is "000".
Note) Even if this value is high, FIFO is not necessarily empty.

bit 0: CMDINPRG (SCSI module command in progress)
This bit goes high while the CXD1804AR/SCSI2 controller block is executing the command written in the SCCMD register (50h).

(2) SCCMD (SCSI module command) command register (write)

SCCMD (SCSI module command) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
50h (W)	CAT1	CAT0	B05	B04	B03	B02	B01	B00	SCCMD

Commands to the CXD1804AR/SCSI2 controller block are written in this register.

bits 7 and 6: CAT1 and 0 (SCSI module command category code 1, 0)

CAT1	CAT0	Mode
0	0	Commands valid in all states
0	1	Commands valid in the Disconnect status
1	0	Commands valid in the target status
1	1	Stream-related commands

bits 5 to 0: B05 to B00 (SCSI module command code B05 to B00)
See the chapter on commands for the details of each command.

1-2-2. 51h

(1) Reserved (read/write)

Reserved

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
51h (R)									Reserved
									Initial value
51h (W)									Reserved

Currently not used.

1-2-3. 52h

(1) Reserved (read/write)

Reserved

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
52h (R)									Reserved
									Initial value
52h (W)									Reserved

Currently not used.

1-2-4. 53h

(1) Reserved (read/write)

Reserved

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
53h (R)									Reserved
									Initial value
53h (W)									Reserved

Currently not used.

1-2-5. 54h

(1) SCSCBMON (SCSI control bus monitor) register (read)

SCSCBMON (SCSI control bus monitor) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
54h (R)	MON BSY	MON SEL	MON MSG	MON CD	MON IO	MON REQ	MON ACK	MON ATN	SCSCBMON
									Initial value

The SCSI control signals on the SCSI bus can be monitored with this register.

All signals are positive logic.

bit 7: MONBSY (monitor BSY)
Monitors the XBSY signal on the SCSI bus.
bit 6: MONSEL (monitor SEL)
Monitors the XSEL signal on the SCSI bus.
bit 5: MONMSG (monitor MSG)
Monitors the XMSG signal on the SCSI bus.
bit 4: MONCD (monitor CD)
Monitors the XCD signal on the SCSI bus.
bit 3: MONIO (monitor IO)
Monitors the XIO signal on the SCSI bus.
bit 2: MONREQ (monitor REQ)
Monitors the XREQ signal on the SCSI bus.
bit 1: MONACK (monitor ACK)
Monitors the XACK signal on the SCSI bus.
bit 0: MONATN (monitor ATN)
Monitors the XATN signal on the SCSI bus.

(2) Reserved (write)

Reserved

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
54h (W)									Reserved

Currently not used.

1-2-6. 55h

(1) SCFIFSTS (SCSI FIFO status) register (read)

SCFIFSTS (SCSI FIFO status) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
55h (R)	FIFE MPTY			FIF FULL	FIF CNT3	FIF CNT2	FIF CNT1	FIF CNT0	SCFIFSTS
	1			0	0	0	0	0	Initial value

The status of the built-in FIFO can be read from this register.

bit 7: FIFEMPTY (FIFO empty)
When this bit is high, the FIFO is empty.
bit 4: FIFFULL (FIFO full)
When this bit is high, the FIFO is full.
bits 3 to 0: FIFCNT3 to 0 (FIFO count 3 to 0)
These bits indicate the used capacity of the built-in FIFO.

(2) Reserved (write)

Reserved

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
55h (W)									Reserved

Currently not used.

1-2-7. 56h

(1) Reserved (read/write)

Reserved

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
56h (R)									Reserved
									Initial value
56h (W)									Reserved

Currently not used.

1-2-8. 57h

(1) SCDATA (SCSI data) register (read/write)

SCDATA (SCSI data) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
57h (R/W)	b07	b06	b05	b04	b03	b02	b01	b00	SCDATA
									Initial value

This register is used to transfer data between the sub CPU bus and the SCSI bus.

After the assert SCSI data command has been executed, the value written in this register is output directly to the SCSI data bus until the deassert SCSI data command is executed. In addition, the SCSI data bus can be monitored by reading this register.

1-2-9. 58h

(1) SCSXFRC (SCSI sub CPU transfer counter) register (read/write)

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
58h (R/W)	"L"	"L"	"L"	b4	b3	b2	b1	b0	SCSXFRC
				0	0	0	0	0	Initial value

This register sets the number of bytes to be transferred by a phase unit of transfer command from the SCSI to the sub CPU. The maximum number of bytes which can be sent from the SCSI to the sub CPU with a single transfer is 16 bytes.

1-2-10. 59h

(1) Reserved (read/write)

Reserved

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
59h (R)									Reserved
									Initial value
59h (W)									Reserved

Currently not used.

1-2-11. 5Ah

(1) Reserved (read/write)

Reserved

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
5Ah (R)									Reserved
									Initial value
5Ah (W)									Reserved

Currently not used.

1-2-12. 5Bh

(1) SCSYNCTL (SCSI synchronous transfer control) register (read/write)

SCSYNCTL (SCSI synchronous transfer control) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
5Bh (R/W)	SYXF RPD3	SYXF RPD2	SYXF RPD1	SYXF RPD0	SYXF ROF3	SYXF ROF2	SYXF ROF1	SYXF ROF0	SCSYNCTL
	0	0	0	0	0	0	0	0	Initial value

This register sets the transfer cycle and transfer offset value during SCSI synchronous transfer. "00h" must be written in this register when performing asynchronous transfer.

The value written in this register can be read by reading this register.

bits 7 to 4: SYXFRPD3 to 0 (synchronous transfer period 3 to 0)

These bits set the transfer cycle for synchronous transfer. The actual synchronous transfer cycle is obtained from the formulas below.

When FASTSCSI = 1 (bit 7 of SCCONF1 = 1)

$$\text{Transfer cycle [ns]} = \frac{1}{f_{CLK}\ [\text{MHz}]} \times 1000 \times (4 + \text{SYXFRPDn})$$

When FASTSCSI = 0 (bit 7 of SCCONF1 = 0)

$$\text{Transfer cycle [ns]} = \frac{1}{f_{CLK}\ [\text{MHz}]} \times 1000 \times (8 + \text{SYXFRPDn})$$

In addition, the transfer rate at this time is obtained from the formula below.

$$\text{Transfer rate [MHz]} = \frac{1}{\text{Transfer cycle [ns]}} \times 1000$$

bits 3 to 0: SYXFROF3 to 0 (synchronous transfer offset 3 to 0)

These bits set the REQ and ACK offset values during synchronous transfer.

When SYXFROF3 to 0 = 0: Asynchronous transfer mode results.

When SYXFROF3 to 0 = 1 to 15: Synchronous transfer is executed at the offset value set in SYXFROF3 to 0.

1-2-13. 5Ch

(1) Reserved (read/write)

Reserved

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
5Ch (R)									Reserved
									Initial value
5Ch (W)									Reserved

Currently not used.

1-2-14. 5Dh

(1) Reserved (read/write)

Reserved

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
5Dh (R)									Reserved
									Initial value
5Dh (W)									Reserved

Currently not used.

1-2-15. 5Eh

(1) SCSCBCTL (SCSI control bus control) register (read/write)

SCSCBCTL (SCSI control bus control) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
5Eh (R/W)	CTL BSY	CTL SEL	CTL MSG	CTL CD	CTL IO	CTL REQ			SCSCBCTL
	0	0	0	0	0	0			Initial value

After the assert SCSI control command has been executed, the SCSI control signals on the SCSI data bus can be driven directly through this register until the deassert SCSI control command is executed. When each bit is set high, the corresponding SCSI control signal is also set high. When this register is read, the value written in this register is read.

Note) Reading this register is not the same as reading the SCSI bus status. The SCSI bus status can be known by reading the SCSCBMON register (54h).

bit 7: CTLBSY (control BSY)
Controls XBSY signal assert/deassert.
bit 6: CTLSEL (control SEL)
Controls XSEL signal assert/deassert.
bit 5: CTLMSG (control MSG)
Controls XMSG signal assert/deassert.
bit 4: CTLCD (control CD)
Controls XCD signal assert/deassert.
bit 3: CTLIO (control IO)
Controls XIO signal assert/deassert.
bit 2: CTLREQ (control REQ)
Controls XREQ signal assert/deassert.

1-2-16. 5Fh

(1) Reserved (read/write)

Reserved

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
5Fh (R)									Reserved
									Initial value
5Fh (W)									Reserved

Currently not used.

1-2-17. 60h

(1) SCCONF0 (SCSI module configuration 0) register (read/write)

SCCONF0 (SCSI module configuration 0) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
60h (R/W)			CDBSIZDF	ANEGDATA	ANEGRQAK				SCCONFIG
			0	0	0				Initial value

This register sets the various parameters for the CXD1804AR/SCSI2 controller block.

bit 5: CDBSIZDF (CDB size definition)
Manipulating this bit changes the definition of the SCCDBSIZ register.
When CDBSIZDF is low

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
69h (R/W)	GP7B1	GP7B0	GP6B1	GP6B0	GP4B1	GP4B0	GP3B1	GP3B0	SCCDBSIZ
	0	0	0	0	0	0	0	0	Initial value

When CDBSIZDF is high

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
69h (R/W)	GP7B1	GP7B0	GP6DB1	GP6DB0	GP6CB1	GP6CB0	GP43B1	GP43B0	SCCDBSIZ
	0	0	0	0	0	0	0	0	Initial value

bit 4: ANEGDATA (active negation on XDB (bits 7 to 0) and XDBP)
If this bit is set high, the XDB (bits 7 to 0) and XDBP pins of the SCSI bus are set to active negation.

bit 3: ANEGRQAK (active negation on XREQ and XACK)
If this bit is set high, the XREQ and XACK pins of the SCSI bus are set to active negation.

1-2-18: 61h

(1) SCCONF1 (SCSI module configuration 1) register (read/write)

SCCONF1 (SCSI module configuration 1) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
61h (R/W)	FAST SCSI	HSXF RSPE	HSXF RAT	SPAR ENB	RSLR TLM3	RSLR TLM2	RSLR TLM1	RSLR TLM0	SCMODE
	0	0	0	0	0	0	0	0	Initial value

This register specifies the SCSI operation mode for the CXD1804AR/SCSI2 controller block.

bit 7: FASTSCSI (Fast SCSI mode)
If this bit is set, synchronous transfer is performed at Fast SCSI timing.

bit 6: HSXFRSPE (halt SCSI transfer upon SCSI parity error)
This bit determines the operation when a parity error occurs on the SCSI bus during SCSI transfer. If this bit is set high, transfer is stopped and the command is interrupted. If this bit is set low, transfer continues. SCSIPERR interrupt is generated in either case.
This bit has no meaning when bit 4 (SPARENB) of the SCCONF1 register is low.

bit 5: HSXFRAT (halt SCSI transfer upon SCSI attention condition)
This bit determines the operation when the ATN condition is established on the SCSI bus during SCSI transfer. If this bit is set high, transfer is stopped and the command is interrupted. If this bit is set low, transfer continues. ATNCOND interrupt is generated in either case.

bit 4: SPARENB (SCSI parity enable)
If this bit is set high, parity detection is performed on the SCSI bus. While this bit is high, parity detection is performed during the selection and information transfer phases. If a parity error is detected while executing selection phase, the CXD1804AR/SCSI2 controller block does not respond to the selection.

bits 3 to 0: RSLRTLM (3 to 0) (Reselection retry limit)
These bits set the number of times for which Reselection is retried until the CXD1804AR/SCSI2 controller block informs the sub CPU that Reselection failed when executing Reselection. The number of retries can be set from 1 to 15 times including the number of Arbitration failures. If "0" is set, the number of retries is infinite.

1-2-19. 62h

(1) SCCONF2 (SCSI module configuration 2) register (read/write)

SCCONF2 (SCSI module configuration 2) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
62h (R/W)							IDAS SIGN	IDUN ASGN	SCCONF2
							0	0	Initial value

bits 1 to 0: IDASSIGN (ID assigned), IDUNASGN (ID unassigned)

The combination of these two bits is used to set the CXD1804AR to the various SCAM states. When not using SCAM, IDASSIGN must be set to 1 and IDUNASGN to 0.

IDASSIGN	IDUNASGN	Status
0	0	SCAM monitor status
0	1	ID unassigned status
1	0	ID assigned status
1	1	Undefined

SCAM monitor status

In this status, the CXD1804AR responds to SCAM selection. If a SCAMSL interrupt is detected in this status, the CXD1804AR must be set to ID unassigned status.

The CXD1804AR also responds if selection of the current ID continues for longer than the SCAM unassigned ID selection response delay (4ms) in this status. If a SLWATN or SLWOATN interrupt is detected in this status, the CXD1804AR must be set to ID assigned status.

ID unassigned status

In this status, the CXD1804AR responds only to SCAM selection. If an ID is assigned by SCAM protocol, the CXD1804AR must be set to ID assigned status.

ID assigned status

In this status, the CXD1804AR responds only to normal selection, and operates as a SCAM tolerant device.

1-2-20. 63h

(1) SCRSLTOT (SCSI Reselection time-out) register (read/write)

SCRSLTOT (SCSI Reselection time-out) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
63h (R/W)	RSLT OUT7	RSLT OUT6	RSLT OUT5	RSLT OUT4	RSLT OUT3	RSLT OUT2	RSLT OUT1	RSLT OUT0	SCRSLTOT
	0	0	0	0	0	0	0	0	Initial value

This register sets the Reselection time-out time. The relationship between the value of this register and the Reselection time-out is shown below.

$$\text{Time-out [ms]} = \frac{1}{f_{CLK}\,[\text{MHz}]} \times 16.384 \times (\text{RSLTOUTn})$$

1-2-21. 64h

(1) Reserved (read/write)

Reserved

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
64h (R)									Reserved
									Initial value
64h (W)									Reserved

Currently not used.

1-2-22. 65h

(1) SCID (SCSI ID) register (read)

SCID (SCSI ID) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
65h (R)	SEL ID2	SEL ID1	SEL ID0	SELI DINV		OWN ID2	OWN ID1	OWN ID0	SCID
	0	0	0	0	0	0	0	0	Initial value

The ID of the initiator which has selected the CXD1804AR and other information can be read from this register.

bits 7 to 5: SELID2 to 0 (selected ID)
The ID of the initiator which has selected the CXD1804AR can be read from these bits.
Even after Disconnect, this value is held until the CXD1804AR responds to the next selection.

bit 4: SELIDINV (selected ID invalid)
If single initiator mode is used during selection, this bit is set high. This indicates that SELID2 to 0 are invalid at this time.

bits 2 to 0: OWNID2 to 0 (Own ID)
The ID of the CXD1804AR/SCSI2 controller block can be read from these bits.

(2) SCID (SCSI ID) register (write)

SCID (SCSI ID) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
65h (W)	REL ID2	REL ID1	REL ID0			OWN ID2	OWN ID1	OWN ID0	SCID

This register sets the initiator ID and the CXD1804AR/SCSI2 controller block's own ID when the CXD1804AR performs Reselect.

bits 7 to 5: RSLID2 to 0 (Reselect ID)
These bits set the ID of the initiator to be reselected.

bits 2 to 0: OWNID2 to 0 (Own ID)
These bits set the CXD1804AR/SCSI2 controller block's own ID.

Note) Own ID should be set before issuing the enable selection command.
Since the initial value for Own ID is low, if the enable selection command is issued before setting Own ID, the CXD1804AR will respond to the selection for ID = low.

1-2-23. 66h

(1) Reserved (read/write)

Reserved

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
66h (R)									Reserved
									Initial value
66h (W)									Reserved

Currently not used.

1-2-24. 67h

(1) Reserved (read/write)

Reserved

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
67h (R)									Reserved
									Initial value
67h (W)									Reserved

Currently not used.

1-2-25. 68h

(1) Reserved (read/write)

Reserved

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
68h (R)									Reserved
									Initial value
68h (W)									Reserved

Currently not used.

1-2-26. 69h

(1) SCCDBSIZ (SCSI CDB size) register (read/write)

SCCDBSIZ (SCSI CDB size) register (when CDBSIZDF = 0)

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
69h (R/W)	GP7 B1	GP7 B0	GP6 B1	GP6 B0	GP4 B1	GP4 B0	GP3 B1	GP3 B0	SCCDBSIZ
	0	0	0	0	0	0	0	0	Initial value

SCCDBSIZ (SCSI CDB size) register (when CDBSIZDF = 1)

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
69h (R/W)	GP7 B1	GP7 B0	GP6D B1	GP6D B0	GP6C B1	GP6C B0	GP43 B1	GP43 B0	SCCDBSIZ
	0	0	0	0	0	0	0	0	Initial value

When the CXD1804AR is selected from the initiator during auto sequence, the number of bytes to be transferred by command phase is determined by the value of the group code field (bits 7 to 5) in the 1st byte of the SCSI CDB's operation code. The CXD1804AR/SCSI2 controller block determines how many bytes are to be transferred according to this value, but groups 7, 6, 4 and 3 are reserved or vendor specific for SCSI standards.

The size of the SCSI CDB (command description block) is defined for each value of the group code field (bits 7 to 5) in the 1st byte of the operation code.

Group	Operation Code	Byte length
Group 0	000x xxxx	6 bytes
Group 1	001x xxxx	10 bytes
Group 2	010x xxxx	10 bytes
Group 3	011x xxxx	Reserved
Group 4	100x xxxx	Reserved
Group 5	101x xxxx	12 bytes
Group 6	110x xxxx	Vendor Specific
Group 7	111x xxxx	Vendor Specific

Reserved and vendor specific items in the table above can be defined by this register. The command length can be set to 6, 10 or 12 bytes.
This register sets the number of bytes to be received when these group commands are received.
When CDBSIZDF is "0", each bit is defined as follows.

bits 7 to 6: GP7B1 to 0 (group 7)
Define the group 7 (vendor specific) command length.

bits 5 to 4: GP6B1 to 0 (group 6)
Define the group 6 (vendor specific) command length.

bits 3 to 2: GP4B1 to 0 (group 4)
Define the group 4 (reserved) command length.

bits 1 to 0: CG3B1 to 0 (group 3)
Define the group 3 (reserved) command length.

When CDBSIZDF is "1", each bit is defined as follows.

bits 7 to 6: GP7B1 to 0 (group 7)
Define the group 7 (reserved) command length.

bits 5 to 4: GP6DB1 to 0 (group 6 Dxh)
Define the group 6D (vendor specific) command length.
This indicates group 6 commands with a CDB operation code of 1101xxxxb.

bits 3 to 2: GP6CB1 to 0 (group 6 Cxh)
Define the group 6C (vendor specific) command length.
This indicates group 6 commands with a CDB operation code of 1100xxxxb.

bits 1 to 0: CG43B1 to 0 (group 4 and group 3)
Define the group 4 (reserved) and group 3 (reserved) command length. The command lengths of these two groups cannot be defined separately.

Two bits are allotted to each of GP7B (1:0), GP6DB (1:0), GP6CB (bits 1, 0), GP43B (bits 1, 0), GP4B (bits 1, 0) and GP3B (bits 1, 0). Command lengths should be set according to the rules listed in the table below.

GPxxB1	GPxxB0	Number of bytes
0	0	Undefined
0	1	6 bytes
1	0	10 bytes
1	1	12 bytes

1-2-27. 6Ah

(1) SCUSTS (SCSI module microcode status) register (read/write)

SCUSTS (SCSI module microcode status) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
6Ah (R)	USTS B7	USTS B6	USTS B5	USTS B4	USTS B3	USTS B2	USTS B1	USTS B0	SCUSTS
	0	0	0	0	0	0	0	0	Initial value

If this register is read when a sequence command has been completed, it indicates how far the sequence has progressed.

(2) Reserved (write)

Reserved

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
6Ah (W)									Reserved

Currently not used.

1-2-28. 6Bh

(1) SCSTCONF (stream configuration) register (read/write)

SCSTCONF (stream configuration) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
6Bh (R)						STDS CPRV			SCSTCONF
									Initial value

This register specifies the exception processing method when executing stream commands.

bit 2: STDSCPRV (stream Disconnect privilege)

If this bit is set high, the bus is disconnected when the buffer becomes empty. If this bit is set low, the bus is not disconnected.

1-2-29. 6Ch

(1) SCSTRSLM (stream Reselection message) register (read/write)

SCSTRSLM (stream Reselection message) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
6Ch (R/W)									SCSTRSLM
	0	0	0	0	0	0	0	0	Initial value

The message to be transferred to the initiator during the Message In phase immediately following Reselection when executing stream commands is set in this register.

1-2-30. 6Dh

(1) SCSTTIOS (stream terminate I/O status) register (read/write)

SCSTTIOS (stream terminate I/O status) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
6Dh (R/W)									SCSTTIOS
	0	0	0	0	0	0	0	0	Initial value

The status to be transferred to the initiator after all data has been transferred when executing stream commands is set in this register.

1-2-31. 6Eh

(1) SCSTTIOM (stream terminate I/O message) register (read/write)

SCSTTIOM (stream terminate I/O message) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
6Eh (R/W)									SCSTTION
	0	0	0	0	0	0	0	0	Initial value

The message to be transferred to the initiator after all data has been transferred when executing stream commands is set in this register.

1-2-32. 6Fh

(1) Reserved (read/write)

Reserved

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
6Fh (R)									Reserved
									Initial value
6Fh (W)									Reserved

Currently not used.

1-3. Common Registers

1-3-1. 70h

(1) INTSTS0 (interrupt status 0) register (read)

INTSTS0 (interrupt status 0) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
70h (R)	DEC INT	DEC TOUT	DRV OVRN	CRCT END	CDR INT	"L"	"L"	SHT SYNC	INTSTS0
									Initial value

bit 7: DECINT (decoder interrupt)

This interrupt is generated when the decoder is executing a command.

(1) During execution of a write-only, monitor-only, or real-time error correction command:
If the Header byte is received from the CD DSP when a Sync mark is detected or inserted, the DECINT status is generated. However, while the Sync mark detection window is open, the DECINT status is not established if the Sync mark interval is less than 2352 bytes.

(2) During repeat correction execution:
The DECINT status is established each time one correction is completed. (CRCTEND interrupt?)

(3) During CD-DA command execution:
The DECINT status is established each time 2352 bytes of data are written.

(4) During subcode buffering execution:
The DECINT status is established when the subcode for one sector is written in the buffer.

bit 6: DECTOUT (decoder time-out)

The DECTOUT status is established when the Sync mark is not detected even after the time it takes to search 3 sectors (40.6ms at normal-speed playback) has elapsed after the decoder has been set to the monitor-only, write-only or real-time correction mode.

bit 5: DRVOVRN (drive overrun)

While the decoder is executing a write-only, real-time correction, or CD-DA command, if buffering in the area specified by DLARA is completed, the DRVOVRN status results.

bit 4: CRCTEND (correction end)

If error correction of the CD-ROM data is completed, the CRCTEND status results.

bit 3 CDRINT (CD-R interrupt)

When the CDRINT status is established, this bit goes high.

bit 0 SHTSYNC (short sync)

The SHTSYNC status is established when the decoder is operating in the monitor-only, write-only, real-time correction or asynchronous correction mode.

(2) CLRINT0 (clear interrupt 0) register (write)

CLRINT0 (clear interrupt 0) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
70h (W)	DEC INT	DEC TOUT	DRV OVRN	CRCT END	CDR INT	"L"	"L"	SHT SYNC	CLRINT0

When each bit of this register is set to "1", the corresponding interrupt status of the INTSTS0 register (70h) is cleared. The bit concerned is automatically set to "0" after its interrupt status has been cleared. Therefore, there is no need for the sub CPU to reset "0".

1-3-2. 71h

(1) INTSTS1 (interrupt status 1) register (read)

INTSTS1 (interrupt status 1) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
71h (R)							TIMER	SUBCSYNC	INTSTS1
									Initial value

The value of each bit in this register indicates that of the corresponding interrupt status. These bits are not affected by the values of the INTEN1 register bits.

bit 1: TIMER

TIMER status is established when the time set in the TIMER-H and L registers has elapsed.

bit 0: SUBCSYNC (subcode sync)

If a subcode Sync mark is detected or inserted while subcode fetching is enabled, the SUBCSYNC status results.

Note that if the SUBCSYNC interrupt is not cleared within 95 WFCK cycles, the SUBCSYNC status is not established the next time a subcode Sync mark is detected or inserted. In this event, the subcode-Q read from the SBQDT register is also not renewed.

(2) CLRINT1 (clear interrupt 1) register (write)

CLRINT1 (clear interrupt 1) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
71h (W)	"L"	"L"	"L"	"L"	"L"	"L"	TIMER	SUBCSYNC	CLRINT1

When each bit of this register is set to "1", the corresponding interrupt status of the INTSTS1 register (71h) is cleared. The bit concerned is automatically set to "0" after its interrupt status has been cleared. Therefore, there is no need for the sub CPU to reset "0".

1-3-3. 72h

(1) INTSTS2 (interrupt status 2) register (read)

INTSTS2 (interrupt status 2) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
72h (R)	FUNCCMPL	CMDIGNR	SCSIRST	ATNCOND	SCSIPERR	SLWATN	SLWOATN	RSLFAIL	INTSTS2
									Initial value

When an interrupt is generated, the bit allotted to that interrupt is set to "1".

Each bit is set regardless of the values of the INTEN2 register (76h).

bit 7: FUNCCMPL (function complete)

Indicates that execution of the command issued to the CXD1804AR/SCSI2 controller block has been completed.

bit 6: CMDIGNR (command ignored)

Indicates that the command issued to the CXD1804AR/SCSI2 controller block was not executed. This interrupt is generated when the CXD1804AR is operating in a mode which does not allow the command given to the CXD1804AR to be executed.

bit 5: SCSIRST (SCSI reset)
Indicates that the XRST signal was driven on the SCSI bus.
Do not write commands in the SCCMD register (50h) until the sub CPU has confirmed that the XRST signal is negated on the SCSI bus by reading the MONRST bit (bit 7) of the SCSTS register (50h).

bit 4: ATNCOND (ATN condition)
When the CXD1804AR/SCSI2 controller block is in the target status, this bit indicates that the initiator drove XATN.

bit 3: SCSIPERR (SCSI parity error)
Indicates that a parity error occurred on the SCSI data bus in the SCSI transfer phase or the selection phase.
This interrupt is not generated when the SPARENB bit of the SCCONF1 register is low.

bit 2: SLWATN (selection with ATN)
Indicates that the CXD1804AR/SCSI2 controller block was selected with ATN by another SCSI device, and that the CXD1804AR/SCSI2 controller block responded to this selection.

bit 1: SLWOATN (selection without ATN)
Indicates that the CXD1804AR/SCSI2 controller block was selected without ATN by another SCSI device, and that the CXD1804AR/SCSI2 controller block responded to this selection.

bit 0: RSLFAIL (Reselection fail)
Indicates that the CXD1804AR/SCSI2 controller block participated in Arbitration during execution of a Reselect command, and that the CXD1804AR/SCSI2 controller block fails or a time-out occurred during Reselection after acquiring the bus by Arbitration. This interrupt is generated only when Reselection fail is repeated for the number of times specified by the RSLRTLM (3:0) bit of the SCCONF1 register.

(2) CLRINT2 (clear interrupt 2) register (write)

CLRINT2 (clear interrupt 2) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
72h (W)	FUNC CMPL	CMD IGNR	SCSI RST	ATN CONT	SCSI PERR	SLW ATN	SLWO ATN	RSL FAIL	CLRINT2

When each bit of this register is set to "1", the corresponding interrupt status of the INTSTS2 register (72h) is cleared. The bit concerned is automatically set to "0" after its interrupt status has been cleared. Therefore, there is no need for the sub CPU to reset "0".

1-3-4. 73h

(1) INTSTS3 (interrupt status 3) register (read)

INTSTS3 (interrupt status 3) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
73h (R)							SCAM INIF	SCAM SL	INTSTS3
									Initial value

When an interrupt is generated, the bit allotted to that interrupt is set to "1".
Each bit is set regardless of the values of the INTEN3 register (77h).

bit 1: SCAMINF (SCAM initiation fail)
Indicates that the CXD1804AR/SCSI2 controller block participated in SCAM initiation and failed at Arbitration.

bit 0: SCAMSL (SCAM selection)
Indicates that the CXD1804AR/SCSI2 controller block was selected with SCAM selection by another SCSI device, and that the CXD1804AR/SCSI2 controller block responded to this selection.

(2) CLRINT3 (clear interrupt 3) register (write)

CLRINT3 (clear interrupt 3) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
73h (W)							SCAM INIF	SCAM SL	CLRINT2

When each bit of this register is set to "1", the corresponding interrupt status of the INTSTS3 register (73h) is cleared. The bit concerned is automatically set to "0" after its interrupt status has been cleared. Therefore, there is no need for the sub CPU to reset "0".

1-3-5. 74h

(1) INTEN0 (interrupt enable 0) register (read/write)

INTEN0 (interrupt enable 0) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
74h (R/W)	DEC INT	DEC TOUT	DRV OVRN	CRCT END	CDR INT			SHT SYNC	INTEN0
									Initial value

Setting each bit of this register high enables interrupt requests to the sub CPU from this IC in response to the corresponding interrupt status. (In other words, if that interrupt status results, the INT pin goes active.) The value of each bit in this register has no effect on their corresponding interrupt status.

bit 7: DECINT (decoder interrupt)
bit 6: DECTOUT (decoder time-out)
bit 5: DRVOVRN (drive overrun)
bit 4: CRCTEND (correction end)
bit 3: CDRINT (CD-R interrupt)
bit 0: SHTSYNC (short sync)

1-3-6. 75h

(1) INTEN1 (interrupt enable 1) register (read/write)

INTEN1 (interrupt enable 1) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
75h (R/W)							TIMER	SUBC SYNC	INTEN1
									Initial value

Setting each bit of this register high enables interrupt requests to the sub CPU from this IC in response to the corresponding interrupt status. (In other words, if that interrupt status results, the INT pin goes active.) The value of each bit in this register has no effect on their corresponding interrupt status.

bit 1: TIMER
bit 0: SUBCSYNC (Subcode Sync)

1-3-7. 76h

(1) INTEN2 (interrupt enable 2) register (read/write)

INTEN2 (interrupt enable 2) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
76h (R/W)	FUNC CMPL	CMD IGNR	SCSI RST	ATN COND	SCSI PERR	SLW ATN	SLWO ATN	RSL FAIL	INTEN2
									Initial value

Setting each bit of this register high enables interrupt requests to the sub CPU from this IC in response to the corresponding interrupt status. (In other words, if that interrupt status results, the INT pin goes active.) The value of each bit in this register has no effect on their corresponding interrupt status.

bit 7: FUNCCMPL (function complete)
bit 6: CMDIGNR (command ignored)
bit 5: SCSIRST (SCSI reset)
bit 4: ATNCOND (ATN condition)
bit 3: SCSIPERR (SCSI parity error)
bit 2: SLWATN (selection with ATN)
bit 1: SLWOATN (selection without ATN)
bit 0: RSLFAIL (Reselection fail)

1-3-8. 77h

(1) INTEN3 (interrupt enable 3) register (read/write)

INTEN3 (interrupt enable 3) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
77h (R/W)							SCAM INIF	SCAM SL	INTEN3
									Initial value

Setting each bit of this register high enables interrupt requests to the sub CPU from this IC in response to the corresponding interrupt status. (In other words, if that interrupt status results, the INT pin goes active.) The value of each bit in this register has no effect on their corresponding interrupt status.

bit 1: SCAMINIF (SCAM initiation fail)
bit 0: SCAMSL (SCAM selection)

1-3-9. 78h

(1) INTSRC (interrupt source) register (read)

INTSRC (interrupt source) register

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
78h (R)						SCSI REL	SCTM REL	DEC REL	INTSRC
									Initial value

The internal block interrupt which drove the interrupt pin can be known by reading this register.

bits 7 to 3: RESERVED

bit 2: SCSIREL (SCSI related)
When this bit is high, this indicates that the interrupt pin is being driven by an INTSTS2 or INTSTS3 register interrupt which is enabled by the INTEN2 or INTEN3 register.

bit 1: SCTMREL (subcode and timer related)
When this bit is high, this indicates that the interrupt pin is being driven by an INTSTS1 register interrupt which is enabled by the INTEN1 register.

bit 0: DECREL (decoder related)
When this bit is high, this indicates that the interrupt pin is being driven by an INTSTS0 register interrupt which is enabled by the INTEN0 register.

(2) Reserved (write)

Reserved

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
78h (W)									Reserved

Currently not used.

1-3-10. 79h

(1) Reserved (read/write)

Reserved

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
79h (R)									Reserved
79h (W)									Reserved

Currently not used.

1-3-11. 7Ah

(1) Reserved (read/write)

Reserved

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
7Ah (R)									Reserved
7Ah (W)									Reserved

Currently not used.

1-3-12. 7Bh

(1) Reserved (read/write)

Reserved

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
7Bh (R)									Reserved
7Bh (W)									Reserved

Currently not used.

1-3-13. 7Ch

(1) Reserved (read/write)

Reserved

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
7Ch (R)									Reserved
7Ch (W)									Reserved

Currently not used.

1-3-14. 7Dh

(1) Reserved (read/write)

Reserved

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
7Dh (R)									Reserved
7Dh (W)									Reserved

Currently not used.

1-3-15. 7Eh

(1) Reserved (read/write)

Reserved

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
7Eh (R)									Reserved
7Eh (W)									Reserved

Currently not used.

1-3-16. 7Fh

(1) Reserved (read/write)

Reserved

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
7Fh (R)									Reserved
7Fh (W)									Reserved

Currently not used.

[2] Description of SCSI Controller Block Commands

The CXD1804AR/SCSI2 core is designed to automatically execute procedures other than data transfer to the greatest extent possible in order to reduce data transfer overloads.

CXD1804AR/SCSI2 core command set

CAT1	CAT0	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0	Description
0	0	0	0	0	0	0	0	NOP
0	0	0	0	0	0	0	1	CHIP Reset
0	0	0	0	0	0	1	1	Flush FIFO
0	0	0	0	0	1	0	0	Assert SCSI Control
0	0	0	0	0	1	0	1	Deasert SCSI Control
0	0	0	0	0	1	1	0	Assert SCSI Data
0	0	0	0	0	1	1	1	Deasert SCSI Data
0	0	0	0	1	0	0	0	Enable Selection
0	0	0	0	1	0	0	1	Disable Selection
CAT1	CAT0	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0	Description
0	1	0	0	0	0	0	0	Reselect and Send Message (s)
0	1	0	0	0	0	0	1	Initiate SCAM
0	1	0	0	0	0	1	0	Reselect, Send Message (s) and Receive Data
0	1	0	0	0	0	1	1	Reselect, Send Message (s) and Send Data
CAT1	CAT0	BUF	SUB	CMD3	CMD2	CMD1	CMD0	Description
1	0	*	*	0	0	0	0	Receive Data
1	0	*	*	0	0	0	1	Send Data
1	0	*	*	0	0	1	0	Reserved
1	0	*	*	0	0	1	1	Reserved
1	0	*	*	0	1	0	0	Reseive Command
1	0	*	*	0	1	0	1	Send Status
1	0	*	*	0	1	1	0	Receive Message
1	0	*	*	0	1	1	1	Send Message
1	0	0	0	1	0	0	0	Disconnect
1	0	0	0	1	0	0	1	Send Message (s) and Disconnect
1	0	0	0	1	0	1	0	Terminate I/O and bus free
1	0	0	0	1	0	1	1	Terminate I/O and link
1	0	0	0	1	1	0	0	Receive Command Sequence
CAT1	CAT0	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0	Description
1	1	0	0	0	0	0	0	Stream Abort
1	1	0	0	0	0	0	1	Stream and Stop
1	1	0	0	0	0	1	0	Stream and Bus Free
1	1	0	0	0	0	1	1	Stream and Link
1	1	0	0	0	1	0	0	Stream Pause

* Either "1" or "0" can be written. However, if the BUF bit is "1", "0" must be written for the SUB bit.

States which allow commands to be executed are limited for each category.

CAT1	CAT0	Description
0	0	Can be executed in all states
0	1	Can be executed only in the Disconnect status
1	0	Can be executed only in the target mode
1	1	Stream commands

2-1. Precautions when Executing Commands

In the CXD1804AR, an interrupt is generated for the sub CPU at the point when an interrupt event occurs. However, the sub CPU must wait until a FUNCCMPL interrupt (INTSTS2, bit 7) is generated.

2-2. Category 00 Commands

These commands can be executed regardless of the CXD1804AR/SCSI2 core status.

2-2-1. NOP (00h)

Description: When this command is issued, a FUNCCMPL interrupt is generated but no other action is taken.
Preparation: None
Operation: After this command is issued, the CMDINPRG bit (SCSTS register (50h), bit 0) goes high. Then, after the FUNCCMPL interrupt is generated, the CMDINPRG bit goes low and the command is completed.
Interrupt: FUNCCMPL function complete (INTSTS2 register (72h), bit 7)
Microcode status:
The microcode status has no meaning with this command.

2-2-2. CHIP reset (01h)

Description: This command initializes the registers (50h to 6Fh, 72h to 73h, and 76h to 77h) inside the SCSI block and resets the microcode PC.
In this event, commands currently being executed are forcibly interrupted.
Preparation: None
Operation: Commands are normally decoded by a microprogram in the CXD1804AR/SCSI2 core. However, when this command is issued, the CXD1804AR/SCSI2 core decodes this command with the hardware instead of the microcode and generates a reset signal internally. Commands currently being executed are also forcibly interrupted.
Interrupt: An interrupt is not generated. After this command is issued, the sub CPU must wait for 150ns before issuing the next command.
Microcode status:
The microcode status has no meaning with this command.

2-2-3. Flush FIFO (03h)

Description: This command clears the FIFO address counter, invalidates all data within the FIFO, and sets the FIFO to empty status.
Preparation: None
Operation: After this command is issued, the FIFO is set to empty status.
Interrupt: An interrupt is not generated.
If the XWAT pin is not used, wait 150ns or more after this command is issued before issuing the next command.
Microcode status:
The microcode status has no meaning with this command.

2-2-4. Assert SCSI control (04h)

Description: This command enables direct control of the SCSI control bus signals through the SCSCBCTL register (5Eh).

Preparation: When this command is issued, the value of the SCSCBCTL register is output as is to the SCSI bus. Therefore, be sure to check the contents of the SCSCBCTL register before executing this command.

Operation: This command enables direct control of the SCSI control bus signals and is then completed.
After this command is executed, if each bit of the SCSCBCTL register (5Eh) allotted to each SCSI control bus signal is set high, the corresponding signal is driven.

Interrupt: An interrupt is not generated.
If the XWAT pin is not used, wait 150ns or more after this command is issued before issuing the next command.

Microcode status:
The microcode status has no meaning with this command.

2-2-5. Deassert SCSI control (05h)

Description: This command prohibits direct control of the SCSI control bus signals through the SCSCBCTL register (5Eh).

Preparation: None

Operation: This command prohibits direct control of the SCSI control bus signals and is then completed.
The SCSI control signals which were controlled directly from the SCSCBCTL register (5Eh) are deasserted. The data written in the SCSCBCTL register is held.

Interrupt: An interrupt is not generated.
If the XWAT pin is not used, wait 150ns or more after this command is issued before issuing the next command.

Microcode status:
The microcode status has no meaning with this command.

2-2-6. Assert SCSI data (06h)

Description: This command enables direct control of the SCSI data bus through the SCDATA register (57h).
Control is disabled immediately after resetting the hardware or issuing the chip reset command.

Preparation: None

Operation: Direct control of each bit of the SCSI data bus is enabled and then the command is completed.
After this command is executed, if data is written in the SCDATA register (57h), this data is output directly to the SCSI data bus. At this time, the FIFO does not perform FIFO functions.

Interrupt: An interrupt is not generated.
If the XWAT pin is not used, wait 150ns or more after this command is issued before issuing the next command.

Microcode status:
The microcode status has no meaning with this command.

2-2-7. Deassert SCSI data (07h)

Description: This command prohibits direct control of the SCSI data bus through the SCDATA register (57h). Direct control of the SCSI data bus is disabled immediately after resetting the hardware or issuing the chip reset command.

Preparation: None

Operation: When this command is executed, direct control of the SCSI data bus is prohibited and then the command is completed. The FIFO operates normally after the command is executed.

Interrupt: An interrupt is not generated.
If the XWAT pin is not used, wait 150ns or more after this command is issued before issuing the next command.

Microcode status:
The microcode status has no meaning with this command.

2-2-8. Enable selection (08h)

Description: This command allows the CXD1804AR/SCSI2 core to respond to the selection. The CXD1804AR/SCSI2 core does not respond to the selection in the following cases.

a) After chip reset
b) After issuing the chip reset command
c) After the Bus-Free status is established by a Disconnect command
d) After the Bus-Free status is established by a terminate (including stream and Bus-Free) command

Operation following the execution of this command varies according to the settings of the IDASSIGN and IDUNASGN bits of the SCCONF2 register (62h).

a) IDASSIGN = 0, IDUNASGN = 0: SCAM monitor status
   1) The CXD1804AR/SCSI2 core responds to SCAM selection.
   2) The CXD1804AR/SCSI2 core responds when selection of the current ID continues for longer than the SCAM unassigned ID selection response delay (4ms).
b) IDASSIGN = 0, IDUNASGN = 1: ID unassigned status
   1) The CXD1804AR/SCSI2 core responds to SCAM selection.
c) IDASSIGN = 1, IDUNASGN = 0: ID assigned status
   1) The CXD1804AR/SCSI2 core responds to normal selection.

Responding to SCAM selection

If SCAM selection is detected in the SCAM monitor or ID unassigned status, a SCAMSL interrupt and then a FUNCCMPL interrupt are generated. After this, the sub CPU must execute SCAM protocol using assert SCSI control and assert SCSI data.

Responding to selection

When normal selection is detected during the ID assigned status, or when selection of the current ID continues for longer than 4 ms in the SCAM monitor status, the following sequences are executed.

a) When responding to selection with ATN
   Bus-Free → Arbitration → Selection with ATN → Message Out → Command
b) When responding to selection without ATN
   Bus-Free → Arbitration → Selection without ATN → Command

Preparation: The following settings must be made before executing the enable selection command.

1) Set the SCCONF0 register (60h)
   Set the appropriate values.
2) Set the SCID register (65h)
   Set the characteristic SCSI ID of the CXD1804AR/SCSI2 core. The initial SCSI ID setting is "0". Therefore, be sure to set the SCSI ID before executing the enable selection command.
3) Set the SCCONF1 register (61h).
   Set the number of Reselection retries for the CXD1804AR/SCSI2 core.
4) Set the SCCONF2 register (62h)
   Set the CXD1804AR status after executing the enable selection command.

Operation: Enable selection operation
If this command is issued, the CXD1804AR/SCSI2 core is set to status which enables selection and then a FUNCCMPL interrupt is generated.

Interrupt: An interrupt is not generated.
If the XWAT pin is not used, wait 150ns or more after this command is issued before issuing the next command.

Microcode status:
The microcode status has no meaning with this command.

(1) When responding to selection with ATN

Bus-Free → Arbitration → Selection with ATN → Message Out → Command

Operation:
1) When the characteristic SCSI ID of the CXD1804AR/SCSI2 core is detected by selection, the CXD1804AR/SCSI2 core responds to this and generates a SLWATN interrupt.
2) Operation shifts to the Message Out phase and a message is received from the initiator.
3) Operation shifts to the command phase and the CDB (command description block) is received. The number of bytes received is determined inside the CXD1804AR/SCSI2 core from the group code field (bits 7 to 5) in the 1st CDB byte of the operation code. Groups for which the CDB size is undefined by SCSI standards (groups 7, 6, 4 and 3) can be defined by the SCCDBSIZ register (69h).

Interrupt: SLWATN Selection with ATN (INTSTS2 register (72h), bit 2)
FUNCCMPL Function complete (INTSTS2 register (72h), bit 7)

Microcode status:
The microcode status value when the command is completed has the following meanings.

Code	Description
01h	An error occurred in the Message Out phase.
02h	A valid identify message was received in the Message Out phase and operation shifted to the command phase.

(2) When responding to selection without ATN

Bus-Free → Arbitration → Selection without ATN → Command

Operation: 1) When the characteristic SCSI ID of the CXD1804AR/SCSI2 core is detected by selection, the CXD1804AR/SCSI2 core responds to this and generates a SLWOATN interrupt.

2) Operation shifts to the command phase and the CDB (command description block) is received. The number of bytes received is determined inside the CXD1804AR/SCSI2 core from the group code field (bits 7 to 5) in the 1st CDB byte of the operation code. Groups for which the CDB size is undefined by SCSI standards (groups 7, 6, 4 and 3) can be defined by the SCCDBSIZ register (69h).

Interrupt: SLWOATN Selection without ATN (INTSTS2 register (72h), bit 1)

FUNCCMPL Function complete (INTSTS2 register (72h), bit 7)

Microcode status:

The microcode status value when the command is completed has the following meaning.

Code	Description
02h	Operation shifted to the command phase.

(3) When responding to SCAM selection

Bus-Free → Arbitration → SCAM selection

Operation: 1) If SCAM selection is detected, a SCAMSL interrupt and then a FUNCCMPL interrupt are generated, and the command is completed.

2) Following this, the sub CPU must execute SCAM protocol using assert SCSI control and assert SCSI data.

Interrupt: SCAMSL SCAM Selection (INTSTS3 register (73h), bit 0)

FUNCCMPL Function complete (INTSTS2 register (72h), bit 7)

Microcode status:

In this case, the microcode status value has no meaning.

2-2-9. Disable selection (09h)

Description: This command sets the CXD1804AR/SCSI2 core so that it does not respond to selection from another SCSI device.

Operation: If this command is issued, the CXD1804AR/SCSI2 core is set so that it does not respond to selection from another SCSI device and then the command is completed.

Interrupt: An interrupt is not generated.

If the XWAT pin is not used, wait 150 ns or more after this command is issued before issuing the next command.

Microcode status:

In this case, the microcode status value has no meaning.

2-3. Category 01 Commands

These commands can be executed only in the Disconnect status.

2-3-1. Reselect sequences (40h, 42h, 43h)

Description: These are auto sequence commands which are executed when attempting reconnection with the initiator after Disconnect.

The Reselect command has the following two levels.

a) After Reselect, operation shifts to the Message In phase and the message is transferred.

1) Reselect and Send Message(s) (40h)
Bus-Free → Arbitration → Reselection → Message In

b) Data transfer (Data In or Data Out phase) is executed after a).

1) Reselect, Send Message(s) and Receive Data (42h)
Bus-Free → Arbitration → Reselection → Message In → Data Out

2) Reselect, Send Message(s) and Send Data (43h)
Bus-Free → Arbitration → Reselection → Message In → Data In

Preparation: A number of operations must be performed before issuing this command.

Common operations:

1) Specify the CXD1804AR operation with the SCCONF0 (60h), SCCONF1 (61h) and SCCONF2 (62h) registers.
2) Set the SCSI ID of the initiator to be reselected and the CXD1804AR's own SCSI ID in the SCID register (65h).
3) Set the FIFO to empty status with the Flush FIFO command and then write the message to be transferred in the Message In phase in the FIFO.

Only when transferring data after executing the Message In phase:

4) The decoder block side must be prepared for transfer in advance using Reselect, Send Message(s) and Receive/Send Data.

Operation: Bus-Free → Arbitration → Reselection

If the Reselect command is executed, first the CXD1804AR/SCSI2 core first waits for Bus-Free and then enter Arbitration. Upon successfully winning the Arbitration, it then shifts to Reselection.

a) When the RSLRTLM (3 to 0) bit of the SCCONF1 register is "00h":
This sequence is repeated until both Arbitration and Reselection are completed successfully.

b) When the RSLRTLM (3 to 0) bit of the SCCONF1 register is greater than "00h":
This sequence is repeated for the number of times set by RSLRTLM. When the number of times reaches the set number, processing stops, a RSLFAIL interrupt and then a FUNCCMPL interrupt are generated, and then the command is completed.

When the CXD1804AR acquires the right to use the bus during the Arbitration phase, operation proceeds to the next step only if reconnection with the initiator is successful in the Reselection phase.

Message In phase

If reconnection is successful, operation shifts to the Message In phase and the message prepared beforehand in the FIFO, before issuing the command, is transferred to the initiator. If the attention condition is established during the transfer, ATNCOND and FUNCCMPL interrupts are generated and transfer stops at that point. However, the first byte of the message (normally identify) is always transferred.

Data In/Data Out phase

Operation shifts to either the Data In or Data Out phase as specified by the command only when the attention condition was not generated by Reselect, Send Message (s) and Receive/Send Data during the Message In phase. Transfer is performed in the DMA mode between the buffer and the SCSI. If the attention condition is established or a parity error occurs on the SCSI bus during the transfer, the corresponding interrupts are generated. Whether or not transfer is stopped by these factors is determined by the setting of the HSXFRSPE or HSXFRAT bits of the SCCONF1 register.

Interrupt: If the transfer is completed normally without problems:

FUNCCMPL Function complete (INTSTS2 register (72h), bit 7)

If the CXD1804AR/SCSI2 core is selected immediately after the command is issued or it fails at Arbitration:

SLWOATN Selected without ATN (INTSTS2 register (72h), bit 1)

SLWATN Selected with ATN (INTSTS2 register (72h), bit 2)

FUNCCMPL Function complete (INTSTS2 register (72h), bit 7)

If the CXD1804AR/SCSI2 core fails at Arbitration or Reselection:

RSLFAIL Reselection fail (INTSTS2 register (72h), bit 0)

FUNCCMPL Function complete (INTSTS2 register (72h), bit 7)

Microcode status:

The microcode status value when the command is completed has the following meanings.

Code	Description
00h	Completed normally.
01h	Reselection failed.
02h	The attention condition was established during the Message In phase.
03h	The attention condition was established during the Data In/Out phase, or a parity error occurred (Data Out phase only).

2-3-2. Initiate SCAM (41h)

Description: If this command is executed, the CXD1804AR/SCSI2 core executes Arbitration without outputting its own ID.

Operation: If this command is executed, the CXD1804AR/SCSI2 core executes Arbitration without outputting its own ID. If the CXD1804AR/SCSI2 core succeeds at Arbitration, the FUNCCMPL interrupt is generated with XBSY and XSEL driven. If the CXD1804AR/SCSI2 core fails at Arbitration, the SCAMINIF and FUNCCMPL interrupts are generated and the command is completed.

Interrupt: FUNCCMPL Function complete (INTSTS2 register (72h), bit 7)

SCAMINIF SCAM initiation fail (INTSTS3 register (73h), bit 1)

2-4. Category 10 Commands

This commands can be executed only in the target mode status. If these commands are executed in any other status, a CMDIGNR interrupt is generated. Commands for targets can be broadly classified into three groups.

a) Phase unit of transfer commands
b) Disconnect commands
c) Terminate I/O commands

2-4-1. Single phase of transfer commands

Single phase transfer commands include the following commands.

a) Receive data (80h)
b) Send data (81h)
c) Receive command (84h)
d) Send status (85h)
e) Receive message (86h)
f) Send message (87h)
g) Receive command sequence (8Ch)

These commands execute the transfer phase of the corresponding name. Each transfer command has three modes. The mode is determined by the combination of the command's BUF (bit 5) and SUB (bit 4) bits.

BUF	SUB	Mode
0	0	Sub CPU – SCSI 1-byte transfer
0	1	Sub CPU – SCSI n-byte transfer (n = 1 to 16)
1	0	Buffer – SCSI transfer
1	1	Undefined

a) Sub CPU – SCSI 1-byte transfer
   1) From the sub CPU to the SCSI:
      The sub CPU must write the data to be transferred in the FIFO beforehand.
   2) From the SCSI to the sub CPU:
      If the command is executed, one byte of data enters the FIFO when a FUNCCMPL interrupt occurs.
b) Sub CPU – SCSI n-byte transfer (n = 1 to 16)
   1) From the sub CPU to the SCSI:
      The sub CPU must write the data to be transferred in the FIFO beforehand.
   2) From the SCSI to the sub CPU:
      The number of bytes to be received must be written in the SXFRC register (58h) before issuing the command. The maximum number of bytes which can be transferred with a single transfer is 16.
      If the command is executed, data enters the FIFO when a FUNCCMPL interrupt occurs. At this time, the number of bytes remaining to be transferred can be known by reading the SXFRC register (58h). If the transfer is not interrupted by an SCSI parity error or the ATN condition, this value is "0".
c) Buffer – SCSI transfer
   The command is issued after setting the transfer at the decoder block side. Data can also be written in the FIFO beforehand.

(1) Receive command sequence (8Ch)

Description: The CDB is analyzed and received in the command phase.

Note) This command should be executed only when not even a single byte has been received yet in the command phase.

Preparation: A number of operations must be performed before issuing this command.

1) Set the number of bytes when receiving a command from a command group which is undefined by SCSI standards with the SCCDBSIZ register (69h).

Operation: After shifting to the command phase, six CDB bytes are received unconditionally. After that, the first CDB byte is analyzed, command group identification is performed and the number of deficient bytes is received.

Interrupt: FUNCCMPL Function complete (INTSTS2 register (72h), bit 7)

Microcode status:

The microcode status has no meaning with this command.

2-4-2. Disconnect commands

These commands are issued in order to release the bus when the CXD1804AR/SCSI2 core has completed a series of operations as the target.

(1) Disconnect (88h)

Description: This command releases the SCSI bus in accordance with SCSI standards and sets the SCSI bus to Bus-Free status.

Interrupt: FUNCCMPL Function complete (INTSTS2 register (72h), bit 7)

Microcode status:

The microcode status has no meaning with this command.

(2) Send Message(s) and Disconnect (89h)

Description: This command executes the Message In phase and then disconnects.

Preparation: A number of operations must be performed before issuing this command.

1) Set the FIFO to empty status with the Flush FIFO command and then write the message to be transferred in Message In phase in the FIFO.

Operation: After shifting to the Message In phase and transferring the FIFO data, the CXD1804AR/SCSI2 core is set to the disable selection status. Then the Bus-Free status is established, a FUNCCMPL interrupt is generated and the command is completed.

Interrupt: FUNCCMPL Function complete (INTSTS2 register (72h), bit 7)

Microcode status:

The microcode status has no meaning with this command.

2-4-3. Terminate I/O commands

These commands are issued in order to release the bus when the CXD1804AR/SCSI2 core has completed a series of operations as the target.

(1) Terminate I/O and Bus-Free (8Ah)

Description: After transferring one byte of the status in the Status phase, operation shifts to the Message In phase and the message is transferred to the initiator. Then, the connection is disconnected and the SCSI bus is set to Bus-Free status.

Preparation: A number of operations must be performed before issuing this command.

1) Set the FIFO to empty status with the Flush FIFO command and then write the one byte to be transferred in the Status phase and the message to be transferred in the Message In phase in the FIFO.

Operation: After shifting to the Status phase and transferring one byte of the FIFO data, operation shifts to the Message In phase and the FIFO data is transferred. Upon completion of the transfer, the CXD1804AR/SCSI2 core is set to the disable selection status. Then Bus-Free status is established, a FUNCCMPL interrupt is generated and the command is completed.

Interrupt: FUNCCMPL Function complete (INTSTS2 register (72h), bit 7)

Microcode status:

The microcode status value when the command is completed has the following meanings.

Code	Description
00h	Completed normally.
01h	The ATN condition was established while executing the Status phase.
02h	The ATN condition was established while executing the Message In phase.

(2) Terminate I/O and link (8Bh)

Description: After transferring one byte of the status in the Status phase, operation shifts to the Message In phase and the message is transferred to the initiator. Then, operation shifts to the command phase, the SCSI CDB is received, and the command is completed.

Preparation: A number of operations must be performed before issuing this command.

1) Set the FIFO to the empty status with the Flush FIFO command and then write the one byte to be transferred in the Status phase and the message to be transferred in the Message In phase in the FIFO.

Operation: After shifting to the Status phase and transferring one byte of the FIFO data, operation shifts to the Message In phase and the FIFO data is transferred. Then, operation shifts to the command phase, the CDB is received, a FUNCCMPL interrupt is generated and the command is completed.

Interrupt: FUNCCMPL Function complete (INTSTS2 register (72h), bit 7)

Microcode status:

The microcode status value when the command is completed has the following meanings.

Code	Description
00h	Completed normally.
01h	The ATN condition was established while executing the Status phase.
02h	The ATN condition was established while executing the Message In phase.
03h	Operation shifted to the command phase after completing terminate I/O processing.

2-5. Category 11 Commands

These commands are stream commands, and can be executed anytime as long as a different command is not currently being executed.

Terminology

1) Completed
   Completed has the following meaning with stream processing.
   Streams being executed cannot be reopened when they are completed.
   Streams are completed when processing finishes normally. Streams can also be completed when they are in interrupted state.
2) Interrupted
   Interrupted has the following meaning with stream processing.
   Streams are interrupted if the ATN condition is established, Reselection fails, or the CXD1804AR responds to a selection while executing the stream. Streams being executed can be reopened when they are in interrupted state.

2-5-1. Stream abort

Description: Stream processing is forcibly completed.

Preparation: Before this command is issued, any one of the following conditions must be met.

a) The stream is interrupted by the ATN condition.
b) The stream is interrupted because Reselection failed.
c) The stream is interrupted because the CXD1804AR responded to a selection.
d) The stream is interrupted after executing the stream pause command.

Operation: After internally resetting the stream related circuits, a FUNCCMPL interrupt is generated and the command is completed.

Interrupt: FUNCCMPL Function complete (INTSTS2 register (72h), bit 7)

Microcode status:

The microcode status has no meaning with this command.

2-5-2. Stream and stop (C1h)

Description: The stream command is executed.

Preparation: A number of operations must be performed before issuing this command.

1) Specify the CXD1804AR operation with the SCCONF0 (60h), SCCONF1 (61h) and SCCONF2 (62h) registers.
2) Specify Disconnect allowed/not allowed and the operation when the ATN condition is established with the SCSTCONF register.
3) Write the message to be transferred in the Message In phase immediately after Reselection, and the data to be transferred in the status and Message In phases of the terminate I/O sequence beforehand in the SCSTRSLM, SCSTTIOS and SCSTTIOM registers, respectively.
4) Prepare for auto transfer on the decoder block side.

Operation: When Disconnect is allowed, the following sequences are executed.

a) The following sequence is executed each time the buffer data reaches the buffer full ratio during transfer.
Reselection → Message In → Data In → Message In → Disconnect
b) The following sequence is executed only during the final connection.
Reselection → Message In → Data In

When Disconnect is not allowed, the following sequence is executed.

a) Data In

Interrupt: FUNCCMPL Function complete (INTSTS2 register (72h), bit 7)

Microcode status:

The microcode status value when the command is completed has the following meanings.

Code	Description
00h	Completed normally.
01h	The CXD1804AR was selected and an error occurred in the Message In phase.
02h	The CXD1804AR was selected and operation shifted to the command phase.
03h	Reselection failed.
04h	The ATN condition was established in the Message In phase immediately after Reselection.
05h	The ATN condition was established in the Data In phase.
06h	The ATN condition was established in the Message In phase during Disconnect.
07h	The ATN condition was established in the Status phase during terminate I/O.
08h	The ATN condition was established in the Message In phase during terminate I/O.

The meaning of each code after the stream pause command (C4h) has been issued is basically the same. However, the meaning of the following codes changes slightly.

Code	Description
00h	Completed normally. However, the stream is interrupted.
04h	The ATN condition was established in the Message In phase immediately after Reselection. When the ATN condition is not established, the data to be transferred has already been transferred and the stream is interrupted.
05h	The ATN condition was established in the Data In phase. When the ATN condition is not established, the data to be transferred has already been transferred and the stream is interrupted.

2-5-3. Stream and Bus-Free (C2h)

Description: The stream command is executed.

Preparation: A number of operations must be performed before issuing this command.

1) Specify the CXD1804AR operation with the SCCONF0 (60h), SCCONF1 (61h) and SCCONF2 (62h) registers.
2) Specify Disconnect allowed/not allowed and the operation when the ATN condition is established with the SCSTCONF register.
3) Write the message to be transferred in the Message In phase immediately after Reselection, and the data to be transferred in the status and Message In phases of the terminate I/O sequence beforehand in the SCSTRSLM, SCSTTIOS and SCSTTIOM registers, respectively.
4) Prepare for auto transfer on the decoder block side.

Operation: When Disconnect is allowed, the following sequences are executed.

a) The following sequence is executed each time the buffer data reaches the buffer full ratio during transfer.
   Reselection → Message In → Data In → Message In → Disconnect
b) The following sequence is executed only during the final connection.
   Reselection → Message In → Data In → Status → Message In → Bus-Free

When Disconnect is not allowed, the following sequence is executed.

a) Data In → Status → Message In → Bus-Free

Interrupt: FUNCCMPL Function complete (INTSTS2 register (72h), bit 7)

Microcode status:

The microcode status value when the command is completed has the following meanings.

Code	Description
00h	Completed normally.
01h	The CXD1804AR was selected and an error occurred in the Message In phase.
02h	The CXD1804AR was selected and operation shifted to the command phase.
03h	Reselection failed.
04h	The ATN condition was established in the Message In phase immediately after Reselection.
05h	The ATN condition was established in the Data In phase.
06h	The ATN condition was established in the Message In phase during Disconnect.
07h	The ATN condition was established in the Status phase during terminate I/O.
08h	The ATN condition was established in the Message In phase during terminate I/O.

The meaning of each code after the stream pause command (C4h) has been issued is basically the same. However, the meaning of the following codes changes slightly.

Code	Description
00h	Completed normally. However, the stream is interrupted.
04h	The ATN condition was established in the Message In phase immediately after Reselection. When the ATN condition is not established, the data to be transferred has already been transferred and the stream is interrupted.
05h	The ATN condition was established in the Data In phase. When the ATN condition is not established, the data to be transferred has already been transferred and the stream is interrupted.

2-5-4. Stream and link (C3h)

Description: The stream command is executed.

Preparation: A number of operations must be performed before issuing this command.

1) Specify the CXD1804AR operation with the SCCONF0 (60h), SCCONF1 (61h) and SCCONF2 (62h) registers.
2) Specify Disconnect allowed/not allowed and the operation when the ATN condition is established with the SCSTCONF register.
3) Write the message to be transferred in the Message In phase immediately after Reselection, and the data to be transferred in the status and Message In phases of the terminate I/O sequence beforehand in the SCSTRSLM, SCSTTIOS and SCSTTIOM registers, respectively.
4) Prepare for auto transfer on the decoder block side.

Operation: The following sequences are executed.

a) The following sequence is executed each time the buffer data reaches the buffer full ratio during transfer.
Reselection → Message In → Data In → Message In → Disconnect

b) The following sequence is executed only during the final connection.
Reselection → Message In → Data In → Status → Message In → Command

When Disconnect is not allowed, the following sequence is executed.

a) Data In → Status → Message In → Command

Interrupt: FUNCCMPL Function complete (INTSTS2 register (72h), bit 7)

Microcode status:

The microcode status value when the command is completed has the following meanings.

Code	Description
00h	Completed normally.
01h	The CXD1804AR was selected and an error occurred in the Message In phase.
02h	The CXD1804AR was selected and operation shifted to the command phase.
03h	Reselection failed.
04h	The ATN condition was established in the Message In phase immediately after Reselection.
05h	The ATN condition was established in the Data In phase.
06h	The ATN condition was established in the Message In phase during Disconnect.
07h	The ATN condition was established in the Status phase during terminate I/O.
08h	The ATN condition was established in the Message In phase during terminate I/O.
09h	Operation shifted to the command phase after executing terminate I/O processing.

The meaning of each code after the stream pause command (C4h) has been issued is basically the same. However, the meaning of the following codes changes slightly.

Code	Description
04h	The ATN condition was established in the Message In phase immediately after Reselection. When the ATN condition is not established, the data to be transferred has already been transferred and the stream is interrupted.
05h	ATN condition was established in the Data In phase. When the ATN condition is not established, the data to be transferred has already been transferred and the stream is interrupted.
09h	Operation shifted to the command phase after executing terminate I/O processing. However, the stream is interrupted.

2-5-5. Stream pause (C4h)

Description: The stream command is interrupted.

This command is executed when the stream is to be interrupted for any reason other than SCSI related factor. For example, upon seek error.

Preparation: This command can be issued anytime while executing the stream command.

Operation: Operation switches to a mode which transfers all transferable data. An interrupt is not generated. After all transferable data has been transferred, the stream command being executed generates a FUNCCMPL interrupt and the command is completed.

Stream commands being executed when the stream pause command is issued perform the following operations.

a) When the stream pause command is issued while executing the Data In phase:

After all transferable data has been transferred, a FUNCCMPL interrupt is generated and the command is completed.

b) When the stream pause command is issued in the Bus-Free condition:

Reselection and the Message In phase are executed regardless of the values of BFFLRT and BFBLKC. If there is transferable data, the Data In phase is executed, a FUNCCMPL interrupt is generated and the command is completed.

The ATN condition following the issue of the stream pause command is processed normally.

Interrupt: An interrupt is not generated for this command.

After this command is issued, an interrupt is generated for stream commands which are being executed at that point when these streams are interrupted or completed. See the description of each command for details.

Microcode status:

The microcode status conforms to the stream commands being executed when the stream pause command is issued.

[3] Appendix A

3-1. List of CD-ROM Decoder Block Registers

3-1-1. CD-ROM decoder block read registers

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
00h	b7	b6	b5	b4	b3	b2	b1	b0	RAWMIN
01h	b7	b6	b5	b4	b3	b2	b1	b0	RAWSEC
02h	b7	b6	b5	b4	b3	b2	b1	b0	RAWBLK
03h	b7	b6	b5	b4	b3	b2	b1	b0	RAWMD
04h	b7	b6	b5	b4	b3	b2	b1	b0	BFMIN
05h	b7	b6	b5	b4	b3	b2	b1	b0	BFSEC
06h	b7	b6	b5	b4	b3	b2	b1	b0	BFHDRBLK
07h	b7	b6	b5	b4	b3	b2	b1	b0	BFMD
08h	b7	b6	b5	b4	b3	b2	b1	b0	BFFILE
09h	b7	b6	b5	b4	b3	b2	b1	b0	BFCHAN
0Ah	b7	b6	b5	b4	b3	b2	b1	b0	BFSUBM
0Bh	b7	b6	b5	b4	b3	b2	b1	b0	BFDTYP
0Ch	MIN UTE	SEC OND	BLO CK	MODE				CDR DTEN	RAWHDR FLG
0Dh	MIN UTE	SEC OND	BLO CK	MODE	FILE	CHAN NEL	SUB MODE	DATA TYPE	BFHDR FLG
0Eh	SHRT SCT	NO SYNC	COR INH	ERIN BLK	COR DONE	EDC NG	ECC NG	TGTN TMET	DECSTS 0
0Fh						EDC ALL0	C MODE	C FORM	DECSTS 1
10h								b8	LSTARA-H
11h	b7	b6	b5	b4	b3	b2	b1	b0	LSTARA-L
12h								b8	LHADR-H
13h	b7	b6	b5	b4	b3	b2	b1	b0	LHADR-L
14h	1024 XFR	512 XFR	SYNC	HEAD ER	SBHE ADER	USER DATA	PARI TY	AUTO XFR	XFRFMT 0
15h	ENBL KEFL	BLKE FLSL	ENBY TFBT	BYTE FLSL	ENSB CBT	ALL SBC	SBCE STS	ZA SQEF	XFRFMT 1
16h	AUTO DIST	MODE SEL	FORM SEL		ENFM 2EDC	MDBY TCTL	EN DLA	ATDL RNEW	DECCTL 0
17h	ENSB QRD		DEC CMD2	DEC CMD1	DEC CMD0	NTCR CT2	NTCR CT1	NTCR CT0	DECCTL 1
18h	REV# 2	REV# 1	REV# 0		CMDO BUSY		CBFW RRDY	CBFR DRDY	XFRSTS
19h	b7	b6	b5	b4	b3	b2	b1	b0	CPUBRDT

Sub CPU read registers (1)

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
1Ah	SUBQ FMSL					MODE 2	FORM 2	XFR SCT	SCTINF
1Bh	SBC OVRN	OVER FLOW	BFNT VAL	NO SYNC	SBC ERR3	SBC ERR2	SBC ERR1	SBC ERR0	SBCSTS
1Ch	SBQ ERR					SHTS BCS	NOSY NC	SUBQ ERR	SBQSTS
1Dh						INCB LKS2	INCB LKS1	INCB LKS0	INC BLKS
1Eh	b7	b6	b5	b4	b3	b2	b1	b0	SBQDT
1Fh						PACK MODE			CHPCTL 1
20h								b8	BFARA#-H
21h	b7	b6	b5	b4	b3	b2	b1	b0	BFARA#-L
22h								b8	CSCTARA-H
23h	b7	b6	b5	b4	b3	b2	b1	b0	CSCTARA-L
24h								b8	DLARA-H
25h	b7	b6	b5	b4	b3	b2	b1	b0	DLARA-L
26h									
27h	b7	b6	b5	b4	b3	b2	b1	b0	TGTMIN
28h	b7	b6	b5	b4	b3	b2	b1	b0	TGTSEC
29h	b7	b6	b5	b4	b3	b2	b1	b0	TGTBLK
2Ah									
2Bh	b23	b22	b21	b20	b19	b18	b17	b16	XFRCNT-H
2Ch	b15	b14	b13	b12	b11	b10	b9	b8	XFRCNT-M
2Dh	b7	b6	b5	b4	b3	b2	b1	b0	XFRCNT-L
2Eh								b8	XFRARA-H
2Fh	b7	b6	b5	b4	b3	b2	b1	b0	XFRARA-L
30h									
31h							XFR POS1	XFR POS0	XFRPOS
32h									
33h					b19	b18	b17	b16	HXFRC-H
34h	b15	b14	b13	b12	b11	b10	b9	b8	HXFRC-M
35h	b7	b6	b5	b4	b3	b2	b1	b0	HXFRC-L
36h									
37h					b19	b18	b17	b16	HADRC-H
38h	b15	b14	b13	b12	b11	b10	b9	b8	HADRC-M
39h	b7	b6	b5	b4	b3	b2	b1	b0	HADRC-L
3Ah									

Sub CPU read registers (2)

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
3Bh					b19	b18	b17	b16	SLADR-H
3Ch	b15	b14	b13	b12	b11	b10	b9	b8	SLADR-M
3Dh	b7	b6	b5	b4	b3	b2	b1	b0	SLADR-L
3Eh									
3Fh					b19	b18	b17	b16	CWADRC-H
40h	b15	b14	b13	b12	b11	b10	b9	b8	CWADRC-M
41h	b7	b6	b5	b4	b3	b2	b1	b0	CWADRC-L
42h									
43h					b19	b18	b17	b16	CRADRC-H
44h	b15	b14	b13	b12	b11	b10	b9	b8	CRADRC-M
45h	b7	b6	b5	b4	b3	b2	b1	b0	CRADRC-L
46h							b9	b8	BFBLKC-H
47h	b7	b6	b5	b4	b3	b2	b1	b0	BFBLKC-L
48h							b9	b8	BFFLRT-H
49h	b7	b6	b5	b4	b3	b2	b1	b0	BFFLRT-L
4Ah	b15	b14	b13	b12	b11	b10	b9	b8	TIMER-H
4Bh	b7	b6	b5	b4	b3	b2	b1	b0	TIMER-L
4Ch	b7	b6	b5	b4	b3	b2	b1	b0	TMRRSL
4Dh								b8	STARTARA-H
4Eh	b7	b6	b5	b4	b3	b2	b1	b0	STARTARA-L

Sub CPU read registers (3)

3-1-2. CD-ROM decoder block write registers

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
00h	CINT POL	RAM SIZE1	RAM SIZE0	RAM8 BITW	RAM 2CAS	EXCK SEL	CLK SEL1	CLK SEL0	CONFIG0
01h	SW OPEN	SYC NGC2	SYC NGC1	SYC NGC0	HWKR QDIS	"L"	SBC ECC1	SBC ECC0	CONFIG1
02h	C2PO L1st	LCH LOW	BCH RED	BCKL MD1	BCKL MD0	LSB 1st	"L"	BFSH DFSL	DSPIF
03h	b7	b6	b5	b4	b3	b2	b1	b0	RFINTVL
04h	DSTB SL1	DSTB SL0	DIS XLAT	XFR BYT1	XFR BYT0	"L"	SBAI TMSL	FAST EXCK	DSPCTL
05h	b7	b6	b5	b4	b3	b2	b1	b0	DSPCMD
06h	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"	
07h	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"	
08h	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"	
09h	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"	
0Ah	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"	
0Bh	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"	
0Ch	"L"	"L"	"L"	"L"	"L"	"L"	"L"	CDR DTEN	CDRMOD
0Dh	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"	
0Eh	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"	
0Fh	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"	
10h	"L"	"L"	"L"	"L"	"L"	"L"	"L"	b8	LSTARA-H
11h	b7	b6	b5	b4	b3	b2	b1	b0	LSTARA-L
12h	"L"	"L"	"L"	"L"	"L"	"L"	"L"	b8	LHADR-H
13h	b7	b6	b5	b4	b3	b2	b1	b0	LHADR-L
14h	1024 XFR	512 XFR	SYNC	HEAD ER	SBHE ADER	USER DATA	PARI TY	AUTO XFR	XFRFMT 0
15h	ENBL KEFL	BLKE FLSL	ENBY TFBT	BYTE FLSL	ENSB CBT	ALL SBC	SBCE STS	ZA SQEF	XFRFMT 1
16h	AUTO DIST	MODE SEL	FORM SEL	"L"	ENFM 2EDC	MDBY TCTL	EN DLA	ATDL RNEW	DECCTL 0
17h	ENSB QRD	"L"	SEC CMD2	DEC CMD1	DEC CMD0	NTCR CT2	NTCR CT1	NTCR CT0	DECCTL 1
18h	CHIP RST	TGT MET	INC TGT	RPCO RTRG	"L"	CLDS PCMD	DSPC MDXF	DSPC MDLT	CHPCTL 0
19h	b7	b6	b5	b4	b3	b2	b1	b0	CPUBWDT
1Ah	SUB FMSL	"L"	"L"	"L"	"L"	MODE 2	FORM 2	XFR SCT	SCTINF
1Bh	b7	b6	b5	b4	b3	b2	b1	b0	BLKESTS
1Ch	b7	b6	b5	b4	b3	b2	b1	b0	SBCESTS

Sub CPU write registers (1)

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
1Dh	"L"	"L"	"L"	"L"	"L"	INCB LKS2	INCB LKS1	INCB LKS0	INC BLKS
1Eh	b7	b6	b5	b4	b3	b2	b1	b0	BYTERSTS
1Fh	"L"	"L"	"L"	"L"	"L"	PACK MODE	"L"	"L"	CHPCTL 1
20h	"L"	"L"	"L"	"L"	"L"	"L"	"L"	b8	BFARA#-H
21h	b7	b6	b5	b4	b3	b2	b1	b0	BFARA#-L
22h	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"	
23h	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"	
24h	"L"	"L"	"L"	"L"	"L"	"L"	"L"	b8	DLARA-H
25h	b7	b6	b5	b4	b3	b2	b1	b0	DLARA-L
26h	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"	
27h	b7	b6	b5	b4	b3	b2	b1	b0	TGTMIN
28h	b7	b6	b5	b4	b3	b2	b1	b0	TGTSEC
29h	b7	b6	b5	b4	b3	b2	b1	b0	TGTBLK
2Ah	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"	
2Bh	b23	b22	b21	b20	b19	b18	b17	b16	XFRCNT-H
2Ch	b15	b14	b13	b12	b11	b10	b9	b8	XFRCNT-M
2Dh	b7	b6	b5	b4	b3	b2	b1	b0	XFRCNT-L
2Eh	"L"	"L"	"L"	"L"	"L"	"L"	"L"	b8	XFRARA-H
2Fh	b7	b6	b5	b4	b3	b2	b1	b0	XFRARA-L
30h	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"	
31h	"L"	"L"	"L"	"L"	"L"	"L"	XFR POS1	XFR POS0	XFRPOS
32h	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"	
33h	"L"	"L"	"L"	"L"	b19	b18	b17	b16	HXFRC-H
34h	b15	b14	b13	b12	b11	b10	b9	b8	HXFRC-M
35h	b7	b6	b5	b4	b3	b2	b1	b0	HXFRC-L
36h	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"	
37h	"L"	"L"	"L"	"L"	b19	b18	b17	b16	HADRC-H
38h	b15	b14	b13	b12	b11	b10	b9	b8	HADRC-M
39h	b7	b6	b5	b4	b3	b2	b1	b0	HADRC-L
3Ah	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"	
3Bh	"L"	"L"	"L"	"L"	b19	b18	b17	b16	SLADR-H
3Ch	b15	b14	b13	b12	b11	b10	b9	b8	SLADR-M
3Dh	b7	b6	b5	b4	b3	b2	b1	b0	SLADR-L
3Eh	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"	
3Fh	"L"	"L"	"L"	"L"	b19	b18	b17	b16	CWADRC-H

Sub CPU write registers (2)

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
40h	b15	b14	b13	b12	b11	b10	b9	b8	CWADRC-M
41h	b7	b6	b5	b4	b3	b2	b1	b0	CWADRC-L
42h	"L"	"L"	"L"	"L"	"L"	"L"	"L"	"L"	
43h	"L"	"L"	"L"	"L"	b19	b18	b17	b16	CRADRC-H
44h	b15	b14	b13	b12	b11	b10	b9	b8	CRADRC-M
45h	b7	b6	b5	b4	b3	b2	b1	b0	CRADRC-L
46h	"L"	"L"	"L"	"L"	"L"	"L"	b9	b8	BFBLKC-H
47h	b7	b6	b5	b4	b3	b2	b1	b0	BFBLKC-L
48h	"L"	"L"	"L"	"L"	"L"	"L"	b9	b8	BFFLRT-H
49h	b7	b6	b5	b4	b3	b2	b1	b0	BFFLRT-L
4Ah	b15	b14	b13	b12	b11	b10	b9	b8	TIMER-H
4Bh	b7	b6	b5	b4	b3	b2	b1	b0	TIMER-L
4Ch	b7	b6	b5	b4	b3	b2	b1	b0	TMRRSL

Sub CPU write registers (3)

3-2. List of SCSI Controller Block Registers

3-2-1. SCSI controller block read registers

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
50h	MON RST	MON DBP			TAPE MODE	TBC ZERO		CMDI NPRG	SCSTS
51h									Reserved
52h									Reserved
53h									Reserved
54h	MON BSY	MON SEL	MON MSG	MON CD	MON IO	MON REQ	MON ACK	MON ATN	SCSCBMON
55h	FIFE MPTY			FIF FULL	FIF CNT3	FIF CNT2	FIF CNT1	FIF CNT0	SCFIF STS
56h									Reserved
57h	B07	B06	B05	B04	B03	B02	B01	B00	SCDATA
58h	"L"	"L"	"L"	B04	B03	B02	B01	B00	SCSXFRC
59h									Reserved
5Ah									Reserved
5Bh	SYXF RPD3	SYXF RPD2	SYXF RPD1	SYXF RPD0	SYXF ROF3	SYXF ROF2	SYXF ROF1	SYXF ROF0	SCSYNCTL
5Ch									Reserved
5Dh									Reserved
5Eh	CTL BSY	CTL SEL	CTL MSG	CTL CD	CTL IO	CTL REQ	CTL ACK	CTL ATN	SCSCBCTL
5Fh									Reserved

List of SCSI2 controller block read registers (1)

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
60h			CDBS IZDF	ANEG DATA	ANEG RQAK				SCCONF0
61h	FAST SCSI	HSXF RSPE	HSXF RAT	HSL SPE	RSL RTC3	RSL RTC2	RSL RTC1	RSL RTC0	SCCONF1
62h							IDAS SIGN	IDUN ASGN	SCCONF2
63h	RSLT OUT7	RSLT OUT6	RSLT OUT5	RSLT OUT4	RSLT OUT3	RSLT OUT2	RSLT OUT1	RSLT OUT0	SCRSLTOT
64h									Reserved
65h	SEL ID2	SEL ID1	SEL ID0	SELI DINV		OWN ID2	OWN ID1	OWN ID0	SCID
66h									Reserved
67h									Reserved
68h									Reserved
69h	GP7 B1	GP7 B0	GP6 B1	GP6 B0	GP4 B1	GP4 B0	GP3 B1	GP3 B0	SCCDBSIZ CDBSIZDF = 0
69h	GP7 B1	GP7 B0	GP6D B1	GP6D B0	GP6C B1	GP6C B0	GP43 B1	GP43 B0	SCCDBSIZ CDBSIZDF = 1
6Ah	USTS B7	USTS B6	USTS B5	USTS B4	USTS B3	USTS B2	USTS B1	USTS B0	SC USTS
6Bh						STDS CPRV			SCSTCONF
6Ch	RSLM SG7	RSLM SG6	RSLM SG5	RSLM SG4	RSLM SG3	RSLM SG2	RSLM SG1	RSLM SG0	SCSTRSLM
6Dh	TIOS TS7	TIOS TS6	TIOS TS5	TIOS TS4	TIOS TS3	TIOS TS2	TIOS TS1	TIOS TS0	SCSTTIOS
6Eh	TIOM SG7	TIOM SG6	TIOM SG5	TIOM SG4	TIOM SG3	TIOM SG2	TIOM SG1	TIOM SG0	SCSTTIOM
6Fh									Reserved

List of SCSI2 controller block read registers (2)

3-2-2. SCSI controller block write registers

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
50h	CAT1	CAT0	B05	B04	B03	B02	B01	B00	SCCMD
51h									Reserved
52h									Reserved
53h									Reserved
54h									Reserved
55h									Reserved
56h									Reserved
57h	B07	B06	B05	B04	B03	B02	B01	B00	SCDATA
58h	B07	B06	B05	B04	B03	B02	B01	B00	SCSXFRC
59h									Reserved
5Ah									Reserved
5Bh	SYXF RPD3	SYXF RPD2	SYXF RPD1	SYXF RPD0	SYXF ROF3	SYXF ROF2	SYXF ROF1	SYXF ROF0	SCSYNCTL
5Ch									Reserved
5Dh									Reserved
5Eh	CTL BSY	CTL SEL	CTL MSG	CTL CD	CTL IO	CTL REQ	CTL ACK	CTL ATN	SCSCBCTL
5Fh									Reserved

List of SCSI2 controller block write registers (1)

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
60h			CDBS IZDF	ANEG DATA	ANEG RQAK				SCCONF0
61h	FAST SCSI	HSXF RSPE	HSXF RAT	SPAR ENB	RSL RTC3	RSL RTC2	RSL RTC1	RSL RTC0	SCCONF1
62h							IDAS SIGN	IDUN ASGN	SCCONF2
63h	RSLT OUT7	RSLT OUT6	RSLT OUT5	RSLT OUT4	RSLT OUT3	RSLT OUT2	RSLT OUT1	RSLT OUT0	SCRSLTOT
64h									Reserved
65h	SEL ID2	SEL ID1	SEL ID0			OWN ID2	OWN ID1	OWN ID0	SCID
66h									Reserved
67h									Reserved
68h									Reserved
69h	GP7 B1	GP7 B0	GP6 B1	GP6 B0	GP4 B1	GP4 B0	GP3 B1	GP3 B0	SCCDBSIZ CDBSIZDF = 0
69h	GP7 B1	GP7 B0	GP6D B1	GP6D B0	GP6C B1	GP6C B0	GP43 B1	GP43 B0	SCCDBSIZ CDBSIZDF = 1
6Ah									Reserved
6Bh						STDS CPRV			SCSTCONF
6Ch	RSLM SG7	RSLM SG6	RSLM SG5	RSLM SG4	RSLM SG3	RSLM SG2	RSLM SG1	RSLM SG0	SCSTRSLM
6Dh	TIOS TS7	TIOS TS6	TIOS TS5	TIOS TS4	TIOS TS3	TIOS TS2	TIOS TS1	TIOS TS0	SCSTTIOS
6Eh	TIOM SG7	TIOM SG6	TIOM SG5	TIOM SG4	TIOM SG3	TIOM SG2	TIOM SG1	TIOM SG0	SCSTTIOM
6Fh									Reserved

List of SCSI2 controller block write registers (2)

3-3. List of Common Registers

3-3-1. Common read registers

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
70h	DEC INT	DEC TOUT	DRV OVRN	CRST END	CDR INT			SHT SYNC	INTSTS0
71h							TIME R	SUBC SYNC	INTSTS1
72h	FUNC CMPL	CMD IGNR	SCSI RST	ATN COND	SCSI PERR	SLW ATN	SLWO ATN	RSL FAIL	INTSTS2
73h							SCAM INIF	SCAN SL	INTSTS3
74h	DEC INT	DEC TOUT	DRV OVRN	CRCT END	CDR INT			SHT SYNC	INTEN0
75h							TIME R	SUBC SYNC	INTEN1
76h	FUNC CMPL	DIS CNCT	SCSI RST	ATN COND	SCSI PERR	SLW ATN	SLWO ATN	RSL FAIL	INTEN2
77h							SCAN INIF	SCAM SL	INTEN3
78h						SCSI REL	SCTM REL	DEC REL	INTSRC
79h									
7Ah									
7Bh									
7Ch									
7Dh									
7Eh									
7Fh									

3-3-2. Common write registers

Adr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reg.
70h	DEC INT	DEC TOUT	DRV OVRN	CRST END	CDR INT			SHT SYNC	CLRINT0
71h							TIME R	SUBC SYNC	CLRINT1
72h	FUNC CMPL	CMD IGNR	SCSI RST	ATN COND	SCSI PERR	SLW ATN	SLWO ATN	RSL FAIL	CLRINT2
73h							SCAM INIF	SCAN SL	CLRINT3
74h	DEC INT	DEC TOUT	DRV OVRN	CRCT END	CDR INT			SHT SYNC	INTEN0
75h							TIME R	SUBC SYNC	INTEN1
76h	FUNC CMPL	CMD IGNR	SCSI RST	ATN COND	SCSI PERR	SLW ATN	SLWO ATN	RSL FAIL	INTEN2
77h							SCAN INIF	SCAM SL	INTEN3
78h									
79h									
7Ah									
7Bh									
7Ch									
7Dh									
7Eh									
7Fh									

3-4. Register Reset Conditions

XRST: XRST pin
CRST: bit 7 of the CHPCTL0 register (0Dh)
SXRS: SXRS pin
RCMD: Chip reset command

3-4-1. CD-ROM decoder block register reset conditions

(1) Sub CPU write registers

Reg.	Adr.	XRST	CRST	XRES	RCMD	Bit 7	6	5	4	3	2	1	0
CONFIG0	00h	O	O			0	0	0	0	0	0	0	0
CONFIG1	01h	O				0	0	1	0	x	x	0	1
DSPIF	02h	O				0	0	1	0	1	0	x	x
RFINTVL	03h					x	x	x	x	x	x	x	x
DSPCTL	04h	O	O			0	0	0	1	1	x	x	x
DSPCMD	05h	O	O			0	0	0	0	0	0	0	0
LSTARA-H	10h	O	O			x	x	x	x	x	x	x	0
LSTARA-L	11h	O	O			0	0	0	0	0	0	0	0
LHADR-H	12h	O	O			x	x	x	x	x	x	x	0
LHADR-L	13h	O	O			0	0	0	0	0	0	0	0
XFRFMT0	14h	O				0	0	0	0	0	0	0	1
XFRFMT1	15h	O	O			0	0	0	0	0	0	0	0
DECCTL0	16h	O	O			1	0	0	x	0	1	0	1
DECCTL1	17h	O	O			0	0	0	0	0	x	0	0
CHPCTL0	18h	O	O			0	0	0	0	x	0	0	0
CPUBWDT	19h	O	O			0	0	0	0	0	0	0	0
SCTINF	1Ah	O	O			x	x	x	x	x	0	0	0
BLKESTS	1Bh	O	O			0	0	0	0	0	0	0	0
SBCESTS	1Ch	O	O			0	0	0	0	0	0	0	0
INCBLKS	1Dh	O	O			x	x	x	x	x	0	0	1
BYTERSTS	1Eh	O	O			0	0	0	0	0	0	0	0
CHPCTL1	1Fh	O	O			x	x	x	x	x	1	x	x
BFARA-H	20h	O	O			x	x	x	x	x	x	x	0
BFARA-L	21h	O	O			0	0	0	0	0	0	0	0
DLARA-H	24h	O	O			x	x	x	x	x	x	x	0
DLARA-L	25h	O	O			0	0	0	0	0	0	0	0
TGTMIN	27h	O	O			0	0	0	0	0	0	0	0
TGTSEC	28h	O	O			0	0	0	0	0	0	0	0
TGTBLK	29h	O	O			0	0	0	0	0	0	0	0
XFRCNT-H	2Bh	O	O			0	0	0	0	0	0	0	0
XFRCNT-M	2Ch	O	O			0	0	0	0	0	0	0	0

Reg.	Adr.	XRST	CRST	XRES	RCMD	Bit 7	6	5	4	3	2	1	0
XFRCNT-L	2Dh	O	O			0	0	0	0	0	0	0	0
XFRARA-H	2Eh	O	O			x	x	x	x	x	x	x	0
XFRARA-L	2Fh	O	O			0	0	0	0	0	0	0	0
XFRPOS	31h	O	O			x	x	x	x	x	x	0	0
HXFRC-H	33h	O	O			x	x	x	x	0	0	0	0
HXFRC-M	34h	O	O			0	0	0	0	0	0	0	0
HXFRC-L	35h	O	O			0	0	0	0	0	0	0	0
HADRC-H	37h	O	O			x	x	x	x	0	0	0	0
HADRC-M	38h	O	O			0	0	0	0	0	0	0	0
HADRC-L	39h	O	O			0	0	0	0	0	0	0	0
SLADR-H	3Bh	O	O			x	x	x	x	0	0	0	0
SLADR-M	3Ch	O	O			0	0	0	0	0	0	0	0
SLADR-L	3Dh	O	O			0	0	0	0	0	0	0	0
CWADRC-H	3Fh	O	O			x	x	x	x	0	0	0	0
CWADRC-M	40h	O	O			0	0	0	0	0	0	0	0
CWADRC-L	41h	O	O			0	0	0	0	0	0	0	0
CRADRC-H	43h	O	O			x	x	x	x	0	0	0	0
CRADRC-M	44h	O	O			0	0	0	0	0	0	0	0
CRADRC-L	45h	O	O			0	0	0	0	0	0	0	0
BFBLKC-H	46h	O	O			x	x	x	x	x	x	0	0
BFBLKC-L	47h	O	O			0	0	0	0	0	0	0	0
BFFLRT-H	48h	O	O			x	x	x	x	x	x	0	0
BFFLRT-L	49h	O	O			0	0	0	0	0	0	0	1
TIMER-H	4Ah	O	O			0	0	0	0	0	0	0	0
TIMER-L	4Bh	O	O			0	0	0	0	0	0	0	0
TMRRSL	4Ch	O	O			1	1	1	1	1	0	1	0
CLRINT0	70h	O	O			0	0	0	0	x	x	x	x
CLRINT1	71h	O	O			x	x	x	x	x	x	0	0
INTEN0	74h	O	O			0	0	0	0	x	x	x	x
INTEN1	75h	O	O			x	x	x	x	x	x	0	0

(2) Sub CPU read registers

Reg.	Adr.	XRST	CRST	XRES	RCMD	Bit 7	6	5	4	3	2	1	0
RAWMIN	00h	O	O			0	0	0	0	0	0	0	0
RAWSEC	01h	O	O			0	0	0	0	0	0	0	0
RAWBLK	02h	O	O			0	0	0	0	0	0	0	0
RAWMD	03h	O	O			0	0	0	0	0	0	0	0
BFMIN	04h	O	O			0	0	0	0	0	0	0	0
BFSEC	05h	O	O			0	0	0	0	0	0	0	0
BFBLK	06h	O	O			0	0	0	0	0	0	0	0
BFMD	07h	O	O			0	0	0	0	0	0	0	0
BFFILE	08h	O	O			0	0	0	0	0	0	0	0
BFCHAN	09h	O	O			0	0	0	0	0	0	0	0
BFSUBM	0AH	O	O			0	0	0	0	0	0	0	0
BFDTYP	0Bh	O	O			0	0	0	0	0	0	0	0
RAWHDRFLG	0Ch	O	O			0	0	0	0	x	x	x	x
BFHDRFLG	0Dh	O	O			0	0	0	0	0	0	0	0
DECSTS0	0Eh	O	O			0	0	0	0	0	0	0	0
DECSTS1	0Fh	O	O			x	x	x	0	0	0	0	0
LSTARA-H	10h	O	O			x	x	x	x	x	x	x	0
LSTARA-L	11h	O	O			0	0	0	0	0	0	0	0
LHADR-H	12h	O	O			x	x	x	x	x	x	x	0
LHADR-L	13h	O	O			0	0	0	0	0	0	0	0
XFRFMT0	14h	O				0	0	0	0	0	0	0	?
			O			0	0	0	0	0	0	0	x
XFRFMT1	15h	O	O			0	0	0	0	0	0	0	0
DECCTL0	16h	O	O			1	0	0	x	0	1	0	1
DECCTL1	17h	O	O			0	0	0	0	0	x	0	0
XFRSTS	18h	O	O			0	0	0	x	0	x	1	0
CPUBRDT	19h					x	x	x	x	x	x	x	x
SCTINF	1Ah	O	O			x	x	x	x	x	0	0	0
SBCSTS	1Bh	O	O			x	x	x	x	x	x	x	x
SBQSTS	1Ch	O	O			x	x	x	x	x	0	0	0
INCBLKS	1Dh	O	O			x	x	x	x	x	0	0	1
SBQDT	1Eh					x	x	x	x	x	x	x	x
CHPCTL1	1Fh	O	O			x	x	x	x	x	1	x	x
BFARA-H	20h	O	O			x	x	x	x	x	x	x	0
BFARA-L	21h	O	O			0	0	0	0	0	0	0	0
CSCTARA-H	22h	O	O			x	x	x	x	x	x	x	0
CSCTARA-L	23h	O	O			0	0	0	0	0	0	0	0

Reg.	Adr.	XRST	CRST	XRES	RCMD	Bit 7	6	5	4	3	2	1	0
DLARA-H	24h	O	O			x	x	x	x	x	x	x	0
DLARA-L	25h	O	O			0	0	0	0	0	0	0	0
TGTMIN	27h	O	O			0	0	0	0	0	0	0	0
TGTSEC	28h	O	O			0	0	0	0	0	0	0	0
TGTBLK	29h	O	O			0	0	0	0	0	0	0	0
XFRCNT-H	2Bh	O	O			0	0	0	0	0	0	0	0
XFRCNT-M	2Ch	O	O			0	0	0	0	0	0	0	0
XFRCNT-L	2Dh	O	O			0	0	0	0	0	0	0	0
XFRARA-H	2Eh	O	O			x	x	x	x	x	x	x	0
XFRARA-L	2Fh	O	O			0	0	0	0	0	0	0	0
XFRPOS	31h	O	O			x	x	x	x	x	x	0	0
HXFRC-H	33h	O	O			x	x	x	x	0	0	0	0
HXFRC-M	34h	O	O			0	0	0	0	0	0	0	0
HXFRC-L	35h	O	O			0	0	0	0	0	0	0	0
HADRC-H	37h	O	O			x	x	x	x	0	0	0	0
HADRC-M	38h	O	O			0	0	0	0	0	0	0	0
HADRC-L	39h	O	O			0	0	0	0	0	0	0	0
SLADR-H	3Bh	O	O			x	x	x	x	0	0	0	0
SLADR-M	3Ch	O	O			0	0	0	0	0	0	0	0
SLADR-L	3Dh	O	O			0	0	0	0	0	0	0	0
CWADRC-H	3Fh	O	O			x	x	x	x	0	0	0	0
CWADRC-M	40h	O	O			0	0	0	0	0	0	0	0
CWADRC-L	41h	O	O			0	0	0	0	0	0	0	0
CRADRC-H	43h	O	O			x	x	x	x	0	0	0	0
CRADRC-M	44h	O	O			0	0	0	0	0	0	0	0
CRADRC-L	45h	O	O			0	0	0	0	0	0	0	0
BFBLKC-H	46h	O	O			x	x	x	x	x	x	0	0
BFBLKC-L	47h	O	O			0	0	0	0	0	0	0	0
BFFLRT-H	48h	O	O			x	x	x	x	x	x	0	0
BFFLRT-L	49h	O	O			0	0	0	0	0	0	0	1
TIMER-H	4Ah	O	O			0	0	0	0	0	0	0	0
TIMER-L	4Bh	O	O			0	0	0	0	0	0	0	0
TMRRSL	4Ch	O	O			1	1	1	1	1	0	1	0
STARTARA-H	4Eh	O	O			x	x	x	x	x	x	x	0
STARTARA-L	4Fh	O	O			0	0	0	0	0	0	0	0
INTSTS0	70h	O	O			0	0	0	0	x	x	x	x
INTSTS1	71h	O	O			x	x	x	x	x	x	0	0
INTEN0	74h	O	O			0	0	0	0	x	x	x	x

Reg.	Adr.	XRST	CRST	XRES	RCMD	Bit 7	6	5	4	3	2	1	0
INTEN1	75h	O	O			x	x	x	x	x	x	0	0
INTSRC	78h	O	O			x	x	x	x	x	x	0	0

3-4-2. SCSI2 control block register reset conditions

(1) Sub CPU write registers

Reg.	Adr.	XRST	CRST	XSRS	RCMD	Bit 7	6	5	4	3	2	1	0
SCSTS	50h	O			O	x	x	x	x	0	1	x	x
SCSCBMON	54h	O			O	x	x	x	x	x	x	x	x
SCFIFSTS	55h	O			O	1	0	0	0	0	0	0	0
SCDATA	57h	O			O	x	x	x	x	x	x	x	x
SCSXFRC	58h	O			O	x	x	x	0	0	0	0	0
SCSYNCTL	5Bh	O			O	0	0	0	0	0	0	0	0
SCSCBCTL	5Eh	O			O	0	0	0	0	0	0	0	0
SCCONF0	60h	O				0	0	0	0	0	0	0	0
SCCOCF1	61h	O			O	x	x	0	0	0	x	x	x
SCCOCF2	62h	O				x	x	x	x	x	x	0	0
SCRSLTOT	63h	O			O	0	0	0	0	0	0	0	0
SCID	65h	O			O	0	0	0	0	x	0	0	0
SCCDBSIZ	69h	O			O	0	0	0	0	0	0	0	0
SCUSTS	6Ah	O		O	O	x	x	x	x	x	x	x	x
SCSTCONF	6Bh	O			O	x	x	x	x	x	0	0	0
SCSTRSLM	6Ch	O			O	0	0	0	0	0	0	0	0
SCSTTIOS	6Dh	O			O	0	0	0	0	0	0	0	0
SCSTTIOM	6Eh	O			O	0	0	0	0	0	0	0	0
INTSTS2	72h	O				0	0	0	0	0	0	0	0
INTSTS3	73h	O				x	x	x	x	x	x	0	0
INTEN2	76h	O			O	0	0	0	0	0	0	0	0
INTEN3	77h	O			O	x	x	x	x	x	x	0	0

(2) Sub CPU read registers

Reg.	Adr.	XRST	CRST	XSRS	RCMD	Bit 7	6	5	4	3	2	1	0
SCCMD	50h	O			O	0	0	0	0	0	0	0	0
SCDATA	57h	O			O	x	x	x	x	x	x	x	x
SCSXFRC	58h	O			O	x	x	x	0	0	0	0	0
SCSYNCTL	5Bh	O			O	x	x	x	x	x	x	x	x
SCSCBCTL	5Eh	O			O	x	x	x	x	x	x	x	x
SCCONF0	60h	O				x	x	0	0	0	x	x	x
SCCONF1	61h	O			O	0	0	0	0	0	0	0	0
SCCONF2	62h	O				x	x	x	x	x	x	0	0
SCRSLTOT	63h	O			O	0	0	0	0	0	0	0	0
SCID	65h	O			O	0	0	0	x	x	0	0	0
SCCDBSIZ	69h	O			O	0	0	0	0	0	0	0	0
SCSTCONF	6Bh	O			O	x	x	x	x	x	0	0	0
SCSTRSLM	6Ch	O			O	0	0	0	0	0	0	0	0
SCSTTIOS	6Dh	O			O	0	0	0	0	0	0	0	0
SCSTTIOM	6Eh	O			O	0	0	0	0	0	0	0	0
CLRINT2	72h	O				0	0	0	0	0	0	0	0
CLRINT3	73h	O				x	x	x	x	x	x	0	0
INTEN2	76h	O			O	0	0	0	0	0	0	0	0
INTEN3	77h	O			O	x	x	x	x	x	x	0	0

[4] Appendix B

4-1. Summary of SCSI Controller Block Commands

CXD1804AR/SCSI2 core block command set

CAT1	CAT0	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0	Description
0	0	0	0	0	0	0	0	NOP
0	0	0	0	0	0	0	1	CHIP Reset
0	0	0	0	0	0	1	1	Flush FIFO
0	0	0	0	0	1	0	0	Assert SCSI Control
0	0	0	0	0	1	0	1	Deasert SCSI Control
0	0	0	0	0	1	1	0	Assert SCSI Data
0	0	0	0	0	1	1	1	Deasert SCSI Data
0	0	0	0	1	0	0	0	Enable Selection
0	0	0	0	1	0	0	1	Disable Selection
CAT1	CAT0	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0	Description
0	1	0	0	0	0	0	0	Reselect and Send Message (s)
0	1	0	0	0	0	0	1	Initiate SCAM
0	1	0	0	0	0	1	0	Reselect, Send Message (s) and Receive Data
0	1	0	0	0	0	1	1	Reselect, Send Message (s) and Send Data
CAT1	CAT0	BUF	SUB	CMD3	CMD2	CMD1	CMD0	Description
1	0	*	*	0	0	0	0	Receive Data
1	0	*	*	0	0	0	1	Send Data
1	0	*	*	0	0	1	0	Reserved
1	0	*	*	0	0	1	1	Reserved
1	0	*	*	0	1	0	0	Reseive Command
1	0	*	*	0	1	0	1	Send Status
1	0	*	*	0	1	1	0	Receive Message
1	0	*	*	0	1	1	1	Send Message
1	0	0	0	1	0	0	0	Disconnect
1	0	0	0	1	0	0	1	Send Message (s) and Disconnect
1	0	0	0	1	0	1	0	Terminate I/O and bus free
1	0	0	0	1	0	1	1	Terminate I/O and link
1	0	0	0	1	1	0	0	Receive Command Sequence
CAT1	CAT0	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0	Description
1	1	0	0	0	0	0	0	Stream Abort
1	1	0	0	0	0	0	1	Stream and Stop
1	1	0	0	0	0	1	0	Stream and Bus Free
1	1	0	0	0	0	1	1	Stream and Link
1	1	0	0	0	1	0	0	Stream Pause

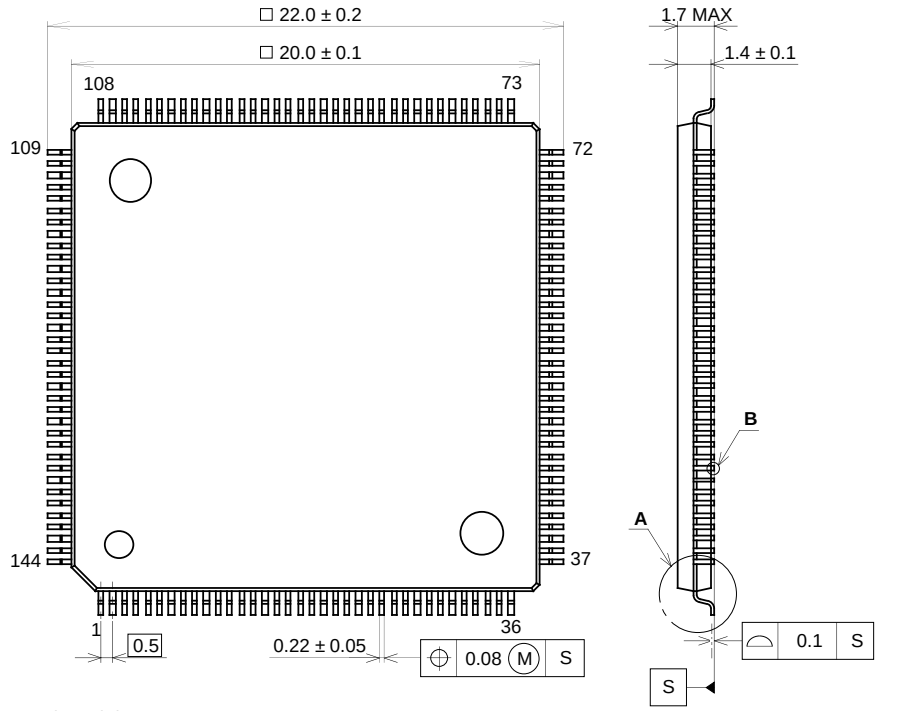
* Either "1" or "0" can be written. However, if the BUF bit is "1", "0" must be written for the SUB bit.

States which allow commands to be executed are limited by category.

CAT1	CAT0	Description
0	0	Can be executed in all states
0	1	Can be executed only in the Disconnect status
1	0	Can be executed only during the target mode
1	1	Stream commands

Package Outline Unit: mm

144PIN LQFP (PLASTIC)



SONY CODE	LQFP-144P-L01
EIAJ CODE	LQFP144-P-2020-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE WEIGHT	1.3 g

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