SONY

CXD1254AR/AQ

CCD Camera Synchronization and Timing Signal Generator

Description

The CXD1254AR and CXD1254AQ Ics generates the necessary synchronization and timing signals for camera systems employing CCD image sensors (ICX044, ICX045, ICX046, etc.).

Features

- Supports color (NTSC) and black & white (EIA/CCIR) systems
- On-chip electronic shutter
- On-chip horizontal (H) driver
- Timing generator for mirror images

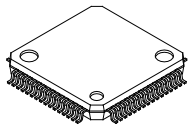
Applications

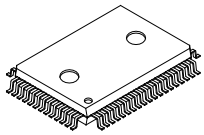
CCD camera systems

Structure

Silicon gate CMOS IC

CXD1254AR	CXD1254AQ
64 pin LQFP (Plastic)	64 pin QFP (Plastic)





Absolute Maximum Ratings (Ta=25 °C, V_{SS}=0 V)

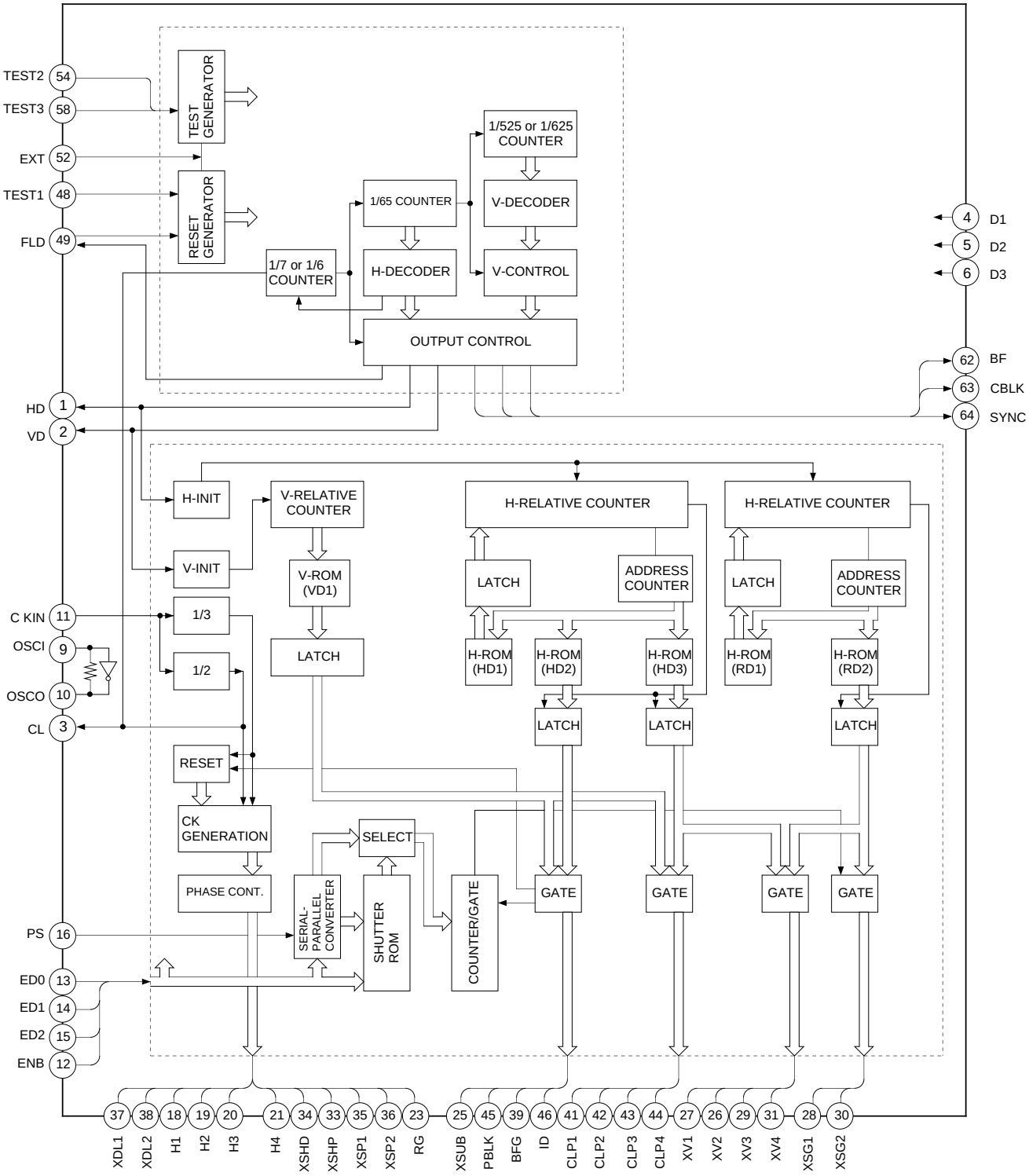
• Supply voltage	V_{SS}	–0.5 to +7.0	V
• Input voltage	V_{SS}	–0.5 to V_{DD} +0.5	V
• Output voltage	V_{SS}	–0.5 to V_{DD} +0.5	V
• Operating temperature		–20 to +75	°C
• Storage temperature		–55 to +150	°C

Recommended Operating Conditions

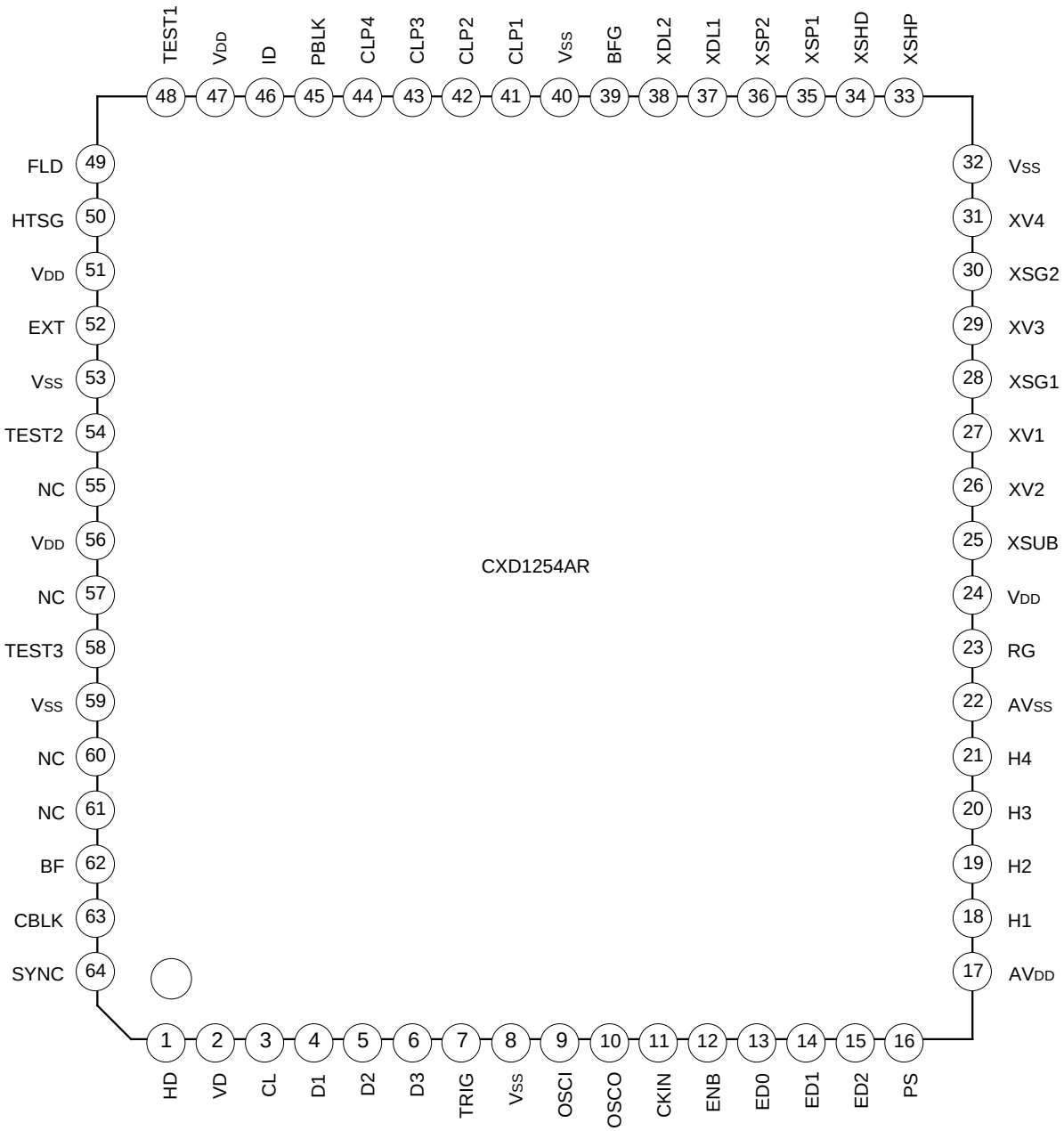
• Supply voltage	4.75 to 5.25	V
• Operating temperature	–20 to +75	°C

E91845B67-TE

Block Diagram (Pin No.s given for CXD1254AR)

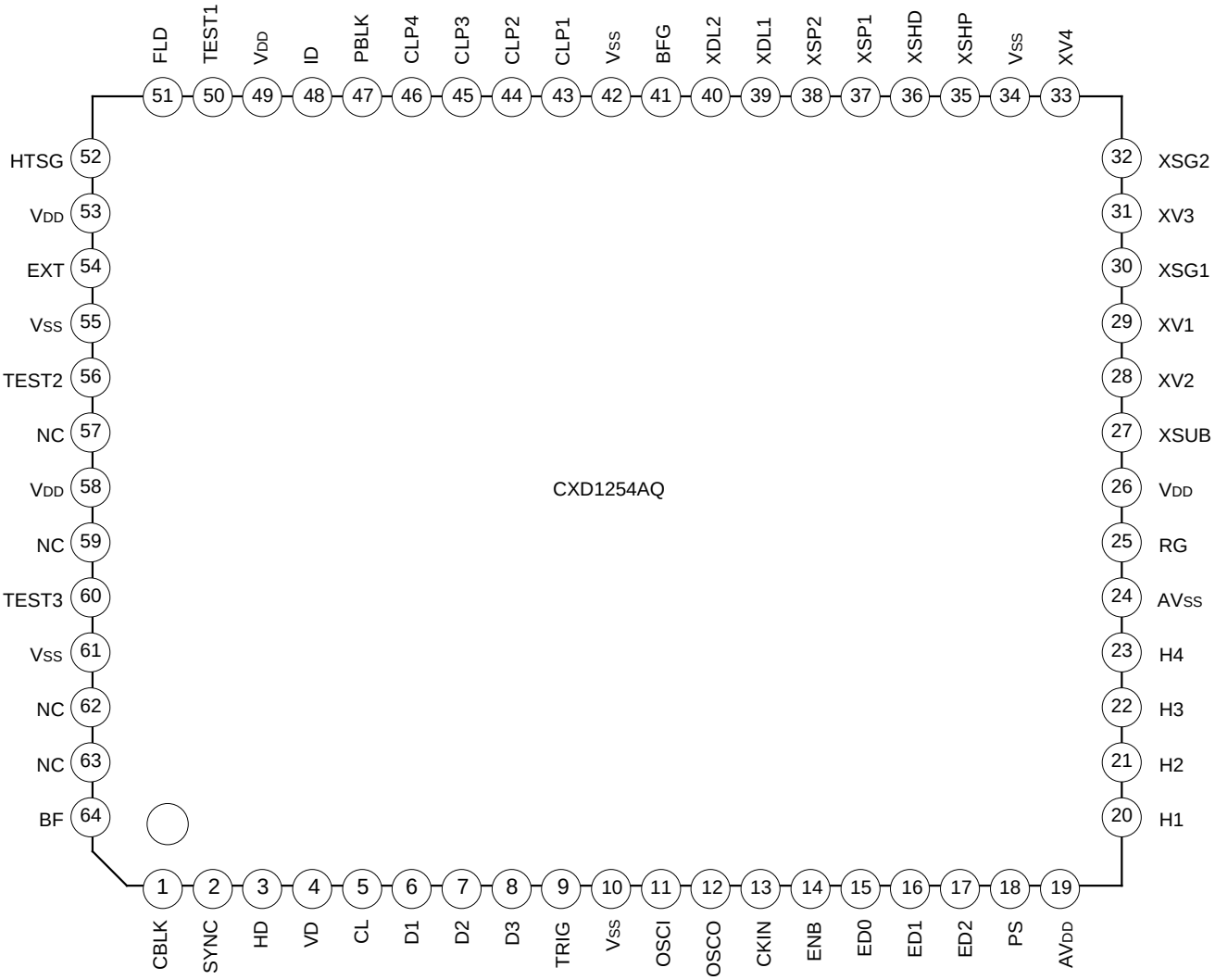


Pin Configuration (1)



Mode	Pin No.	PRESET	Low	High
D1	4	Low	NTSC/EIA	CCIR
D2	5	Low	Normal Image	Mirror Image
D3	6	Low	Color	B/W
ENB	12	High	Normal	Shutter
ED0	13	High	Shutter Speed	
ED1	14	High		
ED2	15	High		
PS	16	High	Serial input	Parallel input
EXT	52	Low	Internal	External
TEST2	54	Low	Normally Low	

Pin Configuration (2)



Mode	Pin No.	PRESET	Low	High
D1	6	Low	NTSC/EIA	CCIR
D2	7	Low	Normal Image	Mirror Image
D3	8	Low	Color	B/W
ENB	14	High	Normal	Shutter
ED0	15	High	Shutter Speed	
ED1	16	High		
ED2	17	High		
PS	18	High	Serial input	Parallel input
EXT	54	Low	Internal	External
TEST2	56	Low	Normally Low	

Pin Description

Pin No.		Pin	I/O	Function
LQFP	QFP			
1	3	HD	O	Horizontal drive pulse output
2	4	VD	O	Vertical drive pulse output
3	5	CL	O	Clock output NTSC/EIA: 14.318 MHz CCIR: 14.1875 MHz
4	6	D1	I	Mode selection "Low": NTSC/EIA "High": CCIR (Pull-down resistor)
5	7	D2	I	Mode selection "Low": Normal "High": Mirror (Pull-down resistor)
6	8	D3	I	Mode selection "Low": Color "High": B/W (Pull-down resistor)
7	9	TRIG	I	Shutter speed setting pulse input (Pull-up resistor)
8	10	V_{SS}	—	GND for signal generator
9	11	OSCI	I	Oscillator input NTSC/EIA: 28.636 MHz CCIR: 28.375 MHz
10	12	OSCO	O	Oscillator output
11	13	CKIN	I	Input for determining oscillator duty cycle
12	14	ENB	I	Shutter selection "Low": Normal "High": Shutter (Pull-up resistor)
13	15	ED0	I	Shutter speed control (Pull-up resistor)
14	16	ED1	I	Shutter speed control (Pull-up resistor)
15	17	ED2	I	Shutter speed control (Pull-up resistor)
16	18	PS	I	Shutter speed setting data format selection "Low": Serial "High": Parallel (Pull-up resistor)
17	19	AV_{DD}	—	Independent power supply for horizontal driver
18	20	H1	O	Clock output for horizontal register driver
19	21	H2	O	Clock output for horizontal register driver (Leave open except for ICX046.)
20	22	H3	O	Clock output for horizontal register driver (Use as H2 except for ICX046.)
21	23	H4	O	Clock output for horizontal register driver (Leave open except for ICX046.)
22	24	AV_{SS}	—	Independent GND for horizontal driver
23	25	RG	O	Reset gate pulse output
24	26	V_{DD}	—	Power supply for timing generator
25	27	XSUB	O	Sensor charge sweep output pulse output
26	28	XV2	O	Clock output for vertical register driver
27	29	XV1	O	Clock output for vertical register driver
28	30	XSG1	O	Sensor charge readout pulse output
29	31	XV3	O	Clock output for vertical register driver
30	32	XSG2	O	Sensor charge readout pulse output
31	33	XV4	O	Clock output for vertical register driver
32	34	V_{SS}	O	GND for timing generator
33	35	XSHP	O	Pre-charge level/sample-and-hold pulse output *1
34	36	XSHD	O	Data sample-and-hold pulse output *1
35	37	XSP1	O	Color separation sample-and-hold pulse output *1
36	38	XSP2	O	Color separation sample-and-hold pulse output *1
37	39	XDL1	O	Pulse output for delay line *1
38	40	XDL2	O	Pulse output for delay line *1
39	41	BFG	O	Burst flag gate pulse output
40	42	V_{SS}	—	GND for timing generator

Pin No.		Pin	I/O	Function
LQFP	QFP			
41	43	CLP1	O	Pulse output for clamp
42	44	CLP2	O	Pulse output for clamp
43	45	CLP3	O	Pulse output for clamp
44	46	CLP4	O	Pulse output for clamp
45	47	PBLK	O	Blanking/cleaning pulse output
46	48	ID	O	Line discrimination pulse output
47	49	V_{DD}	—	Power supply for timing generator
48	50	TEST1	I	Test input/H reset pulse input *2
49	51	FLD	I/O	Field pulse output/V reset pulse input *2
50	52	HTSG	I	XSG1, 2 controller/Test input *2
51	53	V_{DD}	—	Power supply for signal generator
52	54	EXT	I	Synchronization mode selection. "Low": Internal "High": External (Pull-down resistor)
53	55	V_{SS}	—	GND for signal generator
54	56	TEST2	I	Test input (Normally open) (Pull-down resistor)
55	57	NC	—	Used open
56	58	V_{DD}	—	Power supply for signal generator
57	59	NC	—	Used open
58	60	TEST3	I	Test input (Normally fixed at "Low")
59	61	V_{SS}	—	GND for signal generator
60	62	NC	—	Used open
61	63	NC	—	Used open
62	64	BF	O	Burst flag pulse output
63	1	CBLK	O	Composite blanking pulse output
64	2	SYNC	O	Composite synchronization pulse output

(Note) *1…Output determined by mode setting.
*2…Function determined by mode setting.

Outputs for Pins Determined by Mode Setting

*1

Pin	Pin No. (LQFP)	D3 (Pin 6)			
		Low (Color)		High (B/W)	
XSHP	33	O	XSHP (⌐⌐) output	O	SHP (⌐⌐) output
XSHD	34	O	XSHD (⌐⌐) output	O	SHD (⌐⌐) output
XSP1	35	O	XSP1 (⌐⌐) output	O	(Out put stopped)
XSP2	36	O	XSP2 (⌐⌐) output	O	(Out put stopped)
XDL1	37	O	XDL1 output	O	(Out put stopped)
XDL2	38	O	XDL2 output	O	(Out put stopped)

Functions for Pins Determined by Mode Settings

*2

Pin	Pin No. (LQFP)	EXT (Pin 11)			
		Low (Internal)		High (External)	
TEST1	48	I	Test input (Normally low)	I	H reset pulse input
FLD	49	O	FLD output	I	V reset pulse input
HTSG	50	I	XSG1, 2 control input ("Low" : OFF "High" : ON)	I	Test input (Normally low)

Electrical Characteristics

1) DC Characteristics (V_{DD}=5 V ±0.25 V, Topr= –20 to +75 °C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		4.75	5.0	5.25	V
Input voltage	V_{IH1}		0.7 V_{DD}			V
	V_{IL1}				0.3 V_{DD}	V
Output voltage 1	V_{OH1}	I_{OH}=–2 mA	V_{DD}–0.5			V
	V_{OL1}	I_{OL}=4 mA			0.4	V
Output voltage 2 CL, RG, XSHP, XSHD, XSP1, XSP2, XDL1, XDL2	V_{OH2}	I_{OH}=–4 mA	V_{DD}–0.5			V
	V_{OL2}	I_{OL}=8 mA			0.4	V
Output voltage 3 H1, H2, H3, H4	V_{OH3}	I_{OH}=–8 mA	V_{DD}–0.5			V
	V_{OL3}	I_{OL}=8 mA			0.4	V
Output voltage 4 OSC0	V_{OH4}	I_{OH}=–1 mA	V_{DD}/2			V
	V_{OL4}	I_{OL}=1 mA			V_{DD}/2	V
Feedback resistance	R_{FB}	V_{IN}=V_{SS} or V_{DD}	500 k	2 M	5 M	Ω
Pull-up resistor	R_{PU}	V_{IL}=0 V	40 k	100 k	250 k	Ω
Pull-down resistor	R_{PD}	V_{IH}=V_{DD}	40 k	100 k	250 k	Ω

2) Input/Output Capacitance (V_{DD}=V_I=0 V, f_M=1 MHz)

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacitance	C_{IN}			9	pF
Output pin capacitance	C_{OUT}			11	pF
Input/Output pin capacitance	$C_{I/O}$			11	pF

Electronic Shutter Description

Pins for Shutter

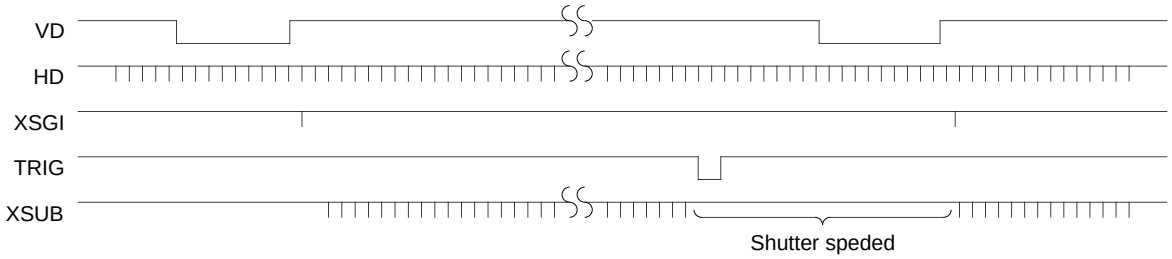
PS, TRIG, ENB	Inputs for overall mode setting
XSUB	Output
ED0, ED1, ED2	Inputs for shutter speed setting

(Note)

- Regardless of shutter speed setting controlled by PS, ED0 to ED2, and TRIG, if ENB is “Low”, the shutter will be OFF.
- The speed set by PS and ED0 to ED2 is subject to control by TRIG.

Mode Description

1. TRIG (Pull-up resistor)
   - For normal shutter operation, TRIG should be either left Open or set at High.
   - For continuous variable shutter operation, input a clock pulse to TRIG.



By taking out XSUB pulses between downward pulses of XSG1 and TRIG, and thus stopping XSUB pulses from the downward pulse of TRIG to the following downward pulse of XSG1, the shutter speed is determined.

In order to increase the range of control when the TRIG pin is used to control the shutter speed, Pins ED0 to ED2 (described in next section) must be pre-set to 1/10000 sec. (Described in later section.)

2. ED0, ED1, and ED2 (Shutter speed control)
   PS (Selects between parallel/serial input)
   ENB (Shutter mode selection)

2-1. PS

Selects either parallel or serial input data format to be used for determining shutter speed.

- Parallel input — Combination of the 3 bits, ED0, ED1, ED2, yields 8 possible shutter speed settings.
- Serial input — Shutter speed is determined by inputting ED0 (strobe), and ED1 (clock), and ED2 (data) to respective pins.

2-1-1. [Parallel input] (PS = H) — For high speed shutter only

Table of Shutter Settings

D1	ENB	ED0	ED1	ED2	Shutter speed
X	L	X	X	X	Shutter OFF
L	H	H	H	H	1/60 (s)
H	H	H	H	H	1/50 (s)
L	H	L	H	H	1/100 (s)
H	H	L	H	H	1/120 (s)
X	H	H	L	H	1/250 (s)
X	H	L	L	H	1/500 (s)
X	H	H	H	L	1/1000 (s)
X	H	L	H	L	1/2000 (s)
X	H	H	L	L	1/4000 (s)
X	H	L	L	L	1/10000 (s)

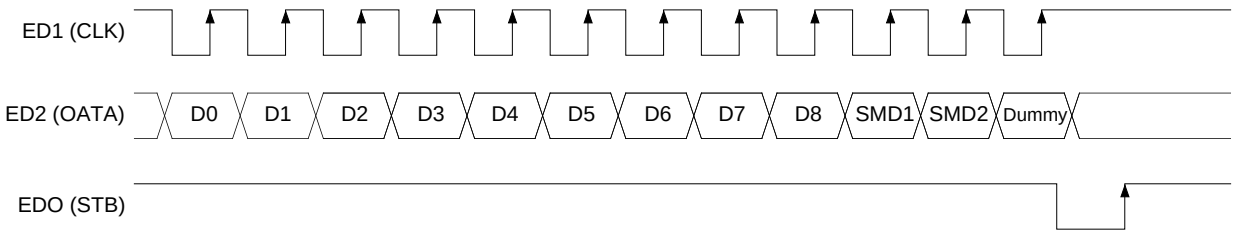
2-1-2. [Serial input] (PS = L)

The combination of serial data SMD1 and SMD2 can be used to select one of four modes.

Shutter Mode

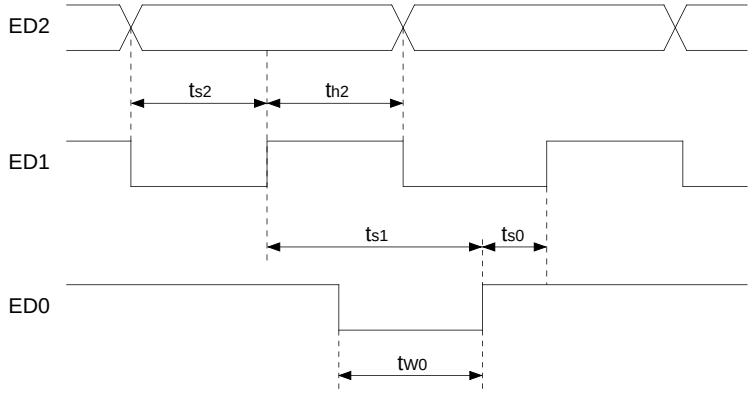
Mode	Flickerless	High-speed shutter	Low-speed shutter	No shutter
SMD1	Low	Low	High	High
SMD2	Low	High	Low	High

- Flickerless — Mode for eliminating flicker caused by oscillation frequency of fluorescent lights.
- High-speed shutter — Shutter speed faster than 1/60 sec. (NTSC/EIA) or 1/50 sec. (CCIR).
- Low-speed shutter — Shutter speed slower than 1/60 sec. (NTSC/EIA) or 1/50 sec. (CCIR).
- No shutter — Shutter operation inactive.



ED2 data is latched in the register on the rising edge of ED1 and the register contents are transferred during the low period of ED0.

AC Characteristics



Symbol		Min.	Max.
t_{s2}	ED2 set-up time referenced from the ED1 rising edge	20 ns	—
t_{h2}	ED2 hold-time referenced from the ED1 rising edge	20 ns	—
t_{s2}	ED1 rise set-up time referenced from the ED0 rising edge	20 ns	—
t_{w0}	ED0 pulse width	20 ns	50 µs
t_{s0}	ED0 rise set-up time referenced from the ED1 rising edge	20 ns	—

2-1-3. [Shutter speed calculation formula]

High-speed Shutter

• For NTSC/EIA

$T = [262_{10} - (1FF_{16} - L_{16})] \times 63.56 + 34.78$ µs • L_{16}: Load value

• For CCIR

$T = [312_{10} - (1FF_{16} - L16)] \times 64 + 35.6$ µs

NTSC/EIA			CCIR		
Load value	Shutter speed	Calculated value	Load value	Shutter speed	Calculated value
$0FA_{16}$	1/10000	1/10169	$0C8_{16}$	1/10000	1/10040
$0FC_{16}$	1/4000	1/4435	$0CA_{16}$	1/4000	1/4349
100_{16}	1/2000	1/2085	$0CE_{16}$	1/2000	1/2068
108_{16}	1/1000	1/1012	$0D6_{16}$	1/1000	1/1004
118_{16}	1/500	1/499	$0E6_{16}$	1/500	1/495
137_{16}	1/250	1/252	105_{16}	1/250	1/250
176_{16}	1/125	1/125	143_{16}	1/125	1/125
196_{16}	1/100	1/100	149_{16}	1/100	1/120

Low-speed Shutter

$N = 2 \times (1FF_{16} - L_{16})$ FLD

"1FF" cannot be used as a load value.

Load value	Shutter speed (FLD)
$1FE_{16}$	2
$1FD_{16}$	4
:	:
101_{16}	508
100_{16}	510

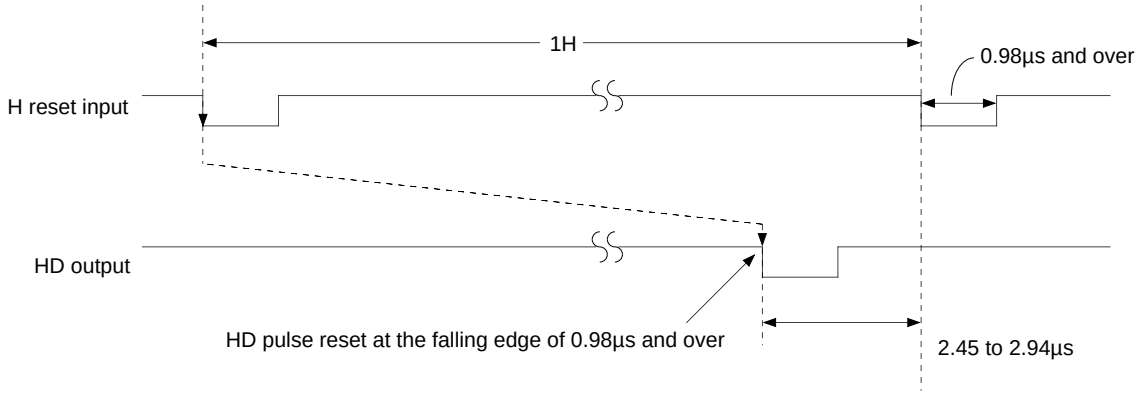
External Synchronization Mode Description

• H Reset

The reset process is started from the first falling edge of the inputted reset pulse. The next reset occurs only when there is a divergence of at least a clock cycles (0.98 µs) from the edge.

The minimum reset pulse width is 0.98 µs.

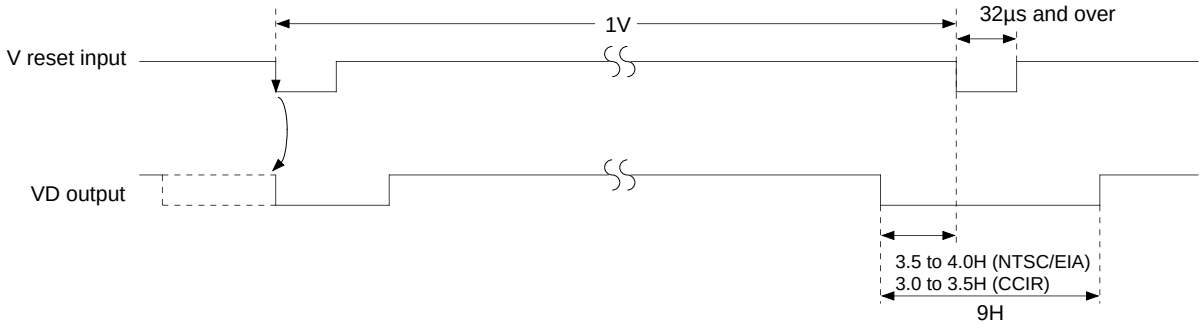
The HD output reset position leads the H reset input by 2.45 to 2.94 µs.



• V Reset

The VD output reset position leads the falling edge of the V reset input by 3.5 to 4.0 H for NTSC/EIA and by 3.0 to 3.5 H for PAL.

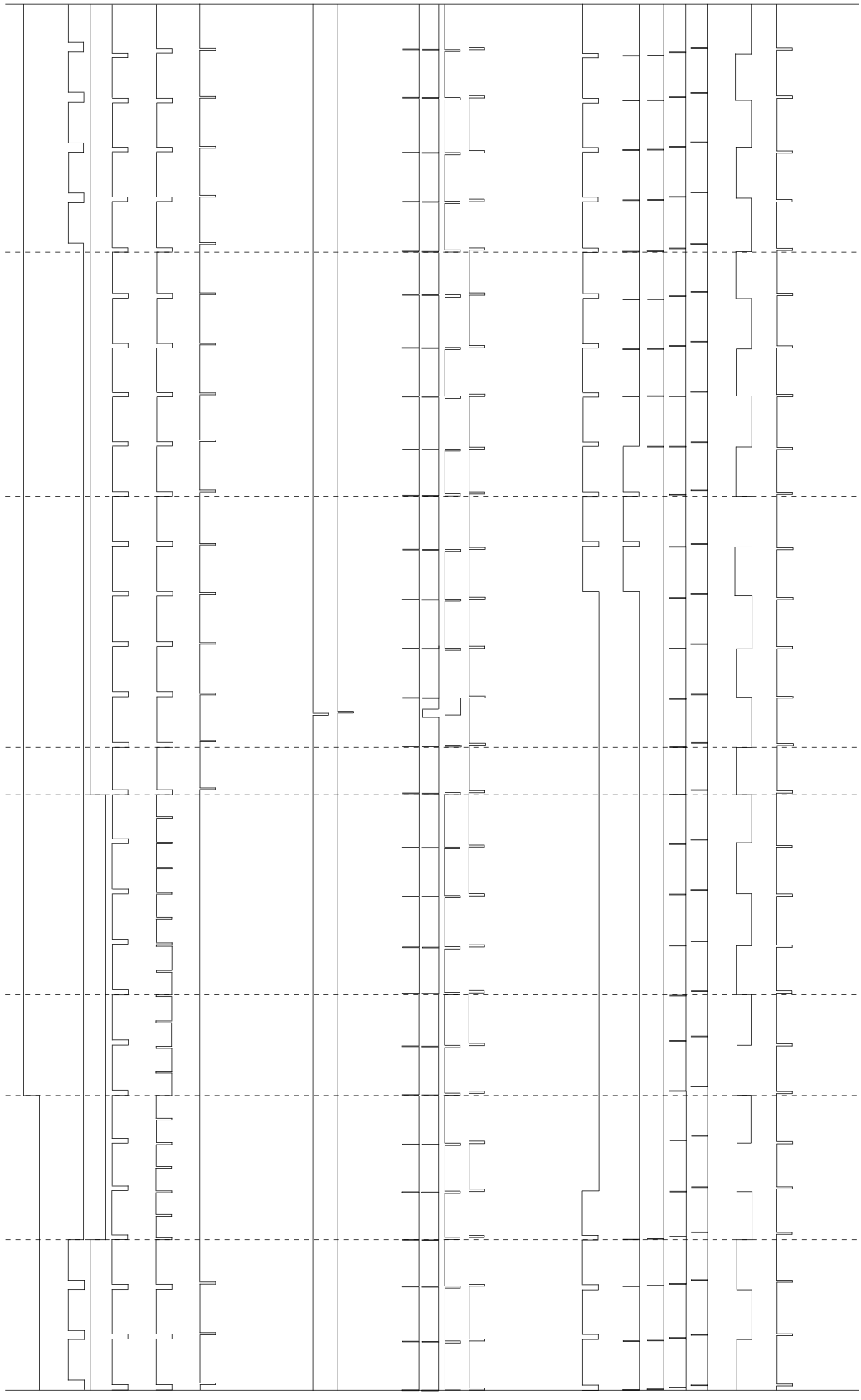
The minimum reset pulse width is 32 µs.



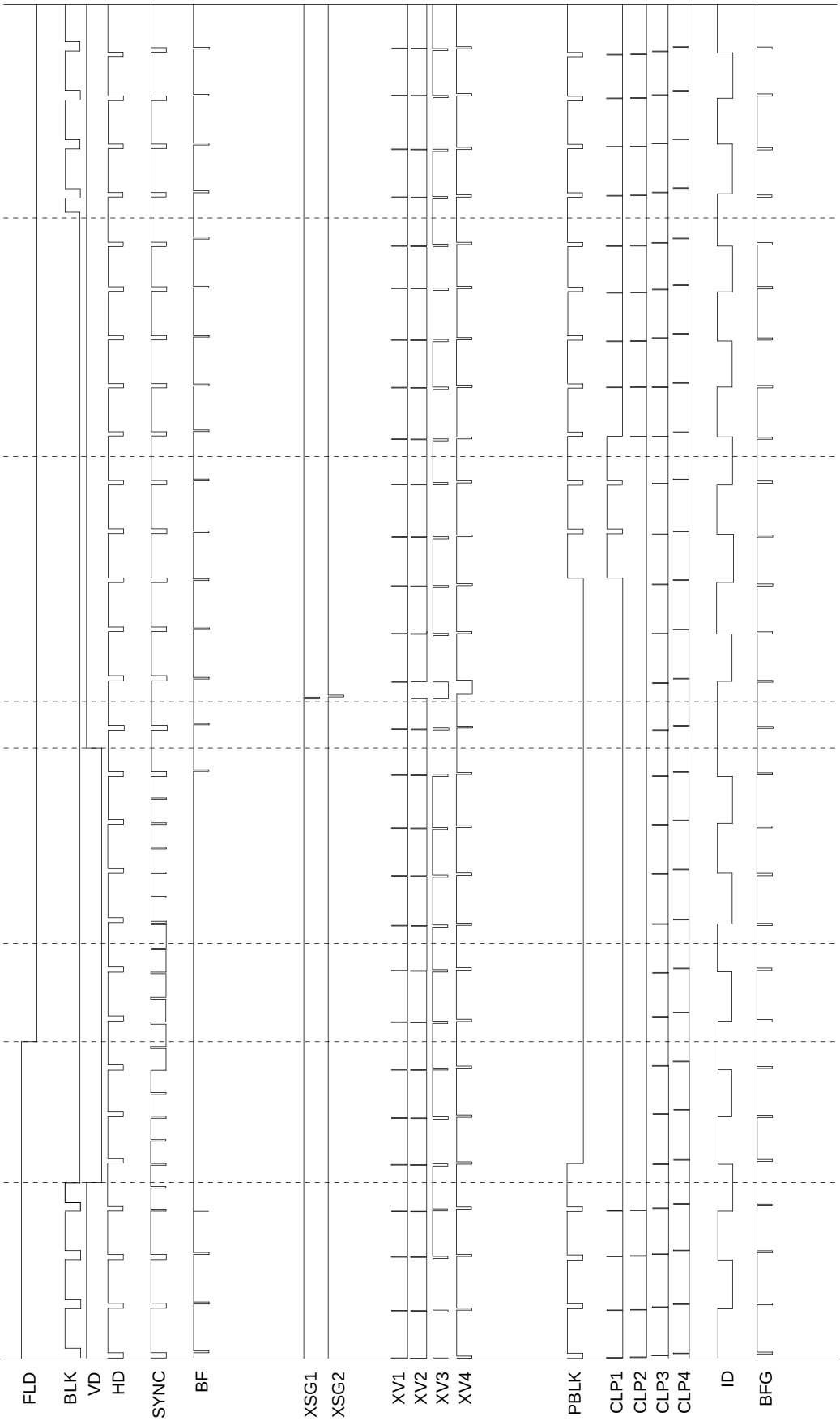
Timing Chart (1) <NTSC/EIA vertical direction>

ODD Field

• For EIA (black & white), the TG system output follows the VD switching point by 1H. (for both ODD and EVEN.)

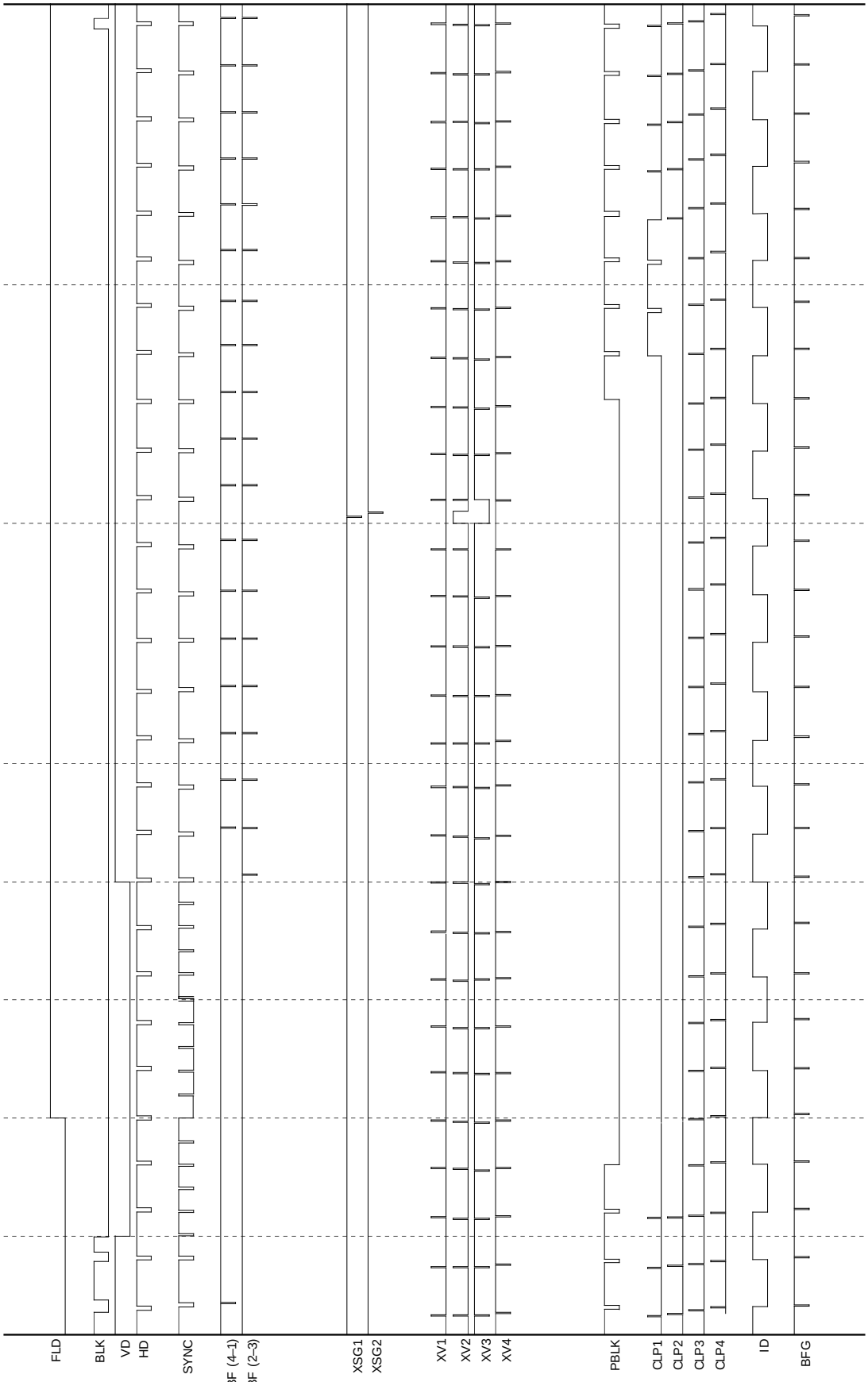


EVEN Field

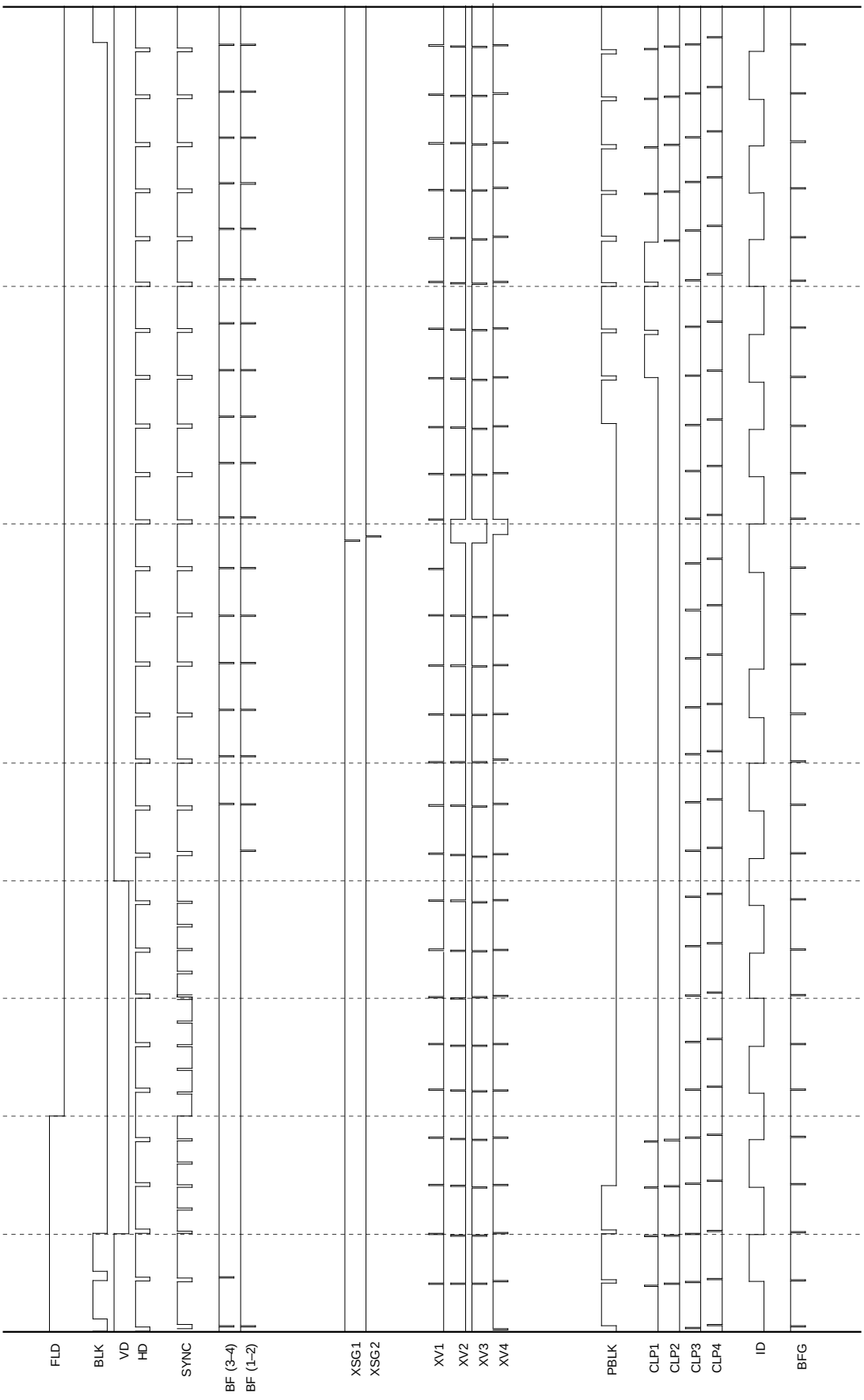

FLD
BLK
VD
HD
SYNC
BF
XSG1
XSG2
XV1
XV2
XV3
XV4
PBLK
CLP1
CLP2
CLP3
CLP4
ID
BFG

Timing Chart (2) <CCIR vertical direction>

ODD Field

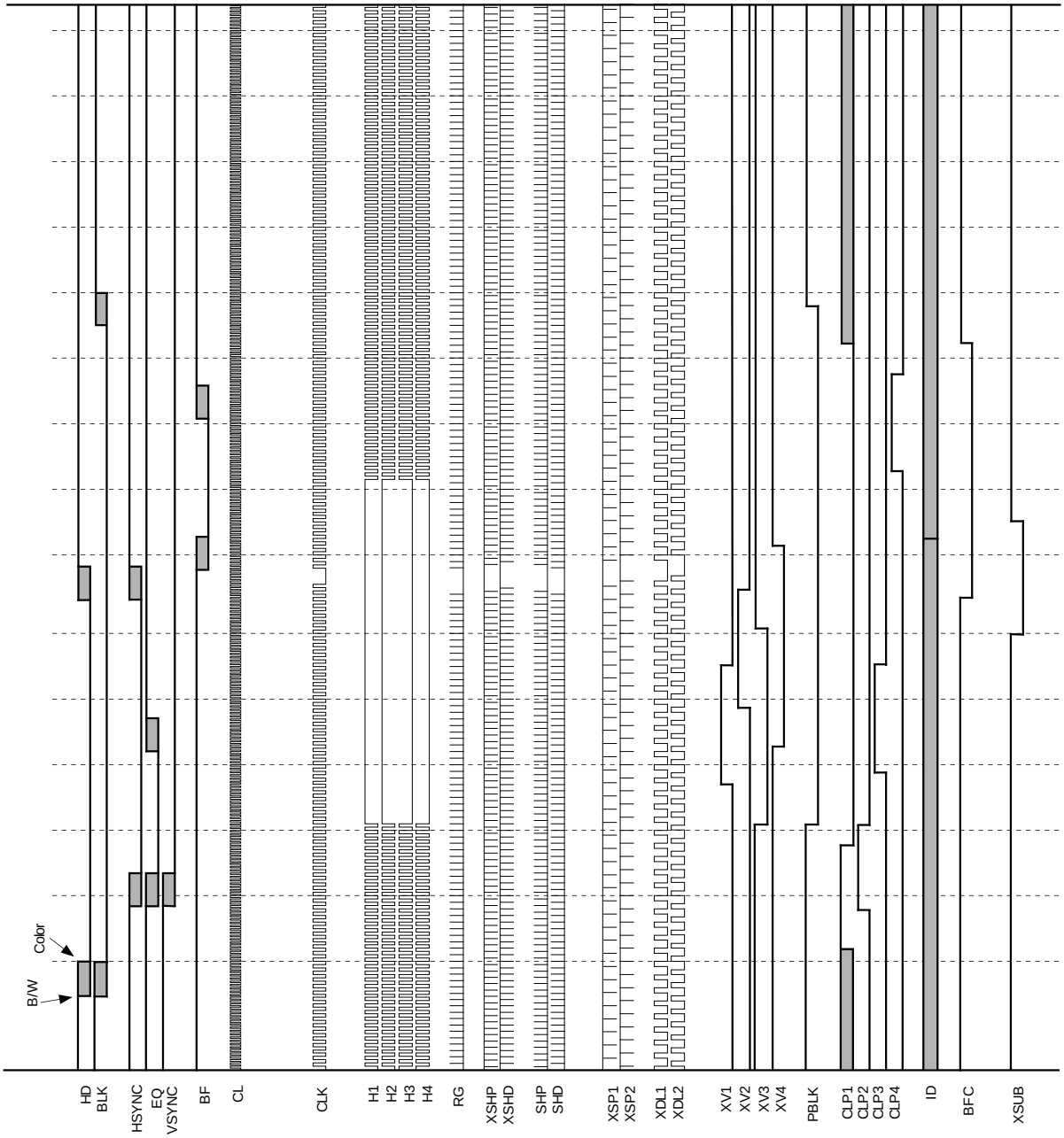


EVEN Field


FLD
BLK
VD
HD
SYNC
BF (3–4)
BF (1–2)
XSG1
XSG2
XV1
XV2
XV3
XV4
PBLK
CLP1
CLP2
CLP3
CLP4
ID
BFG

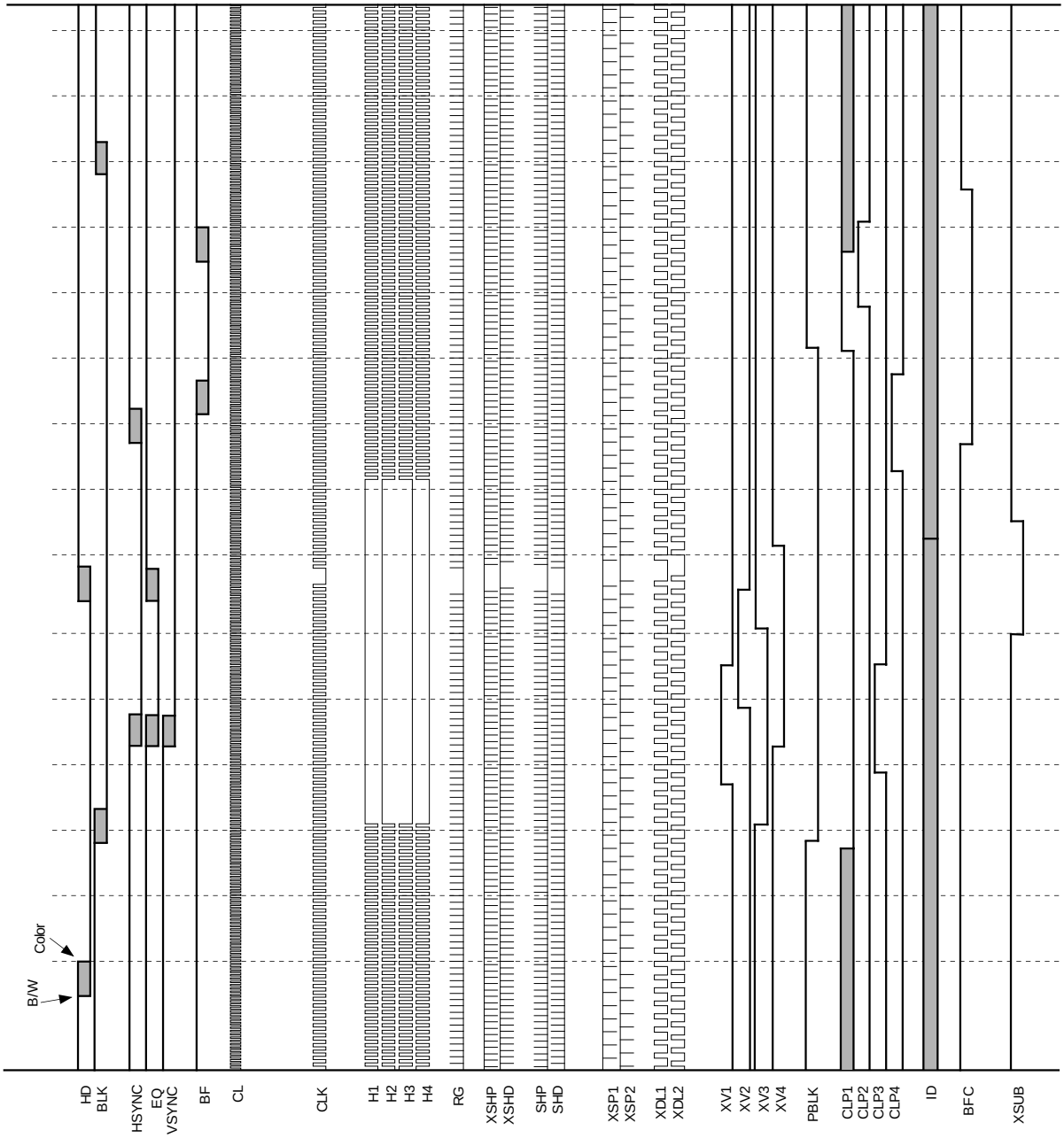
NTSC/EIA Normal Mode H Direction Timing Chart

Timing Chart (3) <NTSC/EIA horizontal direction, normal mode>



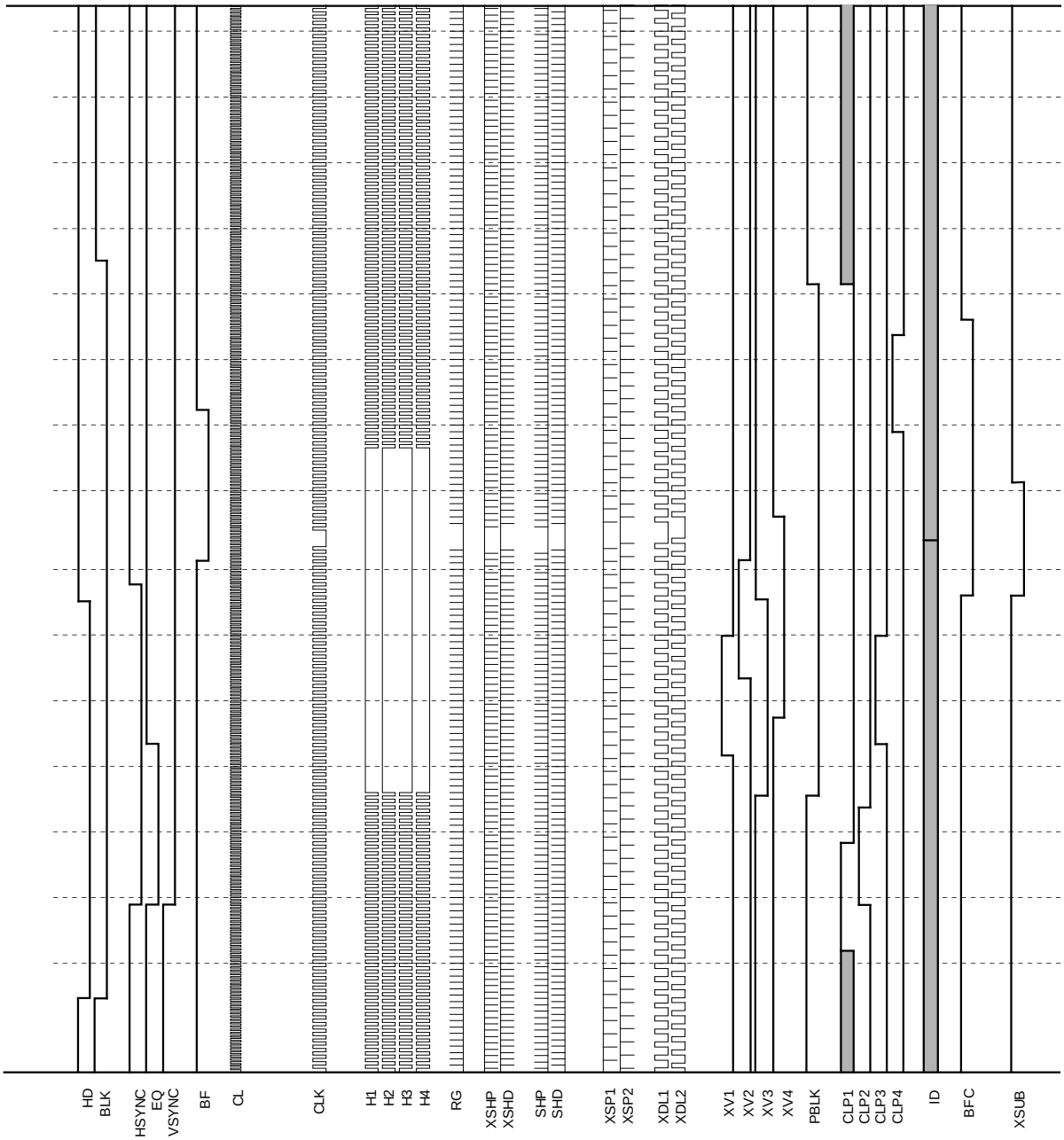
NTSC/EIA Mirror Mode H Direction Timing Chart

Timing Chart (4) <NTSC/EIA horizontal direction, mirror mode>



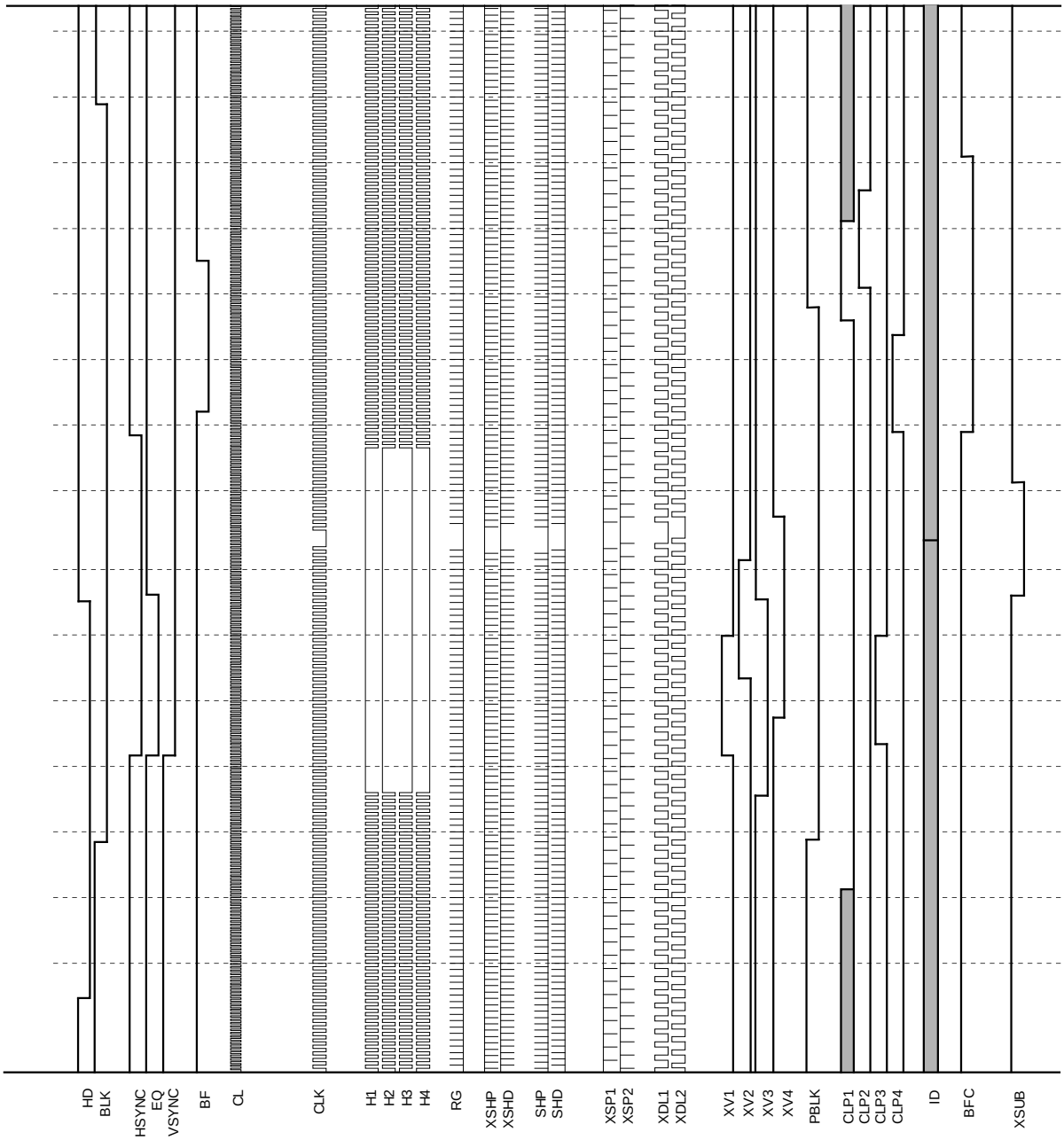
CCIR Normal Mode H Direction Timing Chart

Timing Chart (5) <CCIR horizontal direction, normal mode>



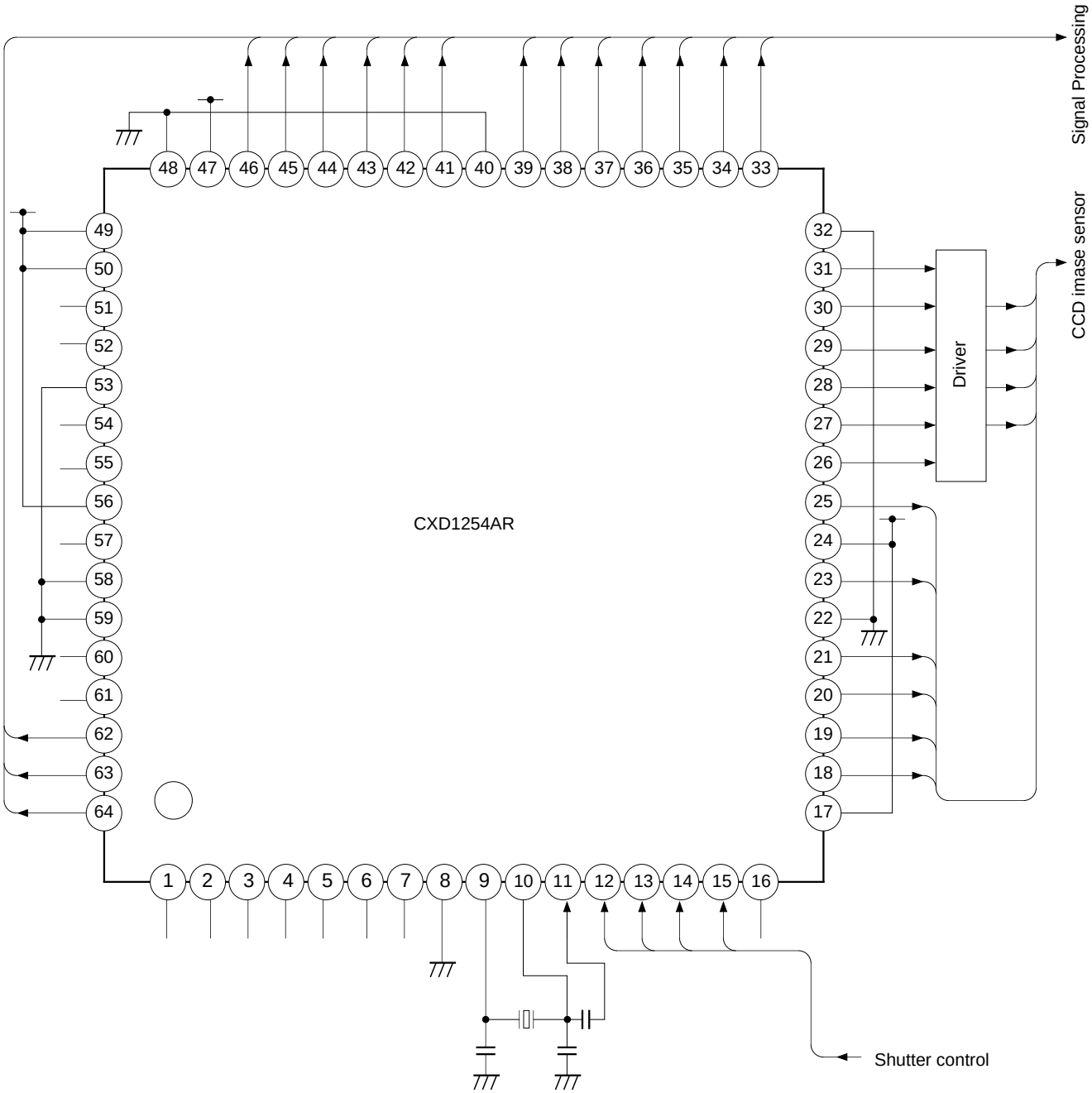
CCIR Mirror Mode H Direction Timing Chart

Timing Chart (6) <CCIR horizontal direction, mirror mode>



Application Circuit

(LQFP Package)



OSC NTSC/EIA : 28.6363MHz
CCIR : 28.375MHz

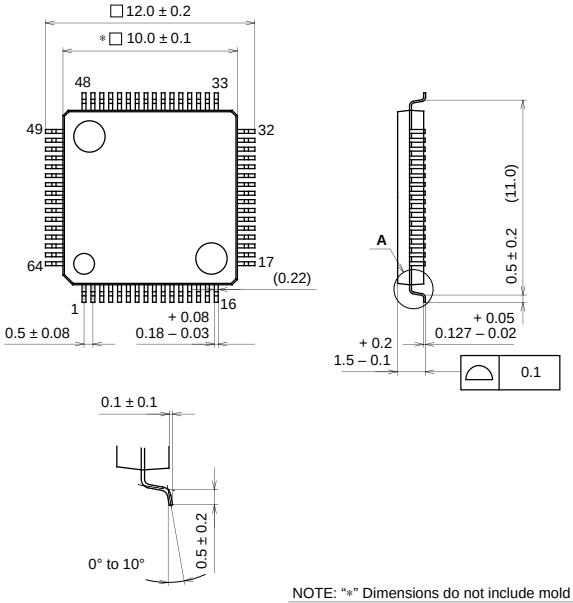
• Please use a clock crystal which operates on a fundamental wave.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit : mm

CXD1254AR

64PIN LQFP (PLASTIC)



NOTE: "*" Dimensions do not include mold protrusion.

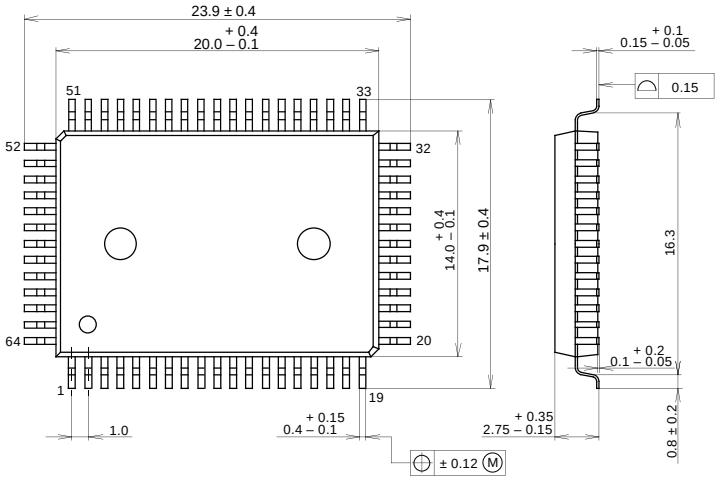
PACKAGE STRUCTURE

SONY CODE	LQFP-64P-L01
EIAJ CODE	QFP064-P-1010
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE WEIGHT	0.3g

CXD1254AQ

64PIN QFP(PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP–64P–L01
EIAJ CODE	*QFP064–P–1420
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	COPPER /42 ALLOY
PACKAGE WEIGHT	1.5g

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