SONY

# CXD1177Q

## 8-bit 40MSPS YC 2-channel D/A Converter

### Description

The CXD1177Q is an 8-bit high-speed D/A converter for video band use. It has an input/output equivalent to 2 channels of Y and C. It is suitable for use of digital TV, graphic display, and others.

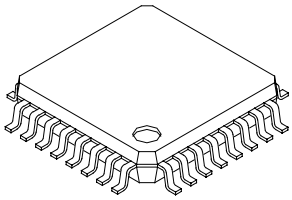
### Features

- Resolution 8-bit
- Maximum conversion speed 40MSPS
- YC 2-channel input/output
- Differential linearity error ±0.3 LSB
- Low power consumption 160 mW
  (200 Ω load at 2 Vp-p output)
- Single 5 V power supply
- Low glitch noise
- Stand-by function

### Structure

Silicon gate CMOS IC

32 pin QFP (Plastic)



### Absolute Maximum Ratings (Ta=25 °C)

| | | | |
|---|---|---|---|
| • Supply voltage | $AV_{DD}$, $DV_{DD}$ | 7 | V |
| • Input voltage (All pins) | $V_{IN}$ | $V_{DD}$ +0.5 to $V_{SS}$ –0.5 | V |
| • Output current (Every each channel) | $I_{OUT}$ | 0 to 15 | mA |
| • Storage temperature | Tstg | –55 to +150 | °C |

### Recommended Operating Conditions

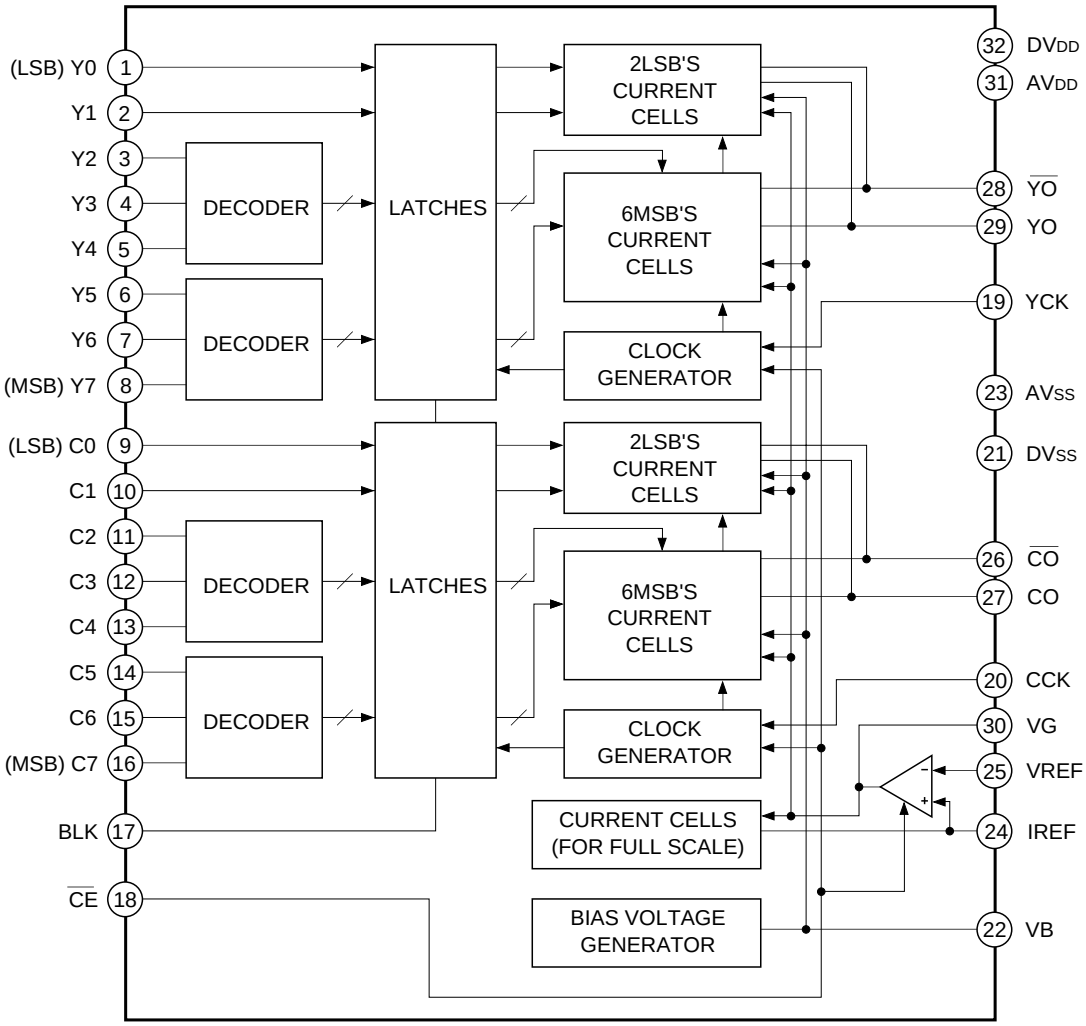
| | | | |
|---|---|---|---|
| • Supply voltage | $AV_{DD}$, $AV_{SS}$ | 4.75 to 5.25 | V |
| | $DV_{DD}$, $DV_{SS}$ | 4.75 to 5.25 | V |
| • Reference input voltage | $V_{REF}$ | 2.0 | V |
| • Clock pulse width | $T_{PW1}$, $T_{PW0}$ | 11.2 ns (min.) to 1.1 µs (max.) | |
| • Operating temperature | Topr | –40 to +85 | °C |



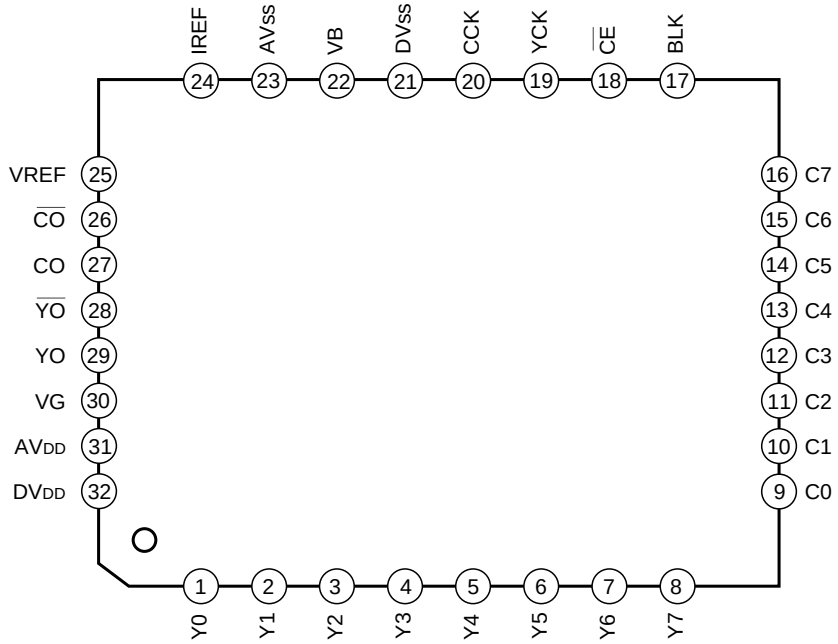


E90602G0X-PS

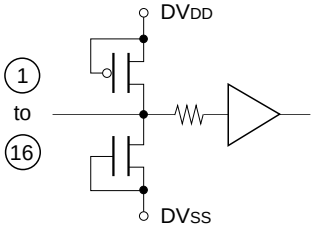
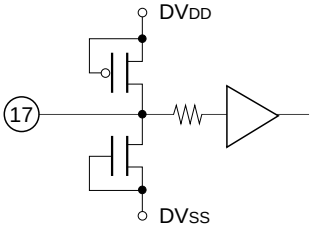
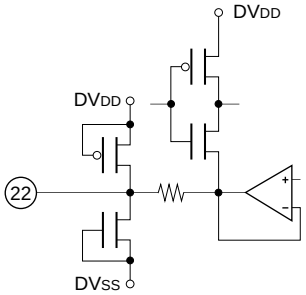
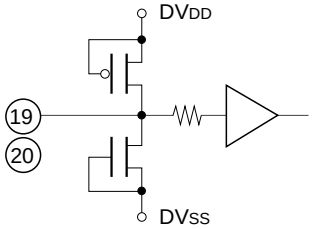
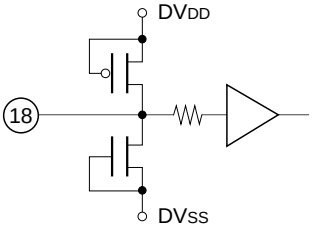
## Block Diagram

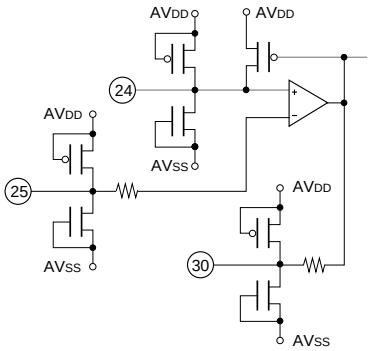
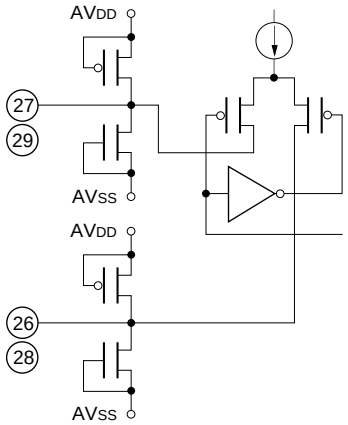



## Pin Configuration



**Pin Description and I/O Pins Equivalent Circuit**

| Pin No. | Symbol | I/O | Equivalent circuit | Description |
|---|---|---|---|---|
| 1 to 8<br>9 to 16 | Y0 to Y7<br>C0 to C7 | I |  | Digital input<br>Y0 (LSB) to Y7 (MSB)<br>C0 (LSB) to C7(MSB) |
| 17 | BLK | I |  | Blanking input.<br>This is synchronized with the clock input signal for each channel.<br>No signal at “H” (Output 0 V).<br>Output condition at “L”. |
| 22 | VB | O |  | Connect a capacitor of about 0.1 µF. |
| 19<br>20 | YCK<br>CCK | I |  | Clock input.<br>Note) Even though only 1 channel is used, be sure to input the clock signal to YCK. |
| 21 | DVSS | — | | Digital ground |
| 23 | AVSS | — | | Analog ground |
| 18 | $\overline{CE}$ | I |  | Chip enable input.<br>This is not synchronized with the clock input signal.<br>No signal (Output 0 V) at “H” and minimizes power consumption. |

| Pin No. | Symbol | I/O | Equivalent circuit | Description |
|---|---|---|---|---|
| 24 | IREF | O |  | Connect a resistance 16 times "RIR" that of output resistance value "ROUT". |
| 25 | VREF | I | | Set full-scale output value. |
| 30 | VG | O | | Connect a capacitor of about 0.1 µF. |
| 31 | AVDD | — | | Analog power supply |
| 27 | CO | O |  | Current output.<br>Voltage output can be obtained by connecting a resistance. |
| 29 | YO | | | |
| 26 | $\overline{CO}$ | | | Inverted current output.<br>Normally dropped to analog ground. |
| 28 | $\overline{YO}$ | | | |
| 32 | DVDD | — | | Digital power supply |

**Electrical Characteristics** ($F_{CLK}$=40 MHz, $AV_{DD}$=$DV_{DD}$=5 V, $R_{OUT}$=200 Ω, $V_{REF}$=2.0 V, Ta=25 °C)

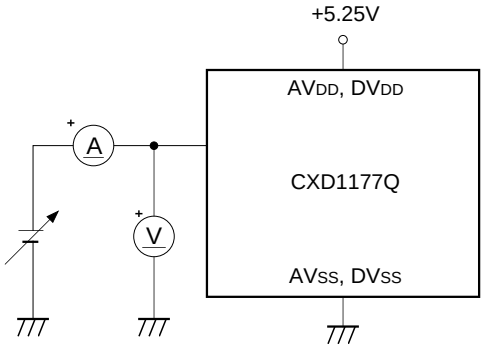
| Item | Symbol | Measurement conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | n | | | | 8 | | bit |
| Conversion speed | $F_{CLK}$ | $AV_{DD}$=$DV_{DD}$=4.75 to 5.25 V<br>Ta=–40 to +85 °C | | 0.5 | | 40 | MSPS |
| Integral non-linearity error | $E_L$ | Endpoint | | –2.5 | | 2.5 | LSB |
| Differential non-linearity error | $E_D$ | | | –0.3 | | 0.3 | LSB |
| Output full-scale voltage | $V_{FS}$ | | | 1.8 | 2.0 | 2.2 | V |
| Output full-scale ratio *1 | $F_{SR}$ | | | 0 | 1.5 | 3.0 | % |
| Output full-scale current | $I_{FS}$ | | | | 10 | 15 | mA |
| Output offset voltage | $V_{OS}$ | When “00000000” data input | | | | 1 | mV |
| Glitch energy | GE | $R_{OUT}$=75 Ω | | | 30 | | pV•s |
| Crosstalk | CT | When 1 kHz sine wave input | | | 57 | | dB |
| Supply current | $I_{DD}$ | When 14.3 MHz color bar data input | $\overline{CE}$=L | | | 32 | mA |
| | $I_{STB}$ | | $\overline{CE}$=H | | | 1.2 | |
| Analog input resistance | $R_{IN}$ | VREF | | 1 | | | MΩ |
| Input capacitance | $C_I$ | | | | | 9 | pF |
| Digital input voltage | $V_{IH}$ | $AV_{DD}$=$DV_{DD}$=4.75 to 5.25 V<br>Ta=–20 to +75 °C | | 2.4 | | | V |
| | $V_{IL}$ | | | | | 0.8 | |
| Digital input current | $I_{IH}$ | $AV_{DD}$=$DV_{DD}$=4.75 to 5.25 V<br>Ta=–20 to +75 °C | | –5 | | 5 | µA |
| | $I_{IL}$ | | | | | | |
| Setup time | ts | $R_{OUT}$=75 Ω | | 5 | | | ns |
| Hold time | th | $R_{OUT}$=75 Ω | | 10 | | | ns |
| Propagation delay time | $t_{PD}$ | | | | 10 | | ns |
| $\overline{CE}$ enable time *2 | $t_E$ | $\overline{CE}$=H→L | | | 2 | 4 | ms |
| $\overline{CE}$ disable time *2 | $t_D$ | $\overline{CE}$=L→H | | | 2 | 4 | ms |

*1 Full-scale output ratio = $\left| \frac{\text{Full-scale voltage for each channel}}{\text{Full-scale voltage average value for each channels}} - 1 \right| \times 100$ (%)

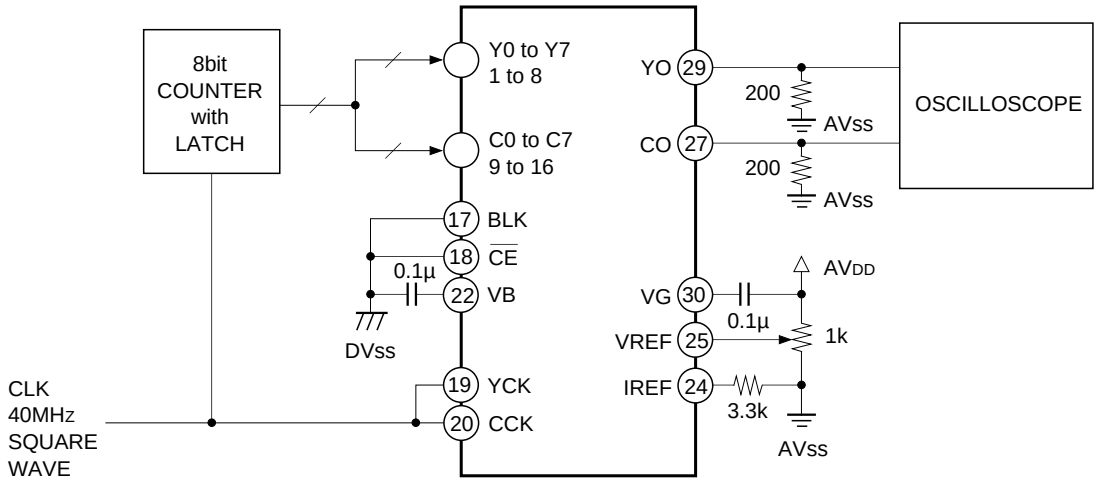
*2 When the external capacitors for the VG pins are 0.1 µF.

**Electrical Characteristics Measurement Circuit**

**Analog Input Resistance**
**Digital Input Current**
} **Measurement Circuit**

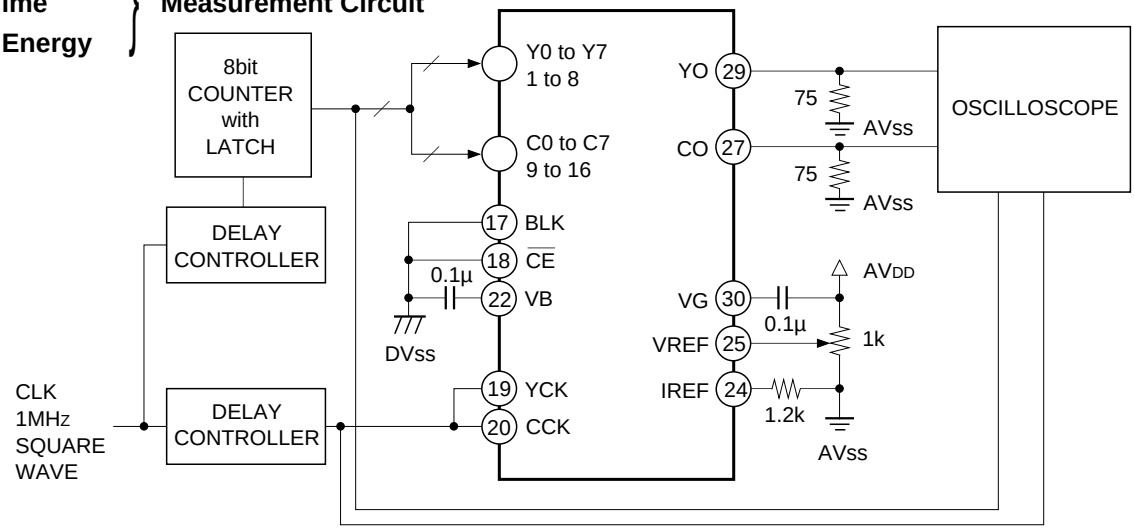


**Maximum Conversion Velocity Measurement Circuit**

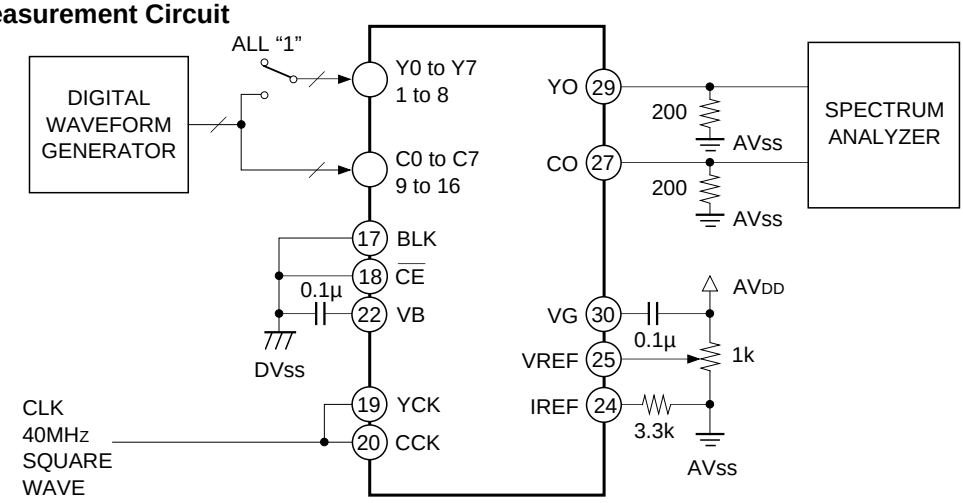



**Setup Time**
**Hold Time**
**Glitch Energy**

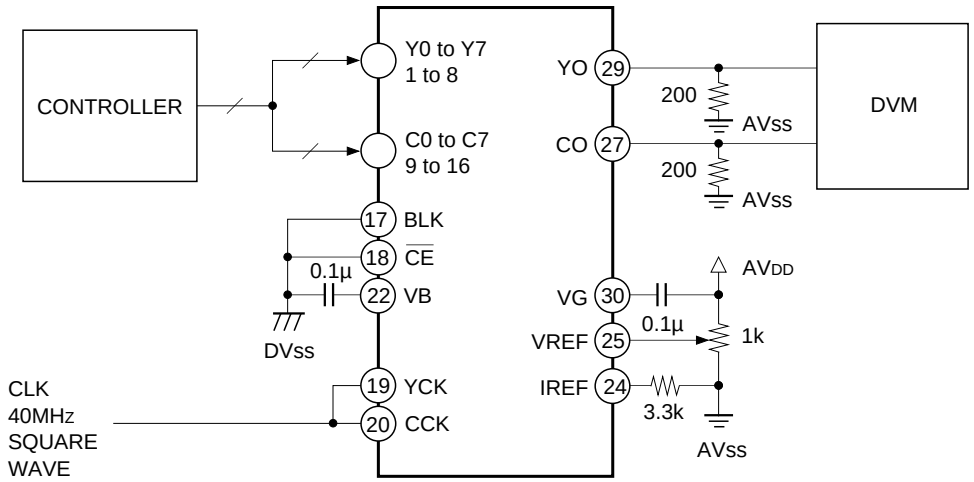
**Measurement Circuit**



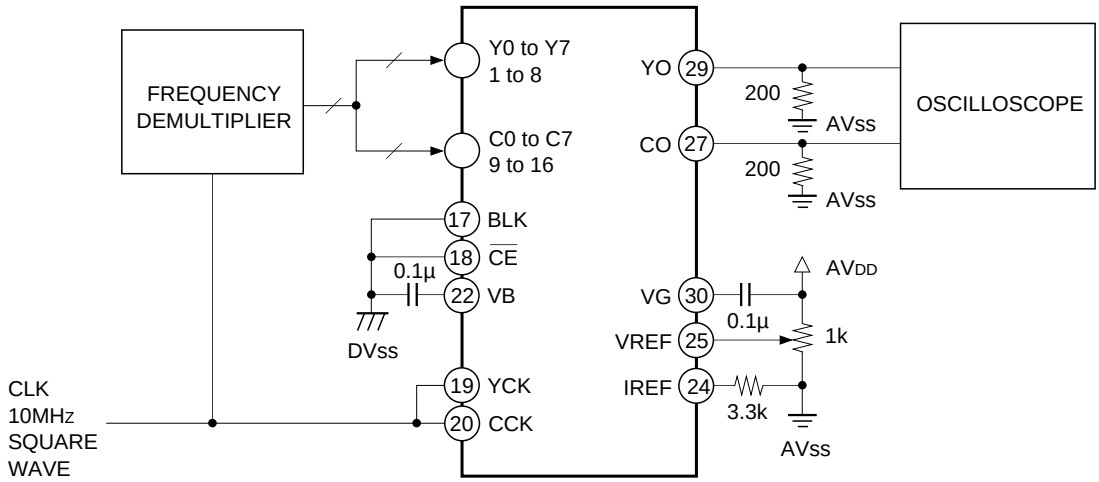

**Crosstalk Measurement Circuit**



## DC Characteristics Measurement Circuit

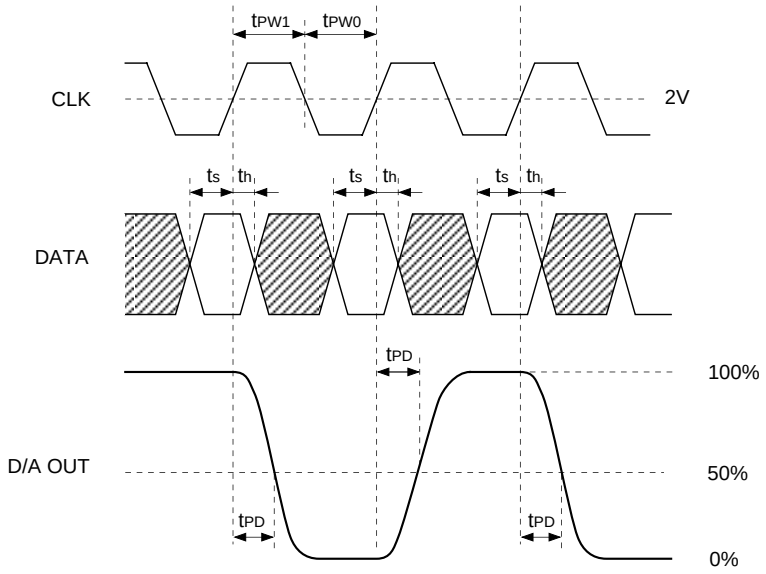



## Propagation Delay Time Measurement Circuit



## Description of Operation

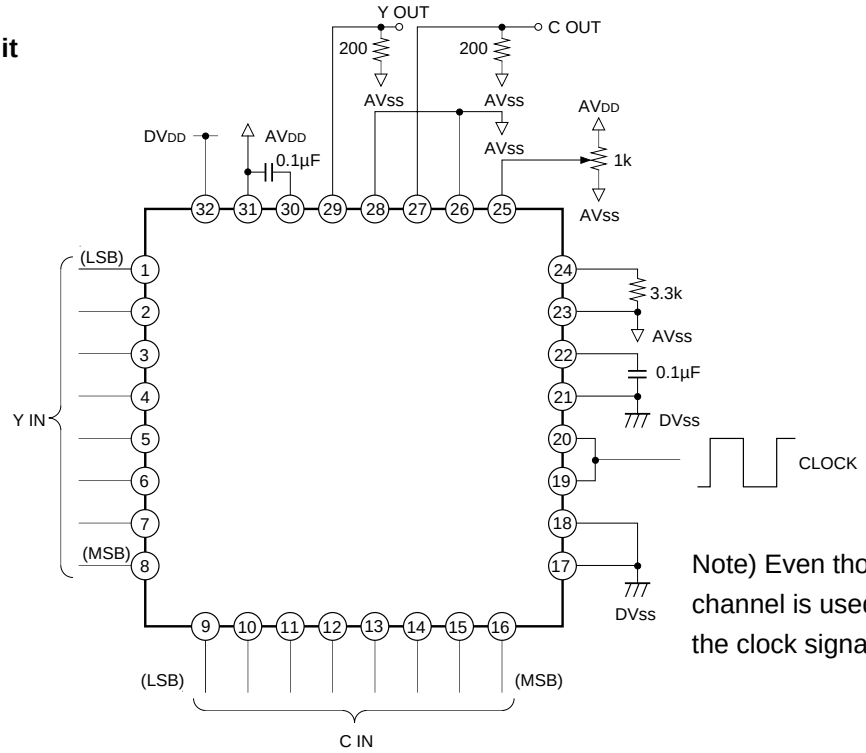
### Timing Chart




**I/O Chart** (When full-scale output voltage at 2.00 V)

| Input code | Output voltage |
|---|---|
| MSB LSB<br>1 1 1 1 1 1 1 1 | 2.0 V |
| : | |
| 1 0 0 0 0 0 0 0 | 1.0 V |
| : | |
| 0 0 0 0 0 0 0 0 | 0 V |

### Application Circuit




Note) Even though only 1 channel is used, be sure to input the clock signal to YCK(Pin 19).

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

**Notes on Operation**

- How to select the output resistance

  The CXD1177Q is a D/A converter of the current output type. To obtain the output voltage connect the resistance to the current output pins Y0, C0. For specifications we have;

  Output full scale voltage $V_{FS}$ = 1.8 to 2.2 [V]

  Output full scale current $I_{FS}$ = less than 15 [mA]

  Calculate the output resistance value from the relation of $V_{FS} = I_{FS} \times R_{OUT}$. Also, 16 times resistance of the output resistance is connected to reference current pin $I_{REF}$. In some cases, however, this turns out to be a value that does not actually exist. In such a case a value close to it can be used as a substitute. Here please note that $V_{FS}$ becomes $V_{FS} = V_{REF} \times 16R_{OUT}/R_{IR}$. $R_{OUT}$ is the resistance connected to the current output pins YO and CO while $R_{IR}$ is connected to $I_{REF}$. Increasing the resistance value can curb power consumption. On the other hand glitch energy and data settling time will inversely increase. Set the most suitable value according to the desired application.

- Phase relation between data and clock

  To obtain the expected performance as a D/A converter, it is necessary to set properly the phase relation between data and clock applied from the exterior. Be sure to satisfy the provisions of the setup time ($t_S$) and hold time ($t_H$) as stipulated in the Electrical Characteristics.

- Power supply and grand

  To reduce noise effects separate analog and digital systems in the device periphery. For the power supply pins, both digital and analog, bypass respective grounds by using a ceramic capacitor of about 0.1 µF, as close as possible to the pin.

- Latch up

  $AV_{DD}$ and $DV_{DD}$ have to be common at the PCB power supply source. This is to prevent latch up due to voltage difference between $AV_{DD}$ and $DV_{DD}$ pins when power supply is turned ON.

- $\overline{YO}$ and $\overline{IO}$ pins

  The $\overline{YO}$ and $\overline{IO}$ pins are the inverted current output pins described in the Pin Description. The sums shown below become the constant value for any input data.

  a) The sum of the currents output form YO and $\overline{YO}$
  b) The sum of the currents output form CO and $\overline{CO}$

  However, the performances such as the linearity error of the inverted current output pin output current is not guaranteed.

- Clock input signal

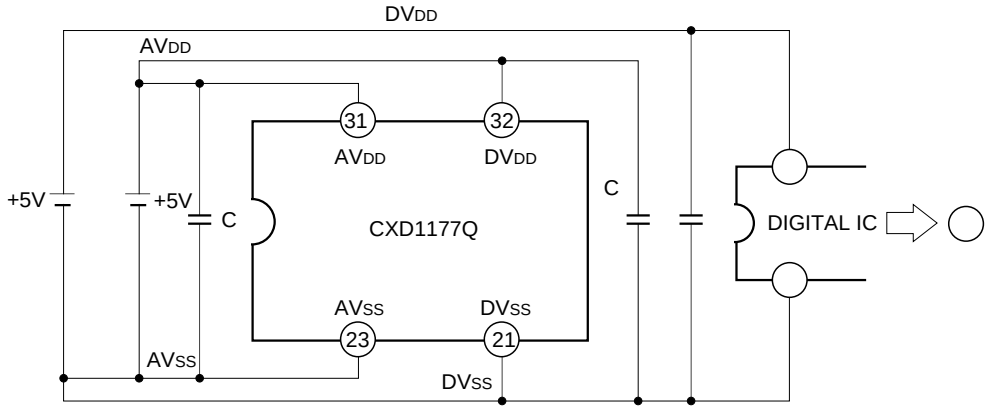
  Even though only 1 channel is used, be sure to input the clock signal to YCK(Pin 19).

**Latch Up Prevention**

The CXD1177Q is a CMOS IC which requires latch up precautions. Latch up is mainly generated by the lag in the voltage rising time of $AV_{DD}$ (Pin 31) and $DV_{DD}$ (Pin 32), when power supply is ON.

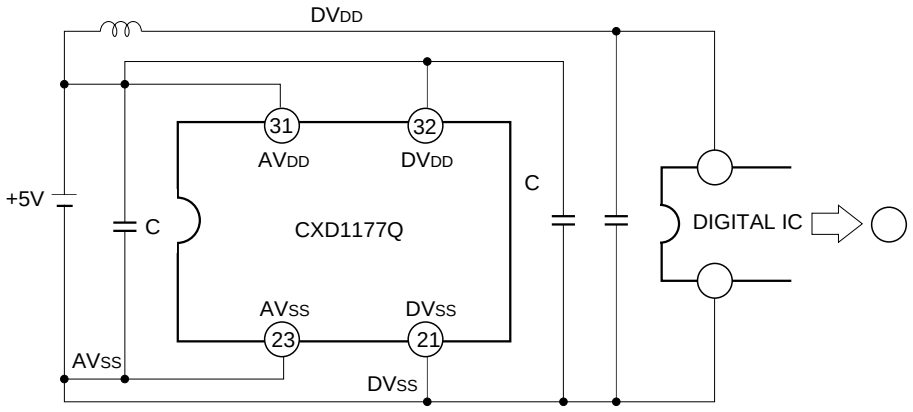
**1. Correct usage**

**a. When analog and digital supplies are from different sources**

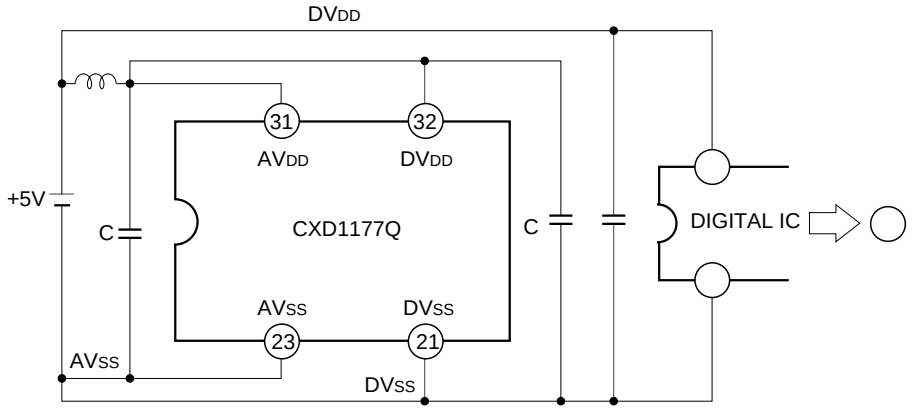



**b. When analog and digital supplies are from a common source**

(i)

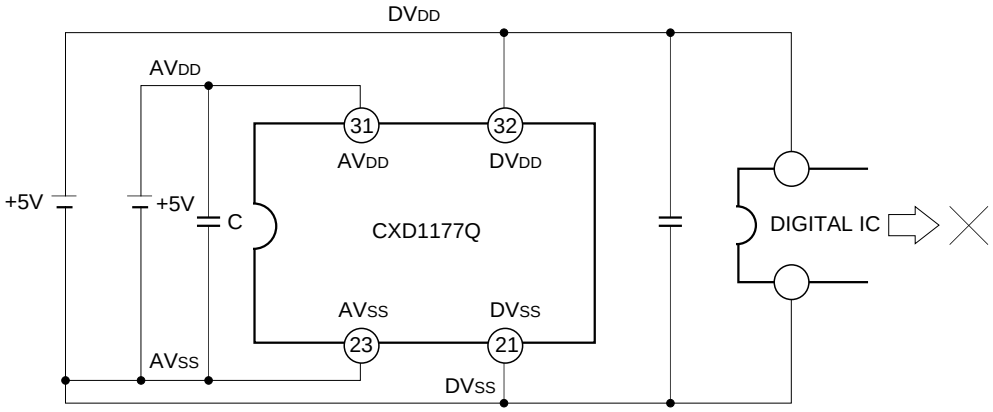



(ii)



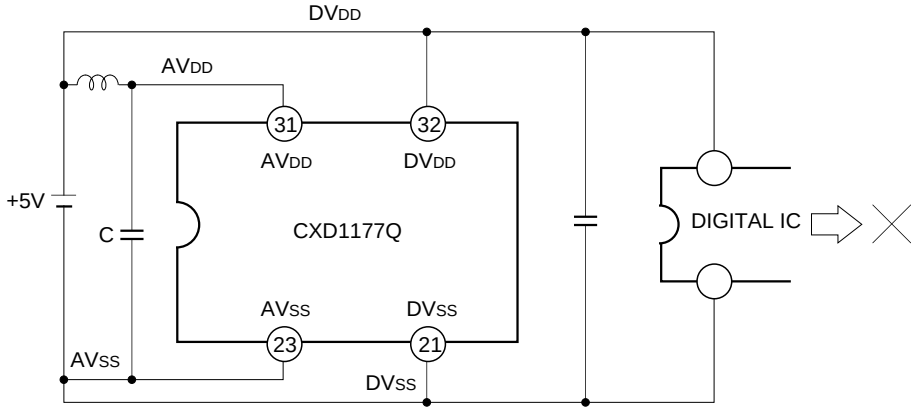
**2. Example when latch up easily occurs**

**a. When analog and digital supplies are from different sources**

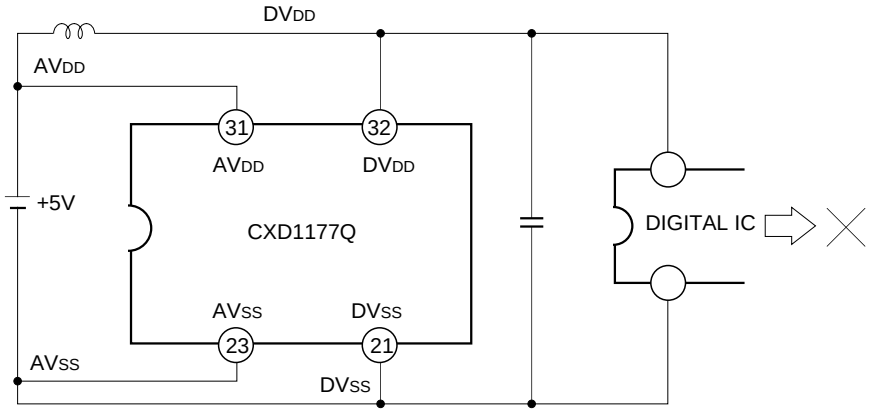



**b. When analog and digital supplies are from common source**

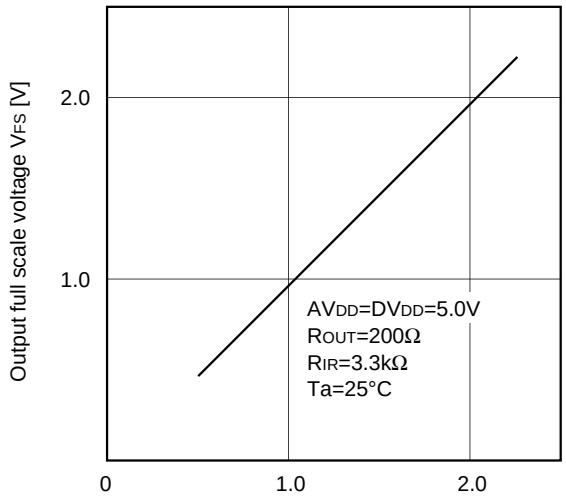
(i)



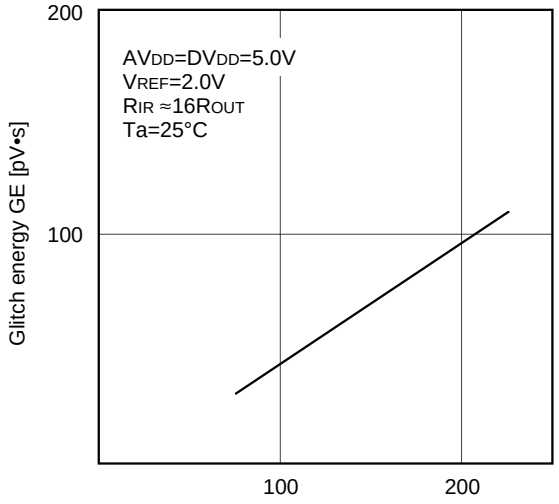

(ii)



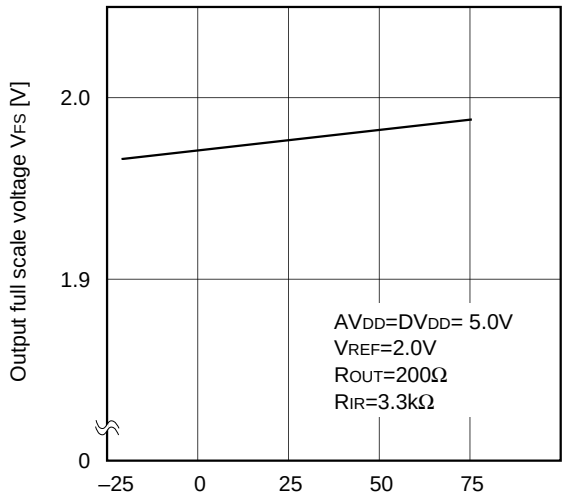
## Example of Representative Characteristics



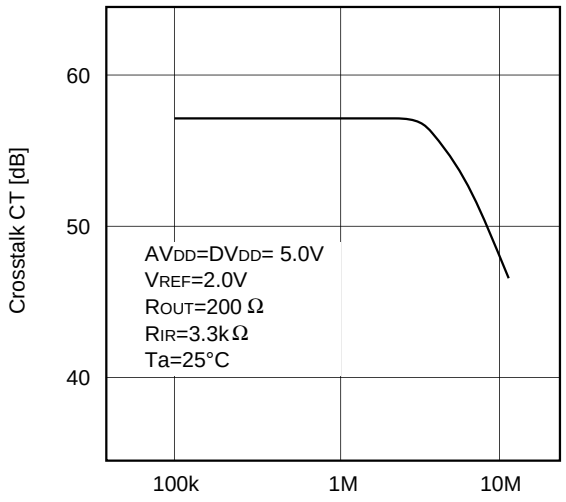

Reference voltage vs. Output full scale voltage




Output resistance vs. Glitch energy



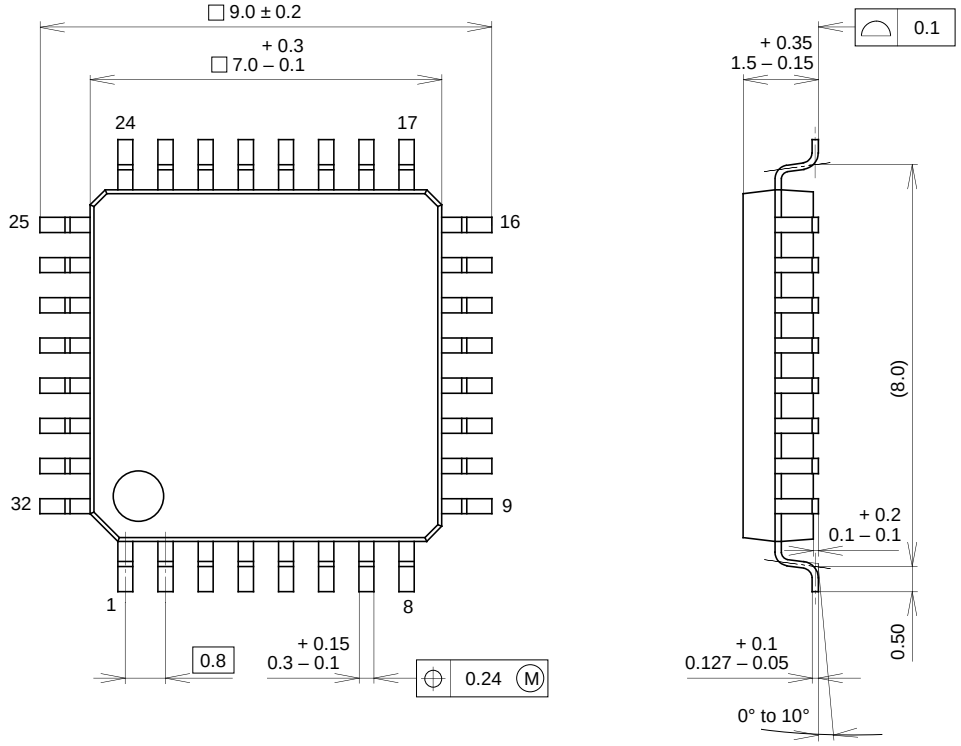

Ambient temperature vs. Output full scale voltage




Output frequency vs. Crosstalk

**Package Outline** Unit : mm

32PIN QFP (PLASTIC)




| | |
|---|---|
| SONY CODE | QFP-32P-L01 |
| EIAJ CODE | QFP032-P-0707 |
| JEDEC CODE | ———— |

| | |
|---|---|
| PACKAGE MATERIAL | EPOXY RESIN |
| LEAD TREATMENT | SOLDER PLATING |
| LEAD MATERIAL | 42 ALLOY |
| PACKAGE MASS | 0.2g |

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