

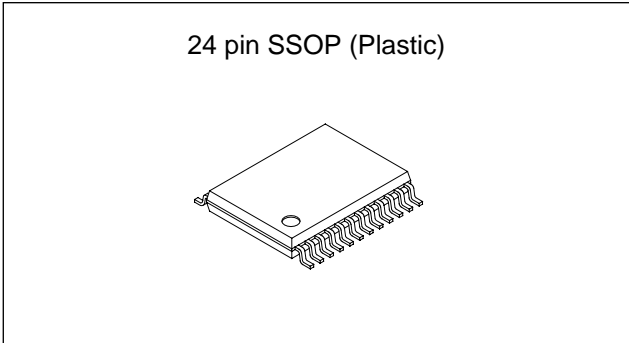
Fibre Channel Repeater

Description

The CXB1585N is a repeater IC with a built-in PLL clock recovery circuit for Fibre Channel 1.06Gbaud. This IC incorporates a port bypass circuit and is suitable for disk array and FC-AL HUB, etc.

Features

- Conforms to ANSI X3T11 Fibre Channel standard
- Single 3.3V power supply
- Low power consumption: 330mW (Typ.)
- Low jitter
- PLL lock detection circuit
- Port bypass circuit
- Small plastic package (24-pin SSOP)



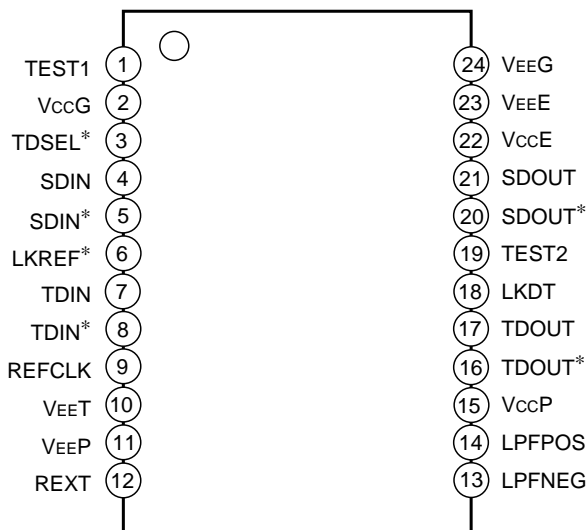
Applications

- Fibre channel arbitrated loop 1.0625Gbaud HUB
- Disk array

Structure

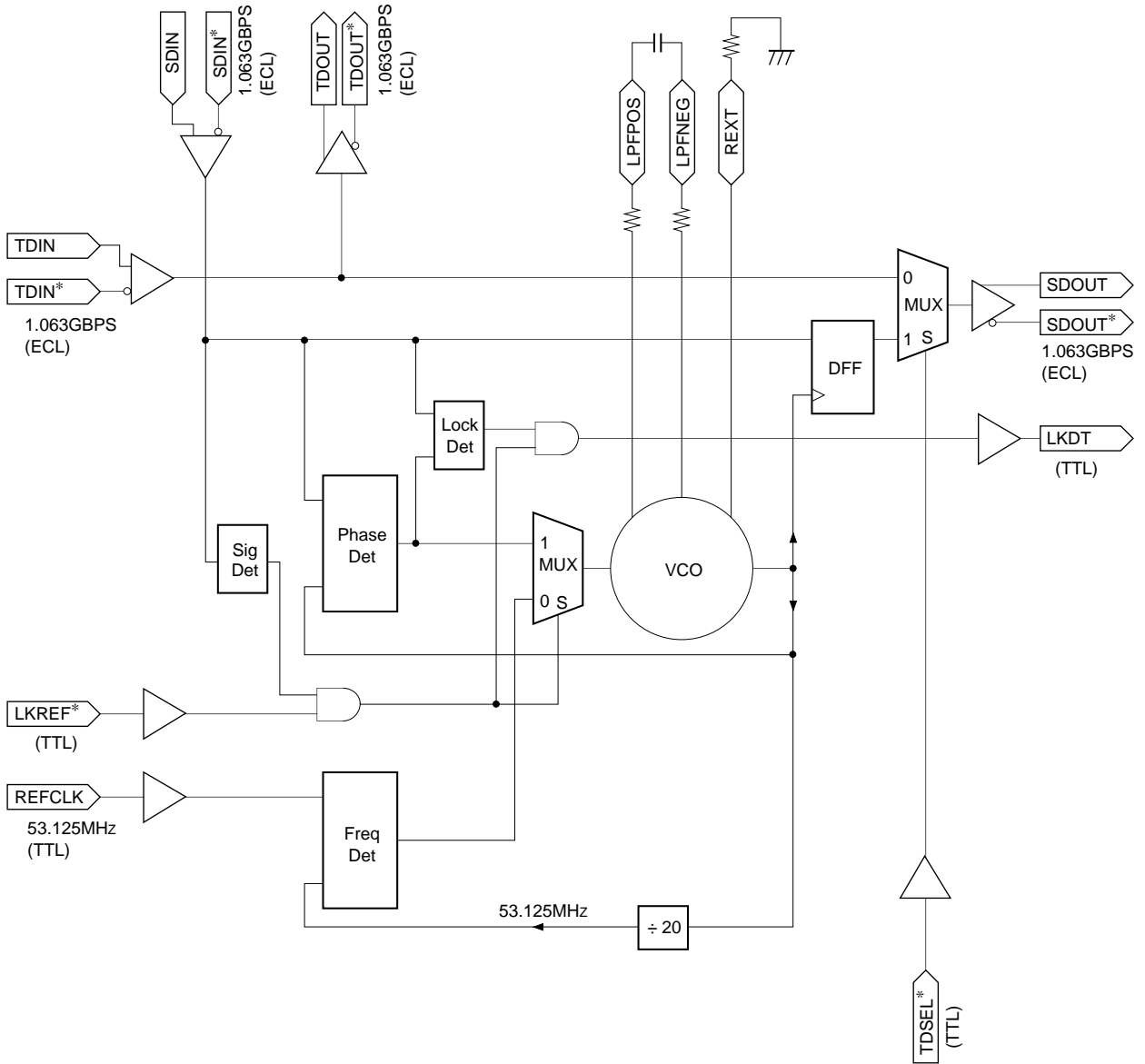
Bipolar silicon monolithic IC

Pin Configuration



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Block Diagram



Absolute Maximum Ratings ($V_{EE E}$, $V_{EE T}$, $V_{EE G}$, $V_{EE P} = 0V$)

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---------------------------------|-------------|--------------|------|----------|------|
| Supply voltage | V_{CC} | -0.3 | | 4 | V |
| TTL DC input voltage | V_{I_T} | -0.5 | | 5.5 | V |
| ECL DC input voltage | V_{I_E} | $V_{CC} - 2$ | | V_{CC} | V |
| ECL differential input voltage | V_{IS_E} | -2 | | 2 | V |
| TTL output current (High level) | I_{OH_T} | -20 | | 0 | mA |
| TTL output current (Low level) | I_{OL_T} | 0 | | 20 | mA |
| ECL output current | I_{O_E} | -30 | | 0 | mA |
| Operating ambient temperature | T_a | -55 | | 70 | °C |
| Storage temperature | T_{stg} | -65 | | 150 | °C |

Recommended Operating Conditions ($V_{EE E}$, $V_{EE T}$, $V_{EE G}$, $V_{EE P} = 0V$)

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---------------------|----------|-------|------|-------|------|
| Supply voltage | V_{CC} | 3.135 | 3.3 | 3.465 | V |
| Ambient temperature | T_a | 0 | | 70 | °C |

Pin Description

| Pin No. | Symbol | Type | Typical pin I/O voltage | Equivalent circuit | Description |
|---------|----------------|--------------|-------------------------|--------------------|---|
| 1, 19 | TEST1 TEST2 | TTL input | 3.3V | | Test pin. Connect to Vcc. |
| 2 | VccG | Power supply | 3.3V | — | Positive power supply for internal logic gate. |
| 3 | TDSEL* | TTL input | TTL level | | High; SDOUT outputs the SDIN retimed data. Low; SDOUT outputs TDIN data. |
| 4, 5 | SDIN SDIN* | ECL input | ECL level | | Serial data input. |
| 6 | LKREF* | TTL input | TTL level | | Low; PLL takes the frequency from REFCLK. |

| Pin No. | Symbol | Type | Typical pin I/O voltage | Equivalent circuit | Description |
|---------|------------------|-------------------------------|-------------------------|--------------------|--|
| 7, 8 | TDIN TDIN* | ECL input | ECL level | | Serial data input. |
| 9 | REFCLK | TTL input | TTL level | | Reference clock input. This pin is used for the PLL to take the frequency. Input 53.125MHz to this pin. |
| 10 | VeeT | Power supply | 0V | | Negative power supply for REFCLK input. |
| 11 | VeeP | Power supply | 0V | | Negative power supply for internal PLL. |
| 12 | REXT | External parts connection pin | — | | Connects the resistor which determines the VCO center frequency. 4.7kΩ resistor should be connected between this pin and VeeP. |
| 13, 14 | LPFNEG LPFPOS | External parts connection pin | — | | Connects the external loop filter. |

| Pin No. | Symbol | Type | Typical pin I/O voltage | Equivalent circuit | Description |
|---------|-----------------|--------------|-------------------------|--------------------|--|
| 15 | VccP | Power supply | 3.3V | | Positive power supply for PLL. |
| 16, 17 | TDOUT* TDOUT | ECL output | ECL level | | Outputs the data input from TDIN via a buffer. |
| 18 | LKDT | TTL output | TTL level | | PLL clock detection signal output. Outputs high level when PLL is locked to the serial data; Outputs low level when LKREF is in the low level or the serial data has no signal. The LKDT output may sporadically go high when the PLL starts to lock to the serial data. |
| 20, 21 | SDOUT* SDOUT | ECL output | ECL level | | Outputs the serial data selected by TDSEL*. |
| 22 | VccE | Power supply | — | | Positive power supply for input/output. |
| 23 | VEEE | Power supply | — | | Negative power supply for input/output. |
| 24 | VEEG | Power supply | — | | Negative power supply for internal logic gate. |

Electrical Characteristics

DC Characteristics

(under the recommended operating conditions)

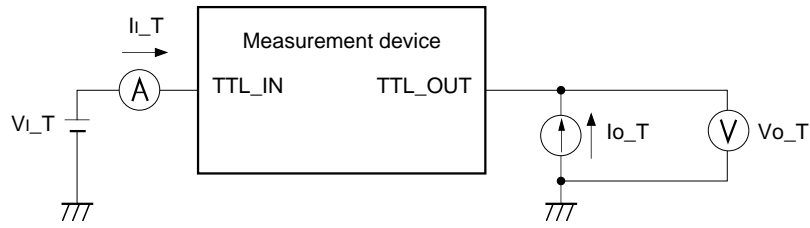
| Item | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|--------------------------------|-------------------|------------------------|------|------------------------|------|--|
| TTL high level input voltage | V _{IH_T} | 2 | | 5.5 | V | |
| TTL low level input voltage | V _{IL_T} | 0 | | 0.8 | V | |
| TTL high level input current | I _{IH_T} | | | 20 | μA | V _{IH} = V _{CC} |
| TTL low level input current | I _{IL_T} | -400 | | | μA | V _{IL} = 0 |
| TTL high level output voltage | V _{OH_T} | 2.2 | | | V | I _{OH} = -0.4mA |
| TTL low level output voltage | V _{OL_T} | | | 0.5 | V | I _{OL} = 2mA |
| ECL high level input voltage | V _{IH_E} | V _{CC} - 1.17 | | V _{CC} - 0.88 | V | |
| ECL low level input voltage | V _{IL_E} | V _{CC} - 1.81 | | V _{CC} - 1.48 | V | |
| ECL differential input voltage | V _{IS_E} | 200 | | 1000 | mV | AC coupling input |
| ECL high level output voltage | V _{OH_E} | V _{CC} - 1.05 | | V _{CC} - 0.81 | V | 50Ω terminated to V _{CC} - 2V |
| ECL low level output voltage | V _{OL_E} | V _{CC} - 1.81 | | V _{CC} - 1.55 | V | 50Ω terminated to V _{CC} - 2V |
| ECL output amplitude | V _{OS_E} | 650 | | | mV | 50Ω terminated to V _{CC} - 2V |
| Current consumption | I _{CC} | | 101 | 127 | mA | Output pins open |
| Power consumption | P _D | | 333 | 438 | mW | Output pins open |

AC Characteristics

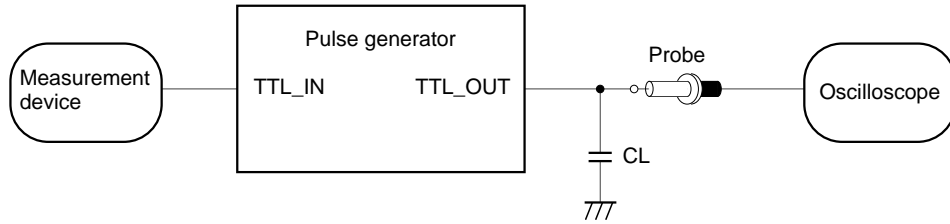
(under the recommended operating conditions)

| Item | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|------------------------|---------------------|------|--------|------|-------|---|
| REFCLK rise time | T _{ir_RC} | | | 4.8 | ns | 0.8 to 2.0V |
| REFCLK fall time | T _{if_RC} | | | 4.8 | ns | 2.0 to 0.8V |
| TTL output rise time | T _{or_T} | | | 3.5 | ns | 0.8 to 2.0V, C _L = 10pF |
| TTL output fall time | T _{of_T} | | | 3.5 | ns | 2.0 to 0.8V, C _L = 10pF |
| ECL output rise time | T _{or_E} | | | 400 | ps | 20 to 80%, C _L ≤ 2pF |
| ECL output fall time | T _{of_E} | | | 400 | ps | 20 to 80%, C _L ≤ 2pF |
| SDIN data rate | SDIN | 1000 | 1062.5 | 1100 | Mbaud | |
| REFCKL cycle tolerance | T _{tol_RC} | -100 | 0 | 100 | ppm | Refer to the SDIN cycle |
| Jitter tolerance | JT | | | 0.7 | UI | |
| Deterministic jitter | Dj | | 0.02 | 0.07 | UI | ±K28.5 serial data |
| Random jitter | RJ | | 0.18 | 0.23 | UI | Serial data |
| Bit sync time | T _{bs} | | | 2500 | bit | FC Idle Pattern |
| Frequency take-in time | T _{fa} | | | 500 | μs | Loop Damping Capacitor C ₁ = 0.01μF |

Electrical Characteristics Measurement Circuit (See “Fig. 3 Power Supply Circuit” regarding the power supply.)

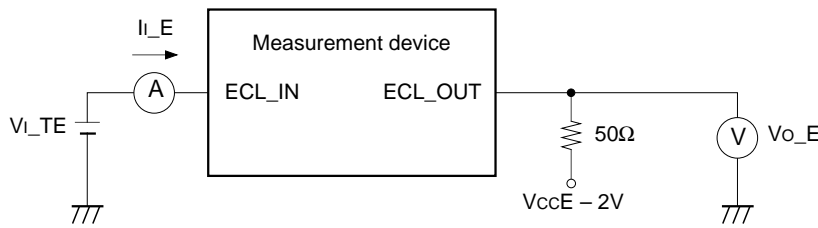


(a) TTL I/O DC characteristics measurement circuit

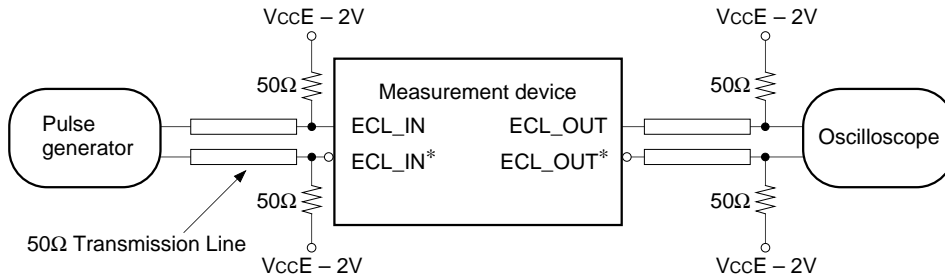


$CL = 10\text{pF}$ (including the probe capacitance)

(b) TTL I/O AC characteristics measurement circuit

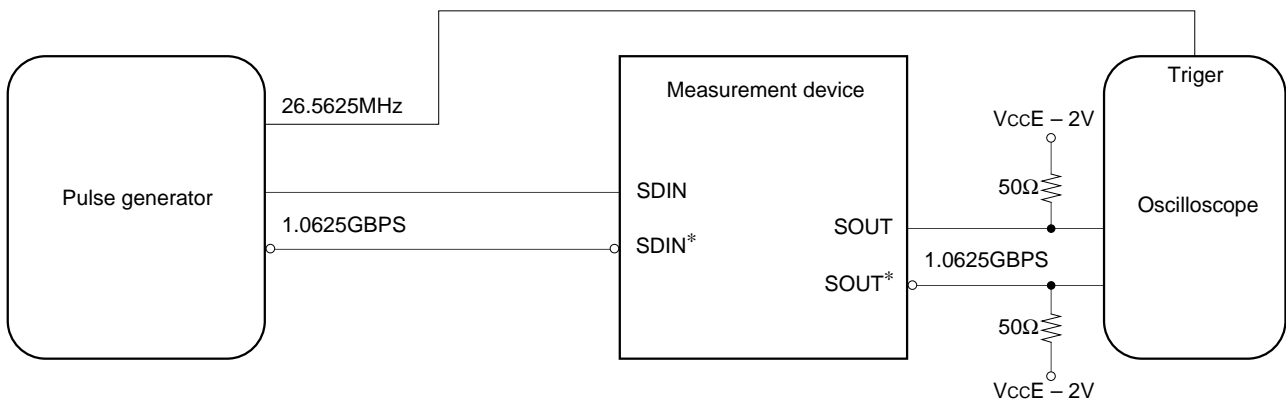


(c) ECL I/O DC characteristics measurement circuit



$CL \leq 2\text{pF}$
(input capacitance of the measurement equipment and floating capacitance)

(d) ECL I/O AC characteristics measurement circuit



(e) Jitter characteristics measurement circuit

Notes on Operation

1. Clock synthesizer (PLL)

The CXB1585N has a PLL-based clock recovery circuit for recovering the clock from the serial data. This clock recovery circuit requires an external loop filter and an external resistor which determines the VCO center frequency. The external part circuit and recommended constant values are shown in the figure below. The parasitic capacitance attached to the IC pins (Pins 12, 13 and 14) which are used to connect external parts should be kept as small as possible in order to obtain the good PLL characteristics. In addition, capacitor C1 should have a small temperature coefficient to reduce the temperature dependence of the VCO oscillation frequency.

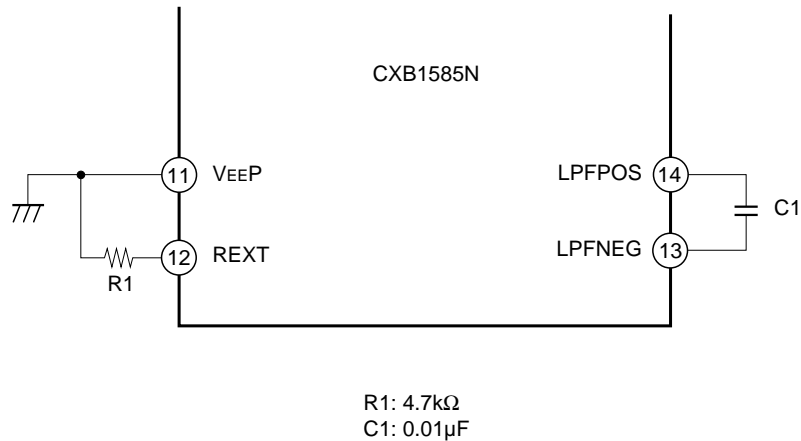
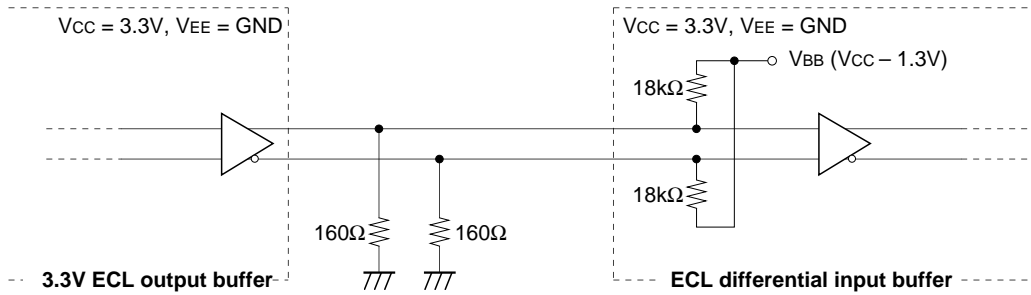


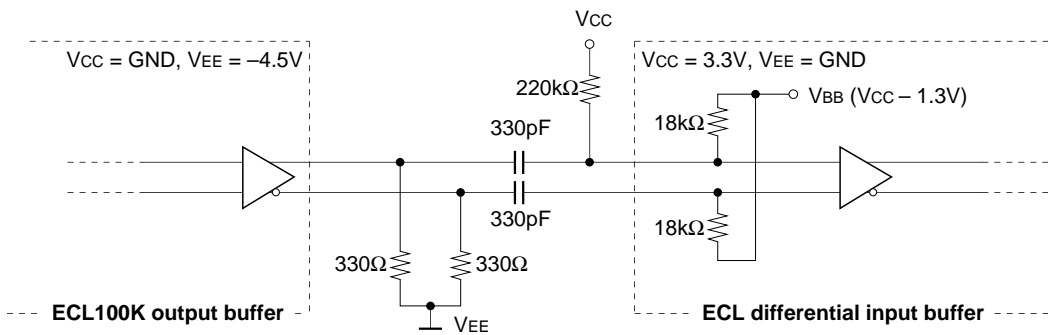
Fig. 1. External Part Circuit and Recommended Constants

2. ECL input circuit

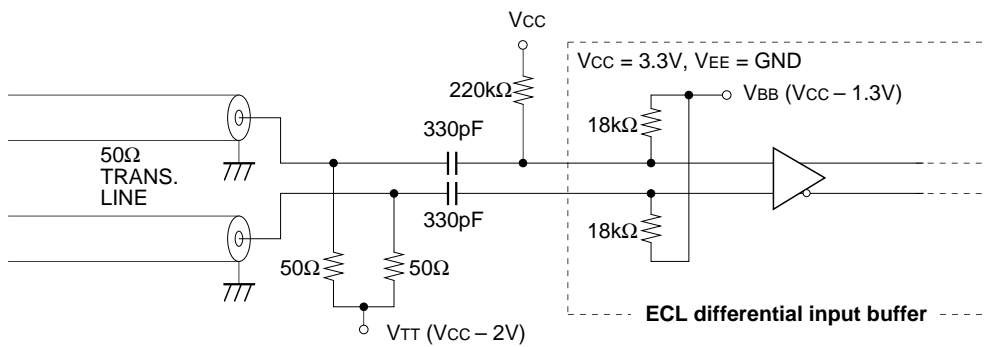
The ECL differential input pins are biased to V_{BB} ($V_{CC} - 1.3V$) via an $18k\Omega$ resistor in the IC. See the figures below for ECL differential input methods.



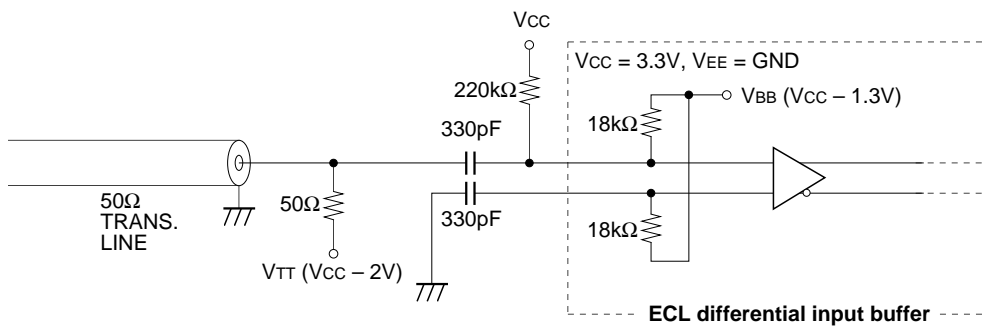
(a) ECL differential signal from 3.3V ECL output buffer



(b) ECL differential signal from ECL 100K output buffer



(c) ECL differential signal from 50Ω transmission line



(d) ECL single signal from 50Ω transmission line

Fig. 2. ECL Input Circuits

3. Power supply

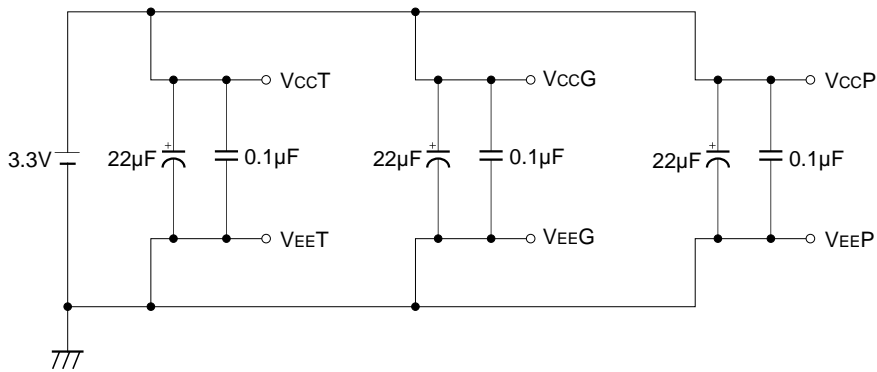
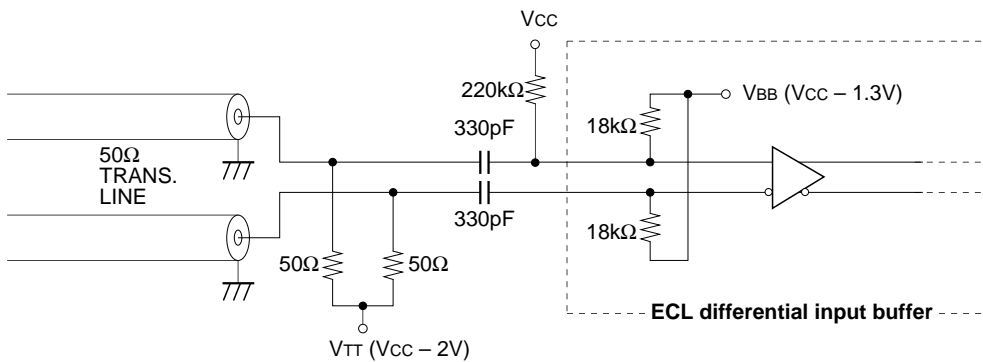


Fig. 3. Power Supply Circuit

4. SDIN, SDIN* inputs

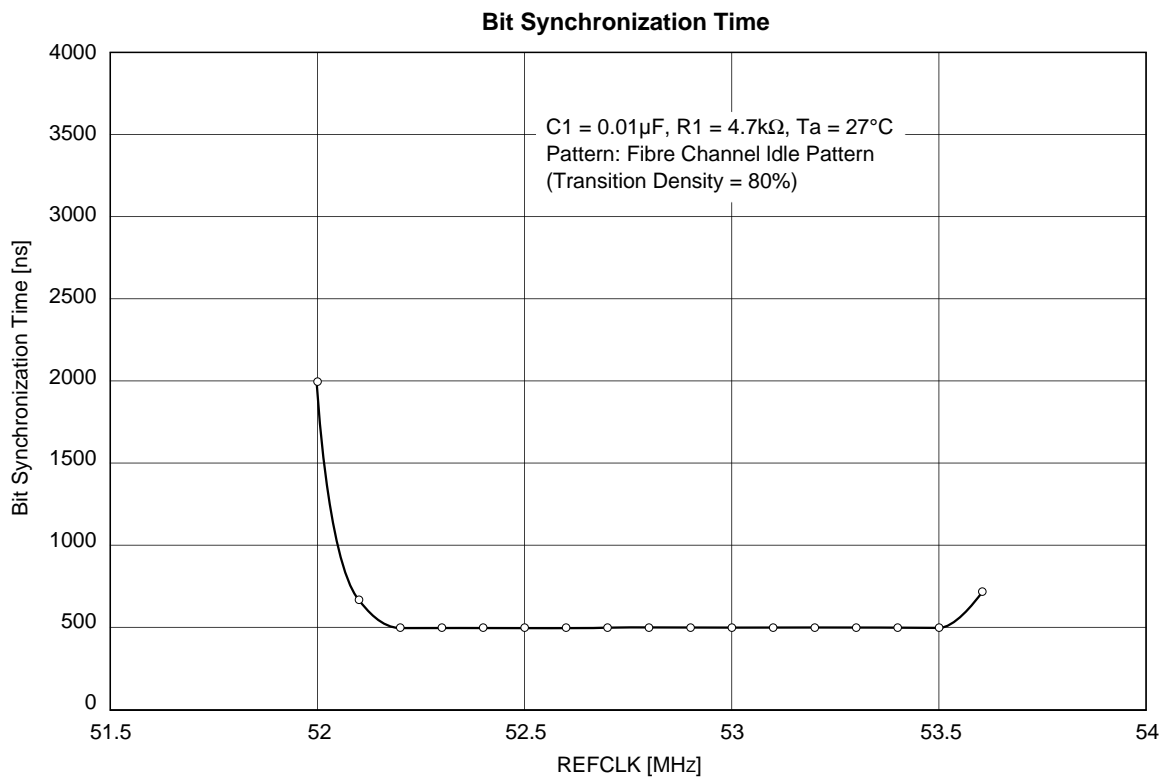
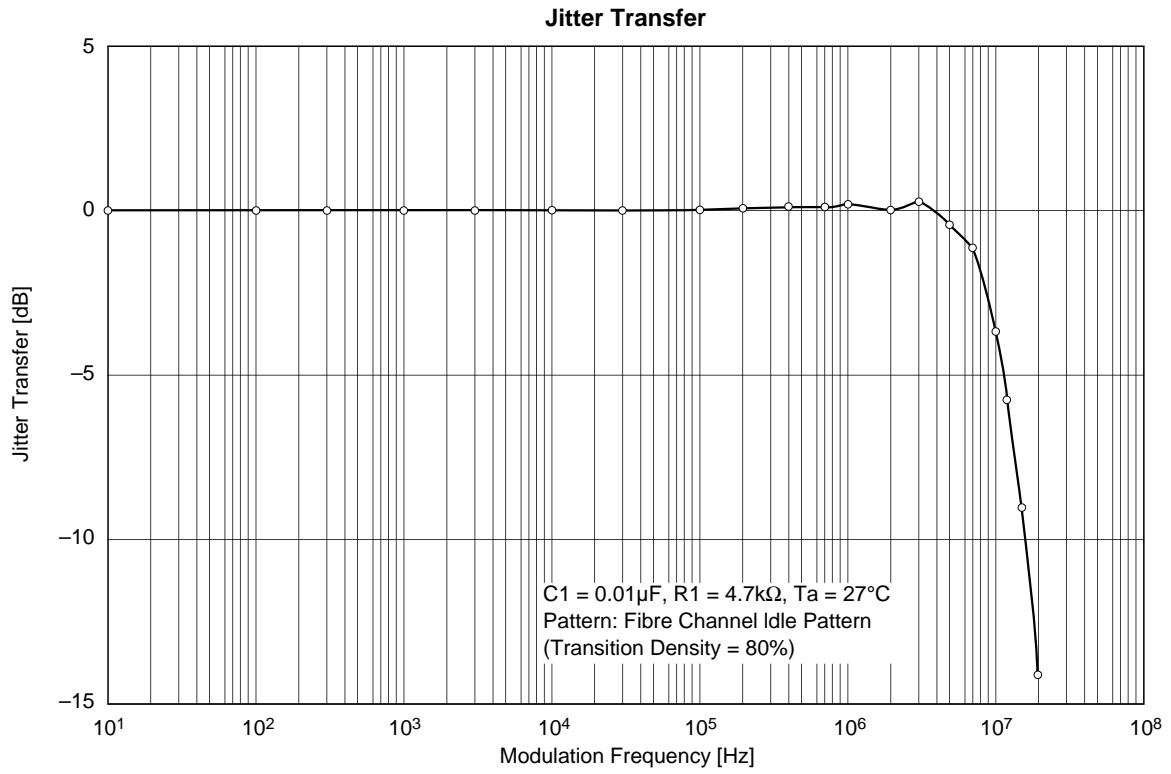
Normally, the VCO performs frequency comparison with the SDIN and SDIN* serial data. When there is no input to SDIN and SDIN*, frequency comparison is executed with REFCLK. However, the frequency may not be compared to REFCLK if the noise and others are detected as a signal for no signal state because the both phases of the ECL differential inputs are internally biased to V_{BB} shown below. As countermeasure to this, connect either of the differential inputs to V_{CC} via a resistor to generate the voltage difference for the both phases.



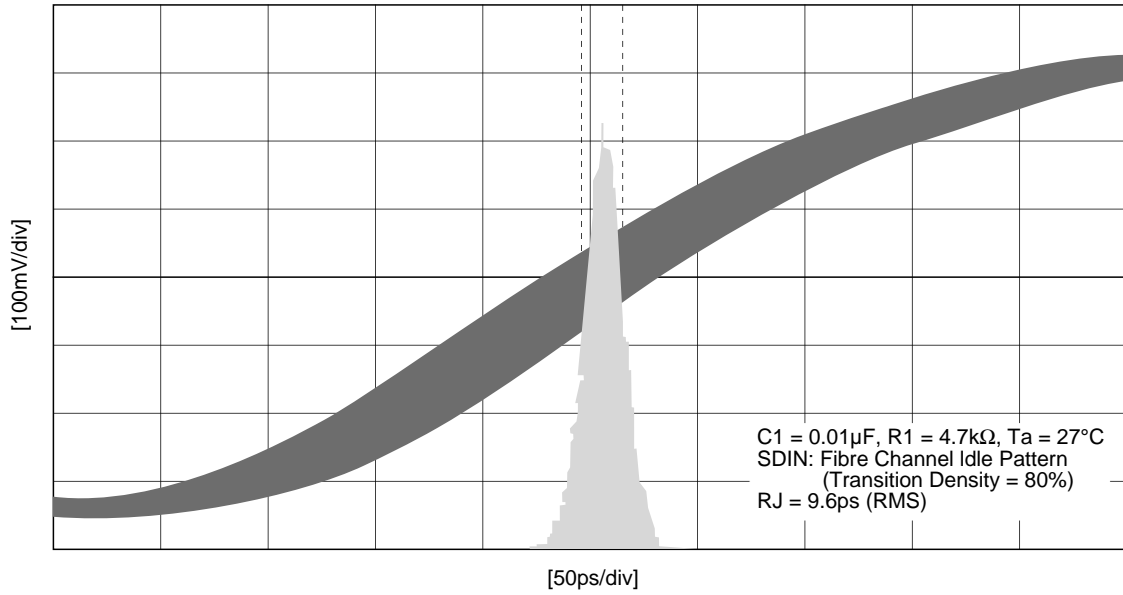
ECL differential signal from 50Ω transmission line

Fig. 4. SDIN and SDIN* Input Example

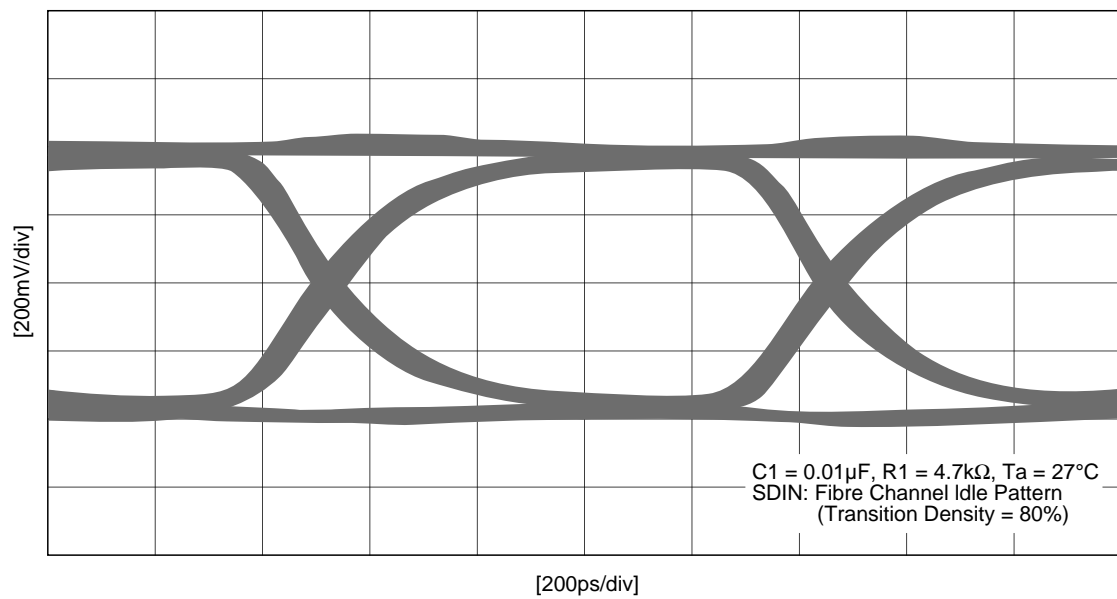
Example of Representative Characteristics



Example of Random jitter measurement (Retimed data 1.0625Gbps)



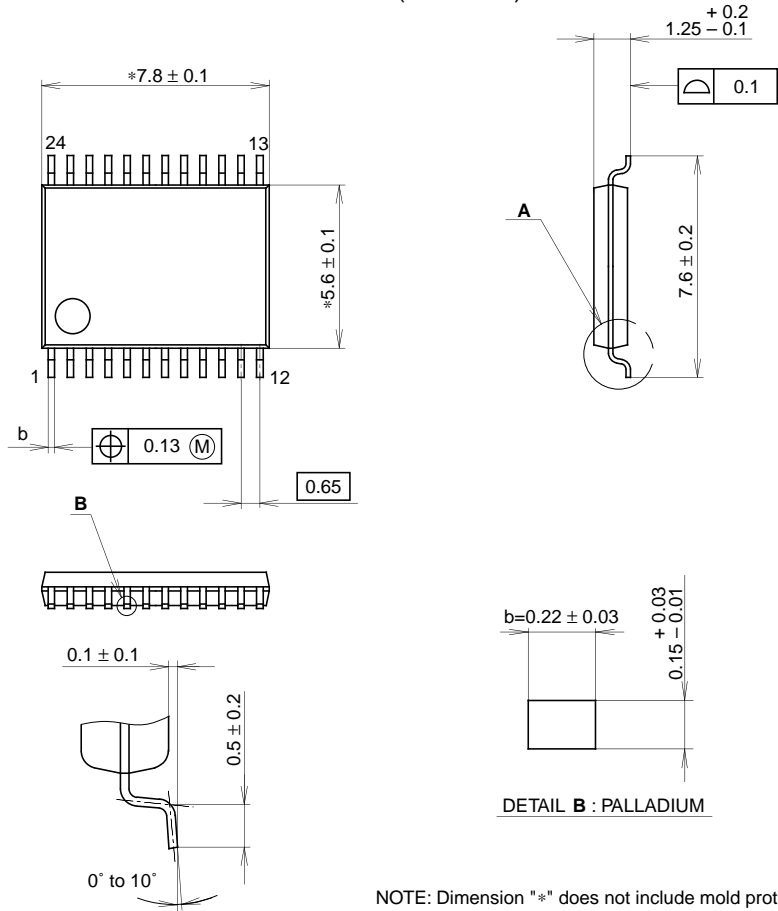
Eye pattern (Retimed data 1.0625Gbps)



Package Outline

Unit: mm

24PIN SSOP (PLASTIC)



DETAIL A

DETAIL B : PALLADIUM

NOTE: Dimension "*" does not include mold protrusion.

| | |
|------------|-----------------------|
| SONY CODE | SSOP-24P-L01 |
| EIAJ CODE | P-SSOP24-7.8x5.6-0.65 |
| JEDEC CODE | _____ |

PACKAGE STRUCTURE

| | |
|------------------|-------------------|
| PACKAGE MATERIAL | EPOXY RESIN |
| LEAD TREATMENT | PALLADIUM PLATING |
| LEAD MATERIAL | COPPER ALLOY |
| PACKAGE MASS | 0.1g |



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