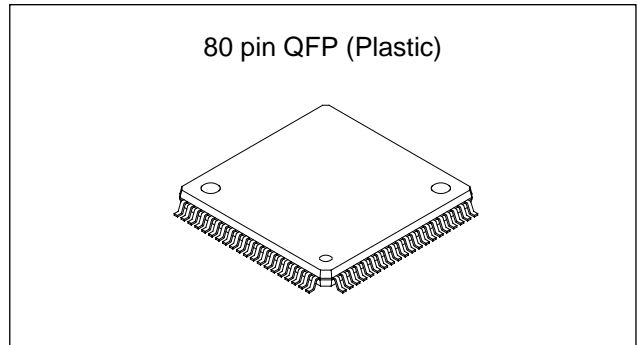


VGA/SVGA/XGA digital data serial receiver

Features

- 1 chip receiver for serial transmission of 18bit color VGA/SVGA/XGA picture
- On chip differential cable driver
- TTL/CMOS compatible interface
- Support 1 pixel/shiftclock mode & 2 pixel/shiftclock mode
- +3.3V single power supply
- Low power consumption
- 80pin Plastic QFP Package (Body size: 14mm × 14mm)



Block Diagram & Pin out

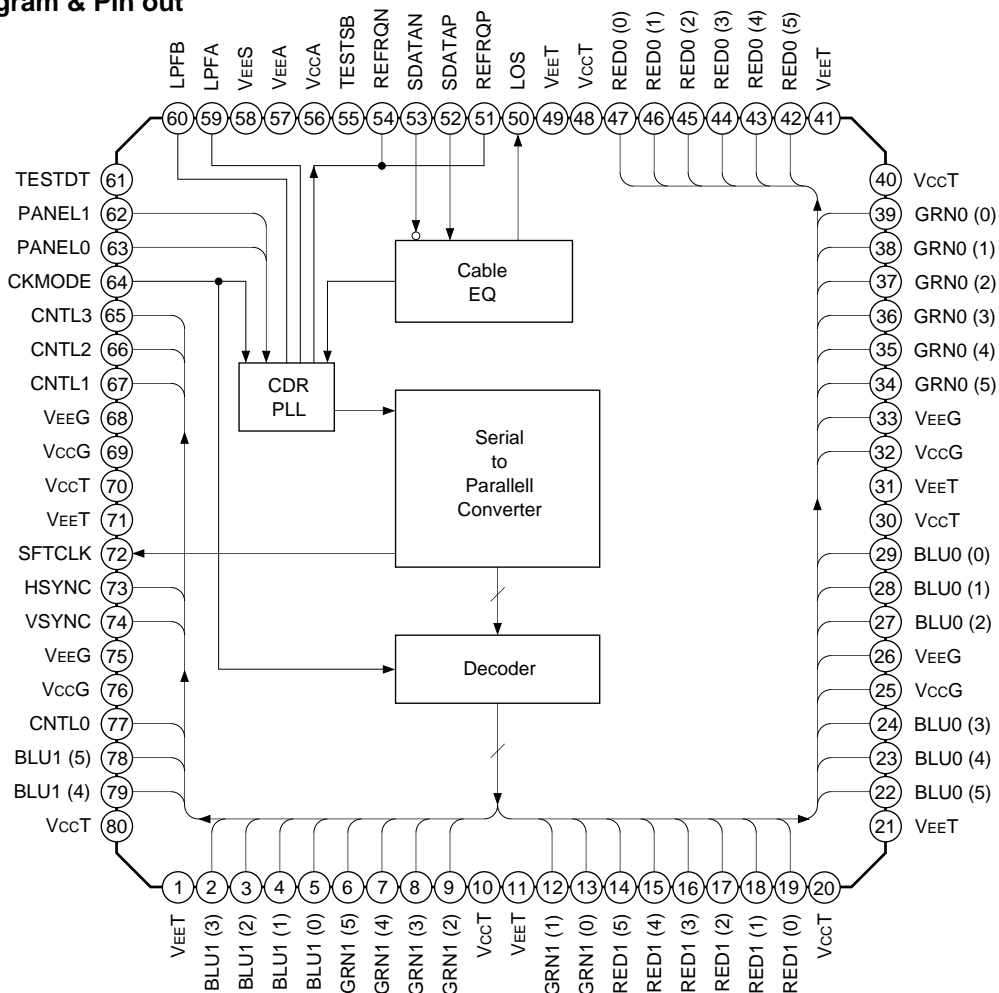


Fig. 1. Block Diagram & Pin out

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## Pin List

## Power/Ground

Pin Name	Pin Number	Descriptions
VccT	10, 20, 30, 40, 48, 70, 80	TTL power supply, should be connected to 3.3V $\pm$ 5%
VEET	1, 11, 21, 31, 41, 49, 71	TTL ground, connected to 0V
VccG	25, 32, 69, 76	Logical core power supply, connected to 3.3V $\pm$ 5%
VEEG	26, 33, 68, 75	Logical core ground, connected to 0V
VccA	56	Analog power supply, connected to 3.3V $\pm$ 5%
VEEA	57	Analog ground, connected to 0V
VEES	58	Analog substrate, connected to 0V

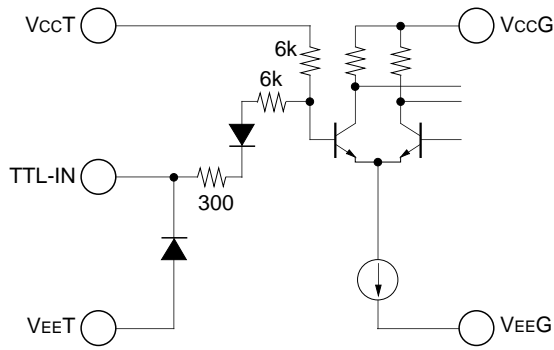
## Digital Signals

Pin Name	Pin Number	Type	Descriptions
SFTCLK	72	TTL out	Shift clock, for the data fetch at falling or rising edge
RED1 (5 to 0) GRN1 (5 to 0) BLU1 (5 to 0)	14, 15, 16, 17, 18, 19 6, 7, 8, 9, 12, 13 78, 79, 2, 3, 4, 5	TTL out	Pixel data input in 1 pixel/sftclk mode 2nd pixel data input in 2 pixel/sftclk mode
RED0 (5 to 0) GRN0 (5 to 0) BLU0 (5 to 0)	42, 43, 44, 45, 46, 47 34, 35, 36, 37, 38, 39 22, 23, 24, 27, 28, 29	TTL out	High fixed in 1 pixel/sftclk mode 1st pixel data input in 2 pixel/sftclk mode
HSYNC	73	TTL out	Hsync data
VSYNC	74	TTL out	Vsync data
CNTL (3 to 0)	65, 66, 67, 77	TTL out	Control data
PANEL (1, 0)	62, 63	TTL in	Panel mode select switch
CKMODE	64	TTL in	Clock mode select switch
LOS	50	TTL out	Los of signal
SDATAP/N	52, 53	Rx	Serial input
REFRQP/N	51, 54	Rx	Refclk request

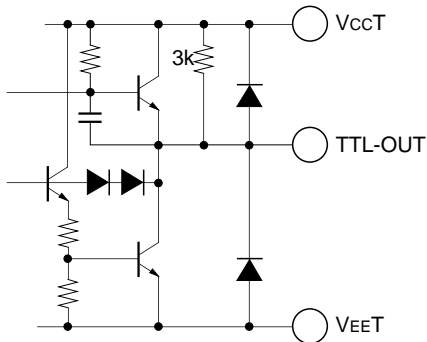
## Special

Pin Name	Pin Number	Descriptions
TESTSB/DT	55, 61	Polarity control of SFTCLK & TEST under fabrication
LPFA/B	59, 60	External loop filter

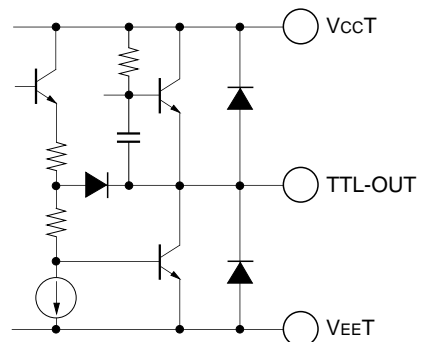
Equivalent I/O circuit



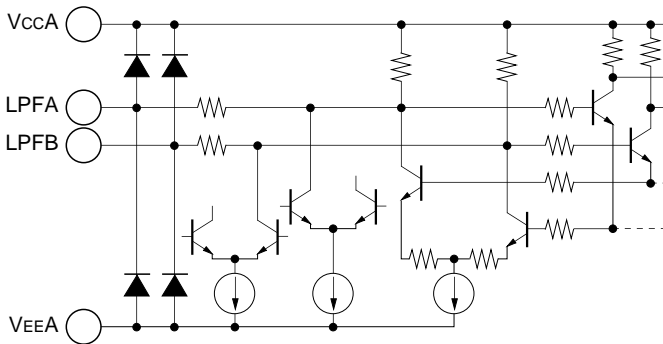
(a) TTL input equivalent circuit



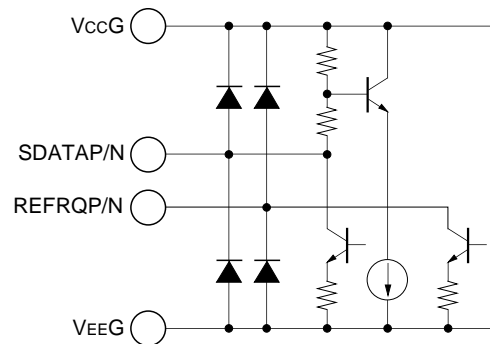
(b) TTL output equivalent circuit  
SFTCLK, LOS



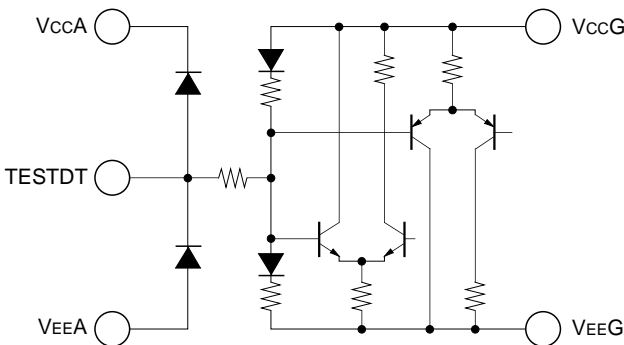
(b') TTL output equivalent circuit  
REDxx, GRNxx, BLUxx, H/V sync, CNTLx



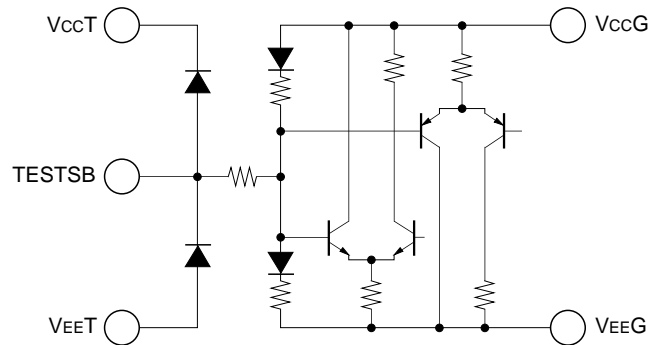
(c) LPFA/B equivalent circuit



(d) SDATAP/N REFRQP/N equivalent circuit



(e) TESTDT equivalent circuit



(f) TESTSB equivalent circuit

## Electrical characteristics

Tab. 1. Absolute Maximum Rating

Description	Symbol	Min.	Typ.	Max.	Unit	Comments
Power supply voltage	V <sub>CC</sub>	-0.3		4	V	
TTL DC input voltage	V <sub>I_T</sub>	-0.5		5.5	V	
TTL output current (High)	I <sub>OH_T</sub>	-20		0	mA	
TTL output current (Low)	I <sub>OL_T</sub>	0		20	mA	
Serial output pin voltage	V <sub>sdout</sub>	-0.5		V <sub>CC</sub> + 0.5	V	
Ambient temperature	T <sub>a</sub>	-55		60	°C	Under bias
Storage temperature	T <sub>stg</sub>	-65		150	°C	

Tab. 2. Recommended Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit	Comments
Power supply voltage (Include V <sub>CC</sub> T5)	V <sub>CC</sub>	3.135	3.3	3.465	V	
Ambient temperature	T <sub>a</sub>	0		60	°C	

Tab. 3. DC Characteristics (Under the recommended conditions. See Tab. 2)

Description	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input HIGH voltage (TTL)	V <sub>IH_T</sub>	2		5.5	V	
Input LOW voltage (TTL)	V <sub>IL_T</sub>	-0.5		0.8	V	
Input HIGH current (TTL)	I <sub>IH_T</sub>			20	μA	V <sub>IN</sub> = V <sub>CC</sub>
Input LOW current (TTL)	I <sub>IL_T</sub>	-400			μA	V <sub>IN</sub> = 0
Output HIGH voltage (TTL)	V <sub>OH_T</sub>	2.25			V	I <sub>OH</sub> = -0.2mA
Output LOW voltage (TTL)	V <sub>OL_T</sub>			0.4	V	I <sub>OL</sub> = 4mA
Output HIGH current (REFREQ)	I <sub>OH_RQ</sub>	-0.1	0	+0.1	mA	See Fig. 2
Output LOW current (REFREQ)	I <sub>OL_RQ</sub>	7.4	8.0	8.6	mA	
Input dynamic range (SDATA)	V <sub>IM_SD</sub>	V <sub>CC</sub> - 0.4		V <sub>CC</sub> + 0.2	V	Common mode voltage
Input dynamic range (SDATA)	V <sub>ID_SD</sub>	-0.5		+0.5	V	Differential voltage
Supply current	I <sub>CC</sub>	230	310	390	mA	2 pixel/sftclk, Outputs open 1 pixel/sftclk, Outputs open
		220	300	380	mA	

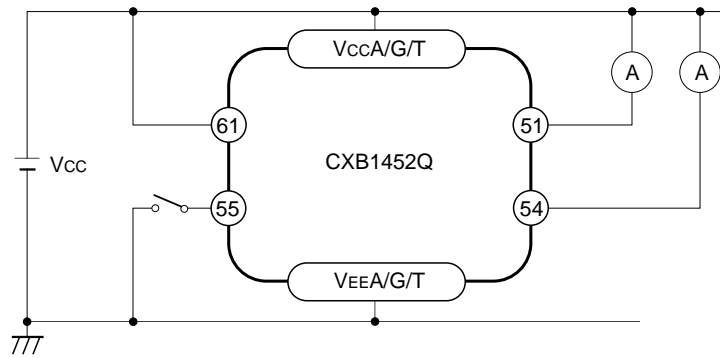


Fig. 2. IOH\_RQ and IO\_L\_RQ DC measurement

Tab. 4. AC Characteristics (Under the recommended conditons. See Tab. 5)

Description	Symbol	Min.	Typ.	Max.	Unit	Conditions
SFTCLK frequency	Fsftclk	20.0	25.0	28.0	MHz	VGA, 1 pixel/sftclk mode
		10.0	12.5	14.0	MHz	VGA, 2 pixel/sftclk mode
		38.0	40.0	48.0	MHz	SVGA, 1 pixel/sftclk mode
		19.0	20.0	24.0	MHz	SVGA, 2 pixel/sftclk mode
		60.0	65.0	68.0	MHz	XGA, 1 pixel/sftclk mode
		30.0	32.5	34.0	MHz	XGA, 2 pixel/sftclk mode
SFTCLK duty factor	Dsftclk	35		65	%	Vth = 1.4V, CL = 10pF
Pixel/Sync/Cntl setup to SFTCLK	Tsetup	24.0			ns	Vth = 1.4V, CL = 10pF
		11.0			ns	VGA, 1 pixel/sftclk 25MHz
		3.5			ns	SVGA, 1 pixel/sftclk 40MHz
		20.0			ns	XGA, 1 pixel/sftclk 65MHz
		20.0			ns	XGA, 2 pixel/sftclk 32.5MHz
Pixel/Sync/Cntl hold to SFTCLK	Thold	6.5			ns	Vth = 1.4V, CL = 10pF
		4.0			ns	VGA, 1 pixel/sftclk 25MHz
		2.5			ns	SVGA, 1 pixel/sftclk 40MHz
		1.0			ns	XGA, 1 pixel/sftclk 65MHz
		1.0			ns	XGA, 2 pixel/sftclk 32.5MHz
SFTCLK rise time	Torc			4.0	ns	0.8V to 2.0V, CL = 10pF
SFTCLK fall time	Tofc			3.0	ns	2.0V to 0.8V, CL = 10pF
Pixel/Sync/Cntl rise time	Tord			7.0	ns	0.8V to 2.0V, CL = 10pF
Pixel/Sync/Cntl fall time	Tord			6.0	ns	2.0V to 0.8V, CL = 10pF
CLOCK mode assert time	TAclk		0.9		µs	
CLOCK mode deassert time	TDclk		50		µs	
LOS signal assert time	TAlos		0.8		µs	
LOS signal deassert time	TDlos		0.1		µs	

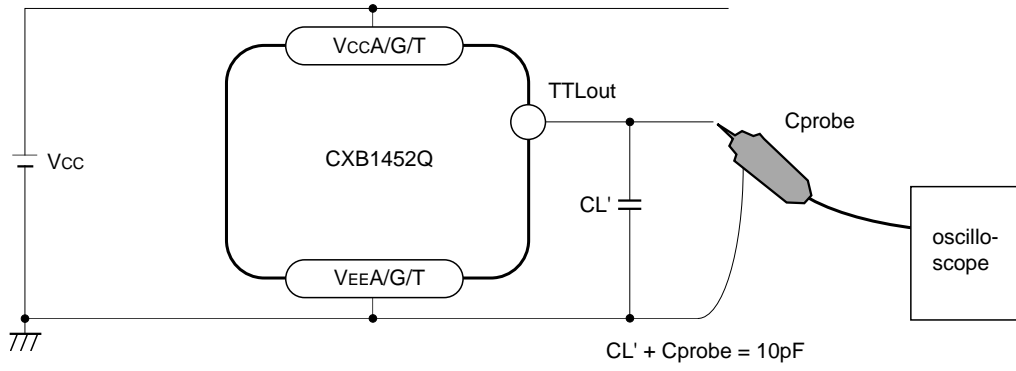


Fig. 3. SDATA waveform measurement

Timing Chart

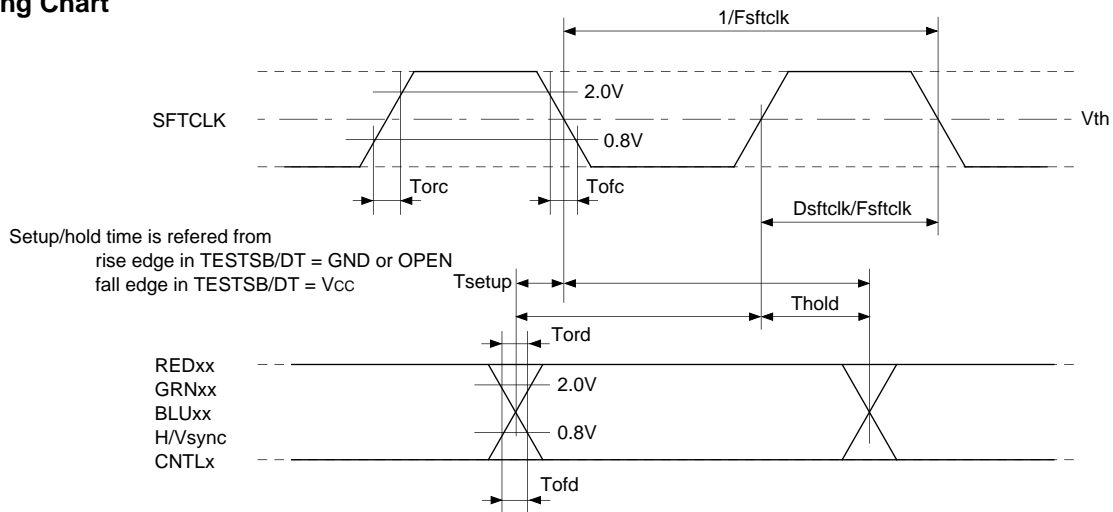


Fig. 4. TTL output timing

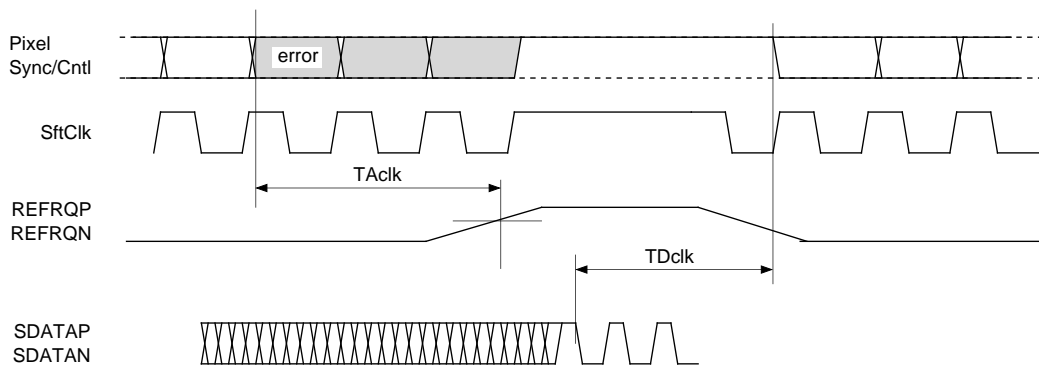


Fig. 5. Refclk request timing

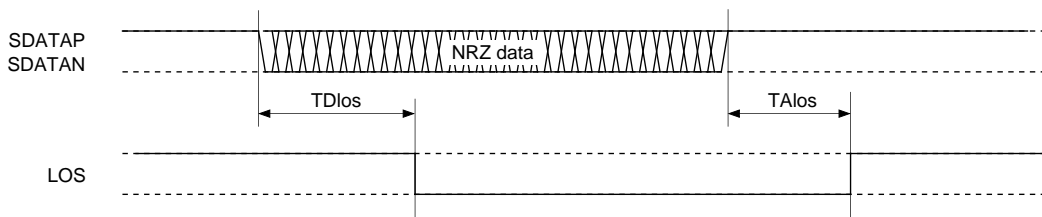


Fig. 6. Idle mode timing

**Operation mode**

CXB1452Q supports 3 panel mode and 2 clock mode switched by the PANEL (1, 0) and CKMODE pin according to the Tab. 5 & 6. The supporting color depth and clock rate are summarized in Tab. 7. These pins are open High TTL inputs.

**Tab. 5. Panel Mode select**

PANEL1	PANEL0	Supporting panel size & color
L	L	VGA (640 × 480) 18bit color
L	H	SVGA (800 × 600) 18bit color
H	L	XGA (1024 × 768) 18bit color
H	H	not supported

**Tab. 6. Clock Mode select**

CKMODE	Supporting clock mode
L	2 pixel/ShiftClock (2ppc)
H	1 pixel/ShiftClock (1ppc)

**Tab. 7. Operation Mode**

Panel Mode	Clock Mode	Color	Shift Clock	Dot Clock	Serial rate
VGA	1 pixel/SftClk	18bit	25MHz	25MHz	600Mbps
	2 pixel/SftClk	18bit	12.5MHz	25MHz	600Mbps
SVGA	1 pixel/SftClk	18bit	40MHz	40MHz	960Mbps
	2 pixel/SftClk	18bit	20MHz	40MHz	960Mbps
XGA	1 pixel/SftClk	18bit	65MHz	65MHz	1560Mbps
	2 pixel/SftClk	18bit	32.5MHz	65MHz	1560Mbps

TESTSB/TESTDT pins select the trigger edge of SFTCLK and test mode according to Tab. 8.

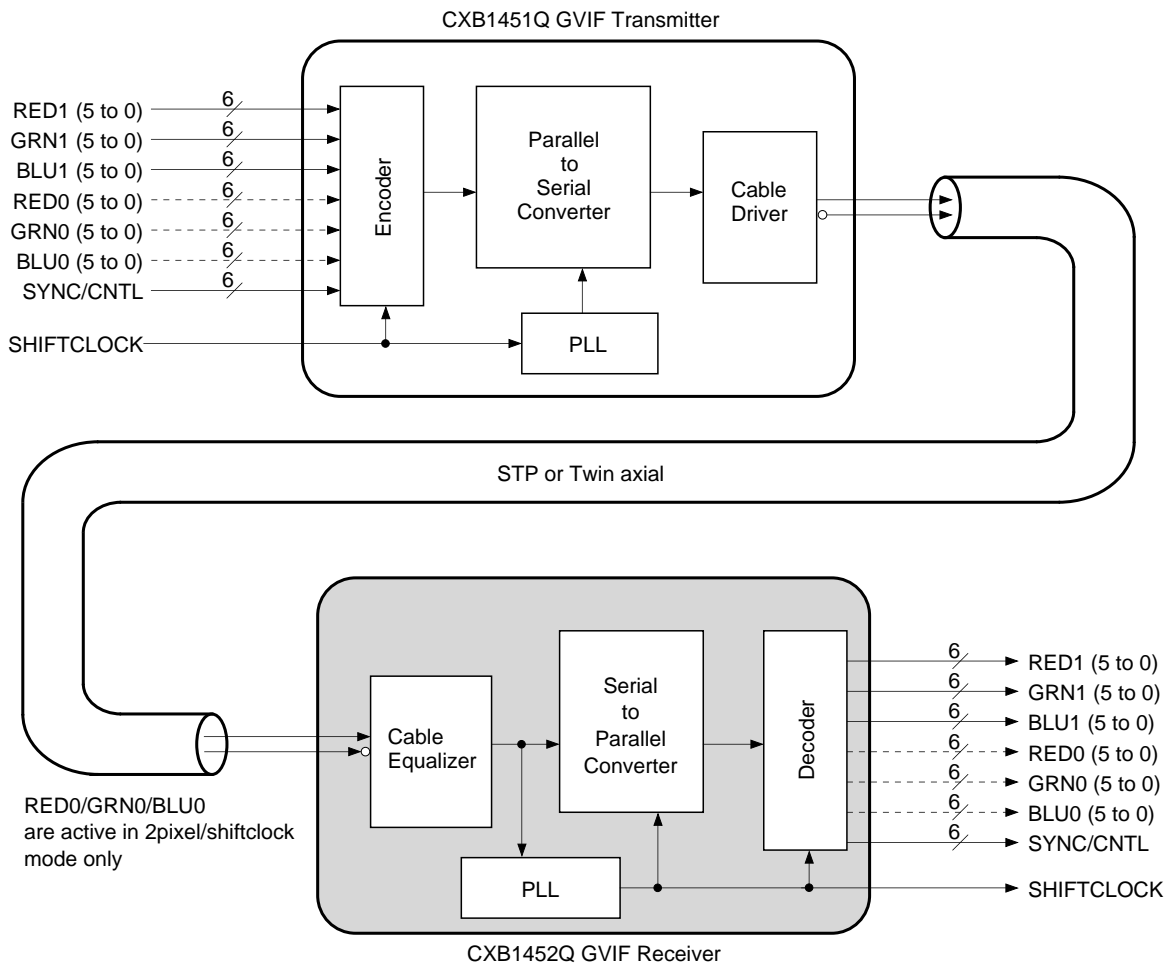
**Tab. 8. SFTCLK polarity & TEST mode**

		TESTSB		
		GND	OPEN	V <sub>cc</sub>
TESTDT	GND	Receiver operation trigger = rising edge		Fabricator reserved TEST mode
	OPEN			
	V <sub>cc</sub>	All TTL out = Low	All TTL out = High	Trigger = falling edge

LOS pin shows the absence of proper level of SDATA signal. LOS pin is High when connector is disconnected or transmitter is idle.

**Applications**

CXB1452Q GVIF receiver is applied to the digital RGB signal transmission for  
 P/C with LCD monitor  
 Video on demand system  
 Monitoring system  
 Graphical controller  
 Projector  
 Digital TV monitor  
 with GVIF transmitter, CXB1451Q.

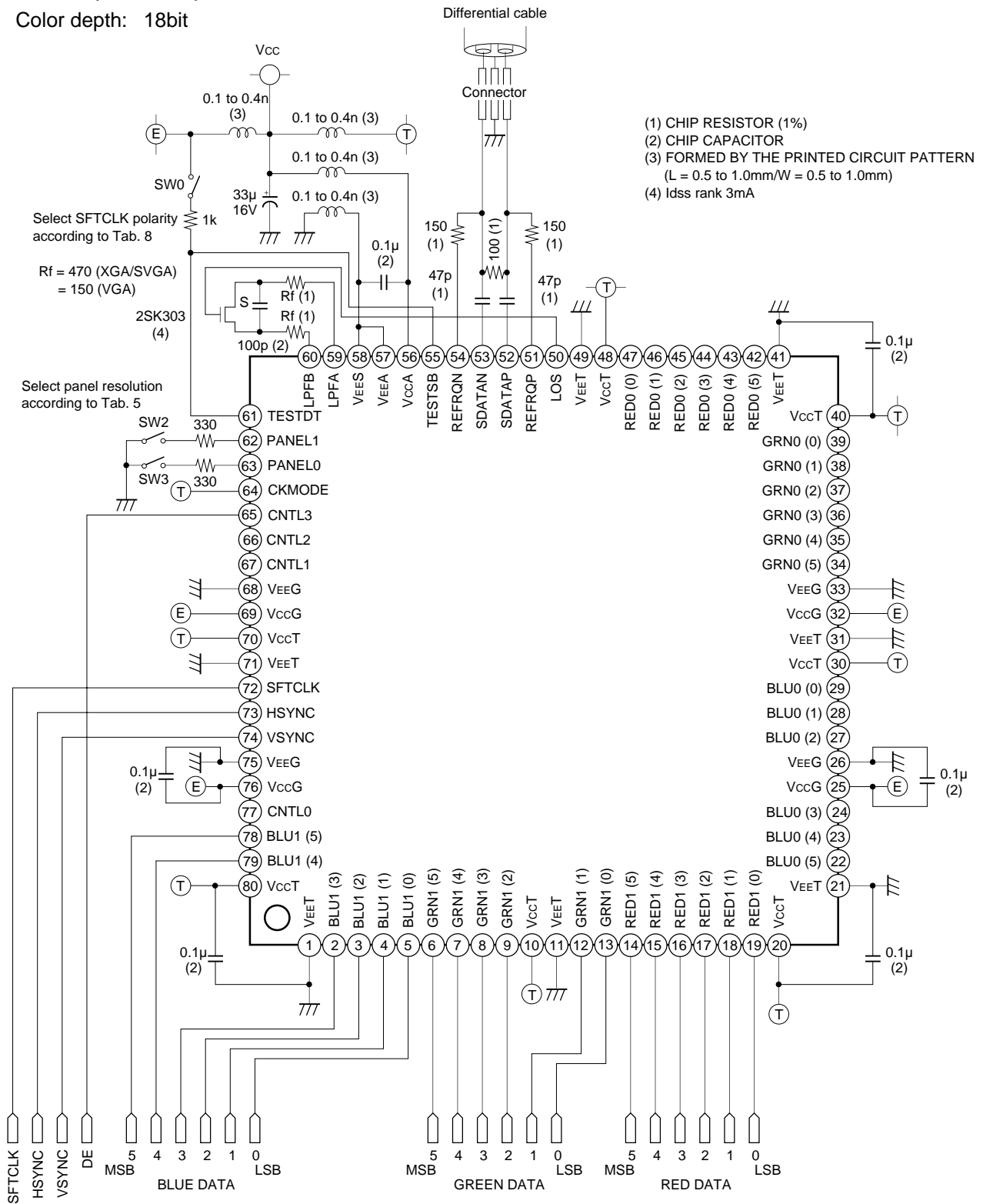


Application Circuit (A)

Clock mode: 1 pixel/sftclk (1ppc)

Picture sync: H/V sync & DE

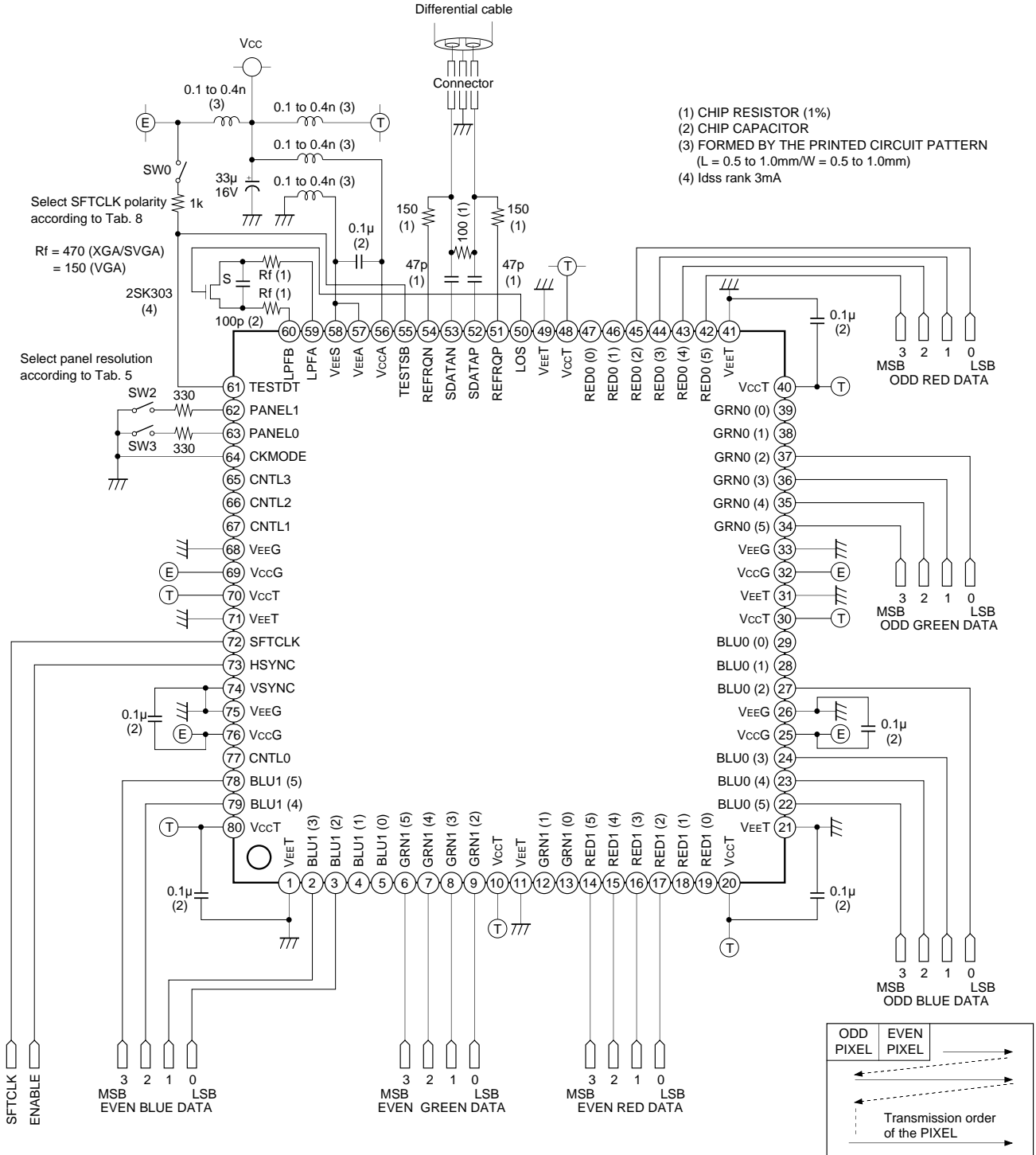
Color depth: 18bit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit (B)

Clock mode: 2 pixel/sftclk  
 Picture sync: ENABLE only  
 Color depth: 12bit



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Recommended Printed Circuit Board Structure

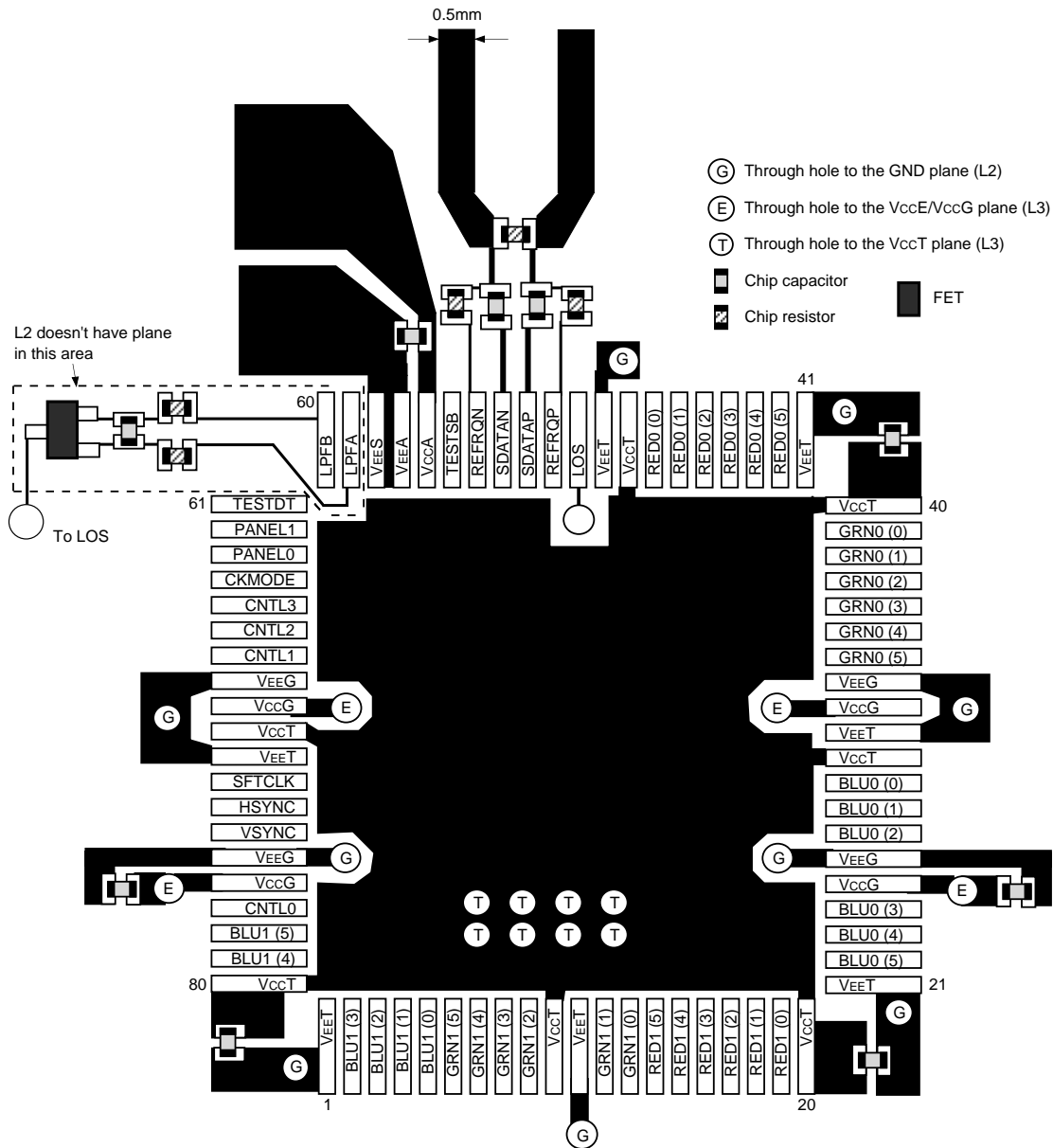


- L1: Cu plate (18μm) + solder coat
- I1: Adhesive Sheet (0.3mm ± 0.09mm)
- L2: Cu plate (36μm)
- I2: Fiber-glass epoxy core (0.8mm)
- L3: Cu plate (36μm)
- I3: Adhesive Sheet (0.3mm)
- L4: Cu plate (18μm) + solder coat

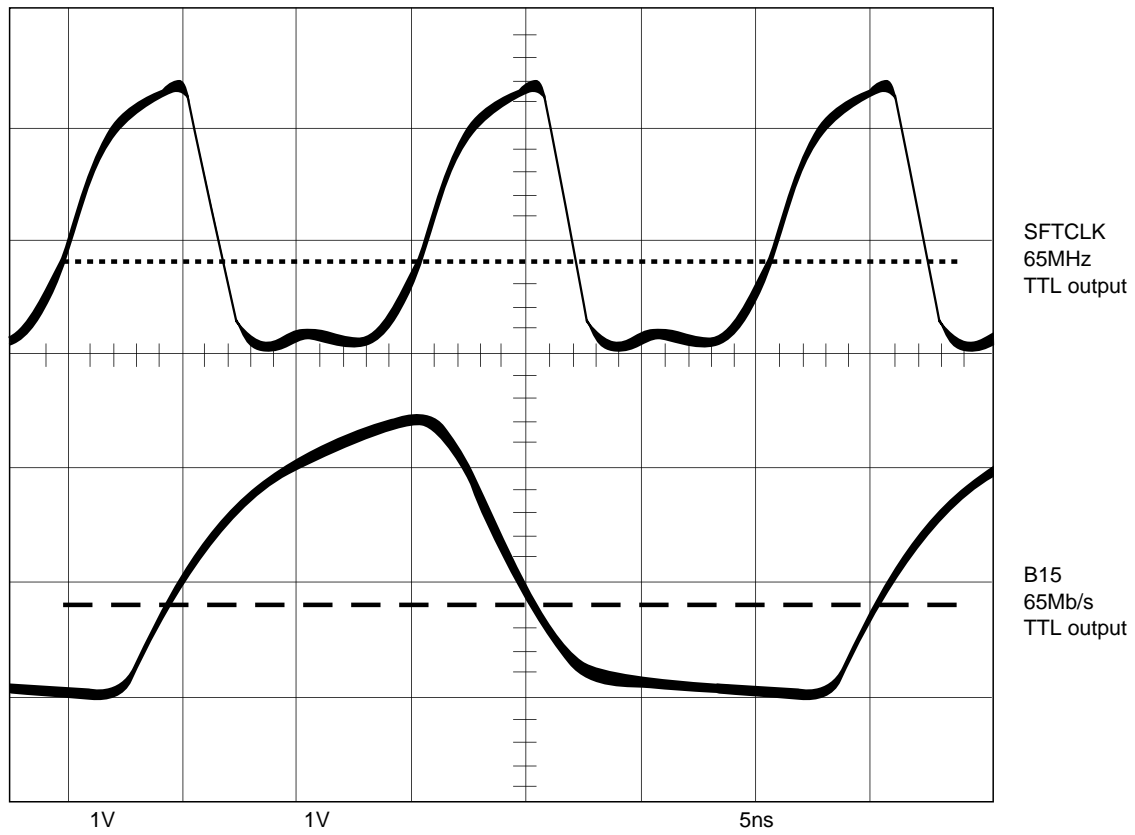
Recommended Printed Circuit Board Pattern

SDATAP/SDATAN pins to the connector path      W = 0.50mm (Z0 = 50Ω)  
 other path      W = 0.25mm

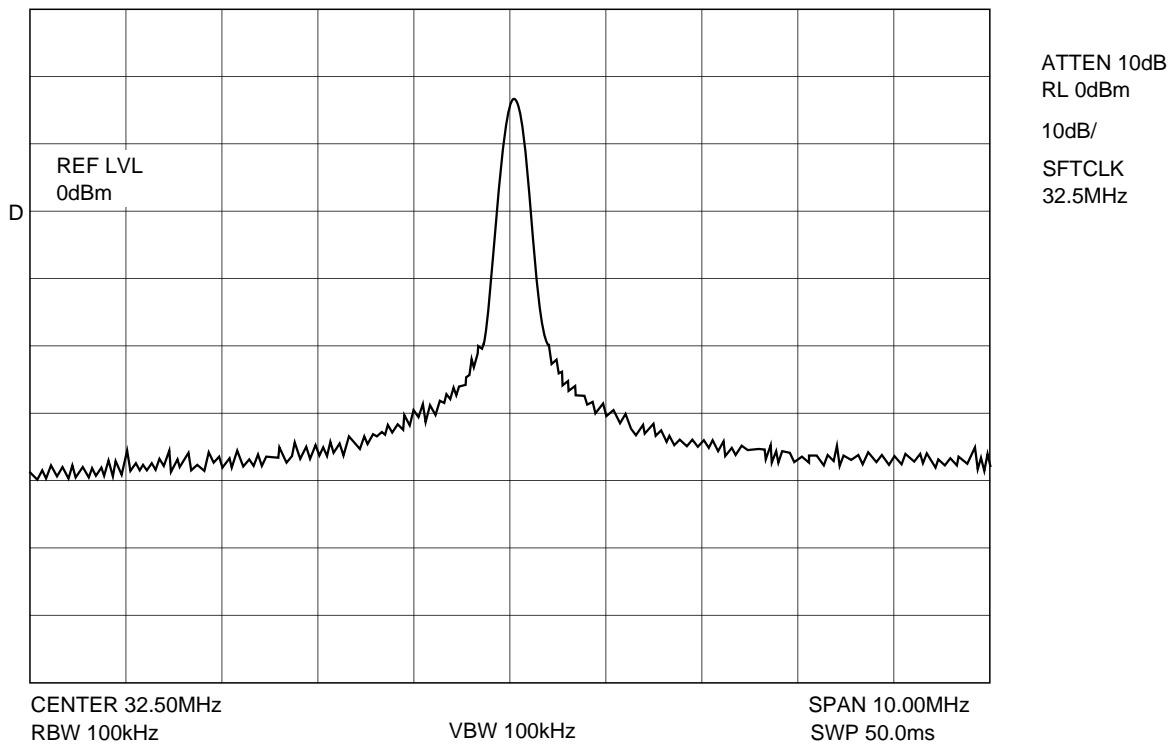
POWER and special signal routing example



TTL output waveform with  $C_L = 10\text{pF}$



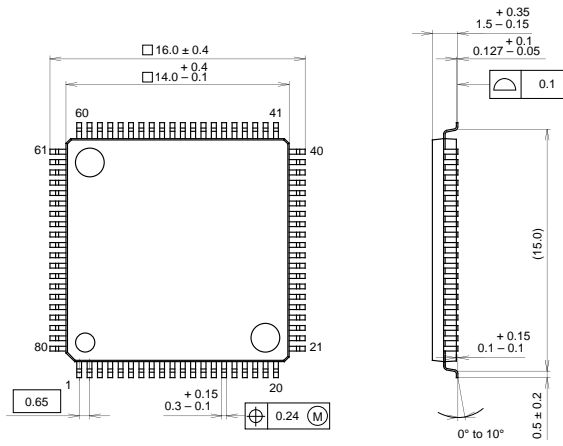
SFTCLK Power spectrum



Package Outline

Unit: mm

80PIN QFP (PLASTIC)



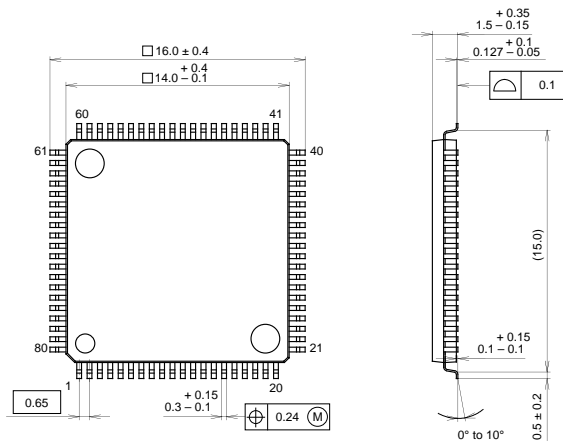
PACKAGE STRUCTURE

SONY CODE	QFP-80P-L03
EIAJ CODE	QFP080-P-1414
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.6g

Kokubu Ass'y

80PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-80P-L03
EIAJ CODE	QFP080-P-1414
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.6g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	42 ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18 $\mu$ m



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