SONY

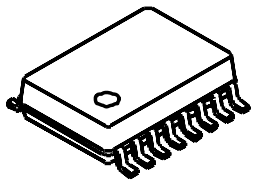
CXA3328TN/EN

Analog Signal Processor RX-IF IC for W-CDMA Cellular Phones

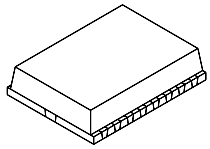
Description

The CXA3328TN/EN is an analog signal processor RX-IF IC for W-CDMA cellular phones. This IC contains a gain control amplifier and quadrature demodulator.

16 pin TSSOP (Plastic)



16 pin VSON (Plastic)



Features

- Wide gain control range
- Linear gain slope
- Wide band (100 to 600MHz)
- Small package
  - 16-pin TSSOP (CXA3328TN)
  - 16-pin VSON (CXA3328EN)
- Low voltage operation (2.7 to 3.3V)

Absolute Maximum Ratings

• Supply voltage	V_{CC}	–0.3 to 5.5	V
• Operating temperature	Topr	–55 to +125	°C
• Storage temperature	Tstg	–65 to +150	°C

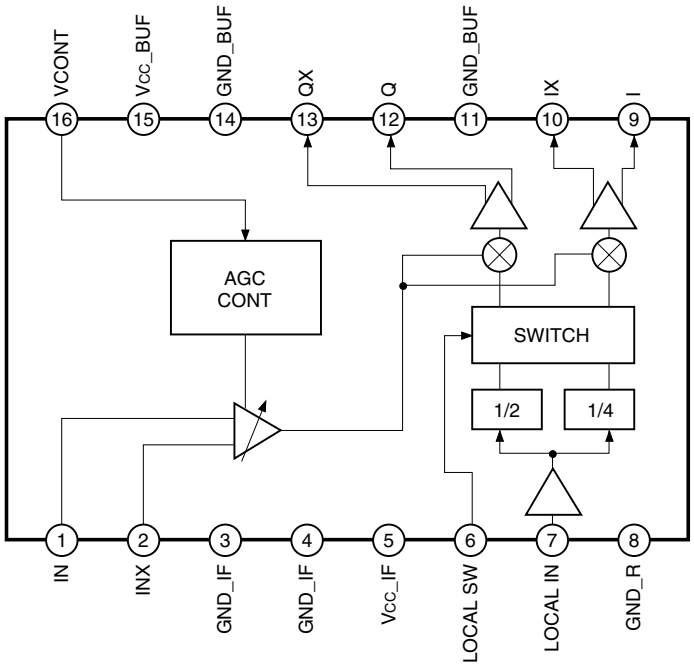
Operating Conditions

• Supply voltage	V_{CC}	2.7 to 3.3	V
• Operating temperature	Ta	–25 to +85	°C

Structure

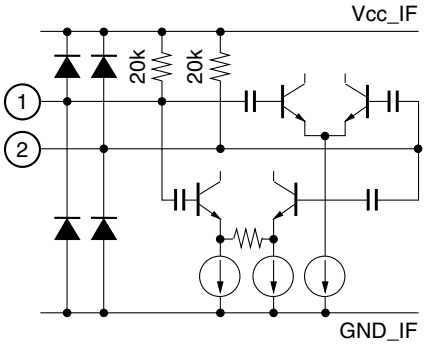
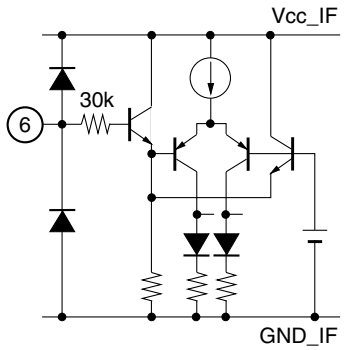
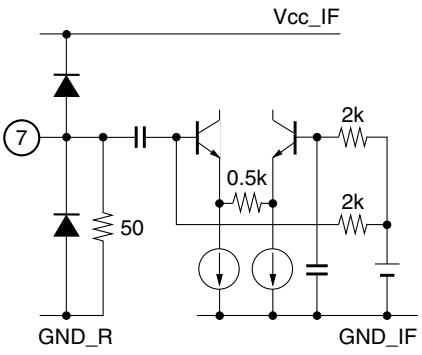
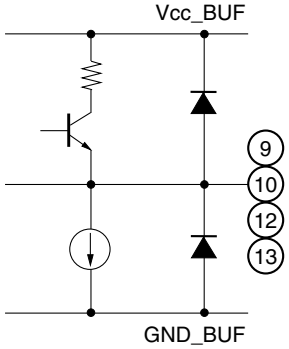
Bipolar silicon monolithic IC

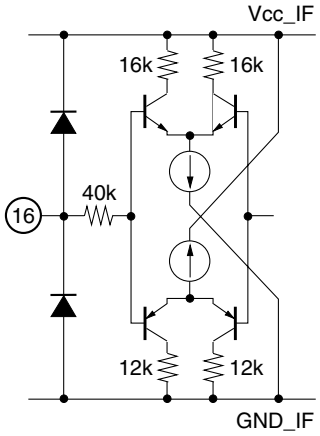
Block Diagram



E00738D24-PS

Pin Description

Pin No.	Symbol	Typical pin voltage [V]	Equivalent Circuit	Pin Description
1, 2	IN, INX	2.85		IF differential input.
3, 4	GND_IF	0		GCA, quadrature demodulator block ground.
5	Vcc_IF	2.85		GCA, quadrature demodulator block Vcc.
6	LOCAL SW	—		Local frequency division ratio setting. High: 1/4 frequency division Low: 1/2 frequency division
7	LOCAL IN	—		Local input.
8	GND_R	0		Local signal GND.
9, 10, 12, 13	I, IX, Q, QX	1.5		Baseband I, Q outputs.

Pin No.	Symbol	Typical pin voltage [V]	Equivalent Circuit	Pin Description
11, 14	GND_BUF	0		Output buffer block ground.
15	Vcc_BUF	2.85		Output buffer block Vcc.
16	VCONT	—		Gain control voltage input.

Electrical Characteristics

Current Consumption

(V_{CC} = 2.85V, Ta = 27°C)

Item	Symbol	Conditions	Measure-ment circuit	Measure-ment point	Min.	Typ.	Max.	Unit
Current Consumption	Icc	Vcont = 1.3V	1	A	8	11	15	mA

I/O Resistance

(V_{CC} = 2.85V, Ta = 27°C)

Item	Symbol	Conditions	Measure-ment circuit	Measure-ment point	Min.	Typ.	Max.	Unit
Input resistance VCONT pin	R_{IVC}	DC measurement: V_{IN} = 2.85V	1	B	10	—	—	kΩ
LO input resistance	R_{ILO}	DC measurement: I_{IN} = 2mA	1	C	37.5	50	62.5	Ω
Output resistance I, IX, Q, QX pins	Z_{OUT}	DC measurement: I_{OUT} = 100µA	1	D, E F, G	80	250	550	Ω

IF I/O Resistance (Design Values)

(V_{CC} = 2.85V, Ta = 27°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
IF input resistance	R_{IIF}	Differential between Pins 1 and 2 380MHz	—	2.6	—	kΩ
IF input capacitance	C_{IIF}	Differential between Pins 1 and 2 380MHz	—	2	—	pF

Input Conditions

(V_{CC} = 2.85V, Ta = 27°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
IF input frequency 1	F_{RXIF1}	LOCAL SW = “L”	—	380	—	MHz
IF input frequency 2	F_{RXIF2}	LOCAL SW = “H”	—	190	—	MHz
LO input frequency	F_{LO}		—	760	—	MHz
LO input level	V_{LO}		–18	–15	–12	dBm

GCA Block (V_{CC} = 2.85V, Ta = 27°C)

Item	Symbol	Conditions	Measure-ment circuit	Measure-ment point	Min.	Typ.	Max.	Unit
Input conversion noise figure	NF	Gain = +65dB	3	A, B C, D	—	—	10	dB
Input conversion 3rd intercept point	IIP3_1	Gain = +65dB F_{RXIF} = 382MHz F_{LO} = 760MHz LOCAL SW = "L"	2	A, B C, D	–58	—	—	dBm
	IIP3_2	Gain = –10dB F_{RXIF} = 382MHz F_{LO} = 760MHz LOCAL SW = "L"	2	A, B C, D	–10	—	—	dBm
Gain flatness	G_F	F_{RXIF} = 382 ± 2.5MHz LOCAL SW = "L" $F_{LO} = 2 \times (F_{RXIF} + 2)$ MHz	2	A, B C, D	–0.25	—	0.25	dB
Minimum gain	G_{MIN}	Vcont = 0.3 [V], 30mVp-p differential output F_{RXIF} = 382MHz F_{LO} = 760MHz LOCAL SW = "L"	2	A, B C, D	—	–25.5	–20.5	dB
Maximum gain	G_{MAX}	Vcont = 2.3 [V], 100mVp-p differential output F_{RXIF} = 382MHz F_{LO} = 760MHz LOCAL SW = "L"	2	A, B C, D	67.5	72.5	—	dB
Gain temperature error	G_{ERR}	Ta = –25 to +85°C	2	A, B C, D	–4	—	4	dB

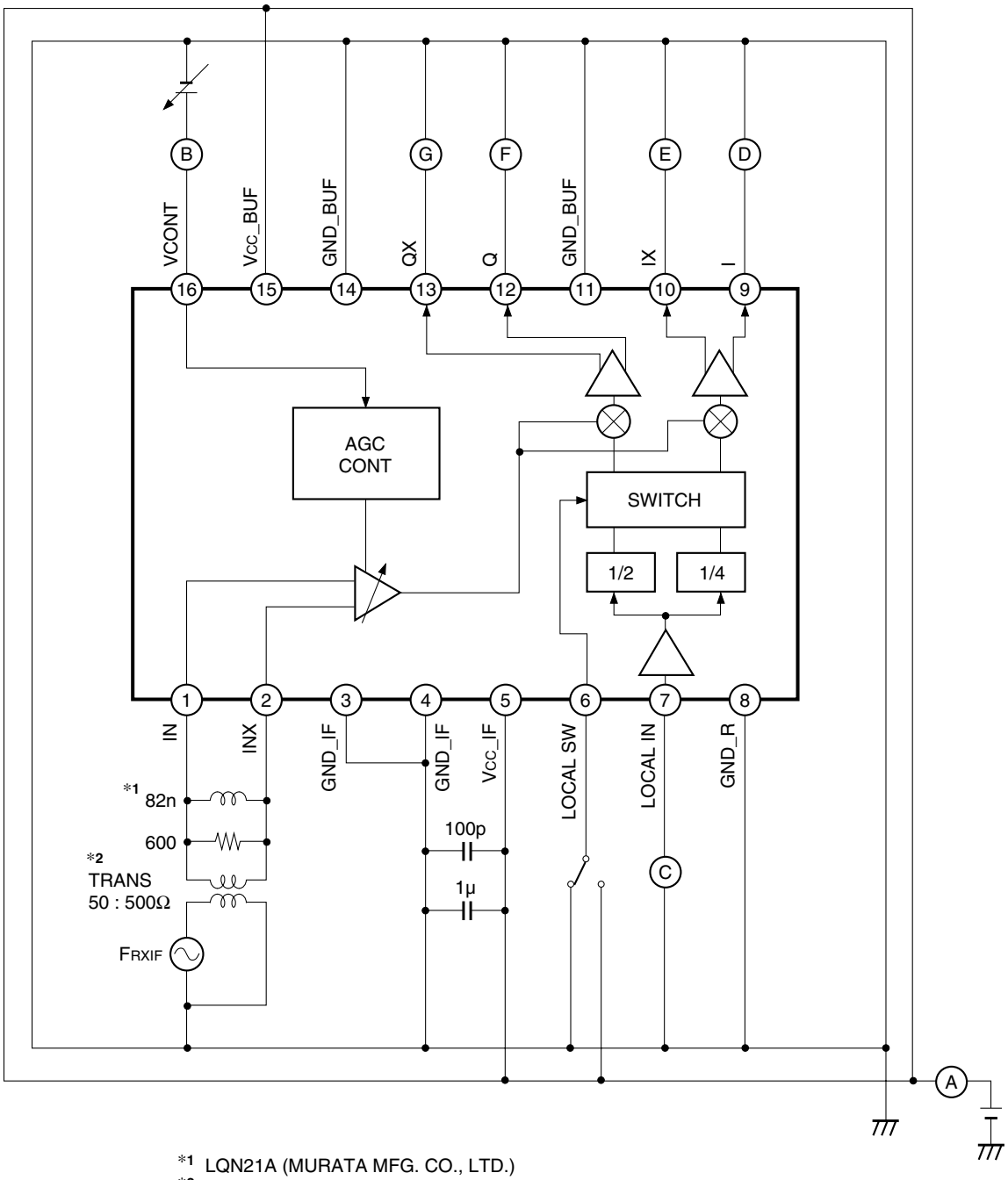
Quadrature Demodulator Block (V_{CC} = 2.85V, Ta = 27°C)

Item	Symbol	Conditions	Measure-ment circuit	Measure-ment point	Min.	Typ.	Max.	Unit
I/Q maximum output amplitude	V_{MAX}	R_L = 10kΩ, C_L = 10pF F_{RXIF} = 382MHz F_{LO} = 760MHz LOCAL SW = "L"	2	A, B C, D	500	—	—	mVp-p
I/Q output band width	V_{BW}	–3dB band width	2	A, B C, D	5	13	—	MHz
I/Q phase error	P_{ERR}	F_{RXIF} = 382MHz F_{LO} = 760MHz LOCAL SW = "L"	2	A, B C, D	–4	—	4	deg
I/Q output amplitude balance	V_{BL}	F_{RXIF} = 382MHz F_{LO} = 760MHz LOCAL SW = "L"	2	A, B C, D	–1.5	—	1.5	dB
I-IX/Q-QX DC offset	V_{OFST}	DC measurement	2	A, B C, D	–200	—	200	mV

Local Frequency Division Ratio

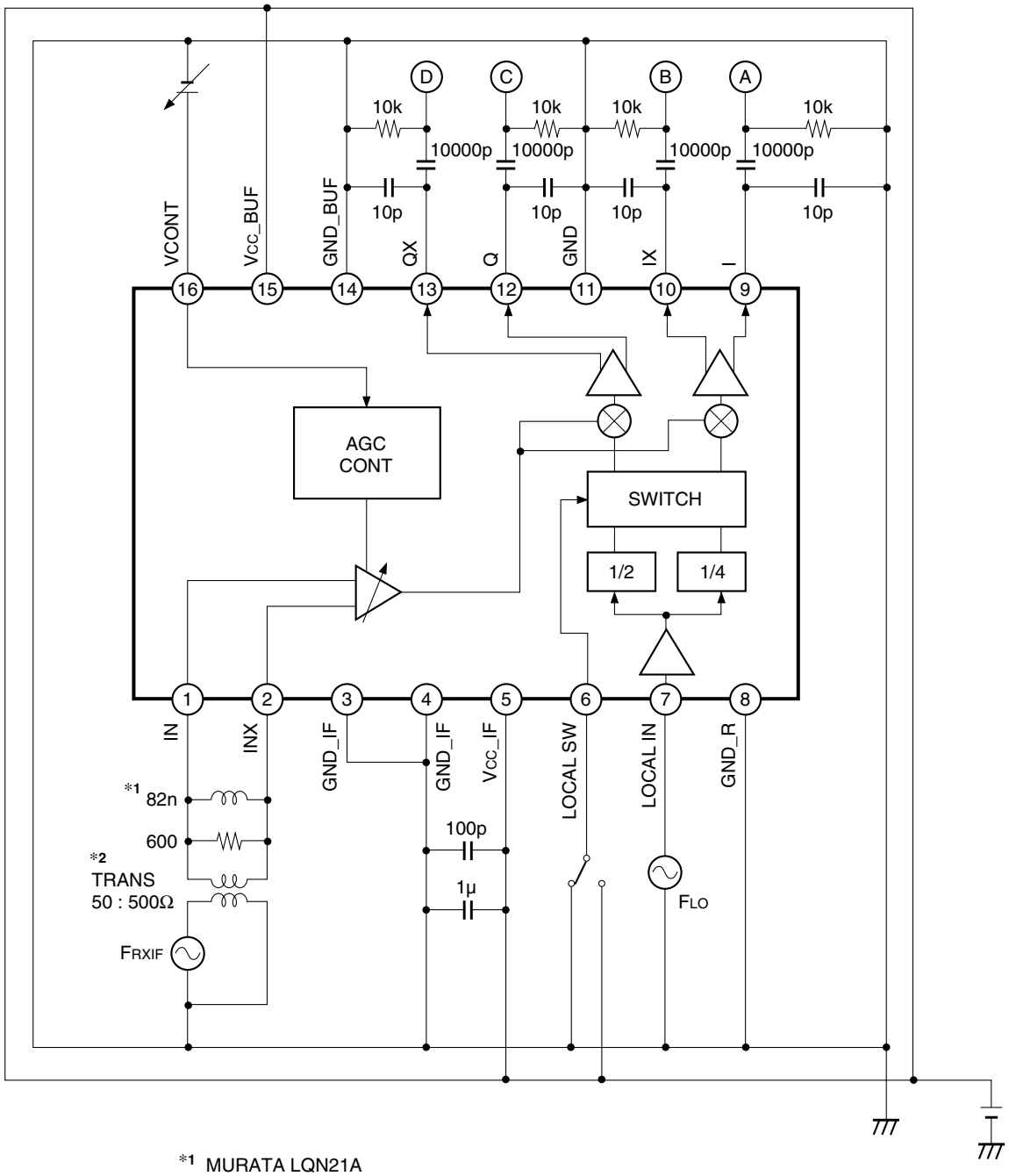
LOCAL SW (Pin 6)	Frequency division ratio
L	1/2
H	1/4

Electrical Characteristics Measurement Circuit 1



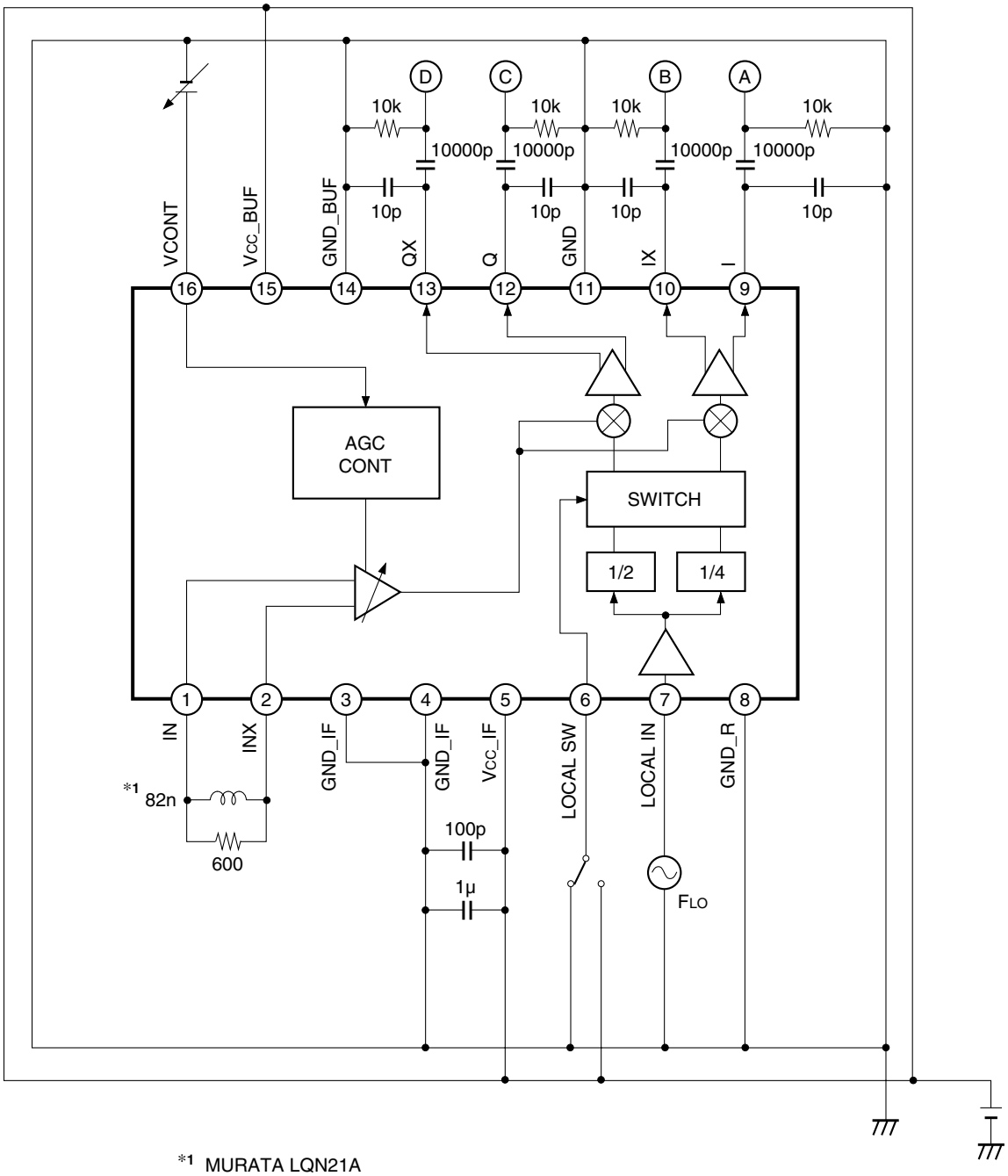
*1 LQN21A (MURATA MFG. CO., LTD.)
*2 616DS-1135 (TOKO, Inc.)

Electrical Characteristics Measurement Circuit 2



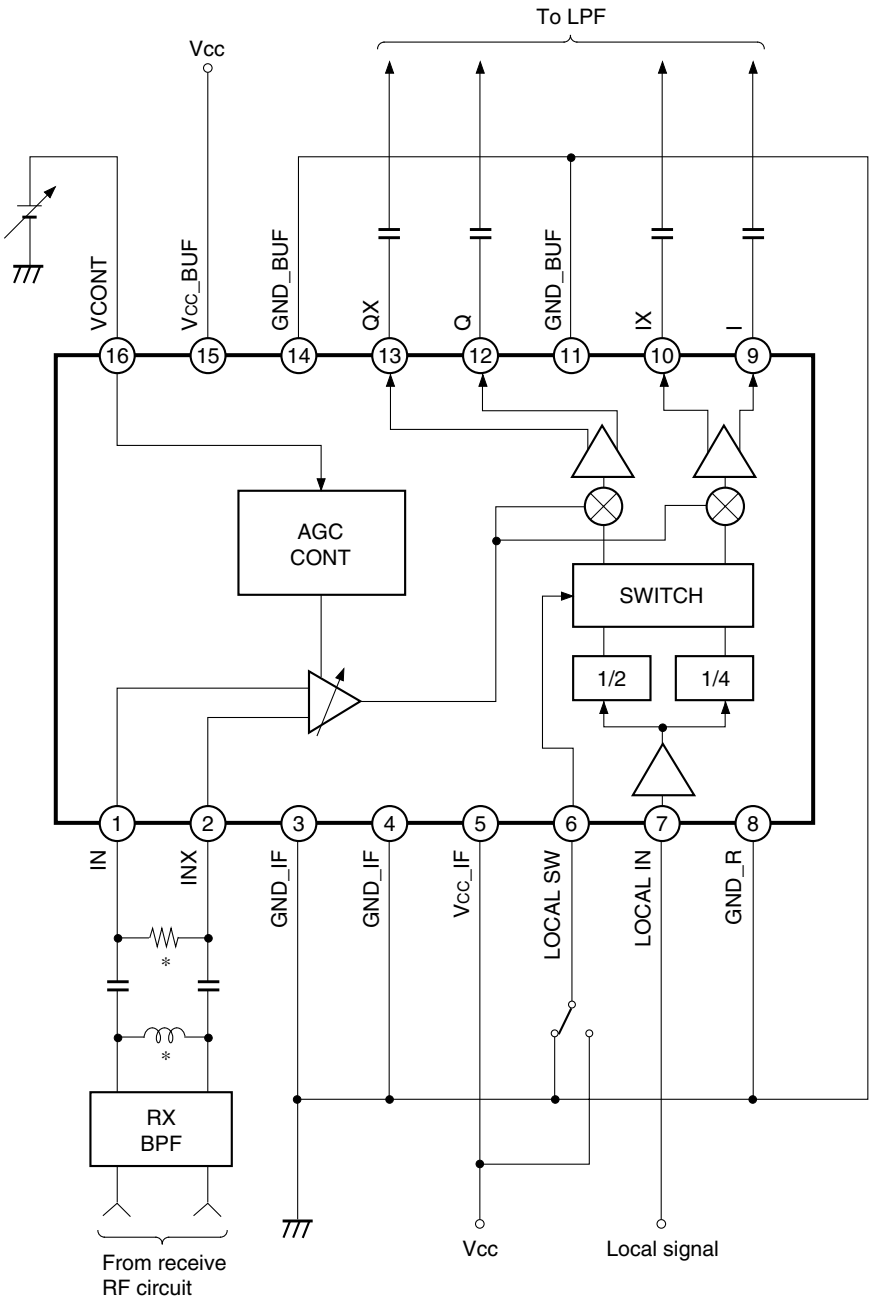
*1 MURATA LQN21A
*2 TOKO 616DS-1135

Electrical Characteristics Measurement Circuit 3



*1 MURATA LQN21A

Application Circuit



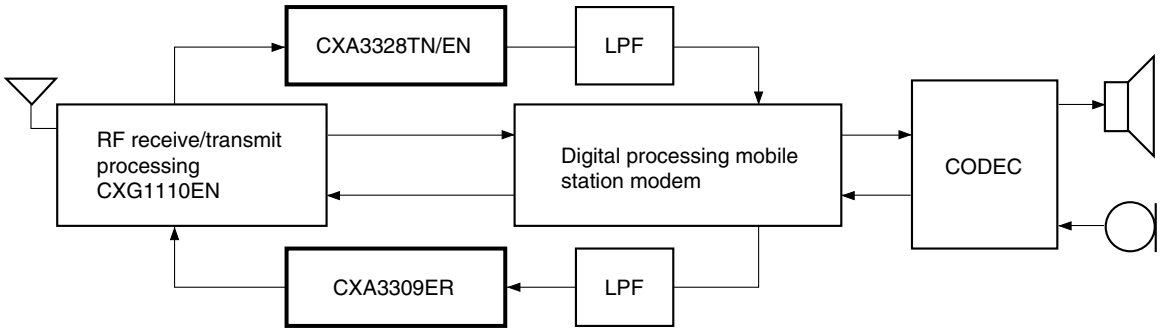
* Adjust this value so that the impedance matching with this IC is optimum.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

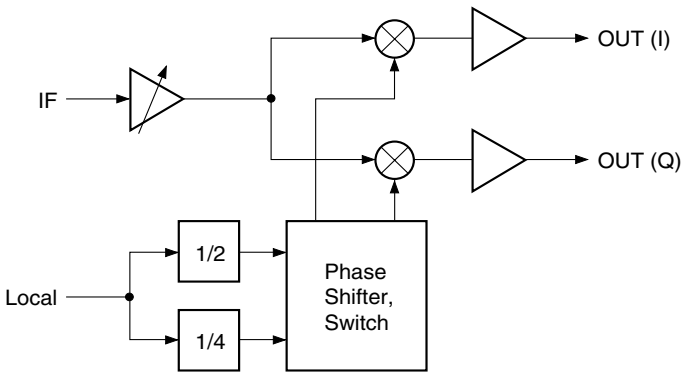
1. Outline of Operation

This IC performs the signal processing between the analog transmit baseband processing block and the analog transmit RF processing block of the cellular phone. The figure below shows the general circuit block diagram for the portable cellular phone using this IC. The input of this IC is connected to the analog RF processing block; the output is connected to the baseband signal processing block.



2. IC Internal Signal Flow

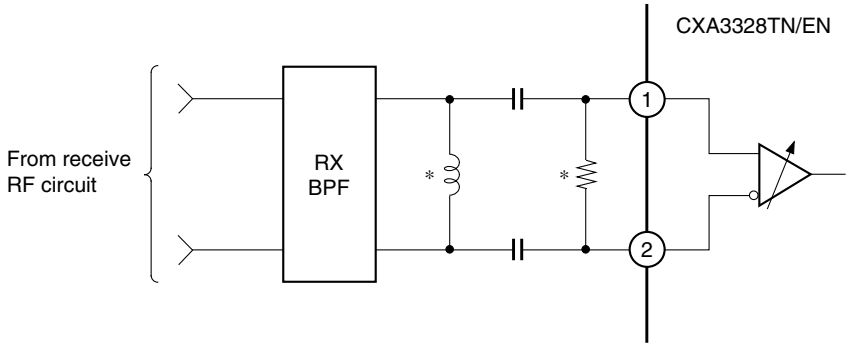
An IF signal and a local signal are input to this IC as shown in the figure below. The IF signal is gain-controlled to the necessary level by the gain control amplifier and is input to the quadrature demodulator block. The local signal is 1/2 or 1/4 frequency-divided. Also, that signal becomes the quadrature I/Q local signal via the FF phase shifter and quadrature-demodulated with the IF signal to become the baseband signal.



Notes on Operation

1. IF Input

The IF signal is differentially input to the IN pin and INX pin of this IC. IF is input to the input pin by AC coupling. The value of the AC coupling is selected so that the transfer power from the receive RF circuit is maximum.



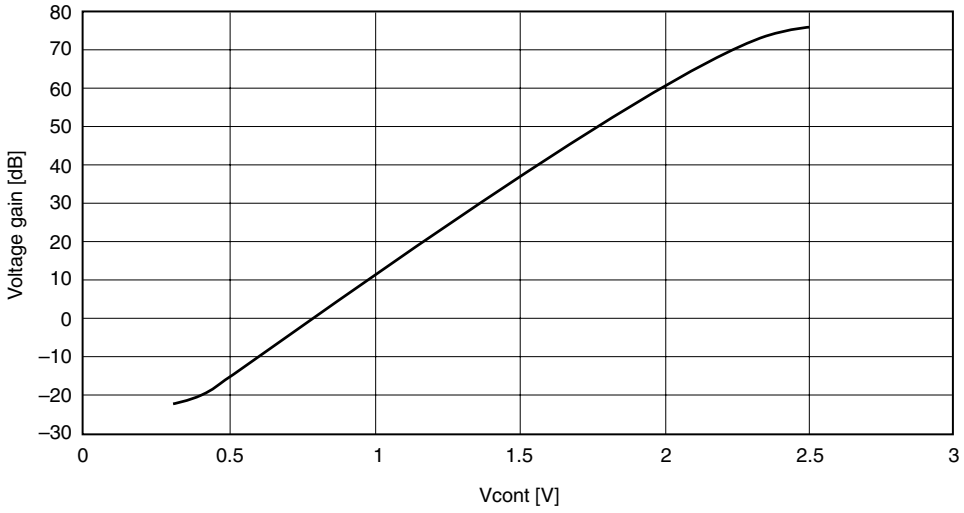
* This value must be the value taken for the optimum impedance matching between the BPF filter and this IC.

2. Notes on Power Supplies

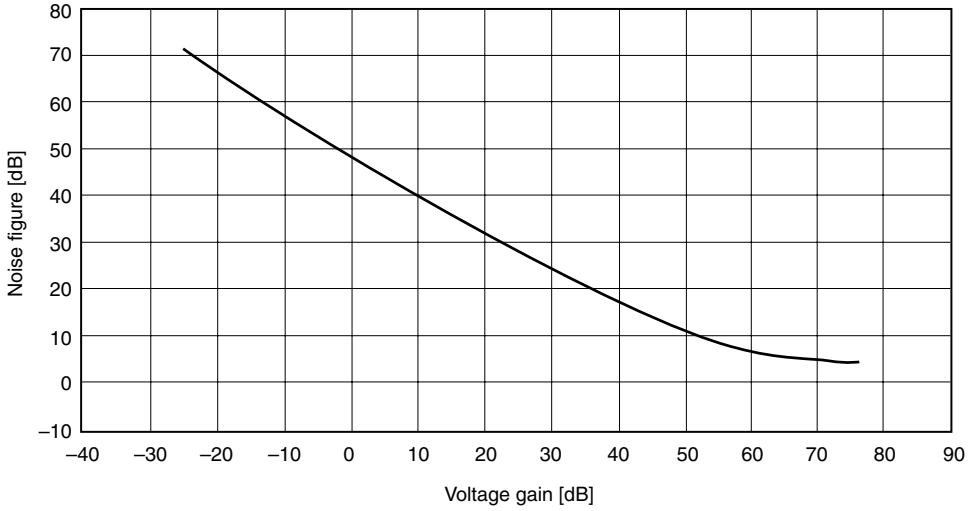
The CXA3328TN/EN is designed to operate by a 2.85V stabilized power supply to allow use with the battery driven portable phones. Using multiple voltage regulators throughout the phone is recommended to minimize the power supply noise in the CXA3328TN/EN power supply input. The recommended power supply range for the CXA3328TN/EN is 2.7 to 3.3V. Decouple the power supplies around the CXA3328TN/EN using 1µF capacitor for each V_{CC} pin. Locate this capacitor as close to the pins as possible, and minimize the series inductance for the pin connections. Using an additional 1nF decoupling capacitor in parallel to the 1µF capacitor is recommended to further reduce the high frequency noise in the power supply input to the CXA3328TN/EN.

Example of Representative Characteristics

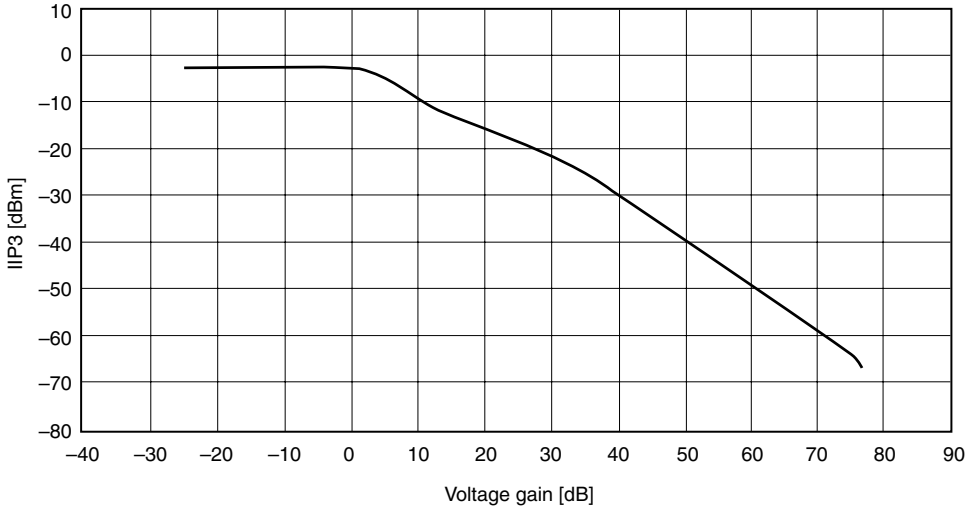
Voltage gain vs. Control voltage Vcont



Noise figure vs. Voltage gain



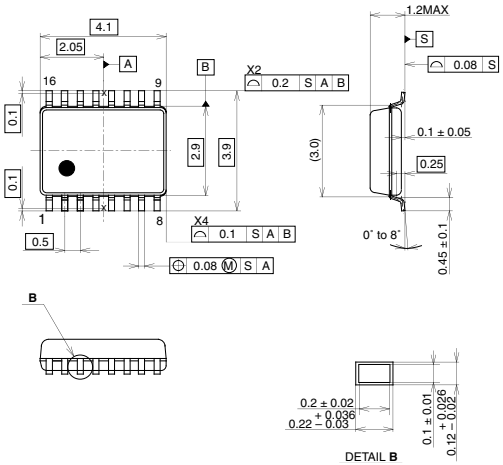
IIP3 vs. Voltage gain



Package Outline Unit: mm

CXA3328TN

16PIN TSSOP (PLASTIC)



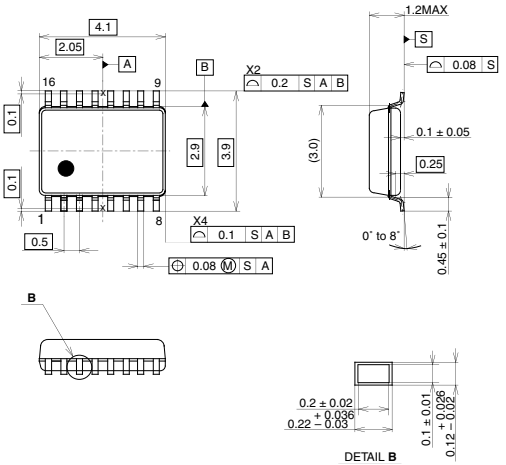
PACKAGE STRUCTURE

SONY CODE	TSSOP-16P-L01
EIAJ CODE	————
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.03g

SCT & Kokubu Ass'y

16PIN TSSOP (PLASTIC)



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JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.03g

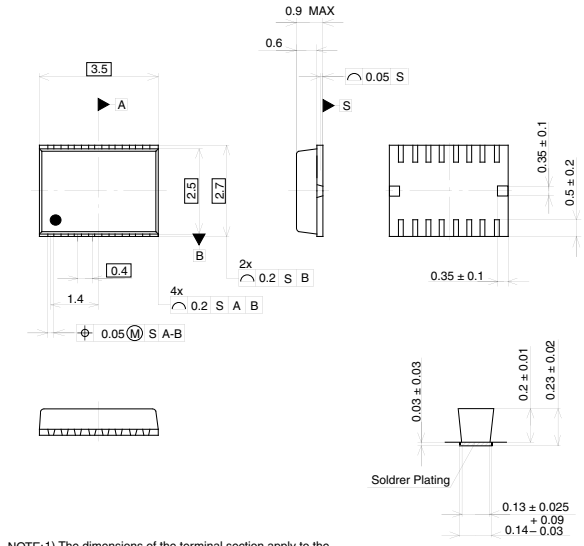
LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm

Package Outline Unit: mm

CXA3328EN

16PIN VSON (PLASTIC)



NOTE: 1) The dimensions of the terminal section apply to the ranges of 0.1mm and 0.25mm from the end of a terminal.

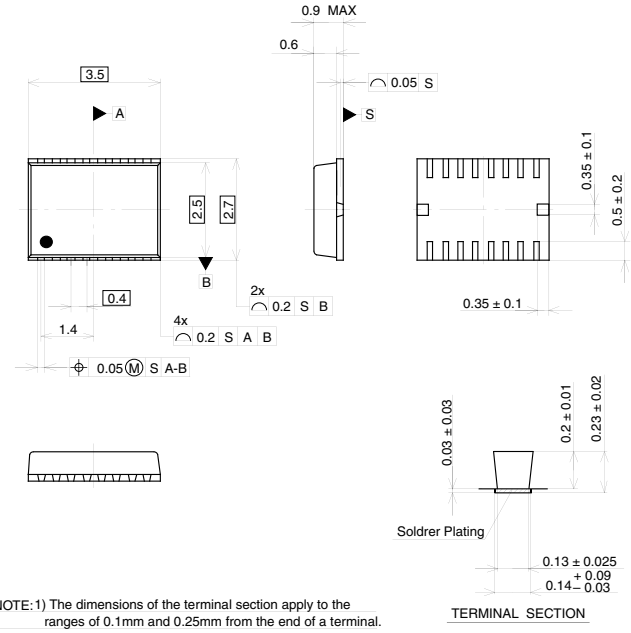
SONY CODE	VSON-16P-01
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.02 g

SCT & Kokubu Ass'y

16PIN VSON (PLASTIC)



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EIAJ CODE	————
JEDEC CODE	————

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LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.02 g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm

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