

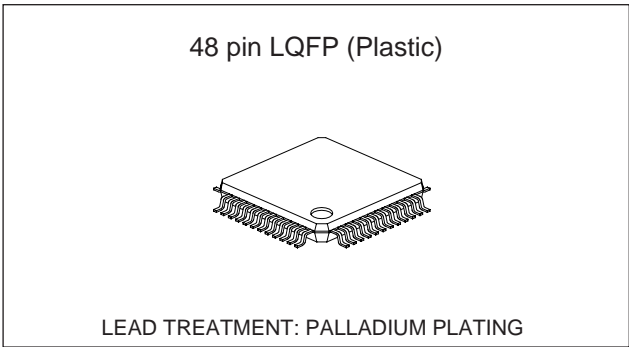
8-bit 160MSPS Flash A/D Converter

**Description**

The CXA3286R is an 8-bit high-speed flash A/D converter capable of digitizing analog signals at the maximum rate of 160MSPS. ECL, PECL or TTL can be selected as the digital input level in accordance with the application. The TTL digital output level allows 1:2 demultiplexed output.

**Features**

- Differential linearity error:  $\pm 0.5\text{LSB}$  or less
- Integral linearity error:  $\pm 0.5\text{LSB}$  or less
- Maximum conversion rate of 160MSPS
- Low input capacitance: 10pF
- Power saving function
- Wide analog input bandwidth: 250MHz
- Low power consumption: 550mW
- 1:2 demultiplexed output
- 1/2 frequency-divided clock output (with reset function)
- Compatible with ECL, PECL and TTL digital input levels
- TTL output "H" levels: 2.8V (Typ.)
- Output voltage control function (VOCLP)
- +3.3V line CMOS IC direct connecting available
- Single +5V power supply operation available
- Ultra-small surface mounting package (48-pin LQFP)



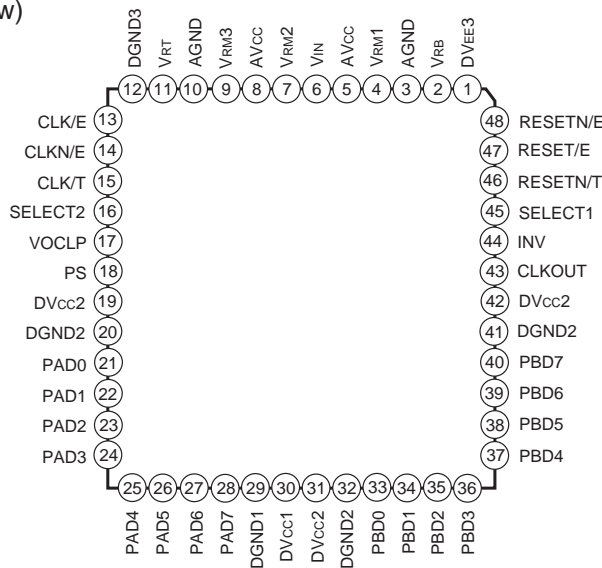
**Structure**

Bipolar silicon monolithic IC

**Applications**

- LCD monitors
- LCD projectors

**Pin Configuration (Top View)**



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**Absolute Maximum Ratings** (Ta = 25°C)

			Unit
• Supply voltage	AVcc, DVcc1, DVcc2	-0.5 to +7.0	V
	DGND3	-0.5 to +7.0	V
	DVEE3	-7.0 to +0.5	V
	DGND3 – DVEE3	-0.5 to +7.0	V
• Analog input voltage	VIN	VRT – 2.7 to AVcc	V
	VRT	2.7 to AVcc	V
• Reference input voltage	VRB	VIN – 2.7 to AVcc	V
	VRT – VRB	2.5	V
	• Digital input voltage	ECL/PECL input pin	DVEE3 – 0.5 to DGND3 + 0.5
	TTL input pin	DGND1 – 0.5 to DVcc1 + 0.5	V
	SELECT2 pin	DGND1 – 0.5 to DVcc1 + 0.5	V
	VOCLP pin	DGND1 – 0.5 to DVcc1 + 0.5	V
	VID*1 ( ***/E – ***N/E )	2.7	V
• Storage temperature	Tstg	-65 to +150	°C
• Allowable power dissipation	Pd	1.4	W

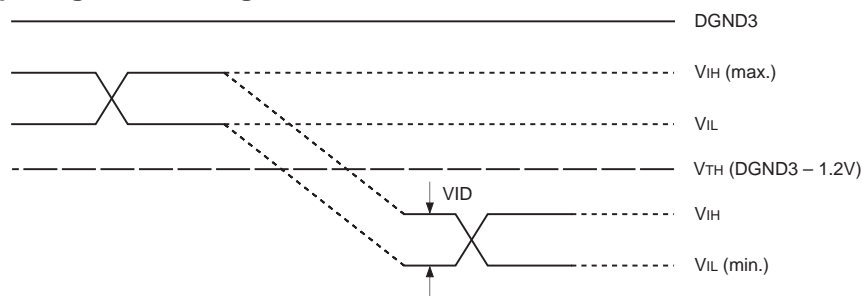
(when mounted on a two-layer glass fabric base epoxy board with dimensions of 50mm × 50mm, 1.6mm thick)

**Recommended Operating Conditions**

		With a single power supply			With dual power supply			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
• Supply voltage	DVcc1, DVcc2, AVcc	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	V
	DGND1, DGND2, AGND	-0.05	0	+0.05	-0.05	0	+0.05	V
	DGND3	+4.75	+5.0	+5.25	-0.05	0	+0.05	V
	DVEE3	-0.05	0	+0.05	-5.5	-5.0	-4.75	V
• Analog input voltage	VIN		VRB	VRT	VRB		VRT	V
• Reference input voltage	VRT	+2.9		+4.1	+2.9		+4.1	V
	VRB	+1.4		+2.6	+1.4		+2.6	V
	VRT – VRB	1.5		2.1	1.5		2.1	V
• Digital input voltage	ECL/PECL input pin	: VIH	DVcc1 + 1.5		DGND3 DVcc1 + 1.5		DGND3	V
		: VIL	DVcc1 + 1.1		VIH – 0.4 DVcc1 + 1.1		VIH – 0.4	V
	TTL input pin	: VIH	2.0		2.0			V
		: VIL			0.8		0.8	V
	SELECT2 pin	: VIH	DVcc1		DVcc1			V
		: VIL	DGND1		DGND1			V
VOCLP pin		DGND1 + 2.4		DVcc1 DGND1 + 2.4		DVcc1	V	
VID*1 ( ***/E – ***N/E )		0.4	0.8		0.4	0.8	V	
• Maximum conversion rate Fc (Straight mode)		125			125			MSPS
	(DMUX mode)	160			160			MSPS
• Ambient temperature	Ta	-20		+75		-20		+75 °C

\*1 VID: Input Voltage Differential

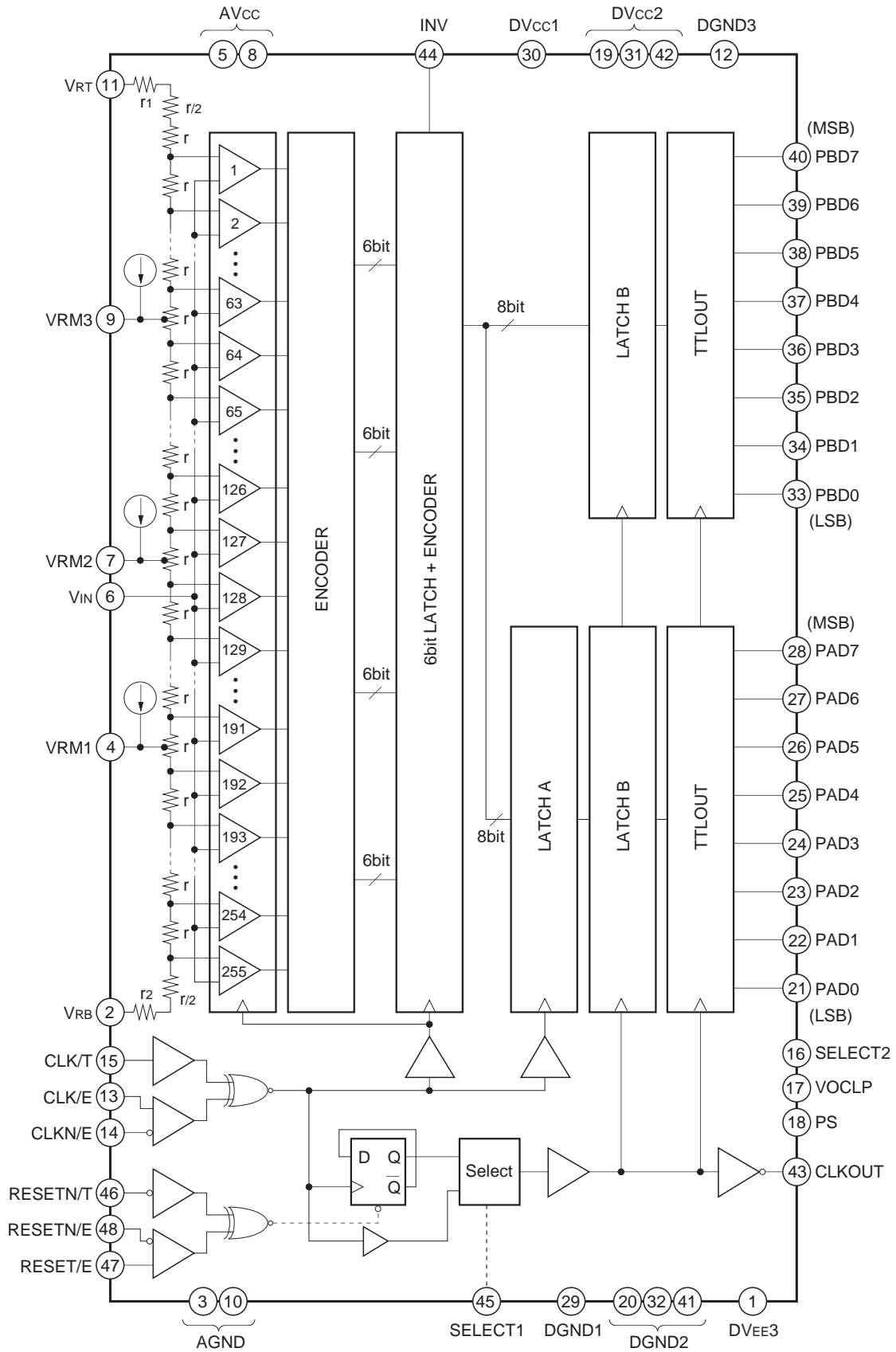
**ECL and PECL input signal switching level**



## Pin Description

[Symbol]	[Pin No.]	[Description]	[Typical voltage level with a single power supply]	[Typical voltage level with dual power supply]
DVEE3	1	Digital power supply	0V	-5.0V
VRB	2	Bottom reference voltage	1.4 to 2.6V	1.4 to 2.6V
AGND	3	Analog ground	0V	0V
VRM1	4	Reference voltage mid point	—	—
AVCC	5	Analog power supply	+5V	+5V
VIN	6	Analog signal input	VRB to VRT	VRB to VRT
VRM2	7	Reference voltage mid point	—	—
AVCC	8	Analog power supply	+5V	+5V
VRM3	9	Reference voltage mid point	—	—
AGND	10	Analog ground	0V	0V
VRT	11	Top reference voltage	2.9 to 4.1V	2.9 to 4.1V
DGND3	12	Digital power supply	+5V	0V
CLK/E	13	ECL/PECL clock input	PECL	ECL
CLKN/E	14	ECL/PECL clock input	PECL	ECL
CLK/T	15	TTL clock input	TTL	TTL
SELECT2	16	Data output switching	DGND1 or open or DVcc1	DGND1 or open or DVcc1
VOCLP	17	TTL high level clamp	Clamp voltage	Clamp voltage
PS	18	Power saving	TTL	TTL
DVcc2	19	Digital power supply	+5V	+5V
DGND2	20	Digital ground	0V	0V
PAD0 to PAD7	21 to 28	PA side data output	TTL	TTL
DGND1	29	Digital ground	0V	0V
DVcc1	30	Digital power supply	+5V	+5V
DVcc2	31	Digital power supply	+5V	+5V
DGND2	32	Digital ground	0V	0V
PBD0 to PBD7	33 to 40	PB side data output	TTL	TTL
DGND2	41	Digital ground	0V	0V
DVcc2	42	Digital power supply	+5V	+5V
CLKOUT	43	Clock output	TTL	TTL
INV	44	Data output polarity inversion	TTL	TTL
SELECT1	45	Output mode selection	TTL	TTL
RESETN/T	46	TTL reset input	TTL	TTL
RESET/E	47	ECL/PECL reset input	PECL	ECL
RESETN/E	48	ECL/PECL reset input	PECL	ECL

Block Diagram



Pin Description and I/O Pin Equivalent Circuit

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
3, 10	AGND		GND		Analog ground. Separated from the digital ground.
5, 8	AVcc		+5V (typ.)		Analog power supply. Separated from the digital power supply.
20, 29 32, 41	DGND1 DGND2		GND		Digital ground.
19, 30 31, 42	DVcc1 DVcc2		+5V (typ.)		Digital power supply.
12	DGND3		+5V (typ.) (With a single power supply)		Digital power supply. Ground for ECL input. +5V for PECL and TTL inputs.
			GND (With dual power supply)		
1	DV <sub>EE3</sub>		GND (With a single power supply)		Digital power supply. -5V for ECL input. Ground for PECL and TTL inputs.
			-5V (typ.) (With dual power supply)		
16	SELECT2	I	DVcc1 or Open or DGND1		Data output switching. When left open, data are output from both PA and PB side output ports. For DVcc1 level, PA side output port outputs data and PB side is in the high impedance state. For DGND1 level, PB side output port outputs data and PA side is in the high impedance state.
17	VOCLP	I	Clamp voltage		TTL output high level clamping. The TTL high level voltage is clamped to the value almost equivalent to the voltage applied to this pin . Even if this pin is left open, the TTL high level is clamped to approximately 2.8V.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
18	PS	I	TTL		<p>Power saving. When left open, this pin goes to high level. When set to low level, the power saving state is established.</p>
13	CLK/E	I	ECL/ PECL		<p>Clock input.</p>
14	CLKN/E	I			<p>CLK/E complementary input. When left open, this pin goes to the threshold voltage. Only CLK/E can be used for operation, but complementary inputs are recommended to attain fast and stable operation.</p>
48	RESETN/E	I			<p>Reset signal input. When set to low level, the built-in CLK frequency divider circuit can be reset.</p>
47	RESET/E	I			<p>RESETN/E complementary input. When left open, this pin goes to the threshold voltage. Only RESETN/E can be used for operation.</p>
15	CLK/T	I	TTL		<p>Clock input.</p>
46	RESETN/T	I			<p>Reset signal input. When left open, this pin goes to high level. When set to low level, the built-in CLK frequency divider circuit can be reset.</p>
44	INV	I	TTL		<p>Data output polarity inversion input. When left open, this input goes to high level. (See Table 1. I/O Correspondence Table.)</p>
45	SELECT1		Vcc or GND		<p>Data output mode selection. (See Table 2. Operation Mode Table.)</p>

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
11	V <sub>RT</sub>	I	4.0V (typ.)		Top reference voltage. By-pass to AGND with a 1μF tantalum capacitor and a 0.1μF chip capacitor.
9	V <sub>RM3</sub>		$V_{RB} + \frac{3}{4}(V_{RT} - V_{RB})$		Reference voltage mid point. By-pass to AGND with a 0.1μF chip capacitor.
7	V <sub>RM2</sub>		$V_{RB} + \frac{2}{4}(V_{RT} - V_{RB})$		Reference voltage mid point. By-pass to AGND with a 0.1μF chip capacitor.
4	V <sub>RM1</sub>		$V_{RB} + \frac{1}{4}(V_{RT} - V_{RB})$		Reference voltage mid point. By-pass to AGND with a 0.1μF chip capacitor.
2	V <sub>RB</sub>	I	2.0V (typ.)		Bottom reference voltage. By-pass to AGND with a 1μF tantalum capacitor and a 0.1μF chip capacitor.
6	V <sub>IN</sub>	I	V <sub>RT</sub> to V <sub>RB</sub>		Analog input.
21 to 28	PAD0 to PAD7	O	TTL		Port A side data output. TTL output; the high level is clamped to approximately 2.8V.
33 to 40	PBD0 to PBD7	O			Port B side data output. TTL output; the high level is clamped to approximately 2.8V.
43	CLKOUT	O			Clock output. (See Table 2. Operation Mode Table.) TTL output; the high level is clamped to approximately 2.8V.

**Electrical Characteristics**

( AV<sub>CC</sub>, DV<sub>CC</sub>1, 2, DGND3 = +5V, AGND, DGND1, 2, DV<sub>EE</sub>3 = 0V, V<sub>RT</sub> = 4V, V<sub>RB</sub> = 2V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution				8		bits
DC characteristics						
Integral linearity error	E <sub>IL</sub>	V <sub>IN</sub> = 2V <sub>p-p</sub> , F <sub>c</sub> = 5MSPS			±0.5	LSB
Differential linearity error	E <sub>DL</sub>				±0.5	LSB
Analog input						
Analog input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = +3.0V + 0.07V <sub>rms</sub>		10		pF
Analog input resistance	R <sub>IN</sub>		7	15	35	kΩ
Analog input current	I <sub>IN</sub>		0	100	285	μA
Reference input						
Reference resistance	R <sub>ref</sub> *2		400	600	740	Ω
Reference current	I <sub>ref</sub> *3		2.7	3.3	5.0	mA
Offset voltage V <sub>RT</sub> side	E <sub>OT</sub>		6	8	10	mV
Offset voltage V <sub>RB</sub> side	E <sub>OB</sub>		0	1.5	3	mV
Digital input (ECL, PECL)						
Digital input voltage: High	V <sub>IH</sub>	V <sub>IH</sub> = DGND3 – 0.8V V <sub>IL</sub> = DGND3 – 1.6V	DV <sub>EE</sub> 3 + 1.5		DGND3	V
: Low	V <sub>IL</sub>		DV <sub>EE</sub> 3 + 1.1		V <sub>IH</sub> – 0.4	V
Threshold voltage	V <sub>TH</sub>		DGND3 – 1.2			V
Digital input current: High	I <sub>IH</sub>			–50	20	μA
: Low	I <sub>IL</sub>			–50	20	μA
Digital input capacitance					5	pF
Digital input (TTL)						
Digital input voltage: High	V <sub>IH</sub>	V <sub>IH</sub> = 3.5V V <sub>IL</sub> = 0.2V	2.0			V
: Low	V <sub>IL</sub>				0.8	V
Threshold voltage	V <sub>TH</sub>			1.5		V
Digital input current: High	I <sub>IH</sub>			–10	5	μA
: Low	I <sub>IL</sub>			–20	0	μA
Digital input capacitance					5	pF
Digital output (TTL)						
Digital output voltage : High	V <sub>OH</sub>	I <sub>OH</sub> = –2mA	2.4			V
: Low	V <sub>OL</sub>	I <sub>OL</sub> = 1mA			0.5	V
Switching characteristics						
Maximum conversion rate	F <sub>c</sub>	DMUX mode	160			MSPS
Aperture jitter	T <sub>aj</sub>			10		ps
Sampling delay	T <sub>ds</sub>		1.2	1.3	1.5	ns
Clock high pulse width	T <sub>pw1</sub>	CLK	2.5			ns
Clock low pulse width	T <sub>pw0</sub>	CLK	2.9			ns
Reset signal setup time	T <sub>rs</sub>	RESETN – CLK	1.0			ns
Reset signal hold time	T <sub>rh</sub>	RESETN – CLK	–0.5			ns
Clock output delay	T <sub>d_clk</sub>	(C <sub>L</sub> = 5pF)	3.0	4.0	6.5	ns
Data output delay	T <sub>do1</sub>	DMUX mode (C <sub>L</sub> = 5pF)		T*4 + 0.5		ns
	T <sub>do2</sub>	(C <sub>L</sub> = 5pF)	3.5	4.5	7.0	ns
Output rise time	T <sub>r</sub>	0.8 to 2.0V (C <sub>L</sub> = 5pF)		1		ns
Output fall time	T <sub>f</sub>	0.8 to 2.0V (C <sub>L</sub> = 5pF)		1		ns

\* These characteristics are for PECL input unless otherwise specified.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Dynamic characteristics						
Input bandwidth		$V_{IN} = 2V_{p-p}, -3dB$	250			MHz
S/N ratio		$\left\{ \begin{array}{l} F_c = 160MSPS, \\ fin = 1kHz F_s \\ DMUX mode \end{array} \right.$		46		dB
		$\left\{ \begin{array}{l} F_c = 160MSPS, \\ fin = 9.999MHz F_s \\ DMUX mode \end{array} \right.$		42		dB
Error rate		$\left\{ \begin{array}{l} F_c = 160MSPS, \\ fin = 1kHz F_s \\ DMUX mode \\ Error > 16LSB \end{array} \right.$			$1 \times 10^{-12}$	TPS*5
		$\left\{ \begin{array}{l} F_c = 160MSPS, \\ fin = 9.999MHz F_s \\ DMUX mode \\ Error > 16LSB \end{array} \right.$			$2 \times 10^{-8}$	TPS
		$\left\{ \begin{array}{l} F_c = 125MSPS, \\ fin = 31.249MHz F_s \\ Straight mode \\ Error > 16LSB \end{array} \right.$			$1 \times 10^{-9}$	TPS
Power supply						
Supply current	$I_{CC} + I_{EE}$		89	108	140	mA
AVcc pin supply current	$I_{Alcc}$		62		87	mA
DVcc1 pin supply current	$I_{Dlcc1}$		22		36	mA
DVcc2 pin supply current	$I_{Dlcc2}$		4.0		15	mA
DGND3 pin supply current	$I_{EE}$		0.5		1.5	mA
Supply current for PS	$I_{CC} + I_{EE}$				5	mA
AVcc pin supply current for PS	$I_{Alcc}$				1.5	mA
DVcc1 pin supply current for PS	$I_{Dlcc1}$				1.5	mA
DVcc2 pin supply current for PS	$I_{Dlcc2}$				1.5	mA
DGND3 pin supply current for PS	$I_{EE}$				0.5	mA
Power consumption	$P_d^{*6}$		480	550	700	mW
Power consumption for PS	$P_d^{*7}$		0.3		25	mW

\*2 Rref: Resistance value between VRT and VRB

$$*3 I_{ref} = \frac{V_{RT} - V_{RB}}{R_{ref}}$$

$$*4 T = \frac{1}{F_c}$$

\*5 TPS: Times Per Sample

$$*6 P_d = (I_{CC} + I_{EE}) \cdot V_{CC} + \frac{(V_{RT} - V_{RB})^2}{R_{ref}}$$

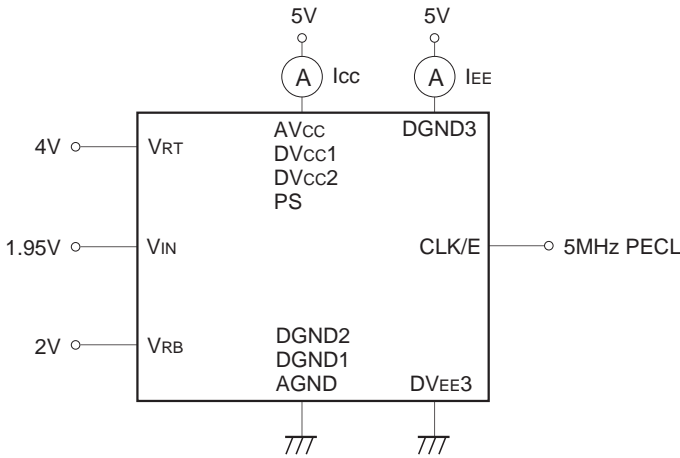
$$*7 P_d = (I_{CC} + I_{EE}) \cdot V_{CC}$$

V <sub>IN</sub>	Step	INV															
		1							0								
		D7			D0				D7			D0					
V <sub>RT</sub>	255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	254	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1
V <sub>RM2</sub>	⋮																
	128	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	127	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
	⋮																
V <sub>RB</sub>	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0
	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Table 1. I/O Correspondence Table

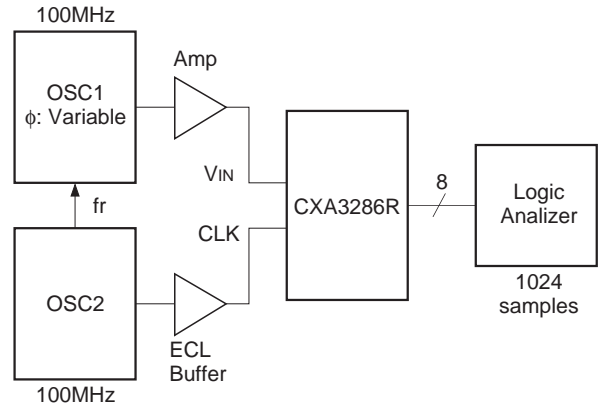
**Electrical Characteristics Measurement Circuit**

**Current Consumption Measurement Circuit**



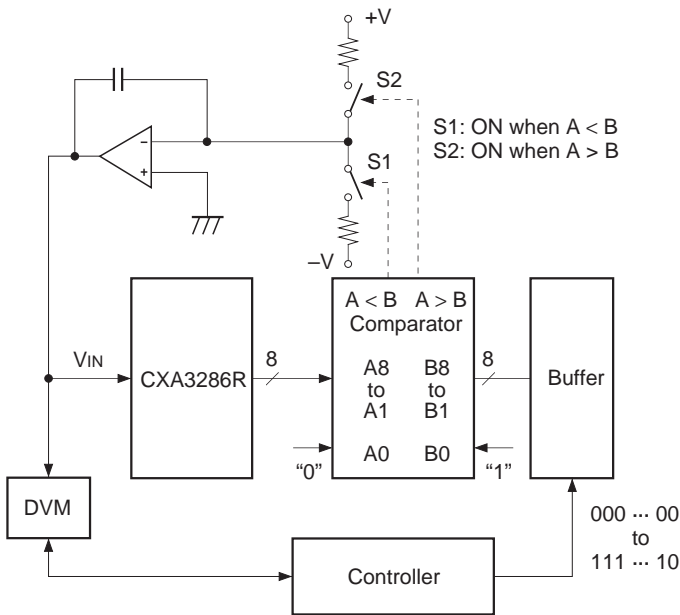
**Sampling Delay Measurement Circuit**

**Aperture Jitter Measurement Circuit**

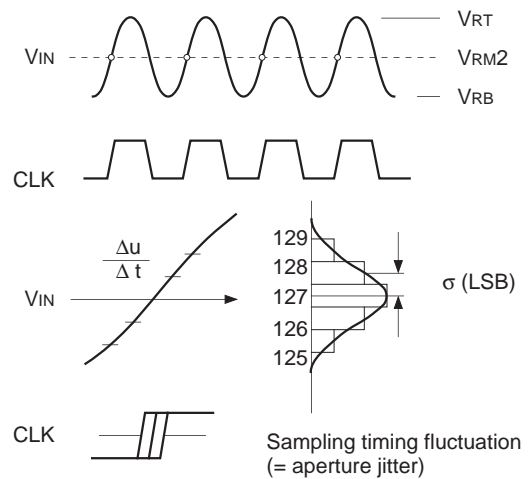


**Integral Linearity Error Measurement Circuit**

**Differential Linearity Error Measurement Circuit**



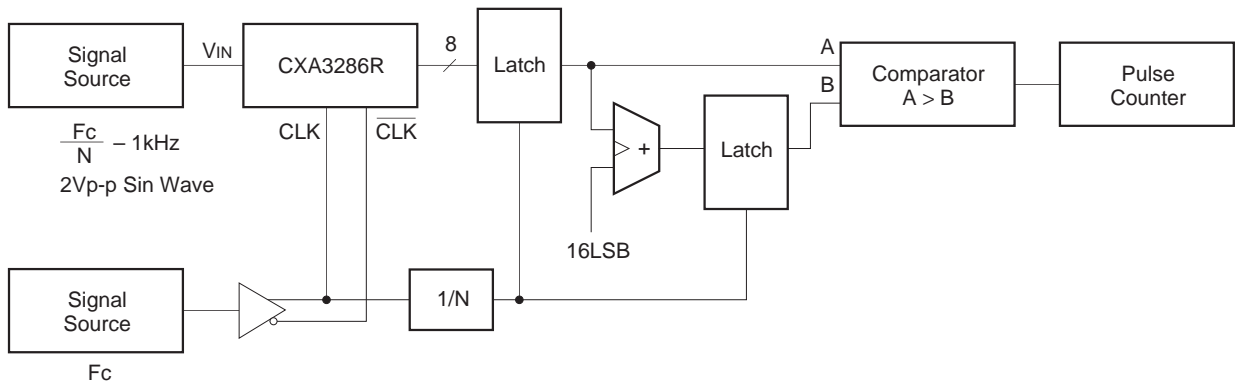
**Aperture Jitter Measurement Method**



Where  $\sigma$  (LSB) is the deviation of the output codes when the largest slew rate point is sampled at the clock which has exactly the same frequency as the analog input signal, the aperture jitter  $T_{aj}$  is:

$$T_{aj} = \sigma / \frac{\Delta u}{\Delta t} = \sigma / \left( -\frac{256}{2} \times 2\pi f \right)$$

**Error Rate Measurement Circuit**



### Description of Operation Modes

The CXA3286R has two types of operation modes which are selected with Pin 45 (SELECT1).

Operation mode	SELECT1 pin	Maximum conversion rate	Data output	Clock output
DMUX mode	Vcc	160MSPS	Demultiplexed output 80Mbps	The input clock is 1/2 frequency divided and output. 80MHz
Straight mode	GND	125MSPS	Straight output 125Mbps	The input clock is inverted and output. 125MHz

**Table 2. Operation Mode Table**

#### 1. DMUX mode (See Application Circuit 1-(1), (2) and (3).)

Set the SELECT1 pin to Vcc for this mode. In this mode, the clock frequency is divided by 2 in the IC, and the data is output after being demultiplexed by this 1/2 frequency-divided clock. The 1/2 frequency-divided clock, which has adequate setup time and hold time for the output data, is output from the clock output pin.

When using the multiple CXA3286R in DMUX mode, the start timing of the 1/2 frequency-divided clocks becomes out of phase, producing operation such as that shown in the example on the next page. As a countermeasure, the CXA3286R has a function that resets the 1/2 frequency-divided clocks.

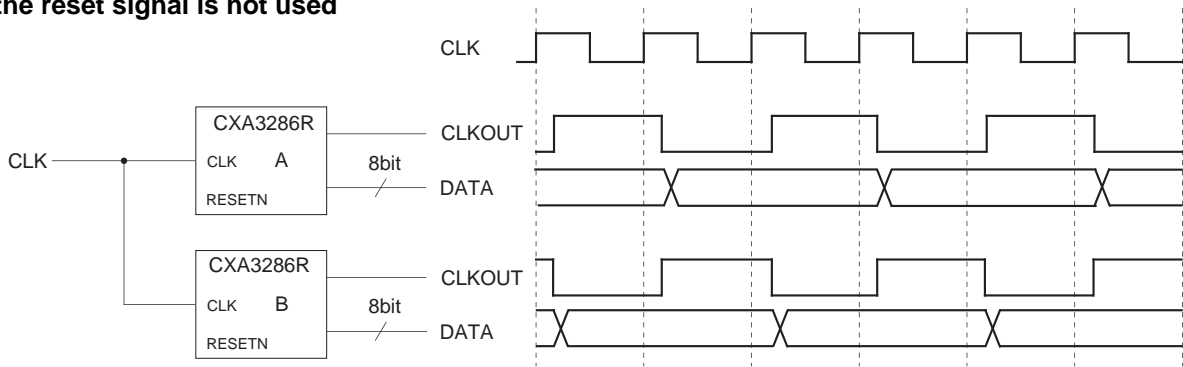
When resetting this 1/2 frequency-divided clock, the low level of the reset signal should be input to the RESETN pin (Pin 46 or 48). The reset signal requires the setup time ( $T_{rs} \geq 1.0\text{ns}$ ) and hold time ( $T_{rh} \geq -0.5\text{ns}$ ) to the clock rising edge because it is synchronized with and taken in the clock.

The reset period can be extended by making the low level period of the reset signal longer because the clock output pin is fixed to low (reset) during the low level period at the clock rising edge. If the reset start timing is regarded as not important, the timing where the reset signal is set from high to low is not so consequence. However, when the reset is released the timing where the reset signal is set from low to high must become significant because the timing is used to commence the 1/2 frequency-divided clock. In this case, the setup time ( $T_{rs}$ ) is also necessary.

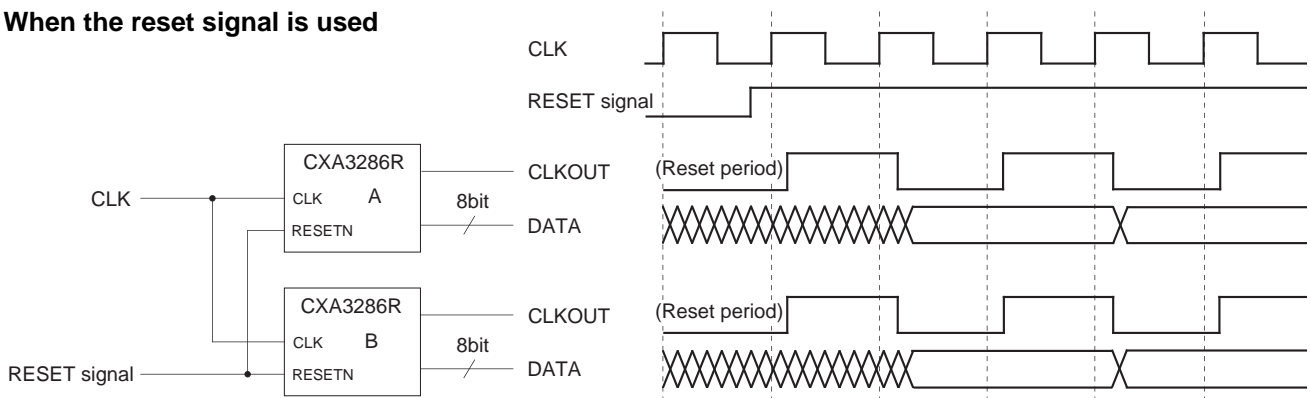
See the timing chart for detail. (This chart shows the example of reset for 2T.)

The A/D converter can operate at  $F_c (\text{min.}) = 160\text{MSPS}$  in this mode.

**When the reset signal is not used**



**When the reset signal is used**



**2. Straight mode** (See Application Circuits 1-(4), (5) and (6).)

Set the SELECT1 pin to GND for this mode. In this mode, data output can be obtained in accordance with the clock frequency applied to the A/D converter for applications which use the clock applied to the A/D converter as the system clock.

The A/D converter can operate at  $F_c$  (min.) = 125MSPS in this mode.

**Digital input level and supply voltage settings**

The logic input level for the CXA3286R supports ECL, PECL and TTL levels.

The power supplies (DV<sub>EE3</sub>, DGND3) for the logic input block must be set to match the logic input (CLK and reset signals) level.

Digital input level	DV <sub>EE3</sub>	DGND3	Supply voltage	Application circuits
ECL	-5V	0V	±5V	(1) (4)
PECL	0V	+5V	+5V	(2) (5)
TTL	0V	+5V	+5V	(3) (6)

**Table 3. Logic Input Level and Power Supply Settings**

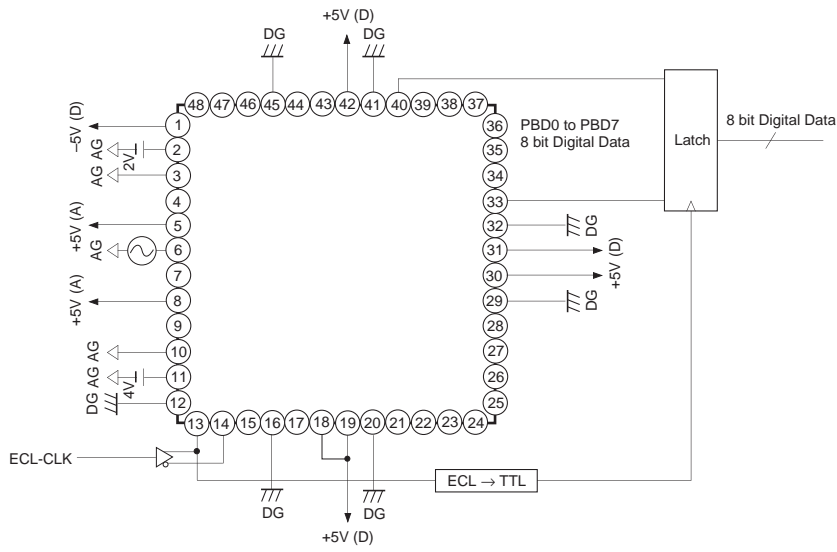
**Description of SELECT2 pin**

The CXA3286R has two systems of data outputs and the port where the data is output can be selected by the SELECT2 pin.

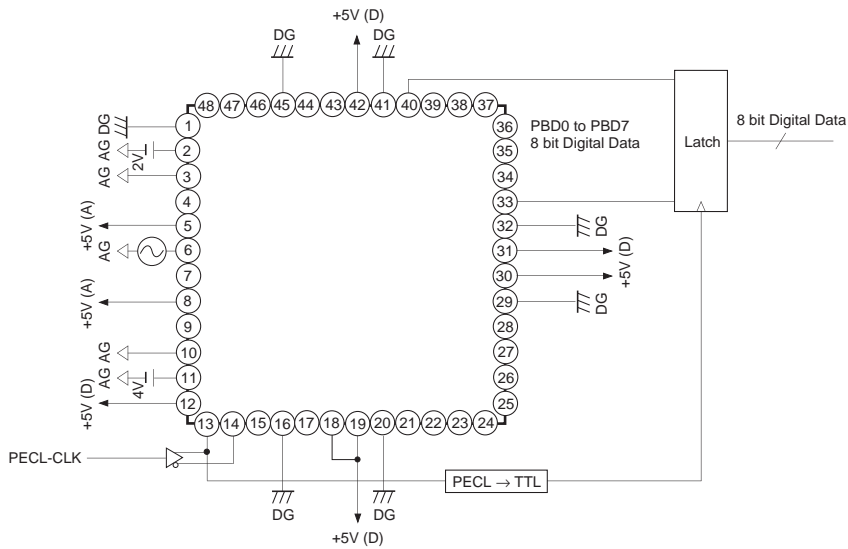
SELECT2 pin	Data output
Open	PA and PB both sides output possible
V <sub>cc1</sub>	PA side output possible; PB side in high impedance
GND1	PB side output possible; PA side in high impedance



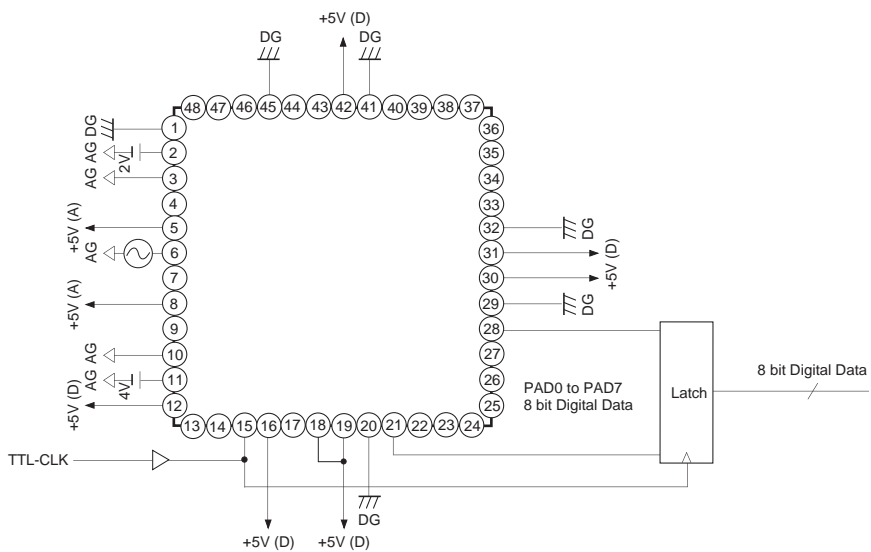
**(4) Straight ECL input**



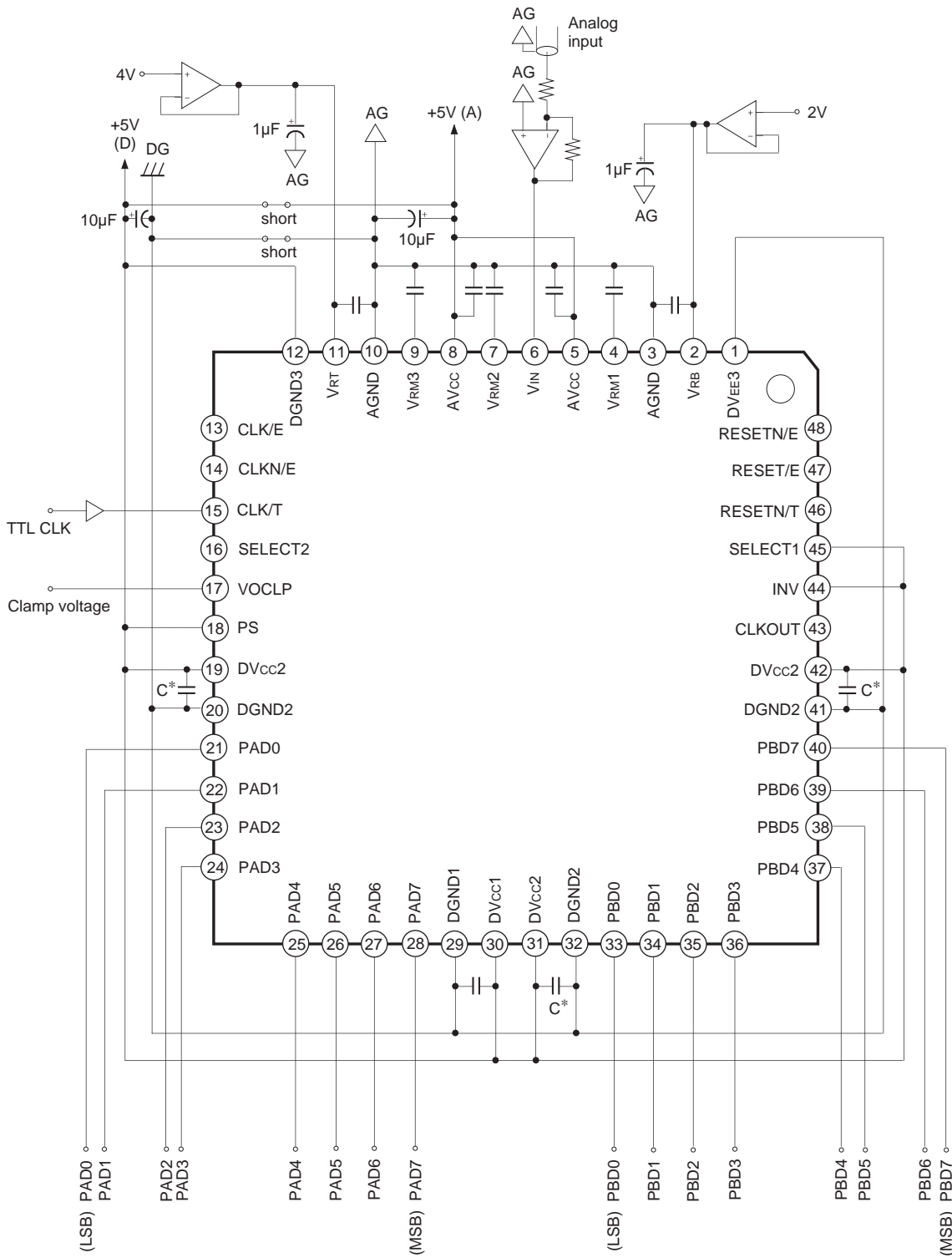
**(5) Straight PECL input**



**(6) Straight TTL input**



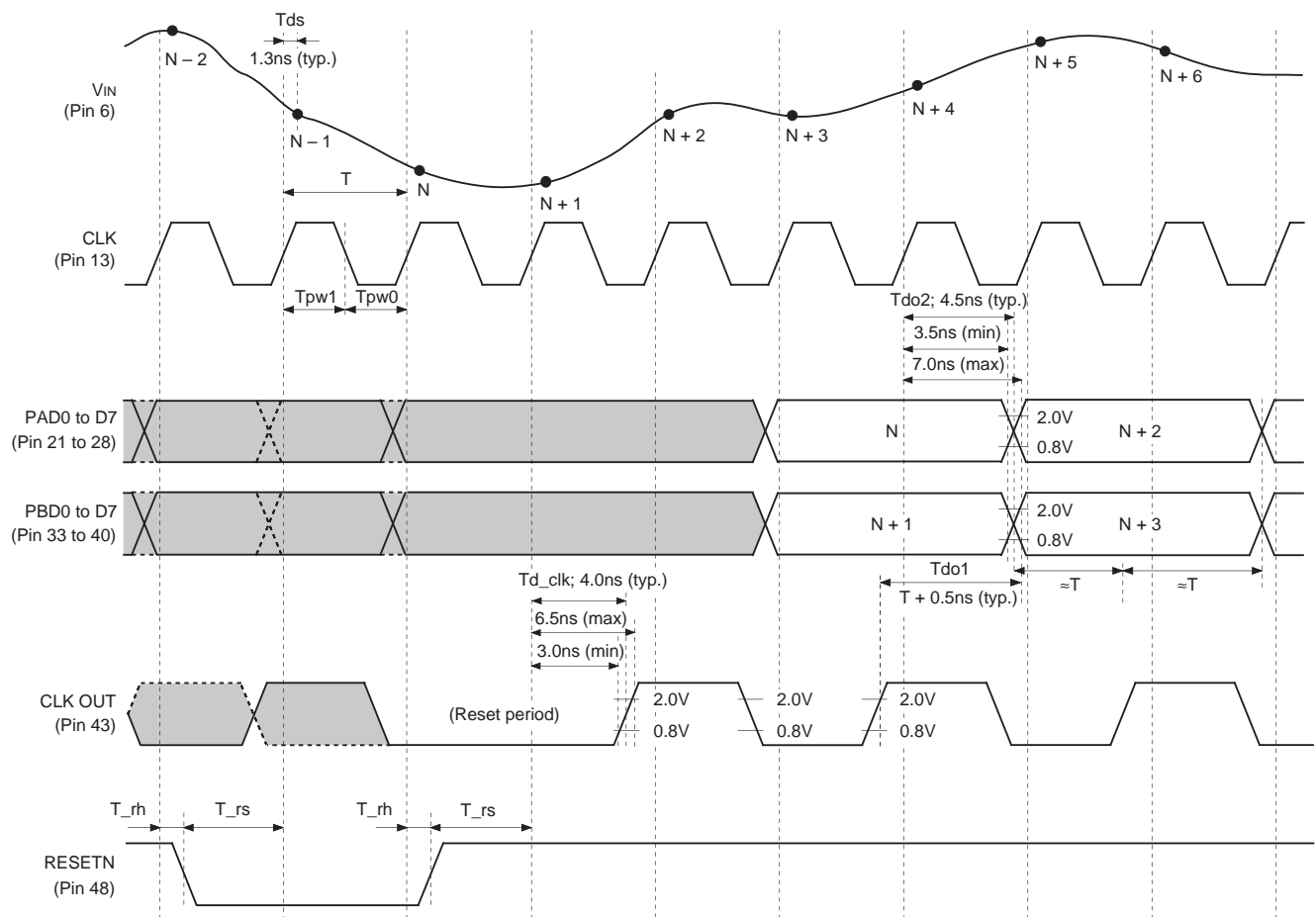
Application Circuit 2 DMUX Mode TTL I/O (When a single power supply is used)



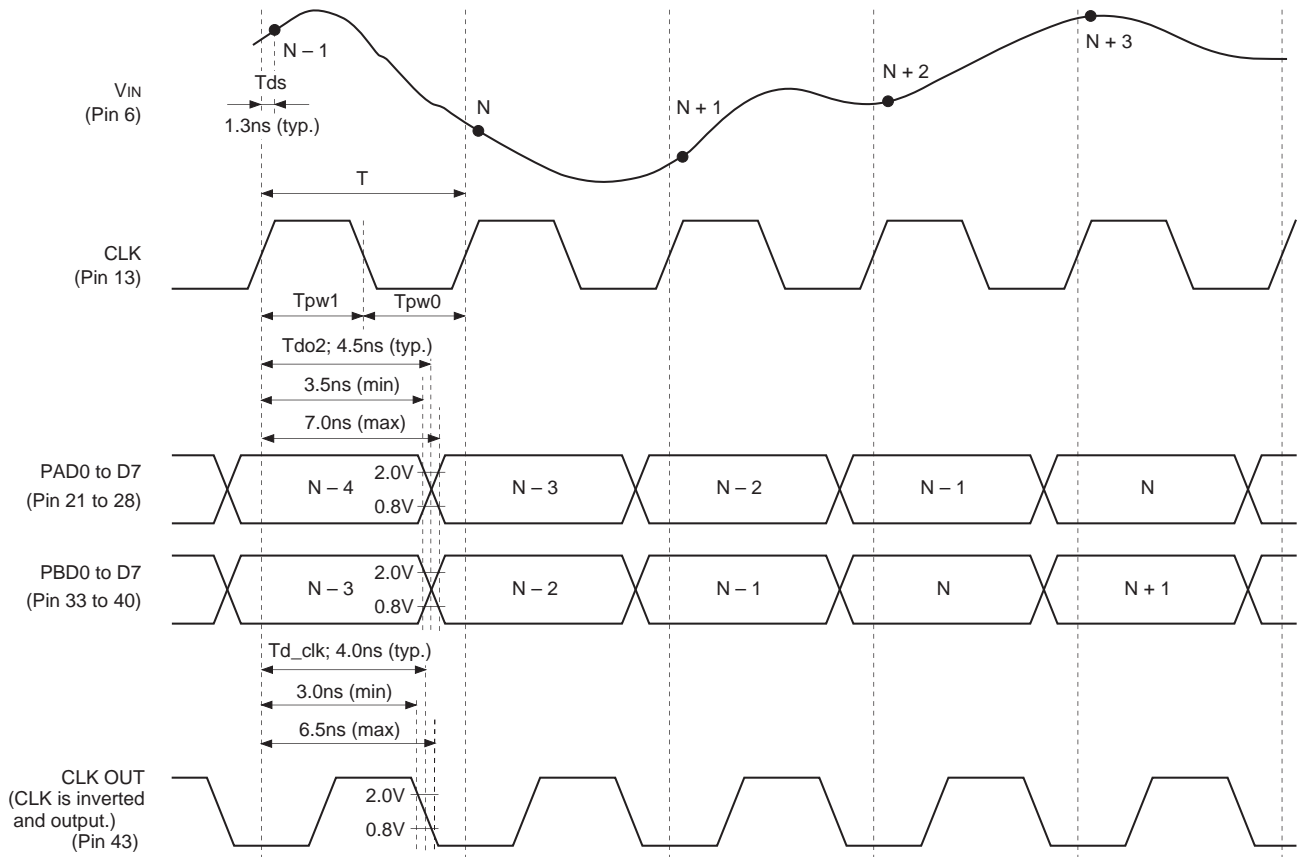
- Short the analog system and digital system at one point immediately under the A/D converter. See the Notes on Operation.
- ||— is the chip capacitor of 0.1µF. Also, C\* is important to suppress the noise generated during the TTL output circuit is operating. Place C\* at the fixed position between the pins with the shortest distance.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

DMUX Mode Timing Chart (Select = Vcc)



**Straight Mode Timing Chart (Select = GND)**

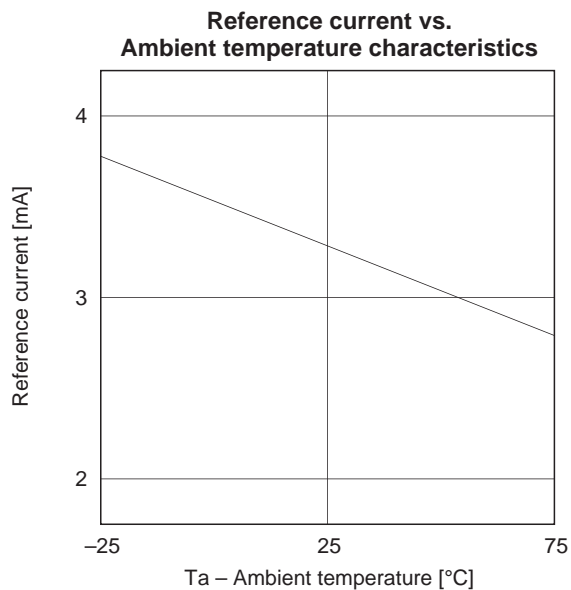
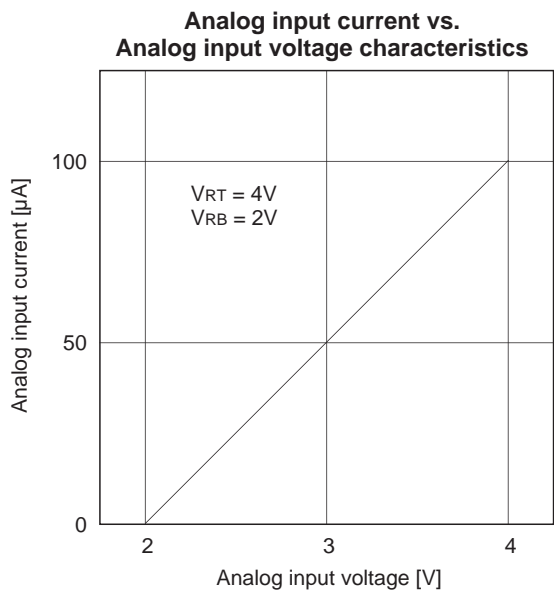
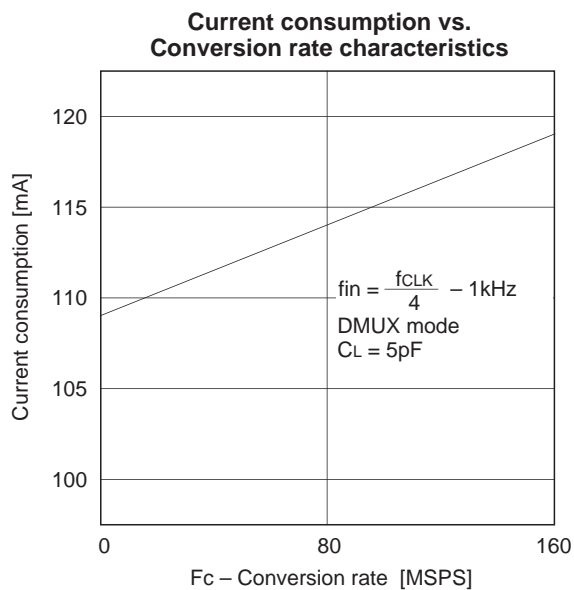
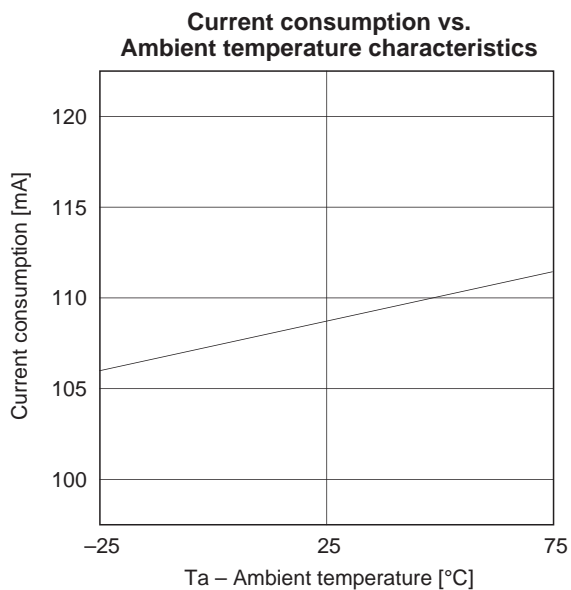


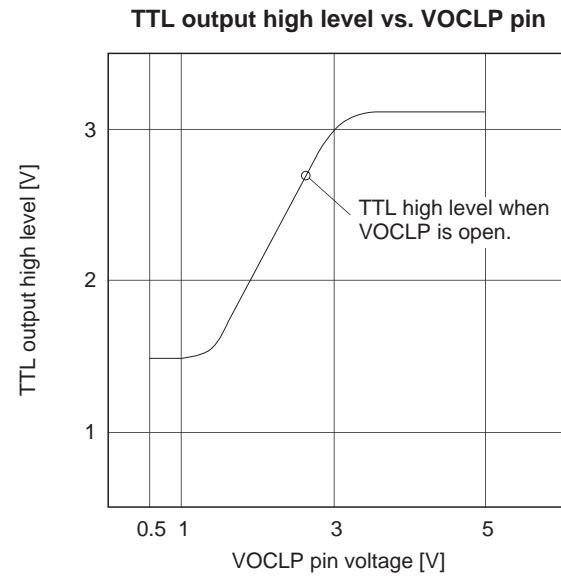
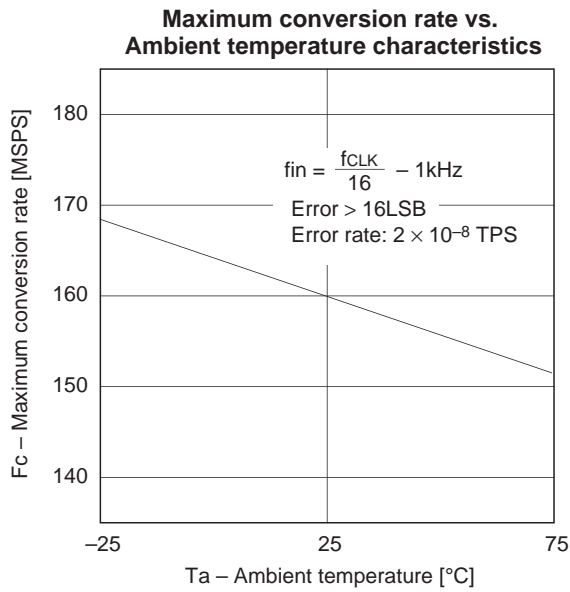
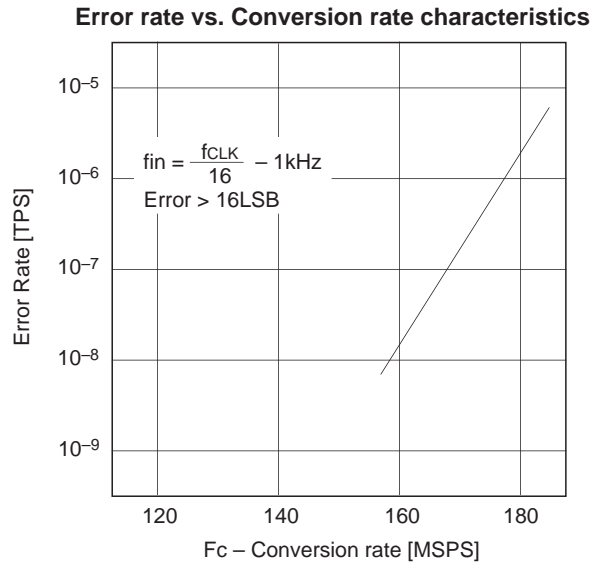
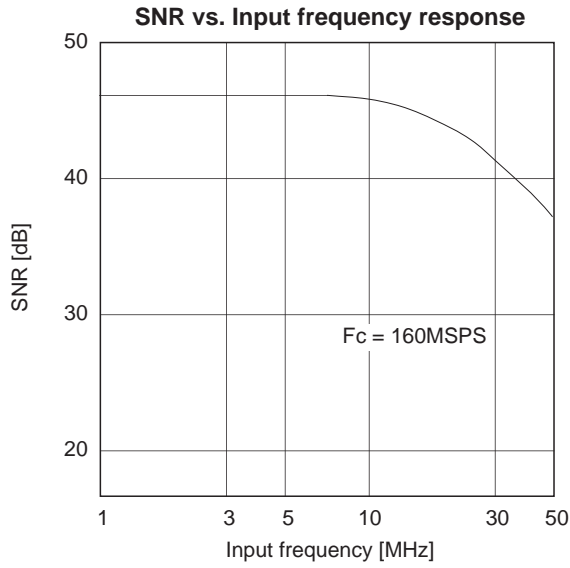
## Notes on Operation

- The CXA3286R has the PECL and TTL input pins for the clock and reset input pins. When the clock is input in PECL level, inputting the reset signal in PECL level is recommended. Also, when the clock is input in TTL level, inputting the reset signal in TTL is recommended.
- The impedance of the input signal should be properly matched to ensure the CXA3286R's stable operation at the high speed.
- The power supply and grounding have a profound influence on converter performance. The power supply and grounding method are particularly important during high-speed operation. General points for caution are as follows.
  - The ground pattern should be as large as possible. It is recommended to make the power supply and ground patterns wider at an inner layer using a multi-layer board.
  - To prevent interference between AGND and DGND and between AVcc and DVcc, make sure the respective patterns are separated. To prevent a DC offset in the power supply pattern, connect the AVcc and DVcc lines at one point each via a ferrite-bead filter, etc. Shorting the AGND and DGND patterns in one place immediately under the A/D converter improves A/D converter performance.
  - Be sure to turn the analog and digital power supplies on simultaneously. If not simultaneously, the IC does not operate correctly.
  - Ground the power supply pins (AVcc, DVcc1, DVcc2, DV<sub>EE3</sub>) as close to each pin as possible with a 0.1 $\mu$ F or larger ceramic chip capacitor.  
(Connect the AVcc pin to the AGND pattern and the DVcc1, DVcc2 and DV<sub>EE3</sub> pins to the DGND pattern.)
  - It is recommended to place the ceramic chip capacitor of 0.1 $\mu$ F or more, in particular, between DVcc2 and DGND2 with the shortest distance. This has the effect to suppress the noise generated when the CXA3286R TTL output circuit operates.
  - The digital output wiring should be as short as possible. If the digital output wiring is long, the wiring capacitance will increase, deteriorating the output slew rate and resulting in reflection to the output waveform since the original output slew rate is quite fast.
- The analog input pin V<sub>IN</sub> has an input capacitance of approximately 10pF. To drive the A/D converter with the proper frequency response, it is necessary to prevent performance deterioration due to parasitic capacitance or parasitic inductance by using a large capacity drive circuit, keeping wiring as short as possible, and using chip parts for resistors and capacitors, etc.
- The V<sub>RT</sub> and V<sub>RB</sub> pins must have adequate by-pass to protect them from high-frequency noise. By-pass them to AGND with approximately 1 $\mu$ F tantal capacitor and 0.1 $\mu$ F chip capacitor as short as possible.
- If the CLKN/E pin is not used, by-pass this pin to DGND with an approximately 0.1 $\mu$ F capacitor. At this time, approximately DGND3 – 1.2V voltage is generated. However, this is not recommended for use as the threshold voltage V<sub>BB</sub> because it is too weak.

- When the digital input level is ECL or PECL level, **\*/E** pins should be used and **\*/T** pins left open. When the digital input level is TTL, **\*/T** pins should be used and **\*/E** pins left open.
- The CXA3286R TTL output high level is clamped to approximately 2.8 V in the IC. This makes it possible to directly interface with the 3.3V system CMOS IC. However, the CXA3286R has the VOCLP pin which is used to clamp the TTL output high level. See the Example of Representative Characteristics for the relationship between the VOCLP pin and the TTL high level.
- The CXA3026AQ has the output pins **P1\*\*** and **P2\*\***. However, in the CXA3286R, these symbols are changed as **PA\*\*** and **PB\*\***. At this time, the P1 side of the CXA3026AQ is changed to the PB side for the CXA3286R; the P2 side of the CXA3026AQ to the PA side for the CXA3286R.
- The pipeline delay of the CXA3286R is smaller by one clock, compared to that of CXA3026AQ.

Example of Representative Characteristics

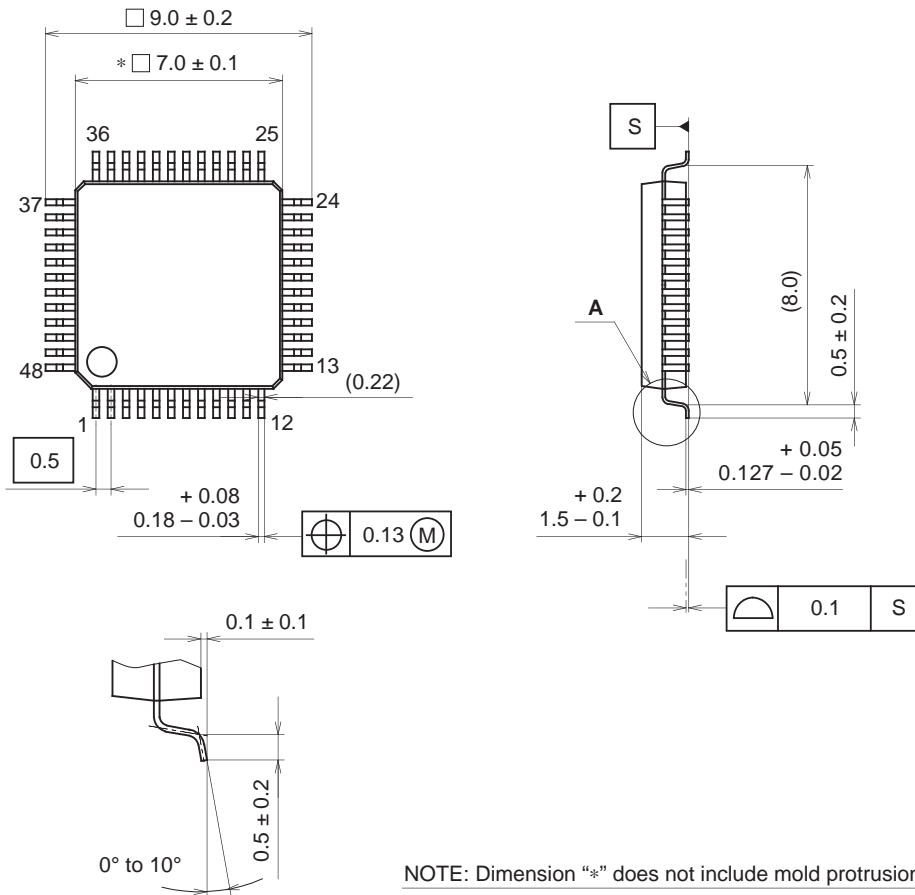




Package Outline

Unit: mm

48PIN LQFP (PLASTIC)



DETAIL A

PACKAGE STRUCTURE

SONY CODE	LQFP-48P-L01
EIAJ CODE	LQFP048-P-0707
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g

NOTE : PALLADIUM PLATING

This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).

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