

10-bit 125MSPS D/A Converter

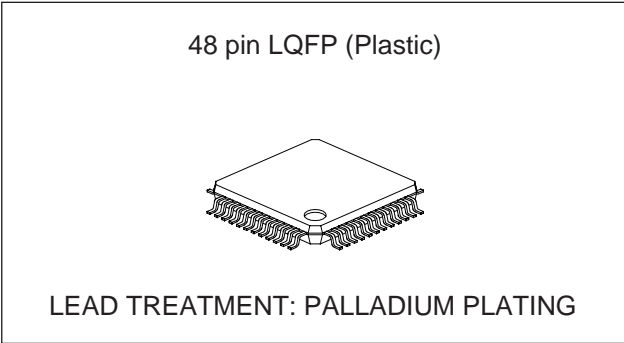
Description

The CXA3197R is a high-speed D/A converter which can perform multiplexed input of two system 10-bit data.

This IC realizes a maximum conversion rate of 125MSPS. Multiplexed operation is possible by inputting the 1/2 frequency-divided clock or by halving the frequency of the clock internally with the clock frequency divider circuit having the reset pin. The data input is at TTL level, and the clock input and reset input can select either TTL or PECL level according to the application.

Features

- Maximum conversion rate:
 - During PECL operation: 125MSPS
 - During TTL operation: 100MSPS
- Resolution: 10 bits
- Low power consumption: 480mW (typ.)
- Data input level: TTL
- Clock, reset input level: TTL and PECL compatible
- 2:1 multiplexed input function
- 1/2 frequency-divided clock output possible by the built-in clock frequency divider circuit
- Voltage output (50Ω load drive possible)
- Single power supply or ±dual power supply operation
- Reset signal polarity switching function



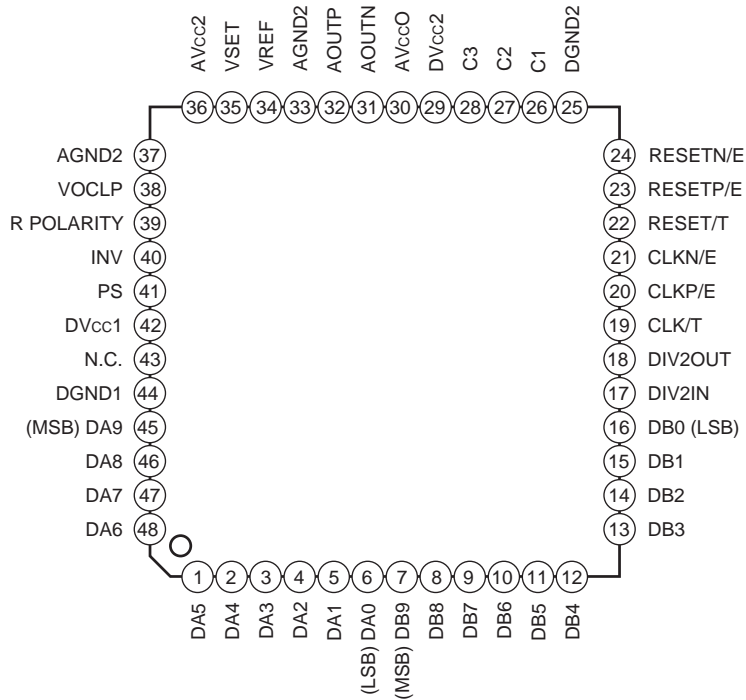
Structure

Bipolar silicon monolithic IC

Applications

- LCD
- DDS
- HDTV
- Communications (QPSK, QAM)
- Measuring devices

Pin Configuration



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Absolute Maximum Ratings (Ta = 25°C)

| | | | |
|-------------------------------|---------------------|----------------------------|----|
| • Supply voltage | AVccO, AVcc2, DVcc2 | -0.5 to +6.0 | V |
| | AGND2, DGND2 | -6.0 to +0.5 | V |
| | DVcc1 | -0.5 to +6.0 | V |
| | AVcc2 – AGND2 | -0.5 to +6.0 | V |
| | AVccO – AGND2 | -0.5 to +6.0 | V |
| • Input voltage (Analog) | DVcc2 – DGND2 | -0.5 to +6.0 | V |
| | VSET | AGND2 – 0.5 to AVcc2 + 0.5 | V |
| | TTL input pin | DGND1 – 0.5 to DVcc1 + 0.5 | V |
| | PECL input pin | DGND1 – 0.5 to DVcc1 + 0.5 | V |
| | PS | DGND1 – 0.5 to DVcc1 + 0.5 | V |
| (Others) | VOCLP | DGND1 – 0.5 to DVcc1 + 0.5 | V |
| | VOCLP | DGND1 – 0.5 to DVcc1 + 0.5 | V |
| • Storage temperature | Tstg | -65 to +150 | °C |
| • Allowable power dissipation | Pd | 1.4 | W |

(when mounted on a two-layer glass fabric base epoxy board with dimensions of 76mm × 114mm, t = 1.6mm)

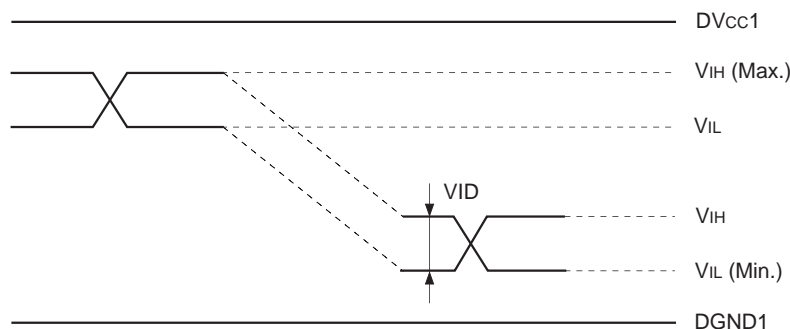
Recommended Operating Conditions

| • Supply voltage | [Single power supply] | | | [Dual power supply] | | | Unit |
|------------------|-----------------------|------|-------|---------------------|------|-------|------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| AVccO | +4.75 | +5.0 | +5.25 | -0.05 | 0.0 | +0.05 | V |
| AVcc2 | +4.75 | +5.0 | +5.25 | -0.05 | 0.0 | +0.05 | V |
| AGND2 | -0.05 | 0.0 | +0.05 | -5.50 | -5.0 | -4.75 | V |
| DVcc1 | +4.75 | +5.0 | +5.25 | +4.75 | +5.0 | +5.25 | V |
| DGND1 | -0.05 | 0.0 | +0.05 | -0.05 | 0.0 | +0.05 | V |
| DVcc2 | +4.75 | +5.0 | +5.25 | -0.05 | 0.0 | +0.05 | V |
| DGND2 | -0.05 | 0.0 | +0.05 | -5.50 | -5.0 | -4.75 | V |

| • Input voltage (Analog) | VSET | | Min. | Typ. | Max. | Unit | |
|------------------------------------|-----------------------|-----------------|-----------------|------|--------------|-------------|---|
| | | | AGND2 + 0.65 | | AGND2 + 1.03 | | |
| (Digital) | TTL input pin | | V _{IH} | | DGND1 + 2.0 | V | |
| | | | V _{IL} | | DGND1 + 0.8 | V | |
| (Others) | PECL input pin | | V _{IH} | | DVcc1 – 1.05 | V | |
| | | | V _{IL} | | DVcc1 – 3.2 | V | |
| | | | VID*1 | 0.5 | | DVcc1 – 1.4 | V |
| | | | VOCLP | | DGND1 + 2.4 | | V |
| • CLK pulse width (for RECL CLK) | | tpw1 | | 3.5 | | ns | |
| | | tpw0 | | 3.5 | | ns | |
| • Maximum conversion rate | During PECL operation | F _c | | 125 | | MSPS | |
| | During TTL operation | F _c | | 100 | | MSPS | |
| • Load resistance | | R _L | | 50 | 50 | ≥ 10k Ω | |
| • Analog output full-scale voltage | R _L ≥ 10kΩ | V _{FS} | | 1.5 | 2.0 | 2.1 V | |
| | R _L = 50Ω | V _{FS} | | 0.75 | 1.0 | 1.05 V | |
| • Operating temperature | | T _a | | -20 | | +75 °C | |

*1 VID: Input Voltage Differential

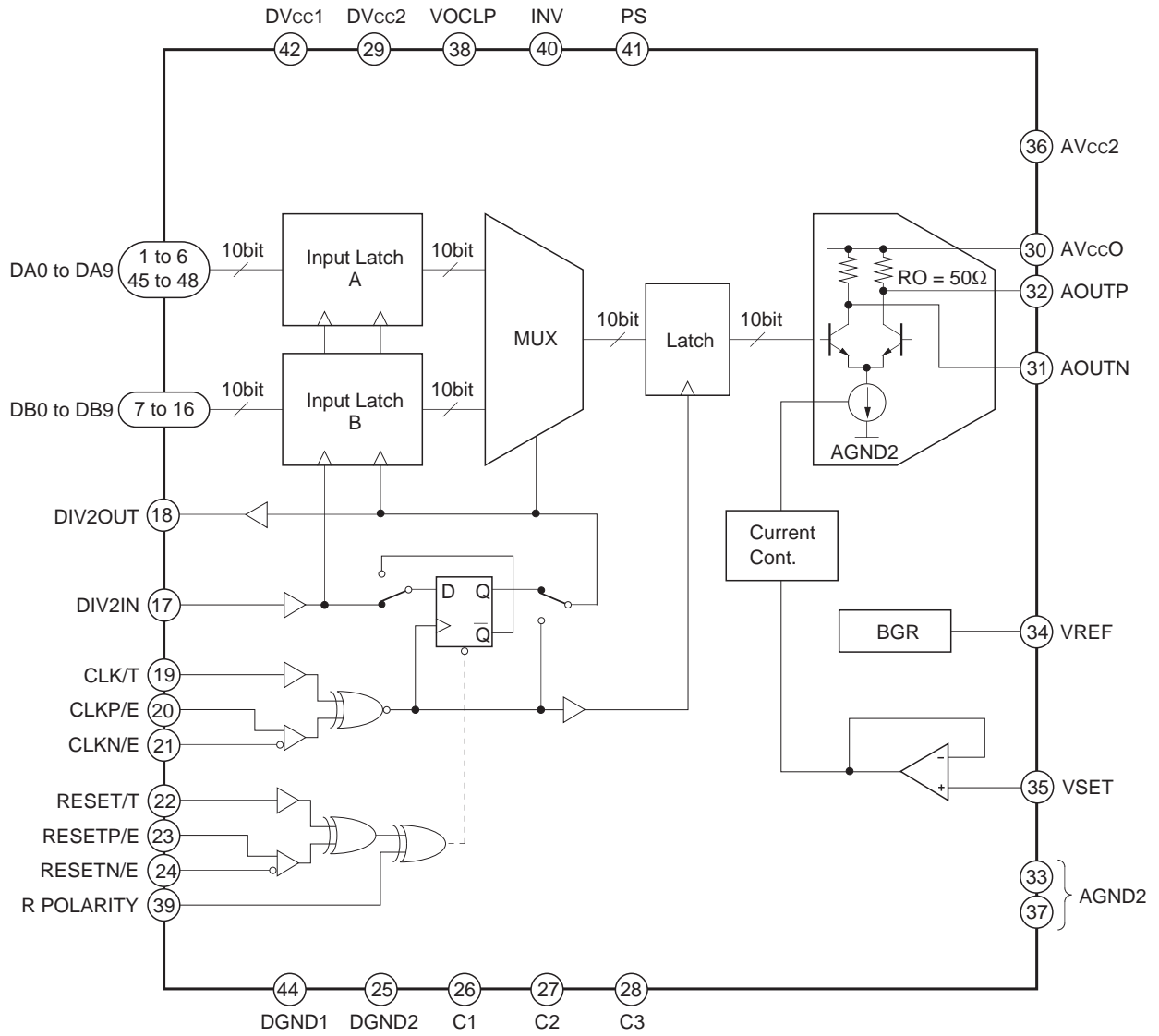
PECL input signal switching level



Pin Description

| [Symbol] | [Pin No.] | [Description] | [Typical voltage level for a single power supply] | [Typical voltage level for dual power supply] |
|------------|------------------|-------------------------------------|--------------------------------------------------------|----------------------------------------------------|
| DA0 to DA9 | 1 to 6, 45 to 48 | Side A data input. | TTL | TTL |
| DB0 to DB9 | 7 to 16 | Side B data input. | TTL | TTL |
| DIV2IN | 17 | 1/2 frequency-divided clock input. | TTL | TTL |
| DIV2OUT | 18 | 1/2 frequency-divided clock output. | TTL | TTL |
| CLK/T | 19 | TTL clock input. | TTL | TTL |
| CLKP/E | 20 | PECL clock input. | PECL | PECL |
| CLKN/E | 21 | PECL clock input. | PECL | PECL |
| RESET/T | 22 | TTL reset input. | TTL | TTL |
| RESETP/E | 23 | PECL reset input. | PECL | PECL |
| RESETN/E | 24 | PECL reset input. | PECL | PECL |
| DGND2 | 25 | Digital ground. | 0V | -5V |
| C1 | 26 | Function setting. | TTL | TTL |
| C2 | 27 | Function setting. | TTL | TTL |
| C3 | 28 | Function setting. | TTL | TTL |
| DVcc2 | 29 | Digital power supply. | 5V | 0V |
| AVccO | 30 | Analog output power supply. | 5V (typ.) | 0V (typ.) |
| AOUTN | 31 | Negative analog output. | $AV_{ccO} - V_{FS}$ | $AV_{ccO} - V_{FS}$ |
| AOUTP | 32 | Positive analog output. | $AV_{ccO} - V_{FS}$ | $AV_{ccO} - V_{FS}$ |
| AGND2 | 33 | Analog ground. | 0V | -5V |
| VREF | 34 | Analog reference voltage. | $AGND2 + 1.25V$ | $AGND2 + 1.25V$ |
| VSET | 35 | Full-scale adjustment. | $AGND2 + 0.65V$ to $AGND2 + 1.03V$ | $AGND2 + 0.65V$ to $AGND2 + 1.03V$ |
| AVcc2 | 36 | Analog power supply. | 5V | 0V |
| AGND2 | 37 | Analog ground. | 0V | -5V |
| VOCLP | 38 | TTL High level clamp. | Clamp voltage | Clamp voltage |
| R POLARITY | 39 | Reset signal polarity switching. | TTL | TTL |
| INV | 40 | Analog output inversion. | TTL | TTL |
| PS | 41 | Power saving. | TTL | TTL |
| DVcc1 | 42 | Digital power supply. | 5V | 5V |
| N.C. | 43 | Not connected. | — | — |
| DGND1 | 44 | Digital ground. | 0V | 0V |

Block Diagram



Pin Description and I/O Pin Equivalent Circuit

| Pin No. | Symbol | I/O | Typical voltage level | Equivalent circuit | Description |
|--------------------|------------|-----|-----------------------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 to 6 45 to 48 | DA0 to DA9 | I | TTL | | Side A data input. |
| 7 to 16 | DB0 to DB9 | I | TTL | | Side B data input. |
| 17 | DIV2IN | I | TTL | | 1/2 frequency-divided clock input. Use this pin in MUX.1A or MUX.2 mode. Leave open for other modes. |
| 18 | DIV2OUT | O | TTL | | 1/2 frequency-divided clock output. The 1/2 frequency-divided clock signal (DIV2OUT) is output in MUX.1A mode. Set to high impedance for other modes. |
| 19 | CLK/T | I | TTL | | Clock input. Use this pin when the clock is input at TTL level. At this time, leave Pins 20 and 21 open. |

| Pin No. | Symbol | I/O | Typical voltage level | Equivalent circuit | Description |
|---------|----------|-----|----------------------------------------------------|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 20 | CLKP/E | I | PECL | | <p>Clock input. Use this pin when the clock is input at PECL level. At this time, leave Pin 19 open. CLKP/E and CLKN/E are complementary and should be used together.</p> |
| 21 | CLKN/E | I | PECL | | <p>CLKP/E complementary input.</p> |
| 22 | RESET/T | I | TTL | | <p>Reset signal input. When multiple CXA3197R are operated at the same time in MUX.1A or MUX.1B mode, the start timing of the internal 1/2 frequency divider circuits should be matched. At this time, the reset signal is used; when the reset signal is at TTL level, Pin 22 is used and Pins 23 and 24 are left open. When the reset signal is at PECL level, Pins 23 and 24 are used and Pin 22 is left open. The reset signal polarity can be set by Pin 39 (R POLARITY). Leave the reset pin open when other modes are used. RESETP/E and RESETN/E are complementary and should be used together.</p> |
| 23 | RESETP/E | I | PECL | | <p>RESETP/E and RESETN/E are complementary and should be used together.</p> |
| 24 | RESETN/E | I | PECL | | <p>RESETP/E and RESETN/E are complementary and should be used together.</p> |
| 25 | DGND2 | | Single power supply: GND Dual power supply: -5V | | Digital power supply. |
| 26 | C1 | I | TTL | | Function setting. |
| 27 | C2 | I | TTL | | Function setting. |
| 28 | C3 | I | TTL | | Function setting. |

| Pin No. | Symbol | I/O | Typical voltage level | Equivalent circuit | Description |
|---------|--------|-----|----------------------------------------------------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29 | DVcc2 | | Single power supply: +5V Dual power supply: GND | | Digital power supply. |
| 30 | AVccO | | Single power supply: +5V Dual power supply: GND | | Analog output power supply. The AVccO pin voltage can be varied within the range that satisfies the analog output compliance voltage. |
| 31 | AOUTN | O | AVccO - VFs | | Negative analog output. The inverse of the positive analog output pin is output. When the positive output is terminated with 50Ω, the inverse output pin should also be terminated with 50Ω even if the inverse output is not used. |
| 32 | AOUTP | O | AVccO - VFs | | Positive analog output. |
| 33 | AGND2 | | Single power supply: GND Dual power supply: -5V | | Analog ground. |
| 34 | VREF | O | AGND + 1.25V (Typ.) | | Reference voltage output. |
| 35 | VSET | I | AGND2 + 0.65V to AGND2 + 1.03V | | Analog output full-scale adjustment. |
| 36 | AVcc2 | | Single power supply: +5V Dual power supply: GND | | Analog power supply. |

| Pin No. | Symbol | I/O | Typical voltage level | Equivalent circuit | Description |
|---------|------------|-----|----------------------------------------------------|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 37 | AGND2 | | Single power supply: GND Dual power supply: -5V | | Analog power supply. |
| 38 | VOCLP | I | Clamp voltage | | TTL output High level clamp. A TTL level signal is output from the DIV2OUT pin in MUX.1A mode. The TTL High level voltage can be clamped to the value approximately equivalent to the voltage applied to this pin. Leave the VOCLP pin open for other modes. |
| 39 | R POLARITY | I | TTL | | Reset signal polarity switching. At High level, the reset polarity is active Low; at Low level, active High. |
| 40 | INV | I | TTL | | Analog output polarity inversion. The analog output is inverted at Low level. |
| 41 | PS | I | TTL | | Power saving. Power saving mode is activated at Low level. Normally pull up the PS pin to High level as this pin is open Low. |
| 42 | DVcc1 | | 5V | | Digital power supply. |
| 43 | N.C. | | | | Not connected. |
| 44 | DGND1 | | 0V | | Digital ground. |

Electrical Characteristics

(DV_{cc1}, DV_{cc2}, AV_{cc2}, AV_{ccO} = +5V, DGND1, DGND2 = 0V, Ta = 25°C)

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|------------------------------------------------------------|------------------------------------------|------------------------------------------------------------------------------------------|-----------------------------------------------------|--------|----------------------------------------------------|----------------|
| Resolution | n | | 10 | 10 | 10 | bit |
| Differential linearity error | DLE | V _{FS} = 1000mV | | | -0.85/+0.5 | LSB |
| Integral linearity error | ILE | | | | -1.2/+0.5 ±1.2 | LSB LSB |
| Digital input (PECL) Digital input voltage | V _{IH} V _{IL} | | DV _{cc1} - 1.05 DV _{cc1} - 3.2 | | DV _{cc1} - 0.5 DV _{cc1} - 1.4 | V V |
| Digital input current | I _{IH} I _{IL} | V _{IH} = DV _{cc1} - 0.8V V _{IL} = DV _{cc1} - 1.6V | 0 -30 | | 20 0 | µA µA |
| Digital input capacitance | | | | | 5 | pF |
| Digital input (TTL) Digital input voltage | V _{IH} V _{IL} | | 2 | | 0.8 | V V |
| Threshold voltage | V _{TH} | | | 1.5 | | V |
| Digital input current | I _{IH} I _{IL} | V _{IH} = 3.5V V _{IL} = 0.2V | -1 -2 | | 1 0 | µA µA |
| Digital input capacitance | | | | | 5 | pF |
| Digital output (TTL) Digital output voltage | V _{OH} V _{OL} | I _{OH} = -2.0mA I _{OL} = 1.0mA | 2.4 | | 0.5 | V V |
| Leak current at high impedance | | When V _O = 5V When V _O = 0V | 10 -1 | | 100 1 | µA µA |
| Digital output rise time | T _r | 0.8 to 2.4V (C _L = 10pF) | 1 | | 1.5 | ns |
| Digital output fall time | T _f | 0.8 to 2.4V (C _L = 10pF) | 0.6 | | 1.2 | ns |
| PS pin input (PS) PS pin input voltage | V _{IH} V _{IL} | | 2 | | | V V |
| PS pin input current | I _{IH} I _{IL} | V _{IH} = 3.5V V _{IL} = 0.2V | 1 -1 | | 0.8 100 0 | µA µA µA |
| Clamp pin (VOCLP) VOCLP pin input current | I _{VOCLP} I _{VOCLP} | V _{VOCLP} = DV _{cc1} V _{VOCLP} = 2.4V | 0 -60 | | 5 -10 | µA µA |
| Analog output characteristics Output full-scale voltage | V _{FS} V _{FS} | | 1.5 0.75 | 2 1 | 2.1 1.05 | V V |
| Output zero offset voltage | V _{OF} V _{OF} | } V _{SET} = AGND2 + 937.5mV | 0 0 | | 20 10 | mV mV |
| Output zero offset voltage | V _{OF} V _{OF} | | | | | |
| Analog output resistance | R _O | | | 50 | | Ω |
| Analog output capacitance | C _O | | | 10 | | pF |
| Absolute amplitude error | EG | V _{SET} = AGND2 + 937.5mV | -4.0 | | 4.0 | % of F.S. |
| Absolute amplitude error temperature characteristics | T _{CG} | V _{FS} = 1000mV at 25°C | | | 60 | ppm/°C |
| Analog output rise time | T _r | } When R _L = 50Ω, } V _{FS} = 1V, 10 - 90% | 0.85 | | 1.05 | ns |
| Analog output fall time | T _f | | 0.75 | | 0.85 | ns |
| Settling time | t _{SET} | | | | 3.5 | ns |
| Glitch energy | GE | | | | 5 | pVsec |
| Compliance voltage | V _{OC} | Mesured to DV _{cc2} *3 | -2.1 | | 1.5 | V |

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---------------------------------------------|-------------------|--------------------------------------------------|--------------|--------------|--------------|--------|
| Reference/control amplifier characteristics | | | | | | |
| VREF pin output voltage | VREF | } I _{REFOUT} = 1mA | AGND2 + 1.18 | AGND2 + 1.25 | AGND2 + 1.32 | V |
| VREF pin output voltage in PS mode | VREF | | AGND2 + 1.18 | AGND2 + 1.25 | AGND2 + 1.32 | V |
| VREF voltage drift coefficient | | | | | 250 | ppm/°C |
| VSET pin input current | ISET | | -5 | | 0 | μA |
| Multiplying bandwidth | | 100mVp-p, SIN, at -3dB | 50 | | | MHz |
| Current consumption | I _{cc} | Total current consumption | 63 | 96 | 129 | mA |
| | D _{Icc1} | D _{Icc1} current consumption | 7 | 15.5 | 24 | mA |
| | D _{Icc2} | D _{Icc2} current consumption | 13 | 19 | 25 | mA |
| | A _{Icc2} | A _{Icc2} current consumption | 6 | 8.5 | 11 | mA |
| | A _{IccO} | A _{IccO} current consumption | 37 | 53 | 69 | mA |
| Current consumption in PS mode *4 | I _{cc} | Total current consumption in PS mode | | 0.432 | 4 | mA |
| | D _{Icc1} | D _{Icc1} current consumption in PS mode | | 0.38 | 1.5 | mA |
| | D _{Icc2} | D _{Icc2} current consumption in PS mode | | 0.001 | 0.2 | mA |
| | A _{Icc2} | A _{Icc2} current consumption in PS mode | | 0.05 | 0.3 | mA |
| | A _{IccO} | A _{IccO} current consumption in PS mode | | 0.001 | 2 | mA |

*2 64-step D.L.E. This indicates the D.L.E. when the INV pin is High and the data input code changes between:

(MSB) (LSB) (MSB) (LSB)
 0 0 0 0 1 1 1 1 1 1 ↔ 0 0 0 1 0 0 0 0 0 0

at the AOUTP side output or between:

(MSB) (LSB) (MSB) (LSB)
 1 1 1 1 0 0 0 0 0 0 ↔ 1 1 1 0 1 1 1 1 1 1

at the AOUTN side output.

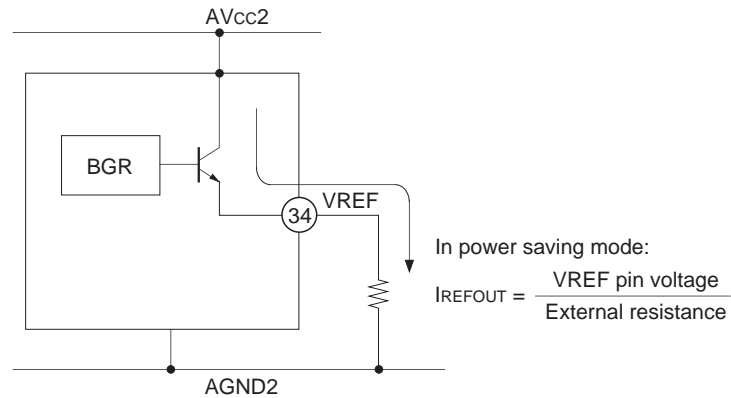
*3 When using the analog output within the compliance voltage range, set AV_{ccO} so that it satisfies the following equations.

$$V_{oc}(\min) = (AV_{ccO} - V_{FS}) - DV_{cc2} \geq -2.1V$$

$$V_{oc}(\max) = (AV_{ccO} - V_{OF}) - DV_{cc2} \leq 1.5V$$

*4 The current consumption in power saving mode does not include the VREF pin output current. When grounding the VREF pin to the AGND2 level using external resistance, a voltage of 1.18 to 1.32V is generated at the VREF pin even in power saving mode. Therefore, the current indicated by the following equation flows from the AVcc2 pin to the VREF pin. This value must be added to obtain the actual current consumption in power saving mode.

$$\frac{\text{VREF pin voltage}}{\text{External resistance}} = I_{\text{REFOUT}}$$



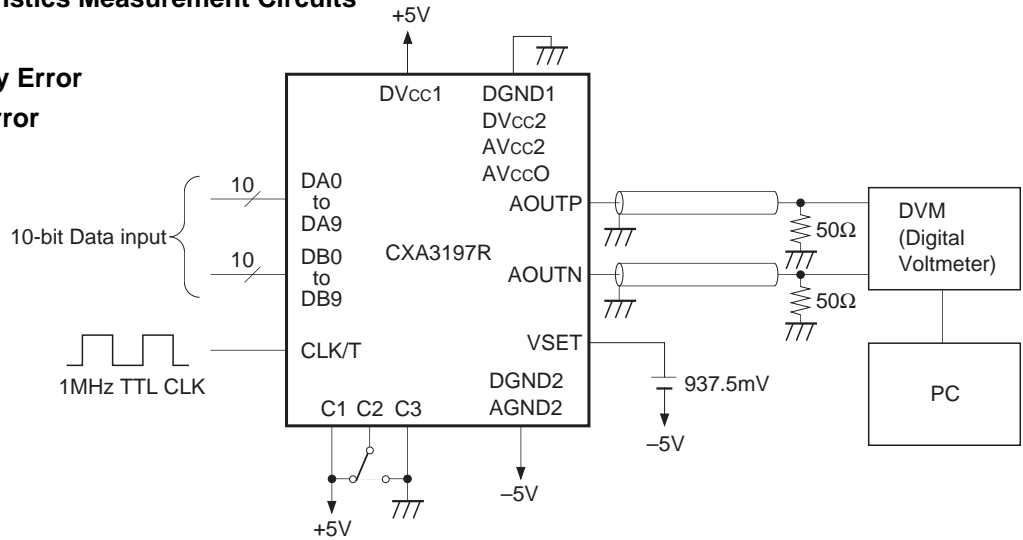
| Switching characteristics | | CLK signal level | | PECL | | TTL | | PECL | | TTL | | Unit | | |
|------------------------------|--------------------------------------|-------------------------|-----------------------|------|------|------|------|------|------|------|------|------|------|------|
| | | Reset signal level | | PECL | | TTL | | PECL | | TTL | | | | |
| | | Symbol | Conditions | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Unit | |
| MUX, 1A mode | Item | | | | | | | | | | | | | |
| | Maximum conversion rate | FC | | 125 | | | 100 | | | | | 125 | MSPS | |
| | Clock High pulse width | Tpw1 | | 3.5 | | 4.5 | | | | | | 3.5 | ns | |
| | Clock Low pulse width | Tpw0 | | 3.5 | | 3.0 | | | | | | 3.5 | ns | |
| | Reset signal setup time | ts-rst | | 0 | | 1.0 | | | | | | 4.0 | ns | |
| | Reset signal hold time | th-rst | | 1.0 | | 3.0 | | | | | | 0 | ns | |
| | DIV2OUT output delay | td-DIV | C _L = 10pF | 5.5 | 6.5 | 8 | 8.0 | 9.5 | 12.0 | 5.5 | 6.5 | 8 | ns | |
| | DIV2OUT to DIV2IN maximum delay time | 2T-tm | | | | | | | 2T-7 | | | | 2T-7 | ns |
| | Data input setup time | ts | | 1.0 | | 1.0 | | | | 1.0 | | | | ns |
| | Data input hold time | th | | 5.0 | | 5.0 | | | | 5.0 | | | | ns |
| | Analog output pipeline delay | t _{PD} (A) | | | | | | 4 | | | | 4 | | CLK |
| | | t _{PD} (B) | | | | | | 5 | | | | 5 | | CLK |
| | Analog output delay | t _{do} | | 5.0 | 5.5 | 6.0 | 6.5 | 7.5 | 8.5 | 5.0 | 5.5 | 6.0 | | ns |
| | MUX, 1B mode | Maximum conversion rate | FC | | 125 | | | 100 | | | | | 125 | MSPS |
| Clock High pulse width | | Tpw1 | | 3.5 | | 4.5 | | | | | | 3.5 | ns | |
| Clock Low pulse width | | Tpw0 | | 3.5 | | 3.0 | | | | | | 3.5 | ns | |
| Reset signal setup time | | ts-rst | | 0 | | 1.0 | | | | | | 4.0 | ns | |
| Reset signal hold time | | th-rst | | 1.0 | | 3.0 | | | | | | 0 | ns | |
| Data input setup time | | ts | | 1.0 | | 1.0 | | | | | | 1.0 | ns | |
| Data input hold time | | th | | 4.0 | | 6.0 | | | | | | 4.0 | ns | |
| Analog output pipeline delay | | t _{PD} (A) | | | | | | 2 | | | | 2 | | CLK |
| | | t _{PD} (B) | | | | | | 3 | | | | 3 | | CLK |
| Analog output delay | | t _{do} | | 5.0 | 5.5 | 6.0 | 6.5 | 7.5 | 8.5 | 5.0 | 5.5 | 6.0 | | ns |

| Switching characteristics | | CLK signal level | | PECL | | | TTL | | | | | |
|------------------------------|----------------------|------------------------------|------------|------|------|------|------|------|------|------|-----|------|
| | | Symbol | Conditions | Min. | Typ. | Max. | Min. | Typ. | Max. | Unit | | |
| Reset signal level | | Reset signal level | | —*4 | | | —*4 | | | | | |
| MUX.2 mode | | Item | | Min. | Typ. | Max. | Min. | Typ. | Max. | Unit | | |
| Switching characteristics | SELE.A, SELE.B modes | Maximum conversion rate | FC | 125 | | | 100 | | | MSPS | | |
| | | Clock High pulse width | Tpw1 | 3.5 | | | 4.5 | | | ns | | |
| | | Clock Low pulse width | Tpw0 | 3.5 | | | 3.0 | | | ns | | |
| | | DIV2IN setup time | ts-DIV | 4.5 | | | 2.0 | | | ns | | |
| | | DIV2IN hold time | th-DIV | 0 | | | 3.5 | | | ns | | |
| | | Data input setup time | ts | 1.0 | | | 1.0 | | | ns | | |
| | | Data input hold time | th | 5.0 | | | 5.0 | | | ns | | |
| | | Analog output pipeline delay | tPD (A) | | | | 2 | | | 2 | CLK | |
| | | | tPD (B) | | | | 3 | | | 3 | | |
| | | Analog output delay | tDO | | | 5.0 | 5.5 | 6.0 | 6.5 | 7.5 | 8.5 | ns |
| | | Maximum conversion rate | FC | | | 125 | | | 100 | | | MSPS |
| | | Clock High pulse width | Tpw1 | | | 3.5 | | | 4.5 | | | ns |
| | | Clock Low pulse width | Tpw0 | | | 3.5 | | | 3.0 | | | ns |
| | | C2 signal setup time | ts-C2 | | | 1.0 | | | 1.0 | | | ns |
| | | C2 signal hold time | th-C2 | | | 2.5 | | | 3.5 | | | ns |
| Data input setup time | ts | | | 1.0 | | | 1.5 | | | ns | | |
| Data input hold time | th | | | 2.0 | | | 3.5 | | | ns | | |
| Analog output pipeline delay | tPD (A) | | | | | | | 1 | | CLK | | |
| | tPD (B) | | | | | | | 1 | | | | |
| Analog output delay | tDO | | | 5.0 | 5.5 | 6.0 | 6.5 | 7.5 | 8.5 | ns | | |

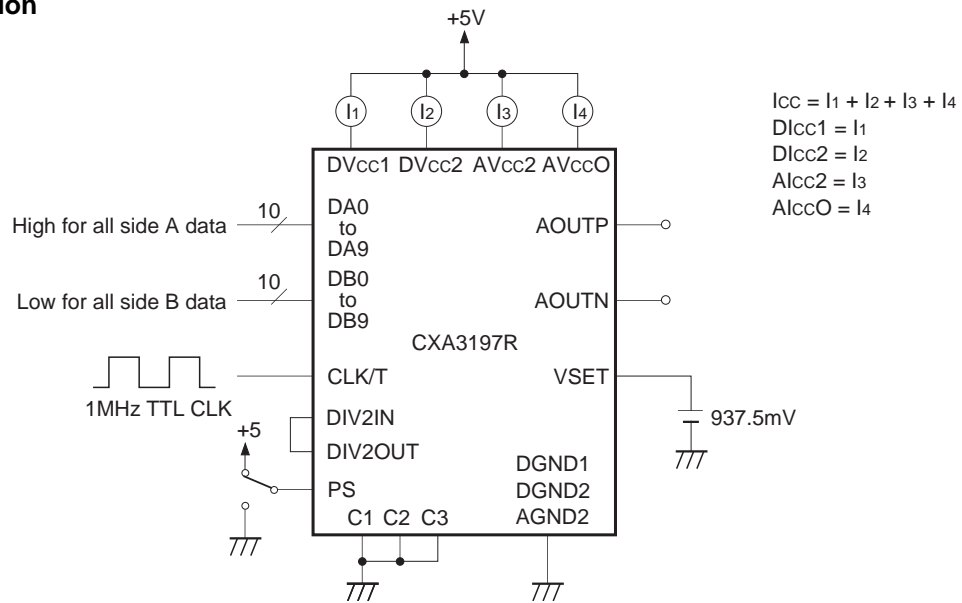
*4 The reset signal is not input in MUX.2, SELE.A or SELE.B mode.

Electrical Characteristics Measurement Circuits

**Differential Linearity Error
Integral Linearity Error**

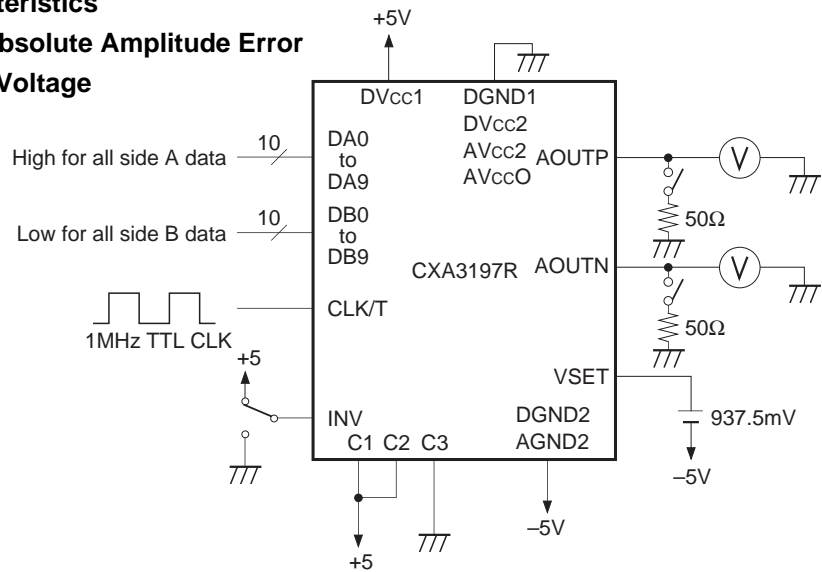


Current Consumption

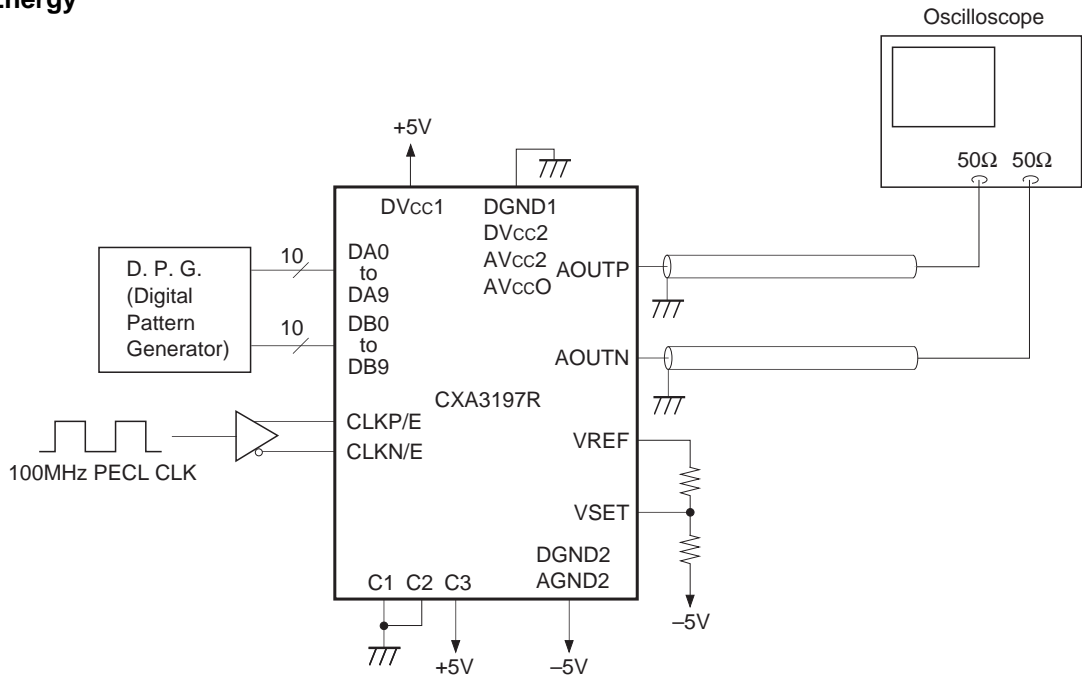


Analog Output Characteristics

**Output Full-Scale Absolute Amplitude Error
Output Zero Offset Voltage**

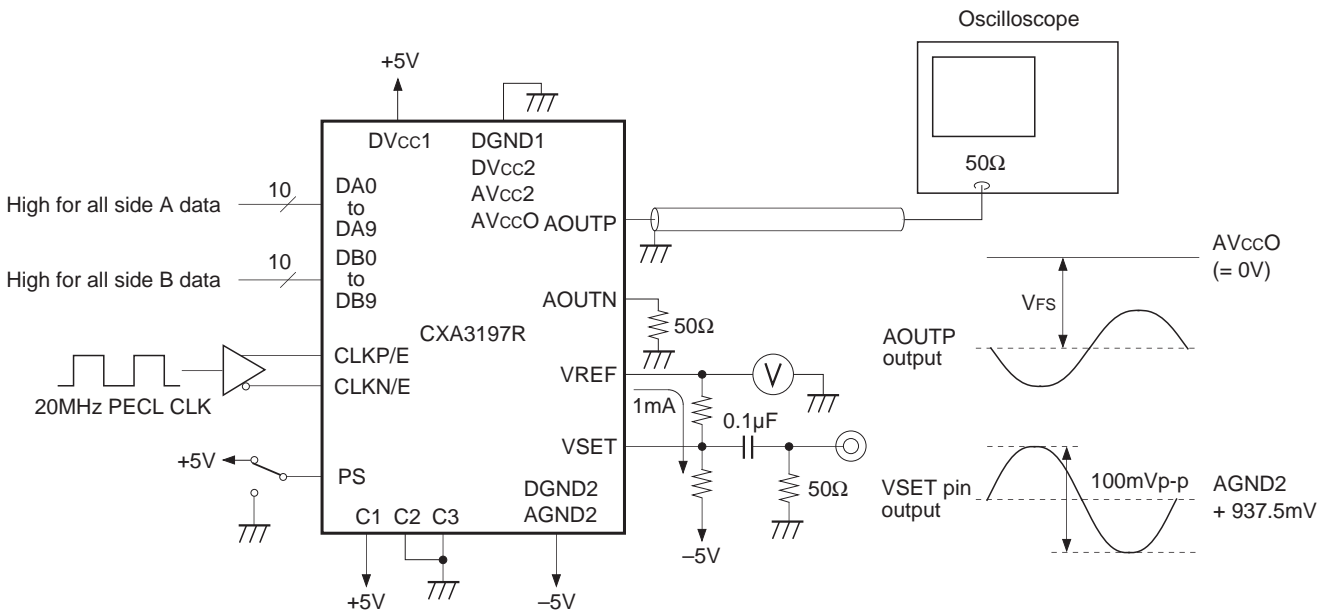


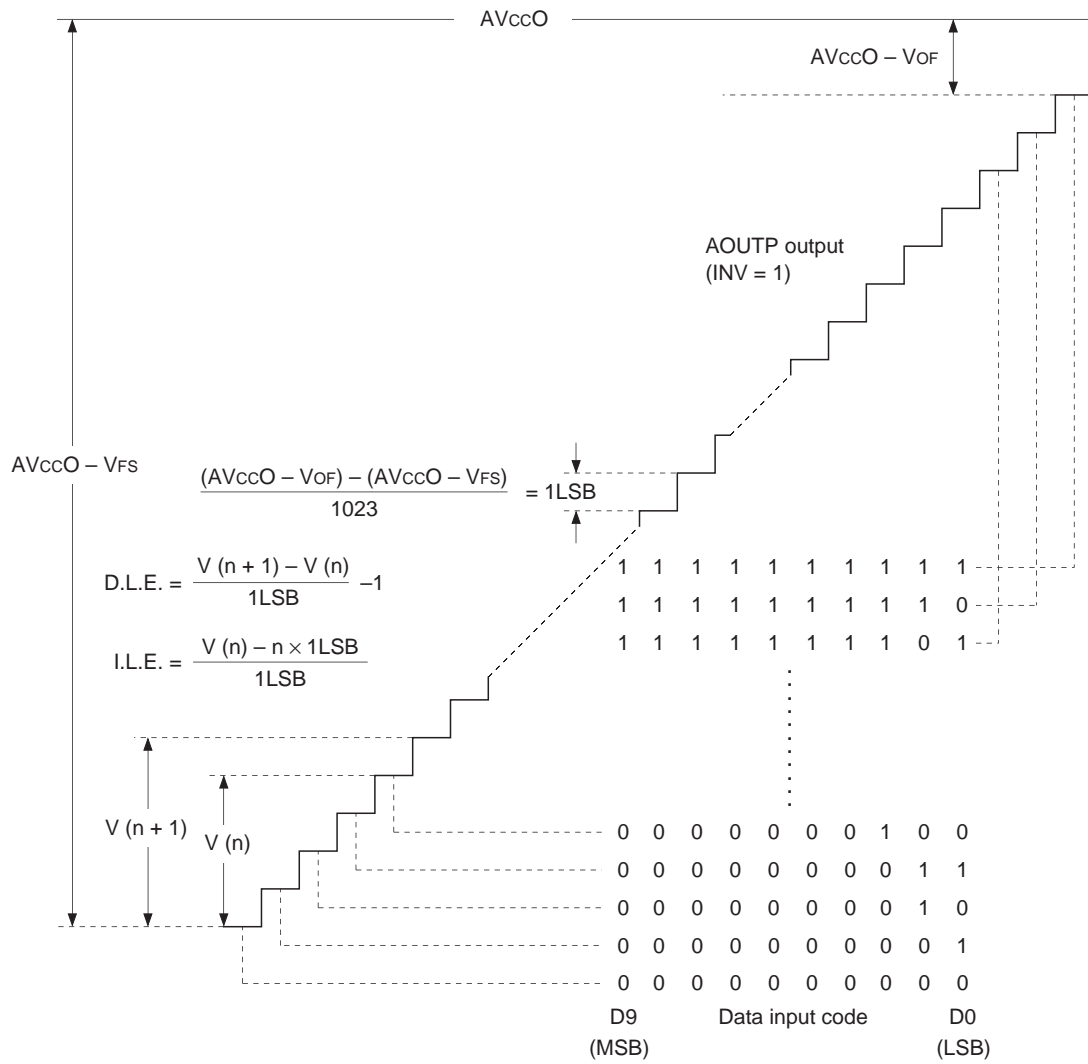
- Analog Output Rise Time
- Analog Output Fall Time
- Settling Time
- Glitch Energy



Reference/Control Amplifier Characteristics

- VREF Pin Output Voltage
- VREF Pin Output Voltage in Power Saving Mode
- Multiplying Bandwidth





| Data input code | | | | Analog output level | |
|---------------------|-------------|---------------------|-------------|---------------------|-------------|
| INV = 1 | | INV = 0 | | AOUTP | AOUTN |
| (MSB) D9 | (LSB) D0 | (MSB) D9 | (LSB) D0 | | |
| 1 1 1 1 1 1 1 1 1 1 | | 0 0 0 0 0 0 0 0 0 0 | | AVccO - VoF | AVccO - VFs |
| ⋮ | | ⋮ | | ⋮ | ⋮ |
| 0 0 0 0 0 0 0 0 0 0 | | 1 1 1 1 1 1 1 1 1 1 | | AVccO - VFs | AVccO - VoF |

Table 1. I/O Correspondence Table

Description of Operation

The CXA3197R has four types of operation modes to support various applications. The operation mode is set by switching the function setting pins (C1, C2 and C3).

Operation Mode Table

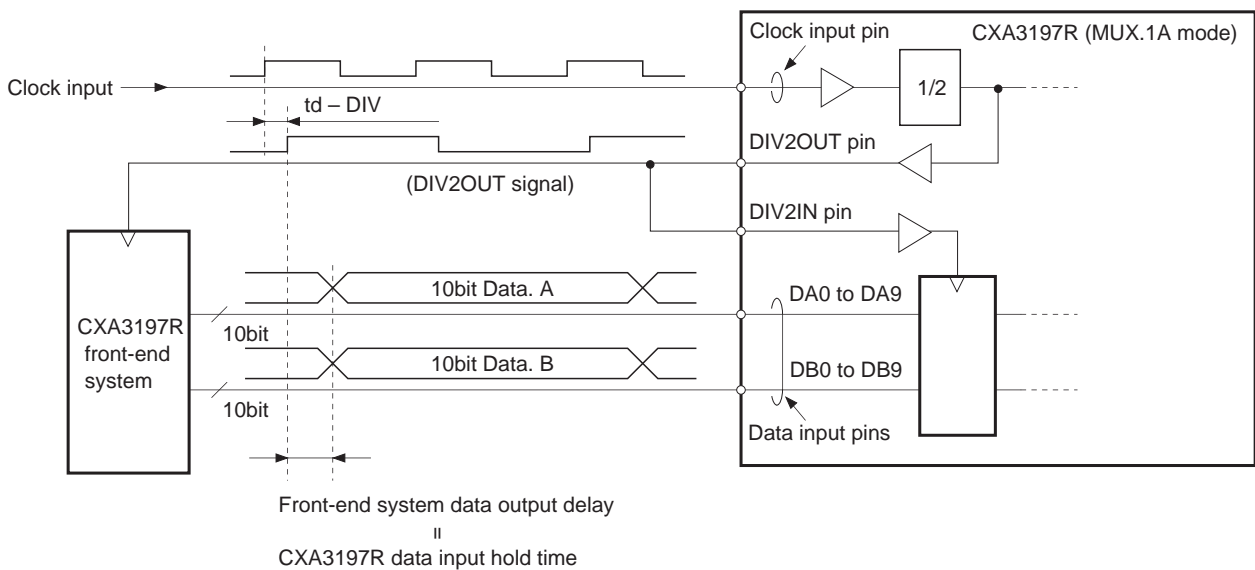
| Mode | C1 | C2 | C3 | CLK IN (MSPS) | Data IN (Mbps) | AOUT (Mbps) | DIV2OUT pin | Description of operation |
|--------|----|----|----|---------------|----------------|-------------|----------------------------|-------------------------------------|
| MUX.1A | 0 | 0 | 0 | 125 | 62.5 | 125 | Outputs CLK/2 at TTL level | MUX operation by the internal CLK/2 |
| MUX.1B | 0 | 0 | 1 | | | | High impedance | MUX operation by the internal CLK/2 |
| MUX.2 | 0 | 1 | 0 | | | | High impedance | MUX operation by DIV2IN |
| SELE.A | 1 | 0 | 0 | | 125 | | High impedance | D/A conversion of side A data input |
| SELE.B | 1 | 1 | 0 | | | | High impedance | D/A conversion of side B data input |

The CXA3197R can input data divided into two systems: A (DA0 to DA9) and B (DB0 to DB9), internally multiplex the data, and output it as an analog signal, making it possible to halve the data rate. This lets the CXA3197R support the TTL data input level in contrast to the ECL data input level for conventional high-speed D/A converters. The clock signal and reset signal input levels can be selected from either TTL or PECL according to the application. (However, setting both signals to either TTL or PECL input level is recommended.)

1. MUX.1A mode

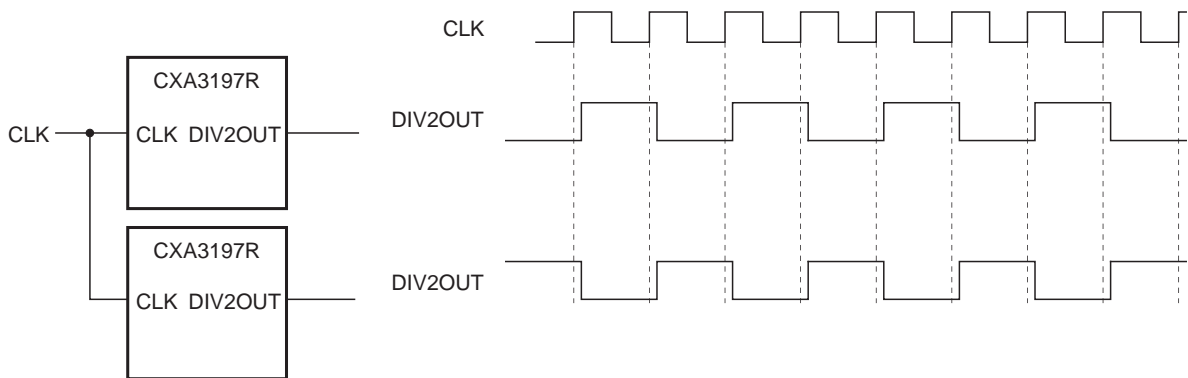
Set C1, C2 and C3 all Low for this mode.

In MUX.1A mode, the frequency of the clock input from the clock input pin is halved internally, and the 1/2 frequency-divided signal is output at TTL level from the DIV2OUT pin. Data synchronized with the DIV2OUT signal (the signal output from the DIV2OUT pin) can be obtained by operating the CXA3197R front-end system with the DIV2OUT signal. The timing at which the data output delay of the CXA3197R front-end system matches with the hold time during CXA3197R data input can be easily set by inputting this synchronized data to the data input pins and the DIV2OUT signal to the DIV2IN pin. The data can be divided and input to two systems: A (DA0 to DA9) and B (DB0 to DB9), internally multiplexed, and extracted as analog output.

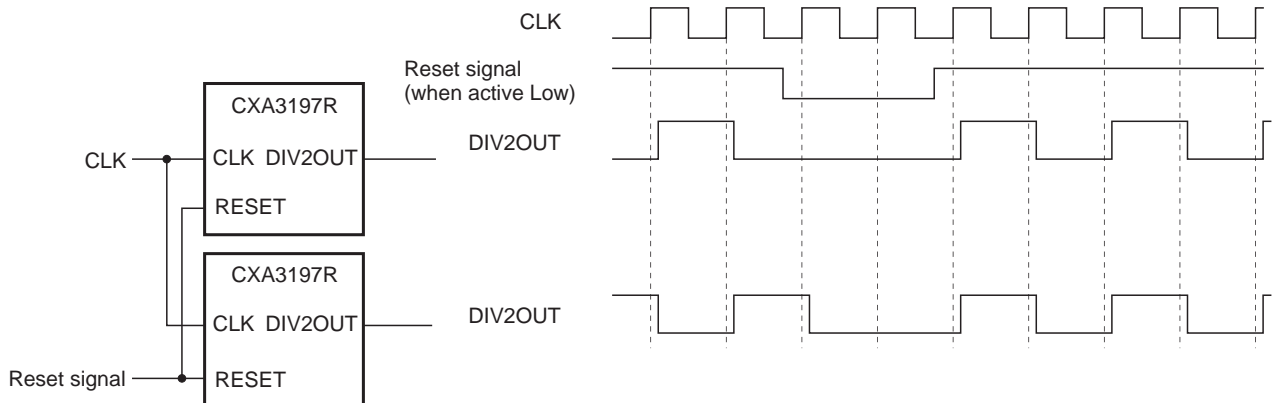


When using the multiple CXA3197R in MUX.1A mode, the start timing of the 1/2 frequency-divided clocks becomes out of phase, producing operation such as that shown in the example below. As a countermeasure, the MUX.1A mode has a function that matches the start timing of the 1/2 frequency-divided clocks with the reset signal. When using a PECL level reset signal, input the reset signal to Pins 23 and 24 (RESETP/E, RESETN/E) and leave Pin 22 (RESET/T) open. When using a TTL level reset signal, input the reset signal to Pin 22 (RESET/T) and leave Pins 23 and 24 (RESETP/E, RESETN/E) open. The reset polarity can be switched by the R POLARITY pin (Pin 39). When the R POLARITY pin is High or open, reset is active Low; when Low, reset is active High. See the timing chart for the detailed timing.

Example when not using the reset signal



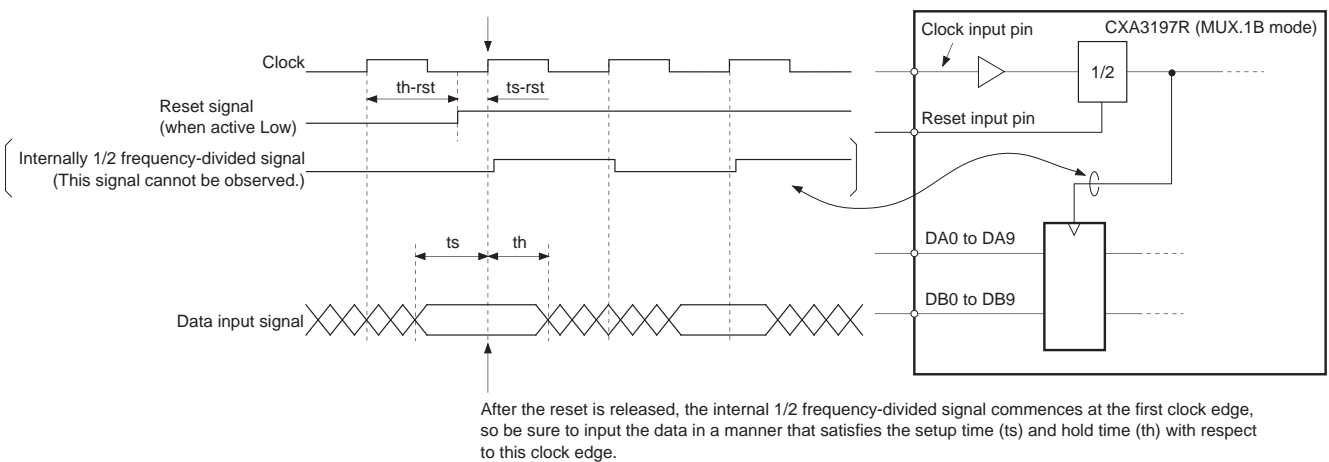
Example when using the reset signal



2. MUX.1B mode

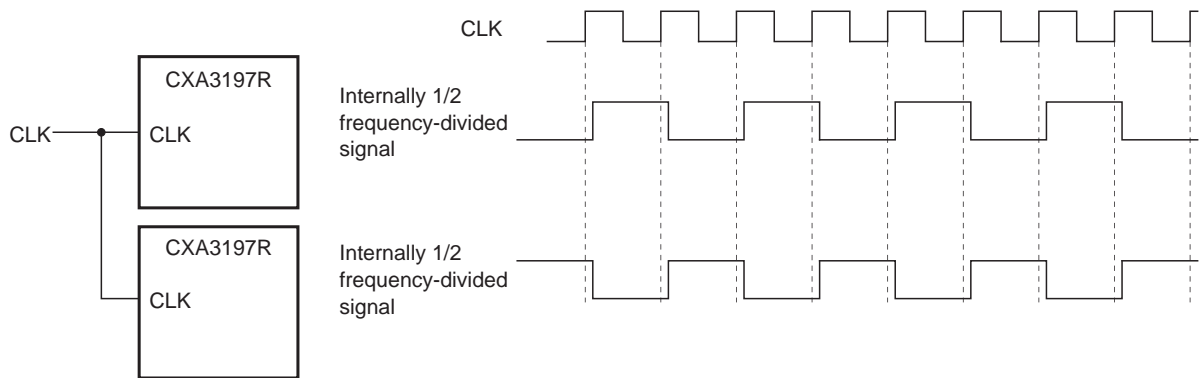
Set C1 and C2 Low and C3 High for this mode.

In MUX.1B mode, the frequency of the clock input from the clock input pin is halved internally, and the data is loaded by this 1/2 frequency-divided signal. The 1/2 frequency-divided signal cannot be observed at this time, so the data is actually loaded by observing the clock and reset signals to estimate the rising edge of the internally 1/2 frequency-divided signal. The data can be divided and input to two systems: A (DA0 to DA9) and B (DB0 to DB9). The data is internally multiplexed, then the system A data is output as an analog signal with a 2-clock pipeline delay, and the system B data as an analog signal with a 3-clock pipeline delay after loading by the clock.

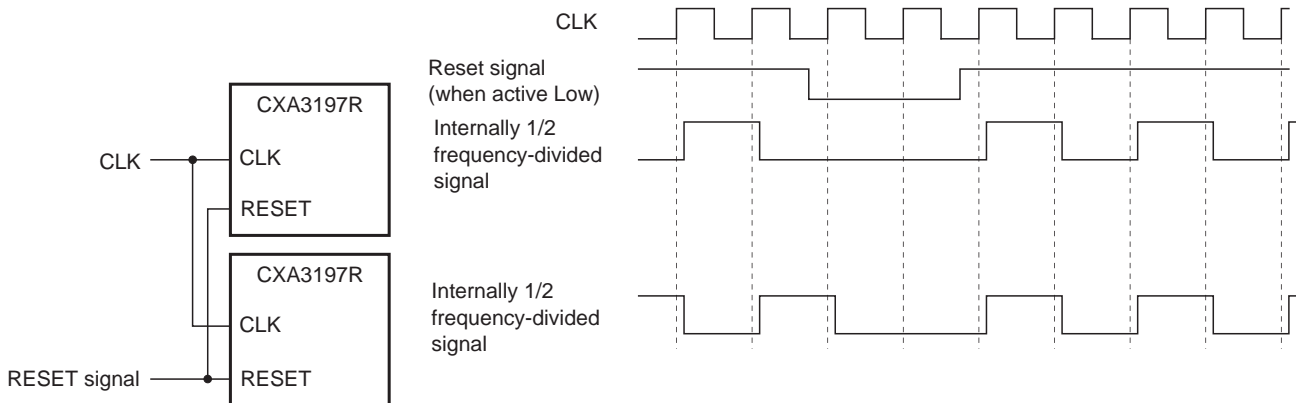


Like MUX.1A mode, when using the multiple CXA3197R in MUX.1B mode, the start timing of the 1/2 frequency-divided clocks becomes out of phase, producing operation such as that shown in the example below. As a countermeasure, the MUX.1B mode also has a function that matches the start timing of the 1/2 frequency-divided clocks with the reset signal. When using a PECL level reset signal, input the reset signal to Pins 23 and 24 (RESETP/E, RESETN/E) and leave Pin 22 (RESET/T) open. When using a TTL level reset signal, input the reset signal to Pin 22 (RESET/T) and leave Pins 23 and 24 (RESETP/E, RESETN/E) open. The reset polarity can be switched by the R POLARITY pin (Pin 39). When the R POLARITY pin is High or open, reset is active Low; when Low, reset is active High. See the timing chart for the detailed timing.

Example when not using the reset signal



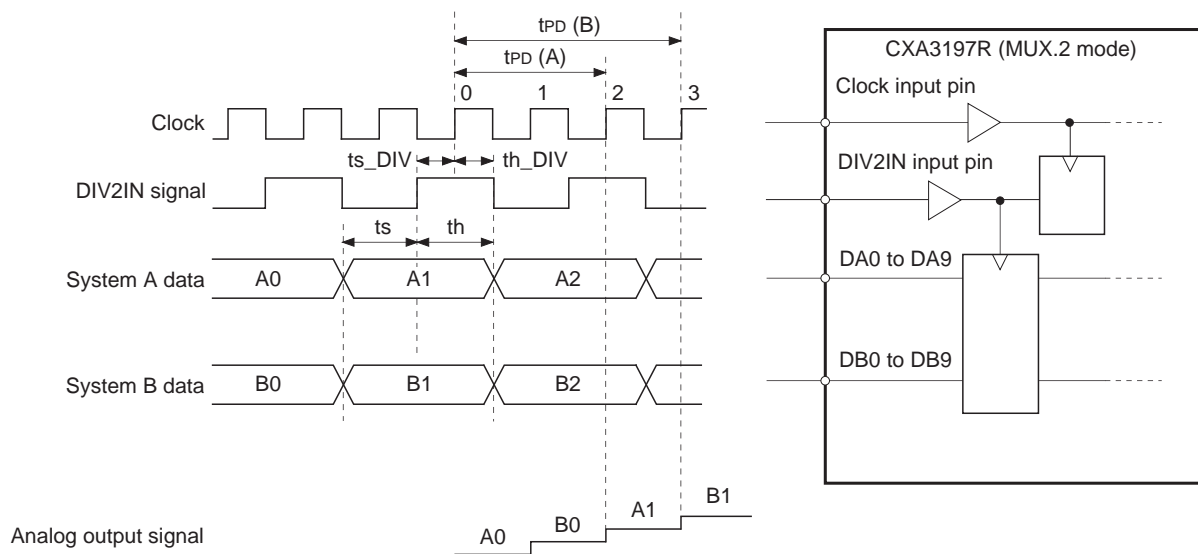
Example when using the reset signal



3. MUX.2 mode

Set C1 and C3 Low and C2 High for this mode.

In MUX.2 mode, the clock is input to the clock input pin, and the signal with a cycle half that of the clock (hereafter, DIV2IN signal) is input to the DIV2IN pin at TTL level. The DIV2IN signal is internally latched by the clock, so consideration must be given to the setup time (t_{s_DIV}) and hold time (t_{h_DIV}) with respect to the clock. In addition, the data is loaded by the DIV2IN signal, so consideration must also be given to the setup time (t_s) and hold time (t_h) with respect to the DIV2IN signal. The data can be divided and input to two systems: A (DA0 to DA9) and B (DB0 to DB9). The data is internally multiplexed, then the system A data is output as an analog signal with a 2-clock pipeline delay, and the system B data as an analog signal with a 3-clock pipeline delay from the clock that loads the DIV2IN signal. See the timing chart for the detailed timing.



4. SELE.A mode and SELE.B mode

Set C1 High and C2 and C3 Low for SELE.A mode.

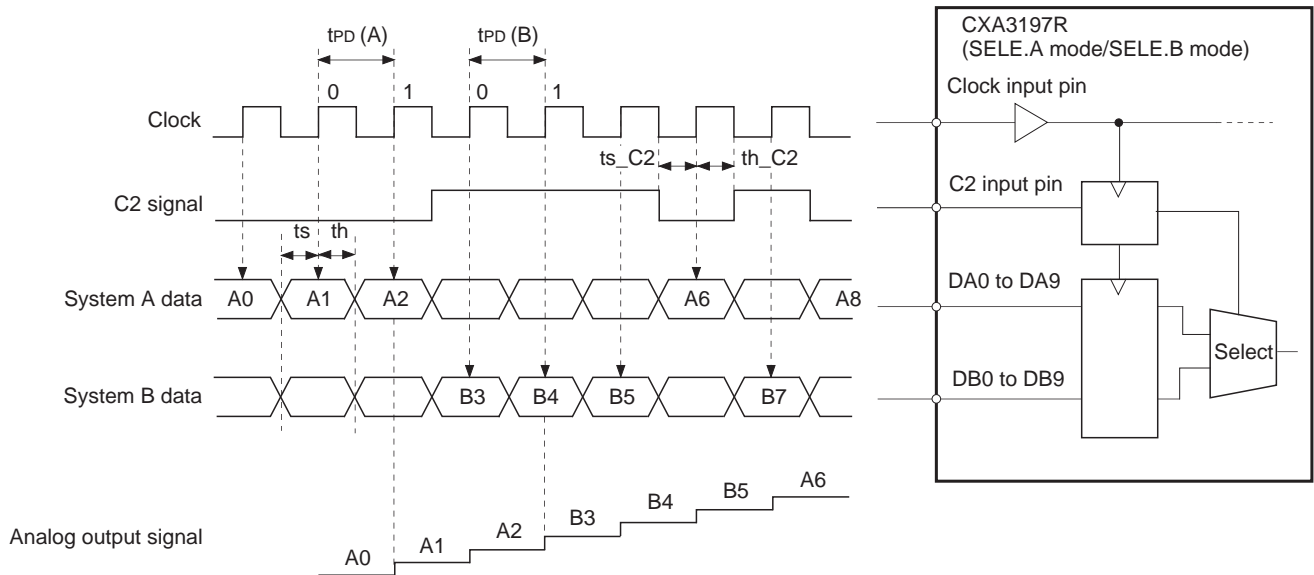
In SELE.A mode, the clock is input to the clock input pin, and the data is input to the system A (DA0 to DA9) data input pins.

Set C1 and C2 High and C3 Low for SELE.B mode.

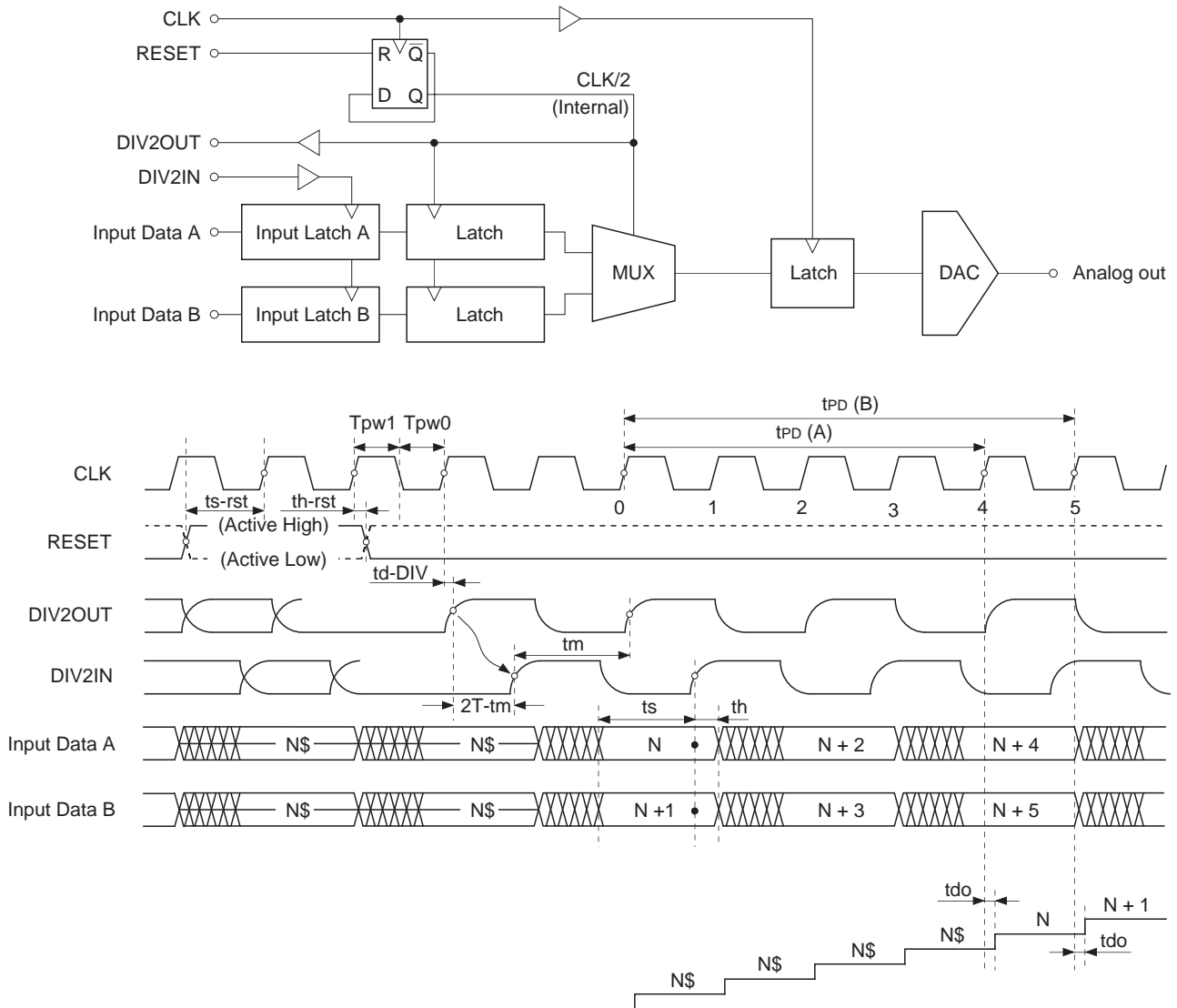
In SELE.B mode, the clock is input to the clock input pin, and the data is input to the system B (DB0 to DB9) data input pins.

In either mode, consideration must be given to the setup time (t_s) and hold time (t_h) with respect to the clock. Also, the data is output as an analog signal with a 1-clock pipeline delay after loading by the clock.

Switching between SELE.A mode and SELE.B mode is done by switching the C2 pin between High and Low levels. Also, the mode can be switched at high speed in sync with the clock by inputting the switching signal (C2 signal) to the C2 pin. The C2 signal is internally latched by the clock, so consideration must be given to the setup time (t_{s_C2}) and hold time (t_{h_C2}) with respect to the clock. See the timing chart for the detailed timing.

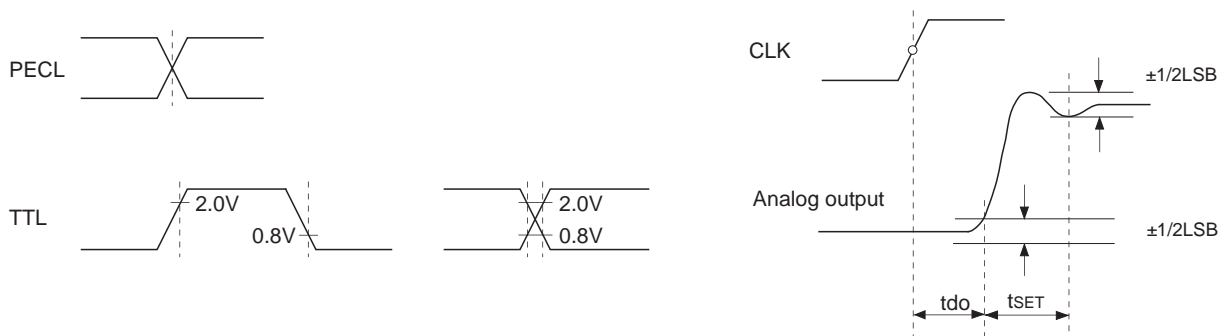


Block Diagram & Timing Chart (MUX.1A Mode)

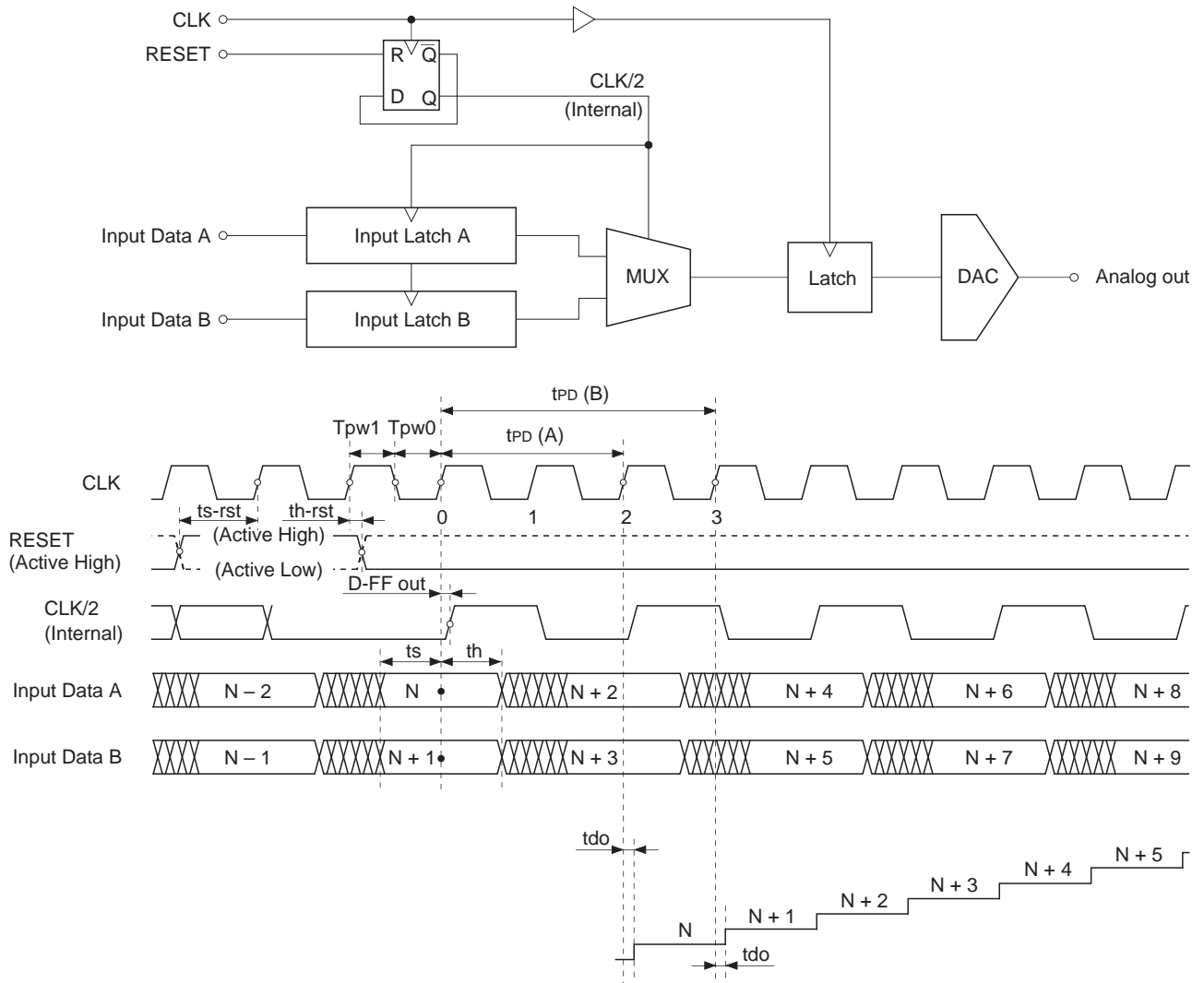


In MUX.1A mode, Data A and Data B are internally multiplexed and then the resulting signal can be analog output. The frequency of the clock is halved by the built-in clock frequency divider circuit and the CLK/2 can be output at TTL level (DIV2OUT). CLK/2 can be reset by the reset signal.

(Timing judgment points)

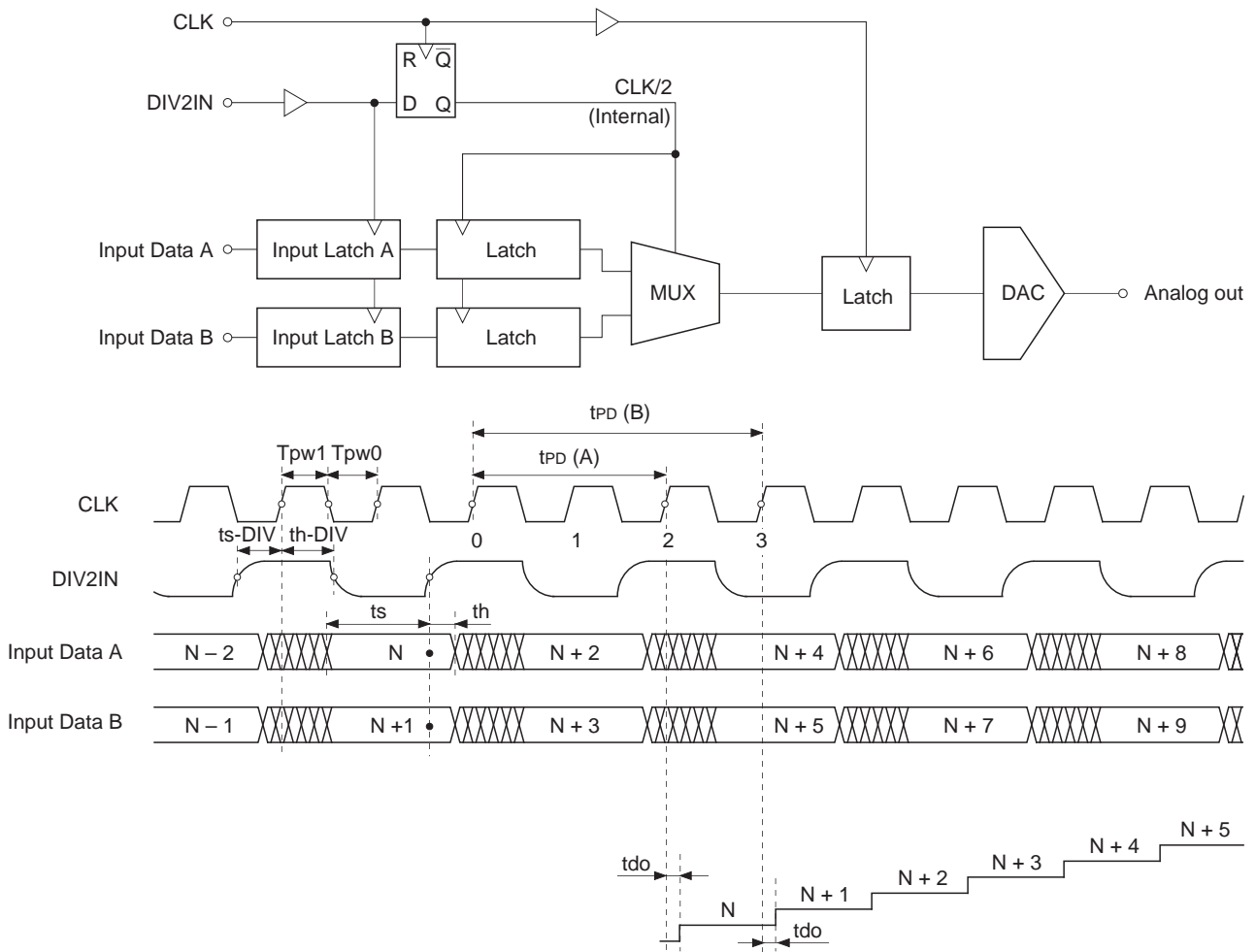


Block Diagram & Timing Chart (MUX.1B Mode)



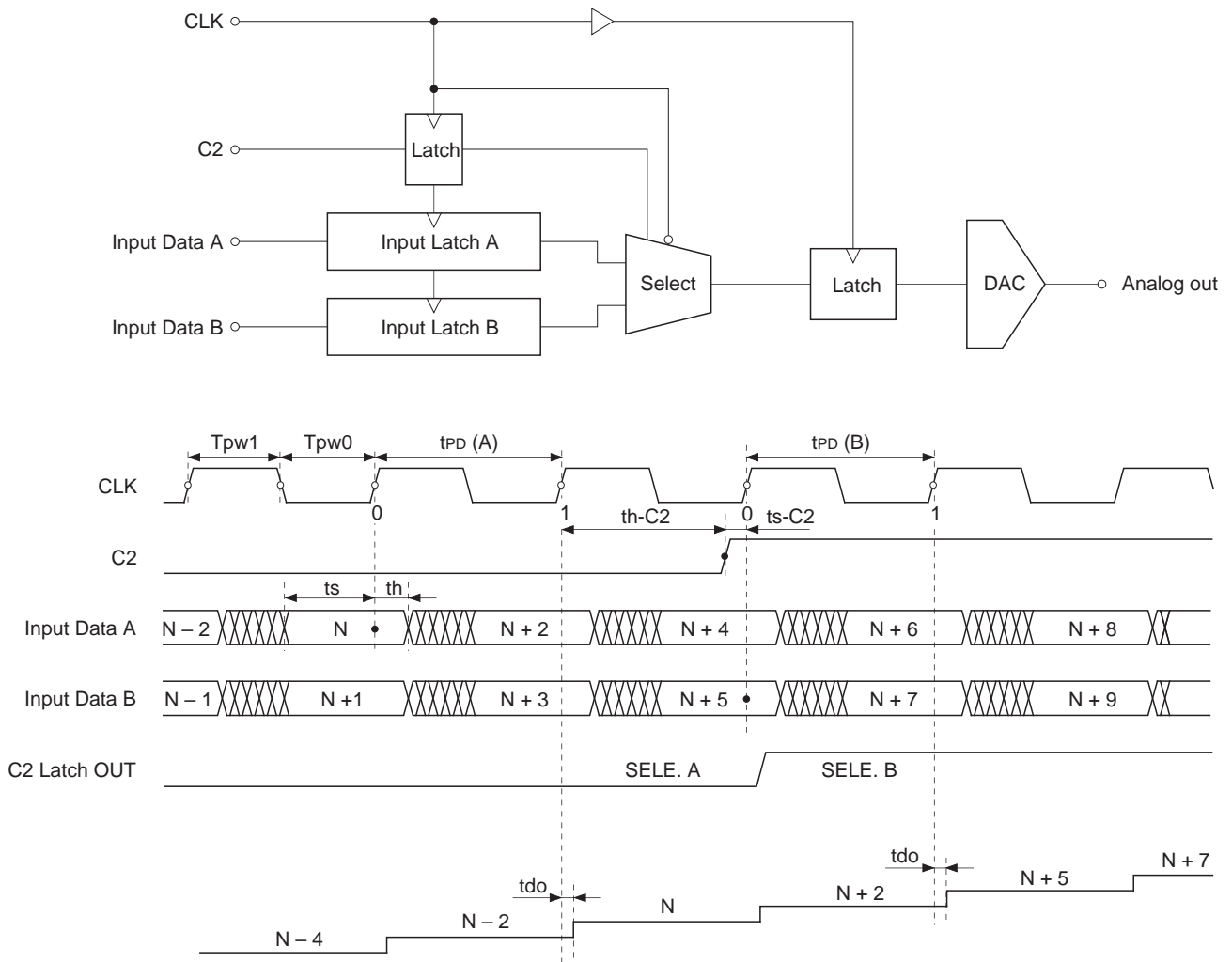
In MUX.1B mode, Data A and Data B are internally multiplexed and then the resulting signal can be analog output. The frequency of the clock is halved by the built-in clock frequency divider circuit. CLK/2 can be reset by the reset signal.

Block Diagram & Timing Chart (MUX.2 Mode)



In MUX.2 mode, the 1/2 frequency-divided clock signal (DIV2IN) and Data A and Data B, which are synchronized with DIV2IN, are provided simultaneously. These signals are internally multiplexed and the resulting signal can be analog output.

Block Diagram & Timing Chart (SELE.A, SELE.B Mode)



In SELE.A and SELE.B modes, input Data A or Data B is selected and the selected data can be analog output. When $C1 = 1$ and $C3 = 0$, Data A is selected for $C2 = 0$, and Data B is selected for $C2 = 1$.

Application Circuit

The circuit shown below is the basic circuit when the analog output is terminated with external resistance of 50Ω for operation with dual ±5V power supply in MUX.2 mode. The analog output uses AVccO as the reference. The analog output full-scale voltage V_{FS} is obtained with the following equation.

$$V_{FS} = \frac{V_{SET}}{375} \times \left(15 + \frac{63}{64}\right) \times R$$

$$R = R_o // R_L$$

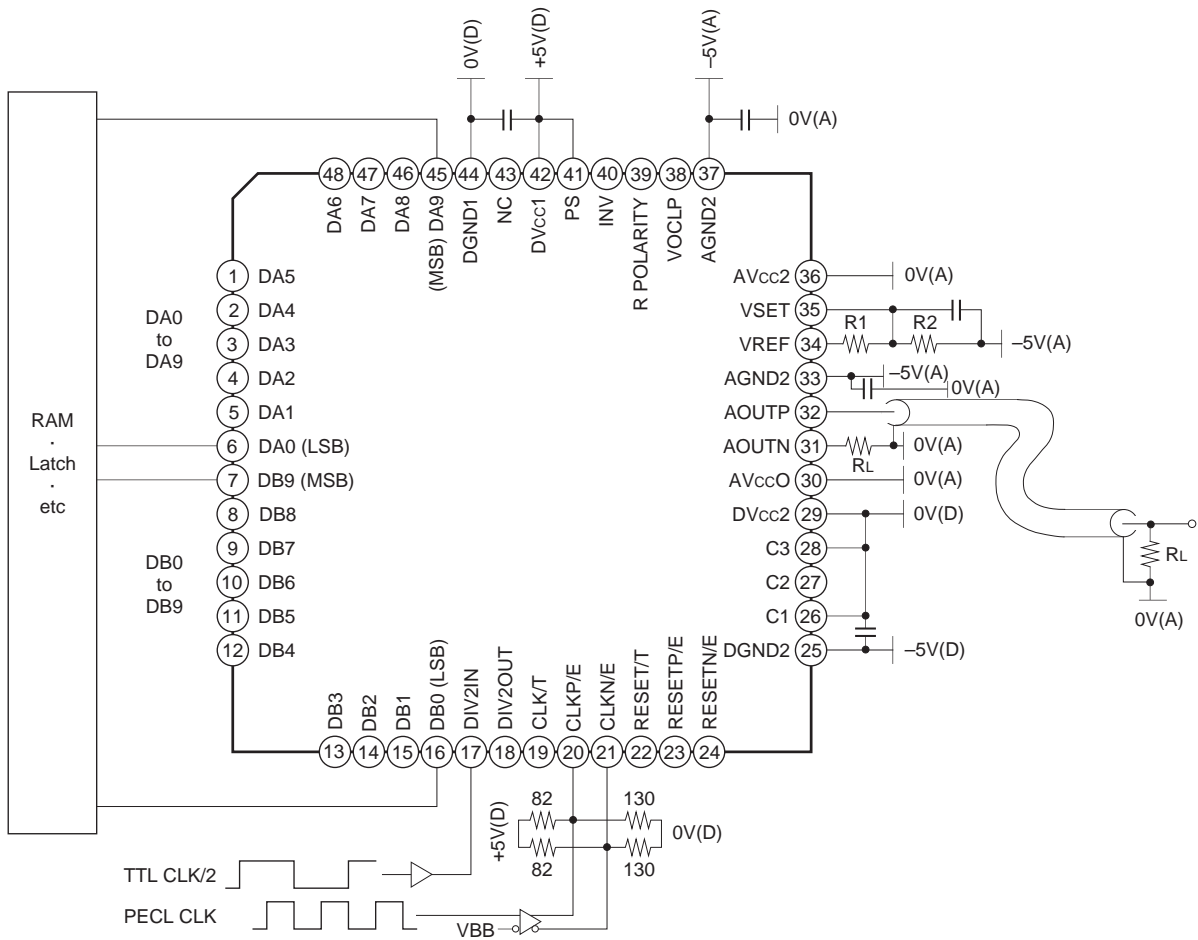
R_o: Output impedance (= 50Ω)

R_L: External termination resistance

$$\text{Here, } V_{SET} = \frac{R_2}{R_1 + R_2} V_{REF}$$

(V_{REF} ≈ 1.2V)

(R₁ + R₂ ≥ 1.2kΩ)



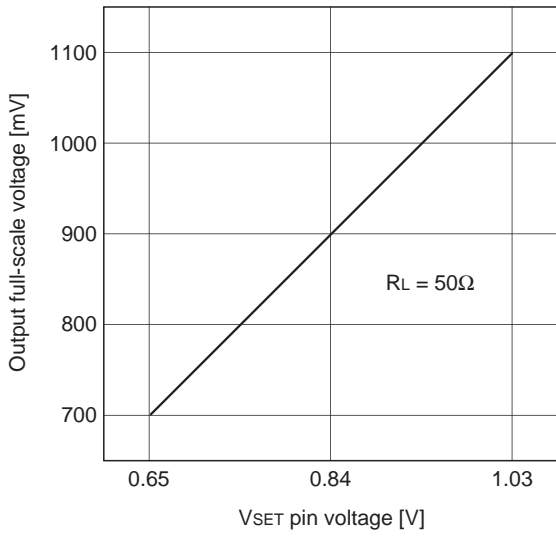
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Use

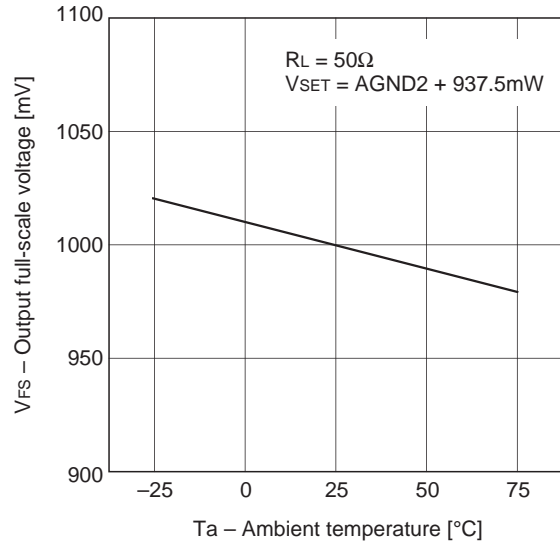
- The CXA3197R has PECL and TTL input pins for the clock and reset inputs. When the clock is input at PECL level, it is recommended to also input the reset signal at PECL level. Likewise, when the clock is input at TTL level, it is recommended to also input the reset signal at TTL level.
- The input signal impedance should be properly matched to ensure the stable CXA3197R operation at high speed.
Particularly when ringing appears in the input clock in the MUX.1A and MUX.1B modes, if this ringing exceeds the clock input threshold value, the internal 1/2 frequency divider circuit may misoperate.
- All TTL input pins of the CXA3197R except for the PS pin go to High level when left open, and only the PS pin goes to Low level when left open. Set the PS pin to High level to operate the IC.
When the PECL input pins are left open, the P (positive) side goes to High level and the N (negative) side goes to Low level. The PECL input pins are complementary, so be sure to use the P and N sides together.
- When the clock and reset input signal level is TTL, ***/T** pins should be used and ***/E** pins left open. When the clock and reset input signal level is PECL, ***/E** pins should be used and ***/T** pins left open.
- The power supply and grounding have a profound influence on converter characteristics. The power supply and grounding method are particularly important during high-speed operation.
General points for caution are as follows.
 - The ground pattern should be as wide as possible. It is recommended to make the power supply and ground wider at an inner layer using a multi-layer board.
To prevent a DC offset from being generated between the analog and digital power supply patterns, it is recommended to connect the patterns at one point via a ferrite-bead filter, etc.
 - When using the CXA3197R with a single power supply, connect DGND1 and DGND2 to a common digital ground, and AGND2 to an analog ground. Also, DVcc1 and DVcc2 should use a common digital power supply, and AVcc2 should be connected to an analog power supply. AVccO serves as the analog output reference, so while it does not need to share the analog power supply, it should be used within the range that satisfies the analog output compliance voltage.
 - When using the CXA3197R with dual power supply, connect DGND1 and DVcc2 to the digital ground, and AVcc2 to the analog ground. DVcc1 uses a positive digital power supply (+5V, typ.), DGND2 uses a negative digital power supply (–5V, typ.), and AGND2 uses a negative analog power supply (–5V, typ.). Like when using a single power supply, the AVccO pin can be used within the range that satisfies the analog output compliance voltage. However, connecting it to the analog ground and using the analog ground as the reference for the analog output is recommended.
 - Ground the power supply pins as close to each pin as possible with a 0.1μF or more ceramic chip capacitor.
When using a single power supply, connect DVcc1 and DVcc2 to the digital ground, and AVcc2 and AVccO to the analog ground.
When using dual power supply, connect DVcc1 and DGND2 to the digital ground, and AGND2 to the analog ground. In this case, when using AVccO within the range that satisfies the compliance voltage, be sure to also connect the AVccO pin to the analog ground using a ceramic chip capacitor.
- The CXA3197R is designed with an analog output impedance of 50Ω. The analog outputs are wired with a characteristic impedance of 50Ω, and waveforms free of reflection can be obtained by terminating the analog outputs with 50Ω. Even when using only one of either AOUTP or AOUTN, if one analog output is terminated with 50Ω, be sure to also terminate the other analog output with 50Ω. (See the Application Circuit.)

Example of Representative Characteristics

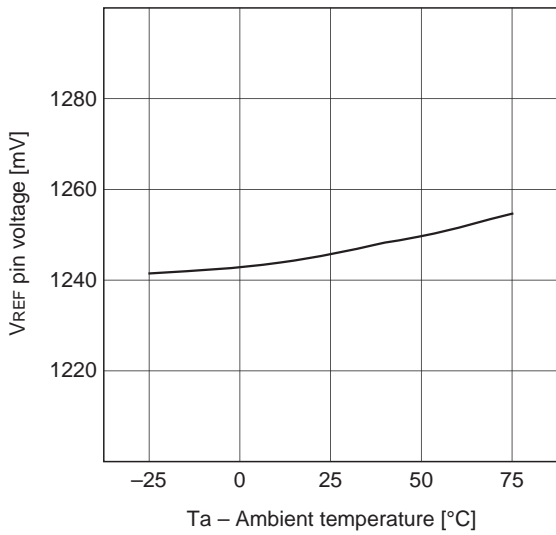
Output full-scale voltage vs. VSET pin voltage



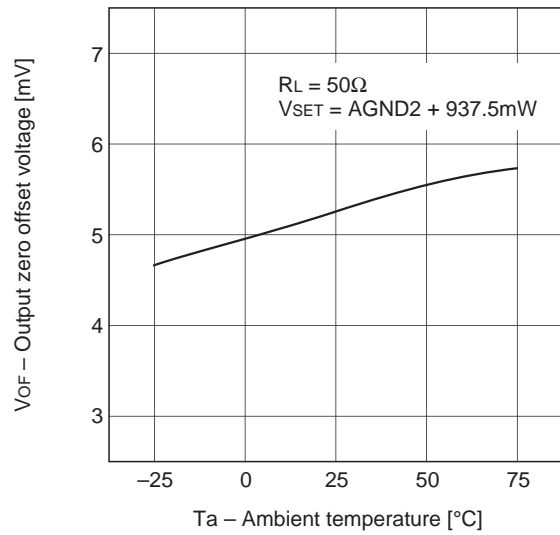
Output full-scale voltage vs. Ambient temperature



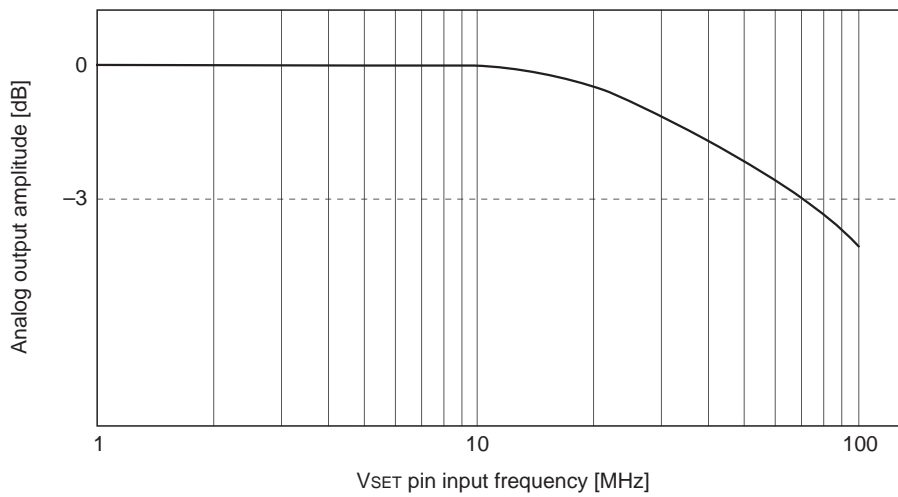
VREF pin voltage vs. Ambient temperature



Output zero offset voltage vs. Ambient temperature



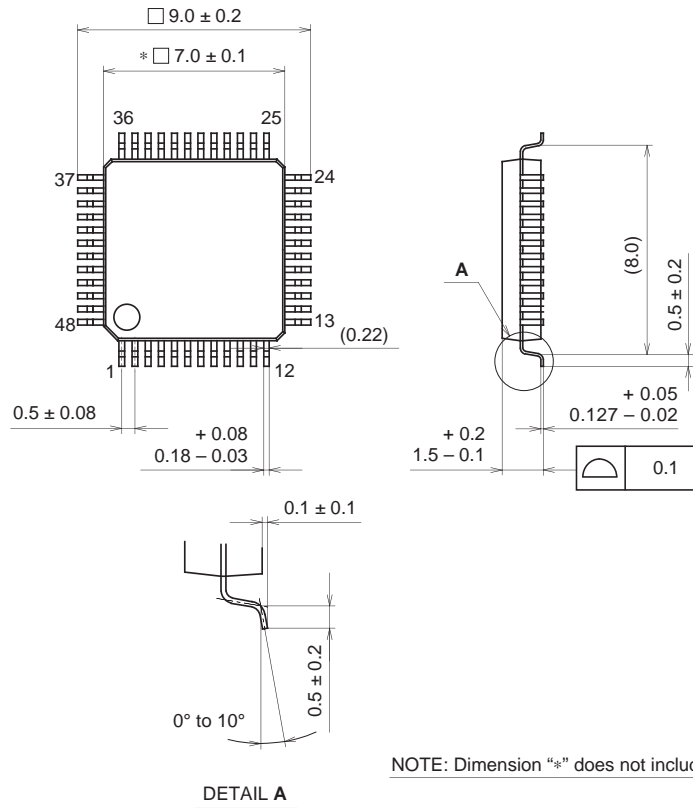
Multiplying bandwidth



Package Outline

Unit: mm

48PIN LQFP (PLASTIC)



| | |
|------------|----------------|
| SONY CODE | LQFP-48P-L01 |
| EIAJ CODE | LQFP048-P-0707 |
| JEDEC CODE | _____ |

PACKAGE STRUCTURE

| | |
|------------------|-----------------------------|
| PACKAGE MATERIAL | EPOXY RESIN |
| LEAD TREATMENT | SOLDER/PALLADIUM PLATING |
| LEAD MATERIAL | 42/COPPER ALLOY |
| PACKAGE MASS | 0.2g |

NOTE : PALLADIUM PLATING

This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).

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