

RF Signal Processor for CD Players

Description

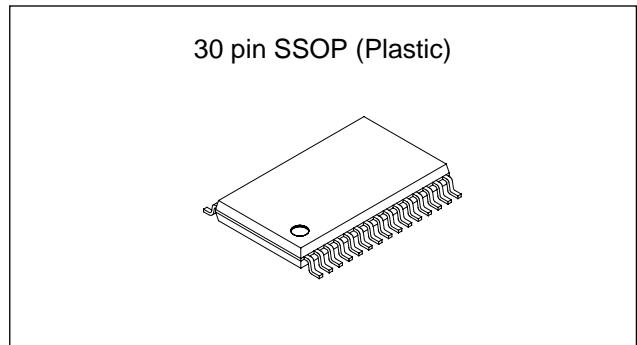
The CXA2647N is an RF signal processing IC for compact disc players.

Features

- RF signal processor supporting 6× speed CD
- RF system VCA circuit
- RF system equalizer
- Supports pickups with built-in RF summing amplifier
- Low current consumption mode (RF off mode)
- ROM/RW switching mode
- Center error amplifier
- Output DC level shift circuit
- TE balance adjustment function

Functions

- RF AC summing amplifier, equalizer, VCA
- RF DC summing amplifier
- Focus error amplifier
- Tracking error amplifier
- Center error amplifier
- Automatic power control
- VC buffer amplifier (analog block, digital block)



Absolute Maximum Ratings

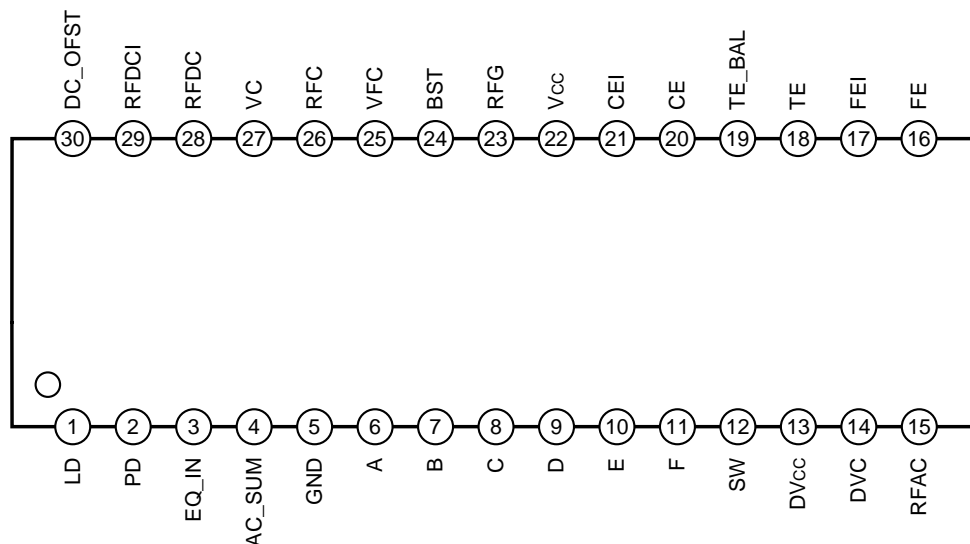
- Supply voltage V_{CC} 7 V
- Storage temperature T_{stg} -65 to +150 °C
- Allowable power dissipation P_D 620 mW

Operating Conditions

- Operating supply voltage range

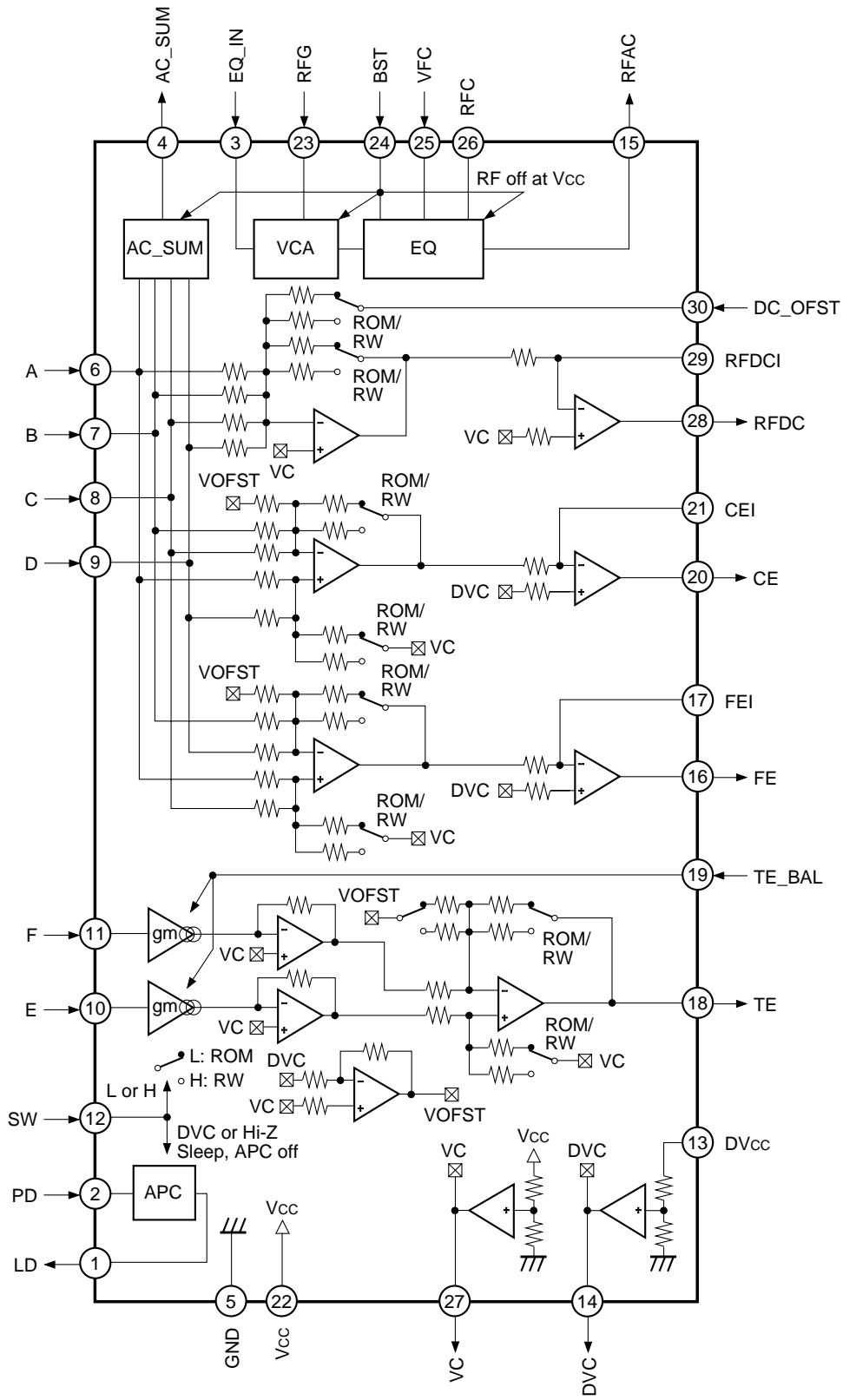
$V_{CC} - GND$	3.0 to 3.6	V
$DV_{CC} - GND$	3.0 to 3.6	V
	(0V ≤ $V_{CC} - DV_{CC}$ < 2V)	
- Operating temperature T_{opr} -30 to +85 °C

Pin Configuration



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Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1	LD	O	APC amplifier output.
2	PD	I	APC amplifier input.
3	EQ_IN	I	RFAC system VCA block and EQ block input.
4	AC_SUM	O	RFAC system RF_SUM output.
5	GND	I	GND.
6	A	I	Signal A input.
7	B	I	Signal B input.
8	C	I	Signal C input.
9	D	I	Signal D input.
10	E	I	Signal E input.
11	F	I	Signal F input.
12	SW	I	Mode switching signal input.
13	DVcc	I	DVcc.
14	DVC	O	DVC output.
15	RFAC	O	RFAC signal output.
16	FE	O	Focus error signal output.
17	FEI	I	FE amplifier virtual ground.
18	TE	O	Tracking error signal output.
19	TE_BAL	I	TE balance adjustment.
20	CE	O	Center error signal output.
21	CEI	I	CE amplifier virtual ground.
22	Vcc	I	Vcc.
23	RFG	I	RFAC system VCA block low frequency gain adjustment.
24	BST	I	EQ boost level adjustment.
25	VFC	I	EQ cut-off frequency adjustment.
26	RFC	I	EQ cut-off frequency adjustment.
27	VC	O	VC voltage output.
28	RFDC	O	RFDC signal output.
29	RFDCI	I	RFDC amplifier virtual ground.
30	DC_OFST	I	RFDC signal output offset adjustment.

Pin Description

Pin No.	Symbol	I/O	Equivalent circuit	Description
1	LD	O		APC amplifier output.
2	PD	I		APC amplifier input.
3	EQ_IN	I		Equalizer circuit input.
4	AC_SUM	O		RFAC summing amplifier output.
5	GND	—	—	GND.

Pin No.	Symbol	I/O	Equivalent circuit	Description
6	A	I		RFAC summing amplifier, RFDC amplifier, focus error amplifier and center error amplifier input.
7	B	I		
8	C	I		
9	D	I		
10	E	I		Tracking error amplifier input.
11	F	I		
12	SW	I		CD-ROM/SLEEP/CD-RW switching input. ROM when connected to GND, RW when connected to DVcc, SLEEP mode when connected to DVC or Hi-Z.
13	DVcc	—	—	Digital power supply.
14	DVC	O		$(DV_{cc} + GND)/2$ voltage output.

Pin No.	Symbol	I/O	Equivalent circuit	Description
15	RFAC	O		RFAC amplifier output.
16	FE	O		Focus error amplifier output.
17	FEI	I		Focus error amplifier gain adjustment. The gain is adjusted by the external resistance value connected between this pin and Pin 16.
18	TE	O		Tracking error amplifier output.
19	TE_BAL	I		Input for adjusting the tracking error amplifiers E and F gain balance with the control voltage.
20	CE	O		Center error amplifier output.
21	CEI	I		Center error amplifier gain adjustment. The gain is adjusted by the external resistance value connected between this pin and Pin 20.

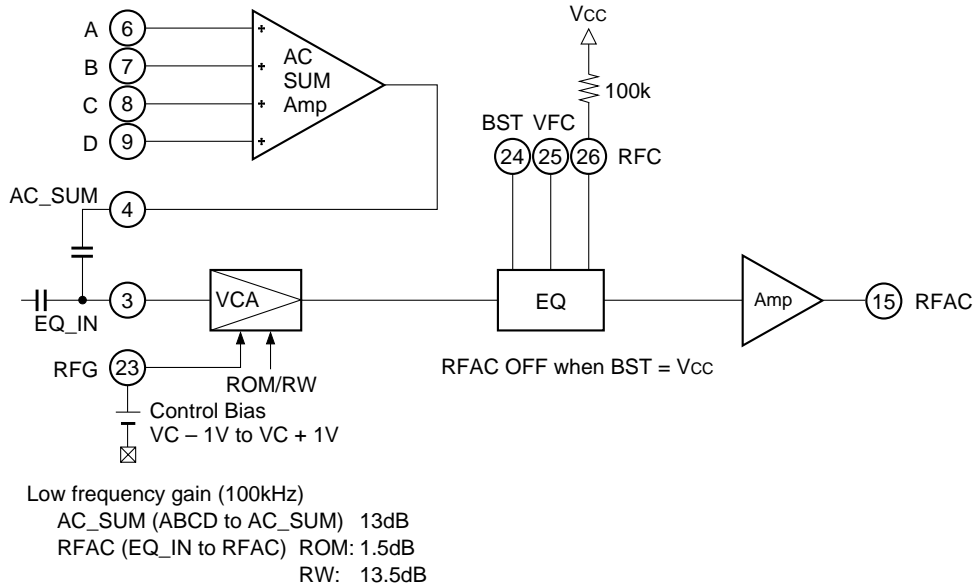
Pin No.	Symbol	I/O	Equivalent circuit	Description
22	Vcc	—	—	Vcc.
23	RFG	I		Input for setting the RFAC low frequency gain with the control voltage.
24	BST	I		Input for adjusting the equalizer circuit boost level with the control voltage.
25	VFC	I		Input for adjusting the equalizer circuit cut-off frequency with the control voltage.
26	RFC	I		Input for adjusting the equalizer circuit cut-off frequency with the external resistance.
27	VC	O		$(V_{cc} + GND)/2$ voltage output.

Pin No.	Symbol	I/O	Equivalent circuit	Description
28	RFDC	O		RFDC amplifier output.
29	RFDCI	I		RFDC amplifier gain adjustment. The gain is adjusted by the external resistance value connected between this pin and Pin 28.
30	DC_OFST	I		Input for adjusting RFDC amplifier offset with the control voltage.

Description of Functions

• **RFAC**

The RF signal input by connecting capacitance to EQ_IN (Pin 3) is equalized, arithmetically amplified and then output from RFAC (Pin 15).



When BST (Pin 24) is connected to Vcc, the RFAC function is turned off and the low consumption mode is entered.

If RF (summing signal) is present at the pickup output pin, input the addition output signal to EQ_IN (Pin 3) coupled by capacitance.

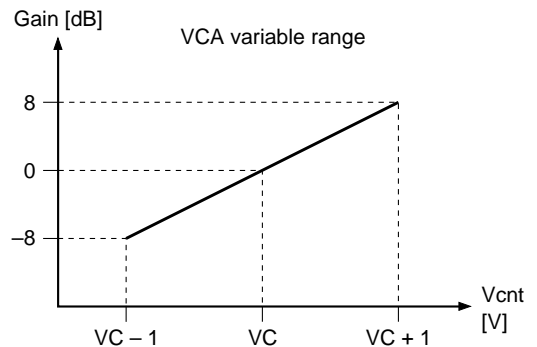
When using a pickup without a summing output function, perform addition with the AC_SUM and then input the signal to EQ_IN (Pin 3) coupled by capacitance.

ROM/RW switching is done by the VCA block, so either input method can be used without problem.

The RW gain is 12dB higher than the ROM gain.

The VCA low frequency gain can be adjusted by the RFG (Pin 23) voltage control.

The control voltage vs. low frequency gain characteristics are shown in the graph to the right.



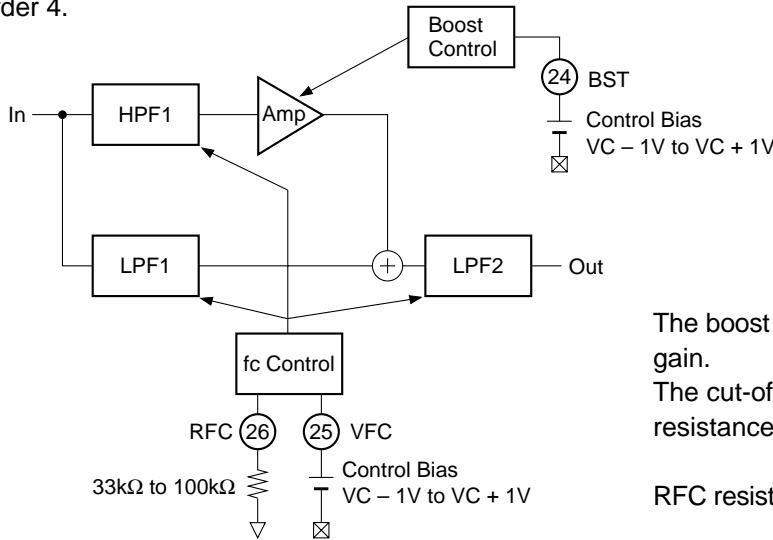
The RFAC pin (Pin 15) is an NPN transistor emitter follower output.

The maximum drive current is approximately 1.4mA.

If the load capacitance distorts the output waveform, connect resistance between the RFAC pin and GND to increase the drive current.

• EQ

The EQ internal block diagram is shown below. The EQ is configured with the filter of the Bessel function of order 4.



$$LPF1 = \frac{79.517fc^2}{S^2 + (17.085fc) S + 79.517fc^2}$$

$$HPF1 = \frac{S^2}{S^2 + (17.085fc) S + 79.517fc^2}$$

$$LPF2 = \frac{99.963fc^2}{S^2 + (12.412fc) S + 99.963fc^2}$$

The boost gain can be adjusted by adjusting the HPF1 gain.

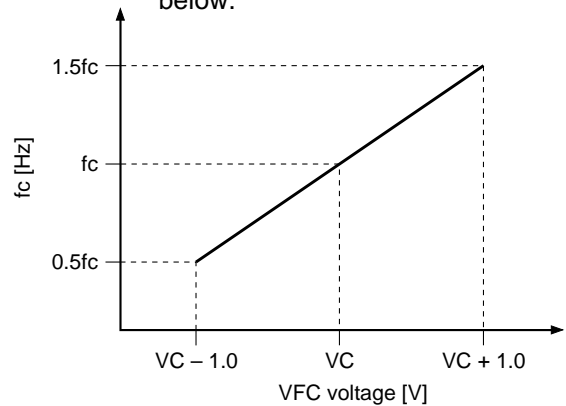
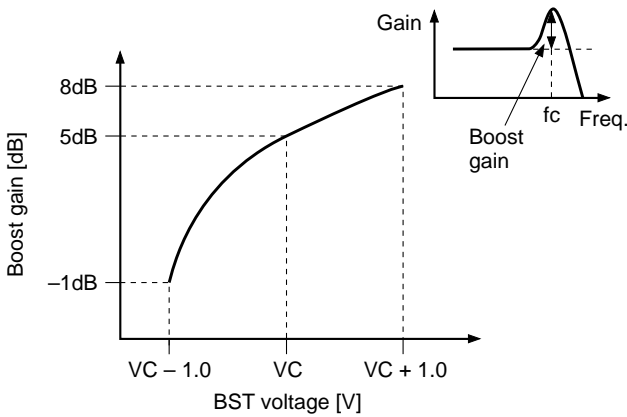
The cut-off frequency is adjusted by the RFC external resistance value and the VFC control voltage value.

RFC resistance value: The cut-off frequency f_c of each filter is adjusted by the Pin 26 external resistance value.

The VFC voltage can be varied using this f_c as the reference.

VFC voltage: f_c can be adjusted by the voltage applied to Pin 25. The cut-off frequency control characteristics are shown in the graph below.

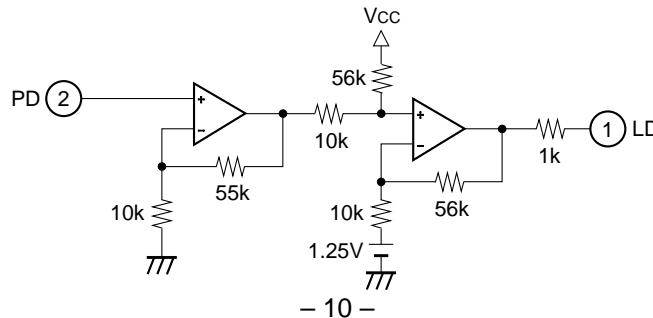
The boost gain can be adjusted by the BST (Pin 24) control voltage.
The control characteristics are shown in the graph below.
The boost gain stands for the increased gain from the low frequency gain in the f_c frequency.



RFC pin external resistor value 100kΩ: $f_c = 1.6\text{MHz}$
33kΩ: $f_c = 4.8\text{MHz}$

• APC (Automatic Power Control)

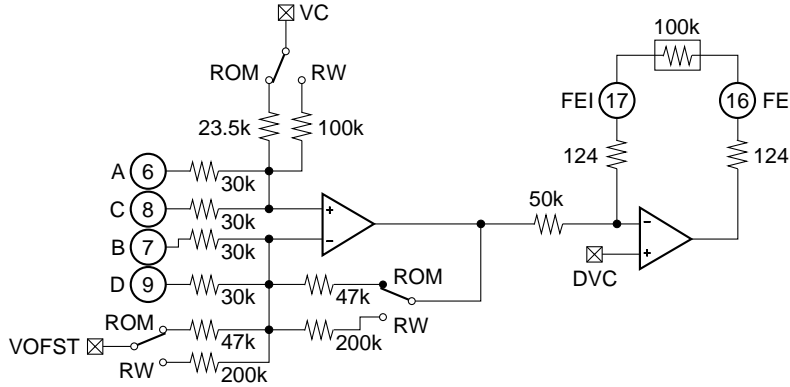
When the laser diode is driven by a constant current, the optical power output has extremely large negative temperature characteristics. Therefore, the current must be controlled to maintain the monitor photodiode output at a constant level. This control is performed by the APC function.



• Focus Error

The signals input to the A and C pins and the B and D pins are arithmetically amplified and the focus error signal is output.

This circuit has ROM/RW switching and offset addition functions.



FE = Gain { (B + D) - (A + C) }

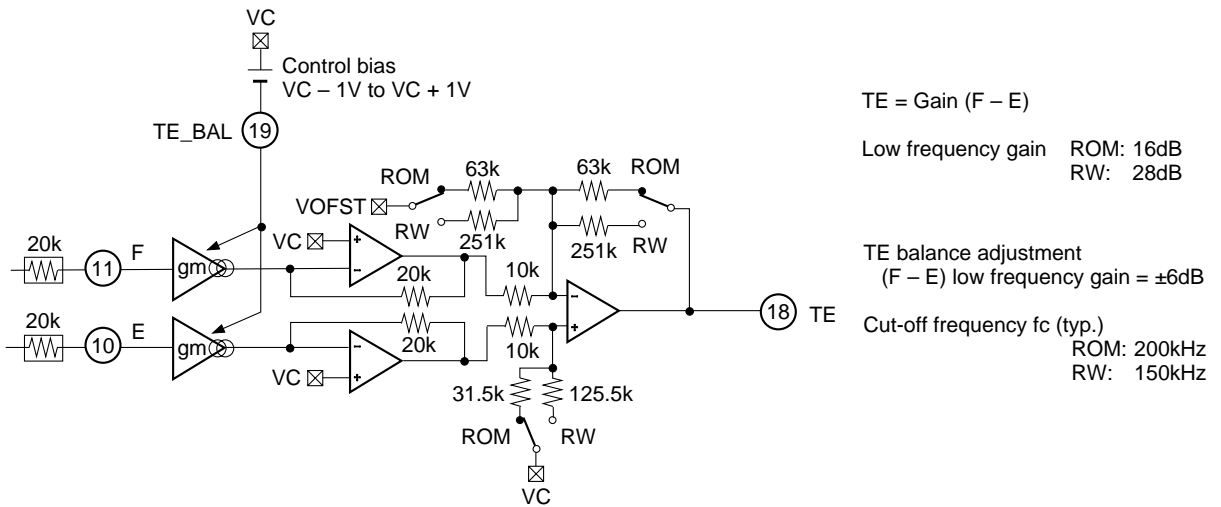
Low frequency gain ROM: 15.5dB
RW: 27.5dB

Cut-off frequency f_c (typ.) ROM: 400kHz
RW: 300kHz

• Tracking Error

The signals input to the E and F pins are arithmetically amplified and the tracking error signal is output.

This circuit has ROM/RW switching and offset addition functions.



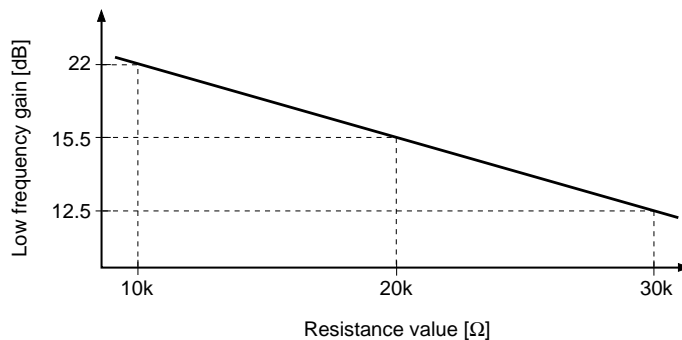
TE = Gain (F - E)

Low frequency gain ROM: 16dB
RW: 28dB

TE balance adjustment
(F - E) low frequency gain = ±6dB

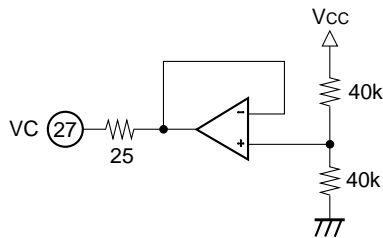
Cut-off frequency f_c (typ.) ROM: 200kHz
RW: 150kHz

External resistance value vs. Low frequency gain for E and F input pins



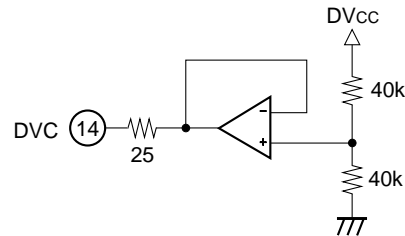
• VC Buffer

This outputs the VC ((1/2) Vcc) voltage.
 The maximum output current is approximately ±3mA.
 Use this voltage as the analog block VC voltage.



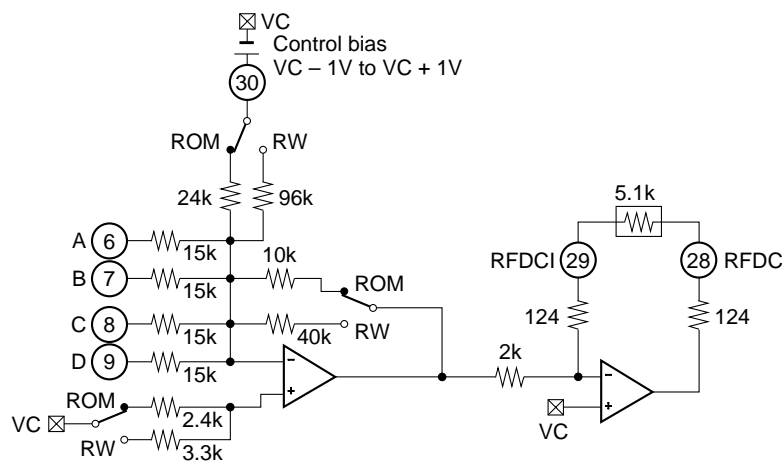
• DVC Buffer

This outputs the DVC ((1/2) DVcc) voltage.
 The maximum output current is approximately ±3mA.
 Use this voltage as the digital block VC voltage.
 The each output DC voltage of FE, TE and CE is level shifted using the DVC voltage as the reference.



• RFDC

The signals input to the A, B, C and D pins are added, amplified and the RFDC signal is output. ROM/RW switching, low frequency gain adjustment and output DC voltage adjustment are possible.



RFDC = Gain (A + B + C + D)
 Low frequency gain ROM: 16.5dB
 RW: 28.5dB

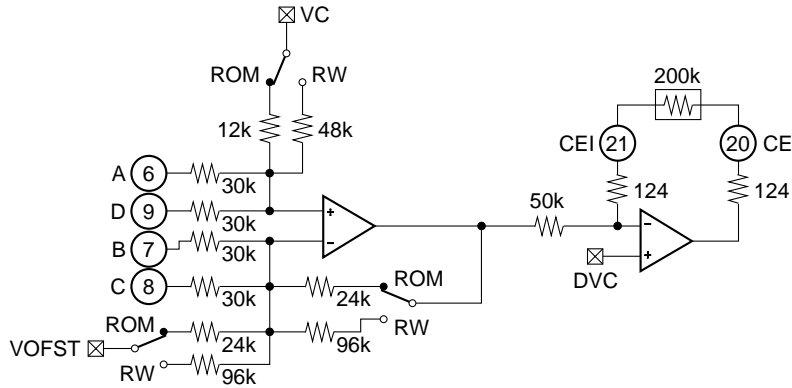
Cut-off frequency f_c (typ.)
 ROM : 15MHz
 RW : 6MHz

The gain can be adjusted by the external resistance connected between Pins 28 and 29.
 The output voltage offset can be adjusted by controlling the Pin 30 voltage.

• Center Error

The signals input to the A and D pins and the B and C pins are arithmetically amplified and the center error signal is output.

ROM/RW switching and offset addition functions are incorporated.



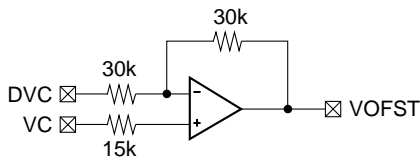
CE = Gain $\{(B + C) - (A + D)\}$ signal is arithmetically amplified. Cut-off frequency f_c (typ.)
 Low frequency gain ROM: 15.5dB ROM: 200kHz
 RW: 27.5dB RW: 200kHz

• Output DC Level Shift

The FE, TE and CE output DC voltages are level shifted to the digital VC voltage (DVC).

The reference voltage of this IC is the VC voltage, and only the output reference voltage changes.

The maximum output voltage of each output signal should be kept to the digital V_{cc} voltage (DV_{cc}) or less in order to protect the DSP IC.



The VC and DVC voltages are arithmetically amplified and output as the VOFST voltage.

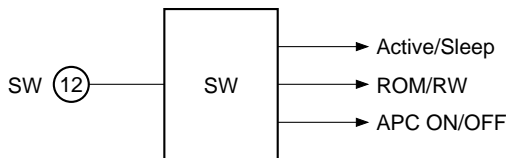
The VOFST voltage serves as the level shift reference voltage, and is distributed to each block.

$$VOFST = 2VC - DVC$$

• SW

This controls the laser (APC) on/off, active/sleep mode, and ROM/RW mode switching.

Switching is controlled by the voltage applied to the SW pin.



SW low/high condition

Low: GND to DVC - 1.2V

High: DVC + 1.2V to V_{cc}

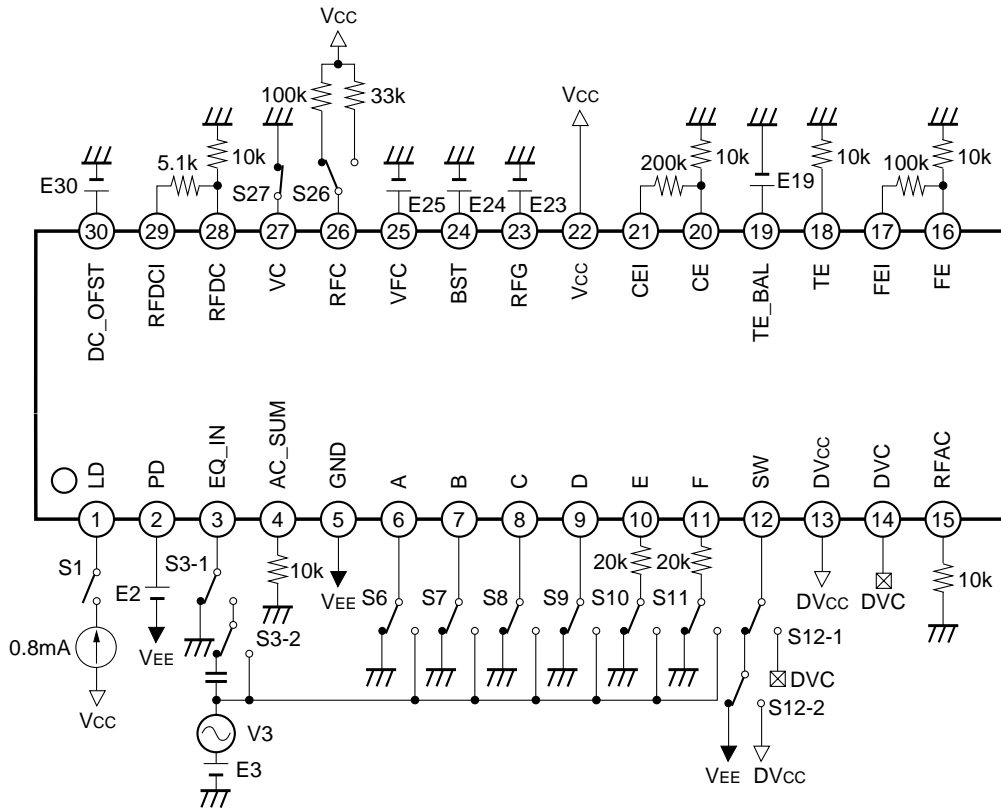
Status of Functions on SW Switching

Control voltage \ Item	APC	Active/Sleep	ROM/RW
V_{cc}	ON	Active	RW
VC or Hi-Z	OFF	Sleep	—
GND	ON	Active	ROM

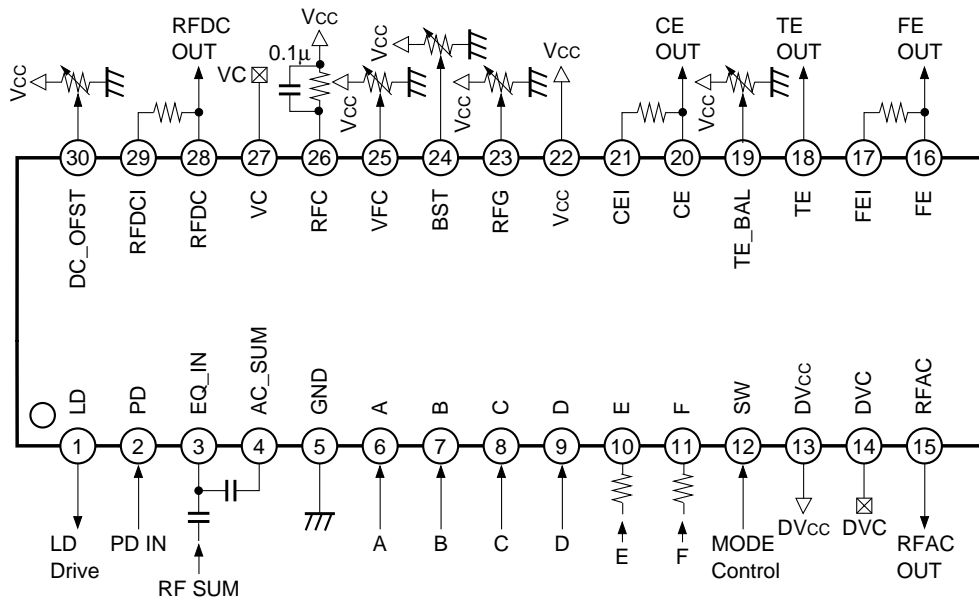
The VC buffer is always in active mode even if it enters sleep mode.

In the function block, MODE SW is always set to active mode.

Electrical Characteristics Measurement Circuit

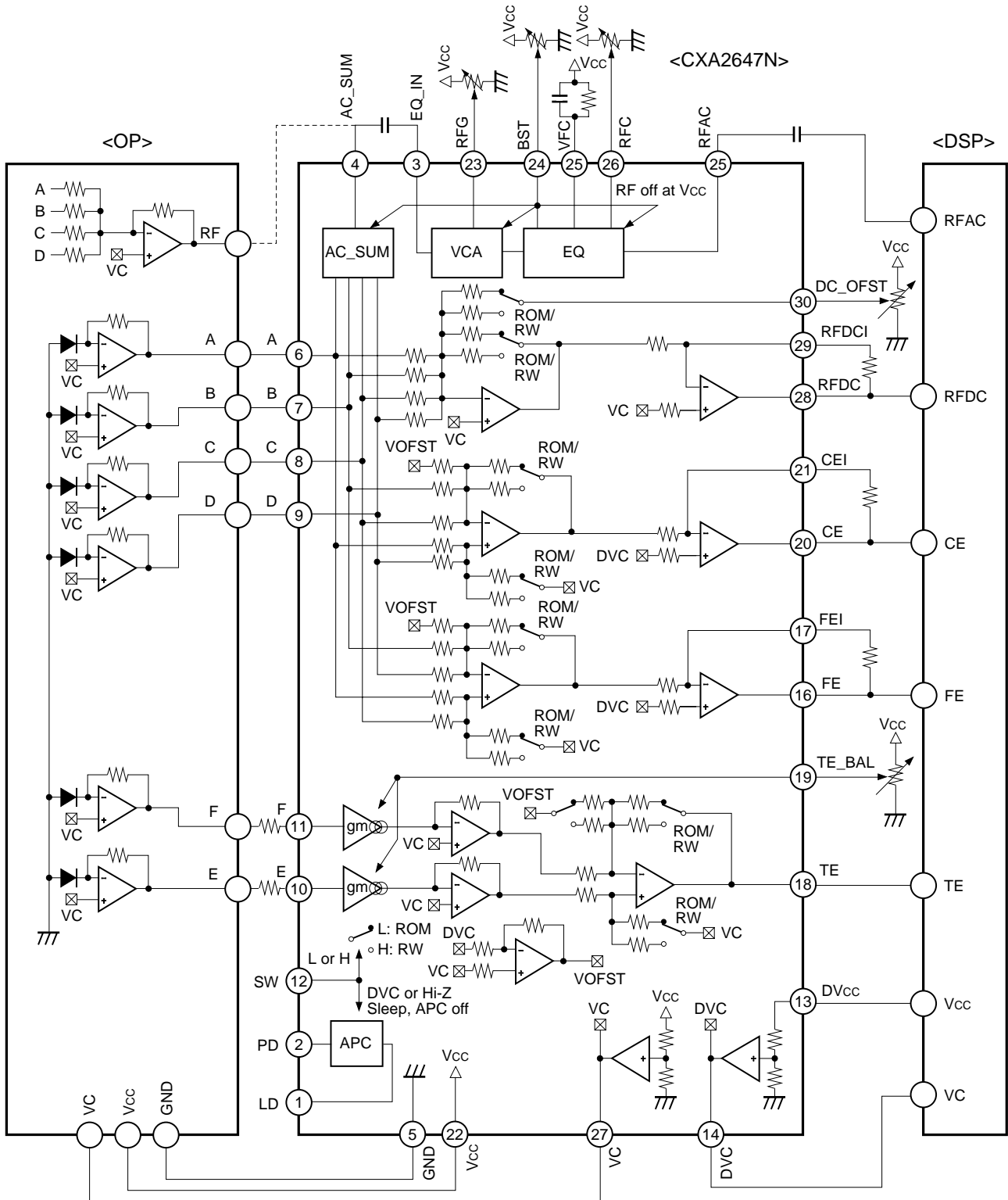


Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Connection Example of DP and DSP

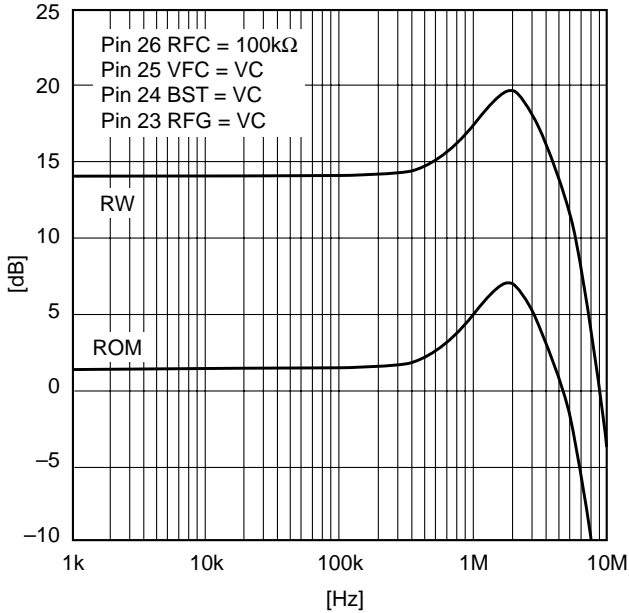


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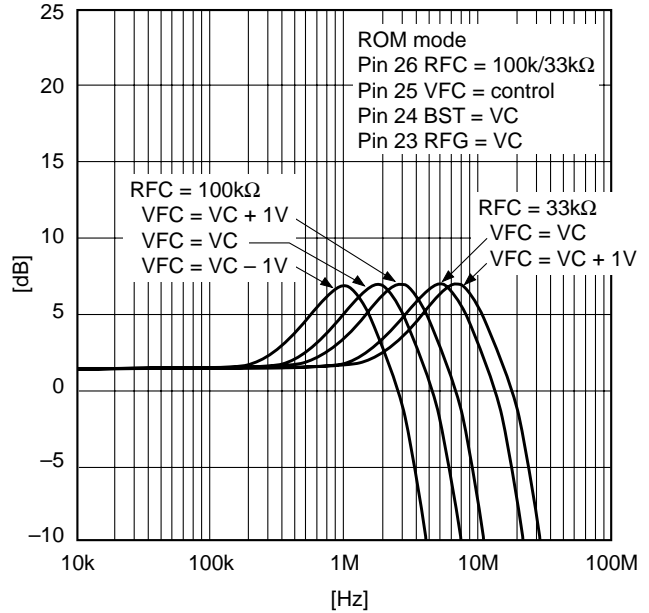
Characteristics Graphs (Vcc = 3.0V, DVcc = 3.0V)

1. EQ characteristics Input: Pin 3 EQ_IN
Output: Pin 15 RFAC

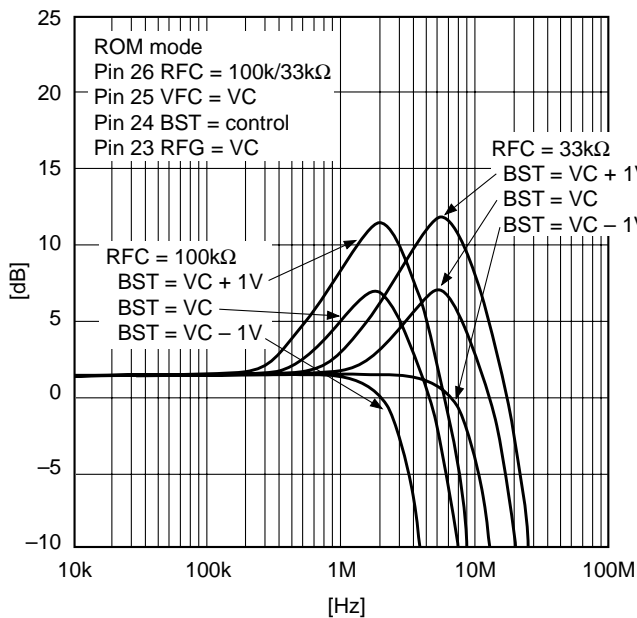
1-1. EQ ROM/RW characteristics



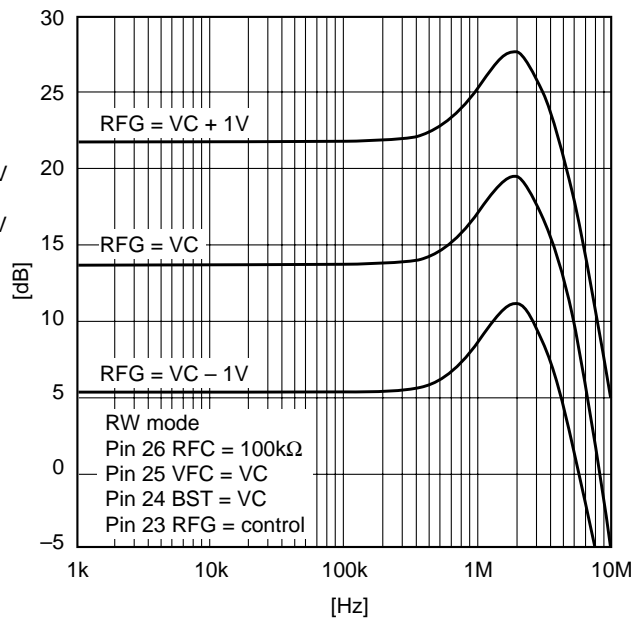
1-2. EQ fc control characteristics



1-3. EQ boost control characteristics



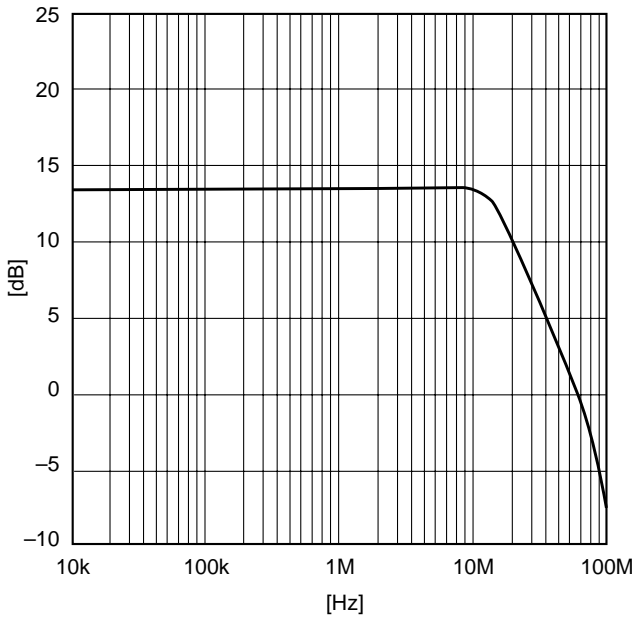
1-4. EQ gain control characteristics



2. AC_SUM characteristics

Input: Pin 6, 7, 8, 9 A, B, C, D

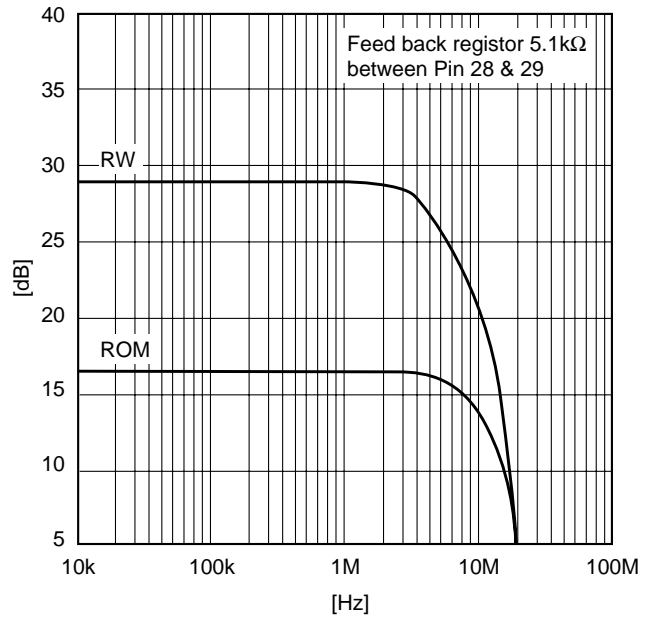
Output: Pin 4 AC_SUM



3. RFDC characteristics

Input: Pin 6, 7, 8, 9 A, B, C, D

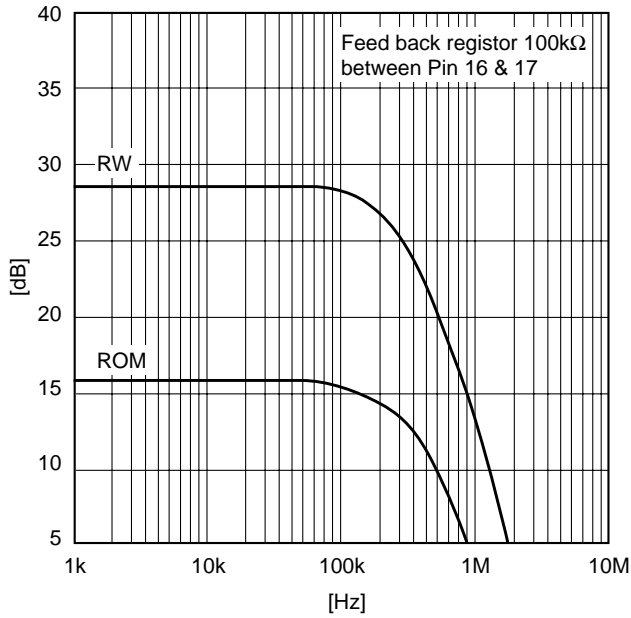
Output: Pin 28 RFDC



3. FE characteristics

Input: Pin 6, 8 A, C

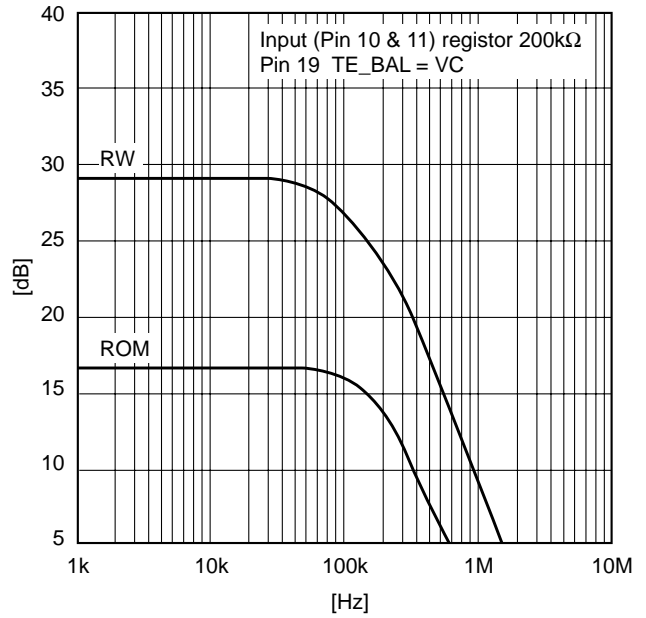
Output: Pin 16 FE



4. TE characteristics

Input: Pin 10 E

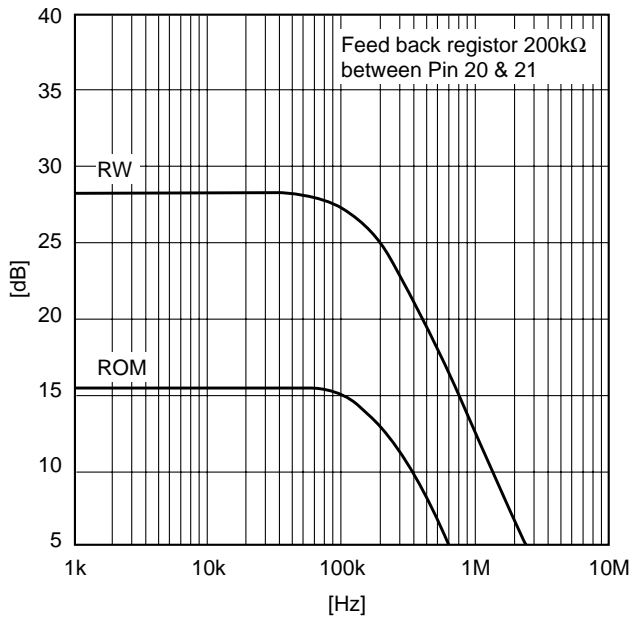
Output: Pin 18 TE



3. CE characteristics

Input: Pin 6, 9 A, D

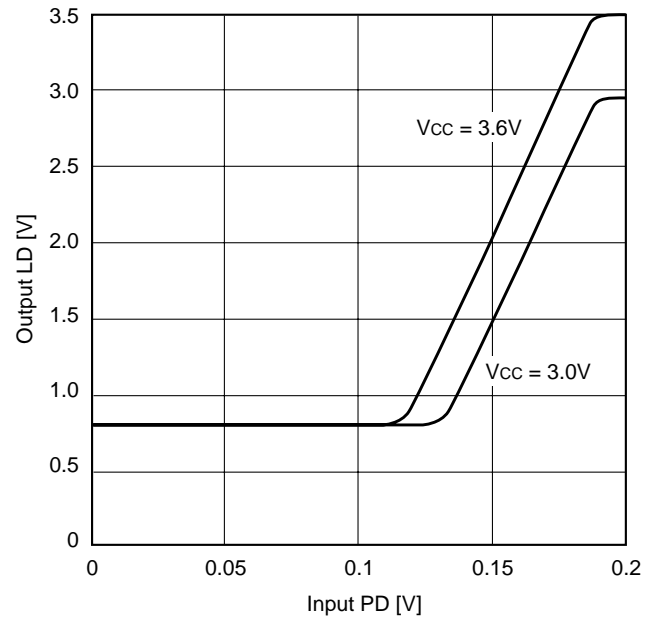
Output: Pin 20 CE



3. APC input/output characteristics

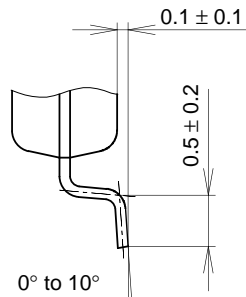
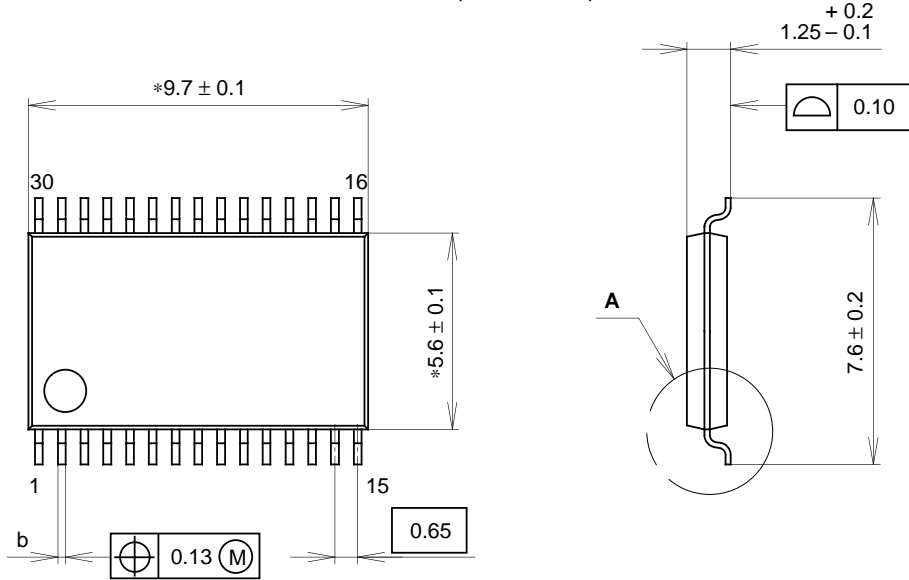
Input: Pin 2 PD

Output: Pin 1 LD

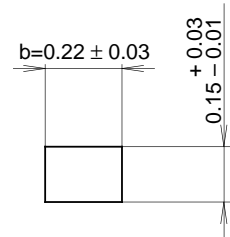


Package Outline Unit: mm

30PIN SSOP (PLASTIC)



DETAIL A



DETAIL B : PALLADIUM

NOTE: Dimension "*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	SSOP-30P-L01
EIAJ CODE	P-SSOP30-5.6x9.7-0.65
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.1g

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