

## Recording/Playback Equalizer Amplifier

### Description

The CXA1998AQ is an IC developed for analog signal processing in tape recorders. Processing for both the recording and playback systems is achieved on one chip.

### Features

- 11-bit serial data interface
- Recording/playback mute function
- Recording equalizer Gp and Fp can be adjusted externally.
- AGC (Automatic Gain Control)
- Comparator for AMS (Automatic Music Sensor)
- Recording/playback equalizer amplifier with 1.7 times speed switching

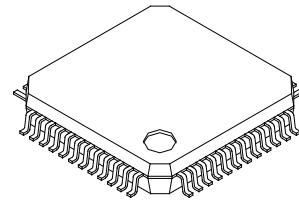
### Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V <sub>CC</sub> , V <sub>DD</sub>	12	V
• Operating temperature	T <sub>opr</sub>	-20 to +75	°C
• Storage temperature	T <sub>stg</sub>	-65 to +150	°C
• Allowable power dissipation	P <sub>D</sub>	645	mW

### Operating Conditions

Supply voltage	V <sub>CC</sub>	6.5 to 10.0	V
	V <sub>DD</sub>	4.5 to 5.5	V

48 pin QFP (Plastic)



### Structure

Bipolar silicon monolithic IC

### Applications

All analog signal processing in the cassette decks of tape recorders and compact music centers

### Applicable Head

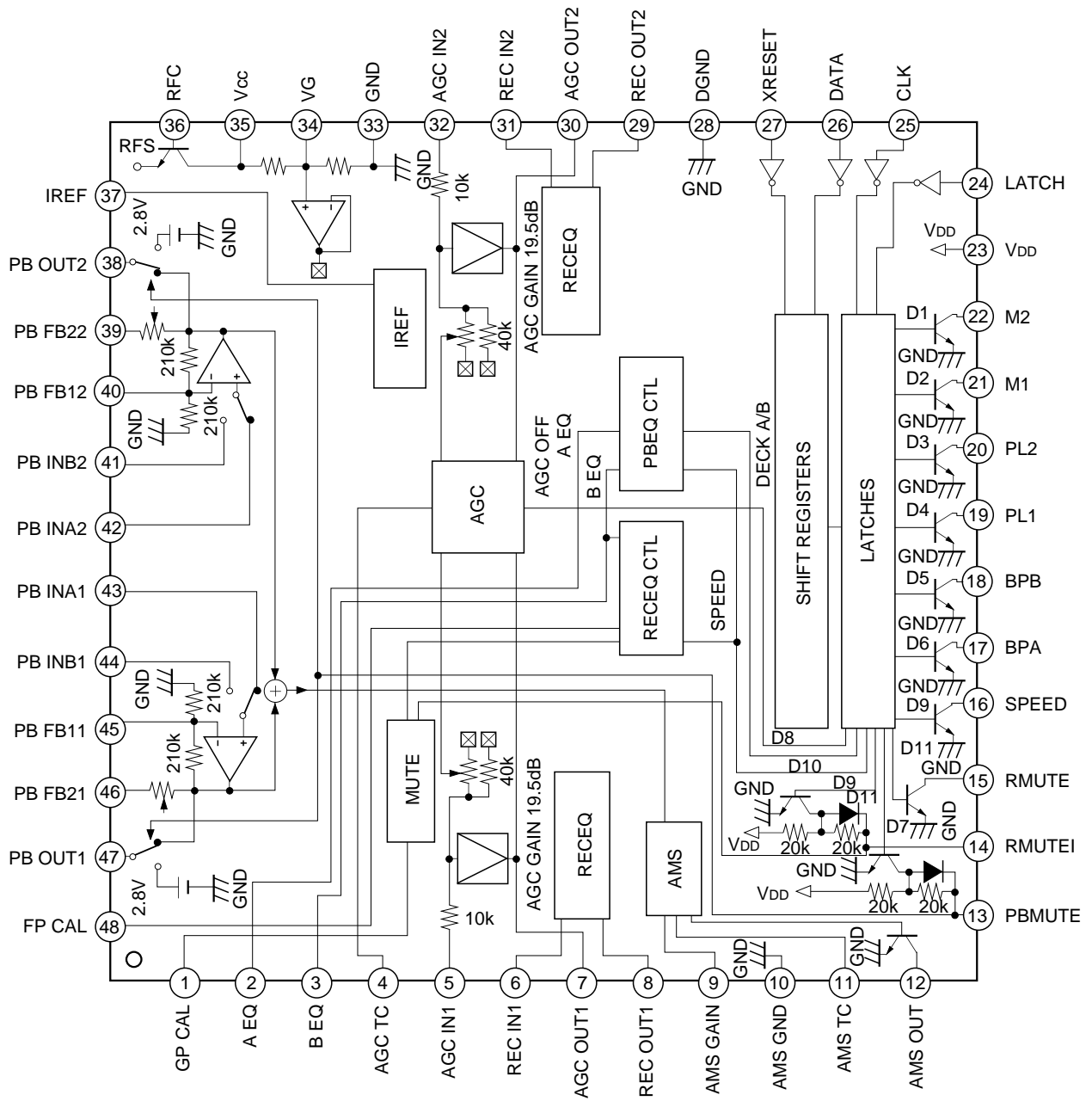
Applicable to MITSUMI ELECTRIC Co., Ltd.

Playback head: BP-7442-CP-6973

Recording/playback head: BC-9242-CB-9267

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Block Diagram and Pin Configuration (Top View)



Pin Description

(Ta = 25°C, Vcc = 8V, VDD = 5V, no signal, RESET ON)

Pin No.	Symbol	DC voltage	I/O	I/O resistance	Equivalent circuit	Description
1	GP CAL	1.2V	—	—		Connects a resistor for determining the high-band peak gain of recording equalizer. Reference setting resistance is 27kΩ.
2	A EQ	—	I	—		Deck A equalizer switch. Low: 120μs EQ High: 70μs EQ
3	B EQ	2.5V (OPEN)	I	53kΩ		Deck B equalizer switch. Low: NORMAL TAPE, 120μs EQ Medium: Cro2 TAPE, 70μs EQ High: METAL TAPE, 70μs EQ
4	AGC TC	0.0V	—	—		Connects a resistor and capacitor for determining AGC attack/recovery time constants.

Pin No.	Symbol	DC voltage	I/O	I/O resistance	Equivalent circuit	Description
5 32	AGC IN1 AGC IN2	4.0V	I	50kΩ		AGC signal input. Input resistance changes between 50kΩ and 100kΩ. AGC functions when the signal of -30dBm or more is input to AGC for AGC ON. (External 47μF//300kΩ for Pin 4)
6 31	REC IN1 REC IN2	4.0V	I	50kΩ		Recording equalizer input.
7 30	AGC OUT1 AGC OUT2	4.0V	O	147Ω		AGC output.
8 29	REC OUT1 REC OUT2	4.0V	O	147Ω		Recording equalizer output.

Pin No.	Symbol	DC voltage	I/O	I/O resistance	Equivalent circuit	Description
9	AMS GAIN	3.5V	—	—		Connects a resistor for determining AMS signal detection level and a capacitor for determining HPF cut-off frequency.
10	AMS GND	0.0V	—	—		AMS block ground.
11	AMS TC	8.0V	—	—		Connects time constant for AMS detection.
12	AMS OUT	8.0V	O	—		AMS output. No signal detection: High Signal detection: Low

Pin No.	Symbol	DC voltage	I/O	I/O resistance	Equivalent circuit	Description
13	PBMUTE	5.0V	—	—		Connects a capacitor for setting time constant for playback mute ON/OFF switching.
14	RMUTE1					Connects a capacitor for setting time constant for recording mute ON/OFF switching.
15	RMUTE	5.0V	O	—		Output for recording mute ON/OFF switch control signal. Outputs D11 from Pin 26 (DATA).
16	SPEED					Output for recording/playback equalizer speed switch control signal. Outputs D9 from Pin 26 (DATA). Low: Normal Speed High: High Speed (1.7 times)
17	BPA	5.0V	O	—		Outputs D6 from Pin 26 (DATA).
18	BPB					Outputs D5 from Pin 26 (DATA).
19	PL1					Outputs D4 from Pin 26 (DATA).
20	PL2					Outputs D3 from Pin 26 (DATA).
21	M1					Outputs D2 from Pin 26 (DATA).
22	M2					Outputs D1 from Pin 26 (DATA).
23	VDD	5.0V	—	—		Power supply of serial data interface block.

Pin No.	Symbol	DC voltage	I/O	I/O resistance	Equivalent circuit	Description
24	LATCH	—	I	—		Serial data interface latch input.
27	XRESET					Serial data interface reset input. Low: Reset. At this time serial data outputs (Pins 15 to 22) are all open (high).
25	CLK	—	I	—		Serial data interface clock input.
26	DATA					Serial data interface serial data input.
28	DGND	0.0V	—	—		Serial data interface block ground.
33	GND	0.0V	—	—		Ground.
34	VG	4.0V	—	60kΩ		Signal reference voltage. Connects a capacitor for ripple rejection.
35	Vcc	8.0V	—	—		Power supply.

Pin No.	Symbol	DC voltage	I/O	I/O resistance	Equivalent circuit	Description
36	RFC	8.0V	—	—		Connects a resistor and capacitor for obtaining stable voltage with power supply ripple rejected.
37	IREF	1.2V	—	—		Connects a resistor (12kΩ) for determining equalizer gains.
48	FP CAL					Connects a resistor for determining the high-band peak frequency of recording equalizer. Reference setting resistance is 27kΩ.
38 47	PB OUT2 PB OUT1	2.8V	O	147Ω		Playback equalizer output.
39 46	PB FB22 PB FB21	2.8V	—	—		Connects a capacitor for determining playback equalizer time constants, such as 120μs and 70μs.

Pin No.	Symbol	DC voltage	I/O	I/O resistance	Equivalent circuit	Description
40 45	PB FB12 PB FB11	1.4V	—	105kΩ		Playback equalizer negative feedback.
41 42 43 44	PB INB2 PB INA2 PB INA1 PB INB1	0.0V	I	70kΩ		Playback equalizer input.

**Note)**

- AMS GND (Pin 10), DGND (Pin 28) and GND (Pin 33) are each independent in the IC and are not connected. Be sure to ground each of the ground pins listed above.
- The resistance of open collector outputs (Pins 15 to 22) can be connected Vcc.

**Electrical Characteristics**

(Ta = 25°C, Vcc = 8.0V, VDD = 5.0V, refer to Electrical Characteristics Measurement Circuit)

Item		Measurement conditions	Min.	Typ.	Max.	Unit
Operating voltage		Vcc	6.5	8.0	10.0	V
		VDD	4.5	5.0	5.5	V
Current consumption		Sum of Vcc and VDD pin currents NORM – NS, no signal	13.5	19.7	25.0	mA
AGC	AGC ON output level	Pin 4 external R300kΩ//C47μF f = 1kHz, Vin = -25dBm	-13.0	-11.0	-9.0	dBm
	AGC ON channel balance	Pin 4 external R300kΩ//C47μF f = 1kHz, Vin = -25dBm	-2.0	0.0	2.0	dB
	AGC ON distortion	Pin 4 external R300kΩ//C47μF f = 1kHz, Vin = 0dBm	—	0.3	1.5	%
	AGC OFF output level	Pin 4 external R300kΩ//C 47μF f = 1kHz, Vin = -25dBm	-7.5	-5.5	-3.5	dBm
AMS	No signal detection threshold level	Pin 9 external R9.1kΩ, C0.015μF Pin 11 external R100kΩ//C0.1μF f = 5kHz, 0dB = -21dBm (at PBEQ reference output level)	-11.5	-8.2	—	dB
Playback equalizer amplifier block	120μs – NS frequency response	f = 315Hz, Vin = -70dBm Reference for frequency response	-23.0	-21.0	-19.0	dBm
	120μs – NS frequency response	f = 2.7kHz, Vin = -58.5dBm at 120μs – NS, 315Hz	-0.1	1.3	2.9	dB
	70μs – NS frequency response	f = 4.5kHz, Vin = -53.8dBm at 120μs – NS, 315Hz	-0.1	1.7	2.9	
	120μs – HS frequency response	f = 5.3kHz, Vin = -52.5dBm at 120μs – NS, 315Hz	1.8	3.0	4.8	
	70μs – HS frequency response	f = 9.1kHz, Vin = -47.8dBm at 120μs – NS, 315Hz	2.1	3.6	5.1	
	Signal handling	120μs – NS, RL = 2.7kΩ f = 1kHz, THD + N = 1%	-10.0	-6.0	—	
	Total harmonic distortion	120μs – NS, RL = 2.7kΩ f = 1kHz, Vin = -56.4dBm	—	0.3	0.7	%
	S/N ratio	120μs – NS, Rg = 470Ω “A” weighting filter	55.0	62.0	—	dB
	Output offset voltage	120μs – NS, Rg = 470Ω, playback mute OFF	2.4	2.7	3.2	V
	Playback mute characteristics	120μs – NS, f = 1kHz, Vin = -51.4dBm	—	-100	-80	dB

Item		Measurement conditions	Min.	Typ.	Max.	Unit
Recording equalizer amplifier block	Reference input level	NORM – NS, 315Hz, input level at which reference output can be obtained	-28.2	-26.7	-25.2	dBm
	Reference output level	NORM – NS, 315Hz	—	-10.0	—	
	Channel balance	NORM – NS, 315Hz, output level difference 1ch-2ch for -26.7dBm input	-1.5	0.0	1.5	dB
	NORM – NS frequency response	f = 3kHz at NORM – NS, 315Hz, reference output -20dB	-1.8	-0.6	0.6	
	NORM – NS frequency response	f = 8kHz at NORM – NS, 315Hz, reference output -20dB	3.4	5.2	7.0	
	NORM – NS frequency response	f = 12kHz at NORM – NS, 315Hz, reference output -20dB	8.7	11.7	14.7	
	CrO <sub>2</sub> – NS frequency response	f = 3kHz at NORM – NS, 315Hz, reference output -20dB	3.7	4.9	6.1	
	CrO <sub>2</sub> – NS frequency response	f = 8kHz at NORM – NS, 315Hz, reference output -20dB	9.9	11.4	12.9	
	CrO <sub>2</sub> – NS frequency response	f = 12kHz at NORM – NS, 315Hz, reference output -20dB	14.8	17.6	20.4	
	METAL – NS frequency response	f = 3kHz at NORM – NS, 315Hz, reference output -20dB	4.7	5.9	7.1	
	METAL – NS frequency response	f = 8kHz at NORM – NS, 315Hz, reference output -20dB	8.7	10.2	11.7	
	METAL – NS frequency response	f = 12kHz at NORM – NS, 315Hz, reference output -20dB	12.9	15.2	17.5	
	NORM – HS frequency response	f = 5kHz at NORM – NS, 315Hz, reference output -20dB	-1.6	0.2	2.2	
	NORM – HS frequency response	f = 15kHz at NORM – NS, 315Hz, reference output -20dB	7.6	9.7	11.8	
	NORM – HS frequency response	f = 20kHz at NORM – NS, 315Hz, reference output -20dB	11.9	14.9	17.4	
	CrO <sub>2</sub> – HS frequency response	f = 5kHz at NORM – NS, 315Hz, reference output -20dB	5.2	6.4	7.6	
	CrO <sub>2</sub> – HS frequency response	f = 15kHz at NORM – NS, 315Hz, reference output -20dB	14.1	16.2	18.3	
	CrO <sub>2</sub> – HS frequency response	f = 20kHz at NORM – NS, 315Hz, reference output -20dB	16.7	19.7	22.7	
	METAL – HS frequency response	f = 5kHz at NORM – NS, 315Hz, reference output -20dB	6.8	8.0	9.2	
	METAL – HS frequency response	f = 15kHz at NORM – NS, 315Hz, reference output -20dB	13.7	15.5	17.3	
METAL – HS frequency response	f = 20kHz at NORM – NS, 315Hz, reference output -20dB	16.9	19.4	21.9		

Item		Measurement conditions	Min.	Typ.	Max.	Unit
Recording equalizer amplifier block	Signal handling	NORM – NS, $R_L = 2.7k\Omega$ $f = 1kHz$ , THD + N = 1%	8.0	8.8	—	dB
	Total harmonic distortion	NORM – NS, $R_L = 2.7k\Omega$ $f = 1kHz$ , 0dB	—	0.2	0.5	%
	S/N ratio	NORM – NS, $R_g = 5.1k\Omega$ “A” weighting filter	57.0	60.6	—	dB
	Output offset voltage	NORM – NS	3.6	4.0	4.4	V
	Recording mute characteristics	NORM – NS, $f = 1kHz$ 8dB	—	-100	-80	dB
Control voltage low level 1	A-EQ (Pin 2)	0.0	—	0.5	V	
Control voltage high level 1	A-EQ (Pin 2)	2.5	—	$V_{CC}$		
Control voltage low level 2	B-EQ (Pin 3)	0.0	—	0.5		
Control voltage medium level 1	B-EQ (Pin 3)	2.2	—	2.8		
Control voltage high level 2	B-EQ (Pin 3)	4.2	—	$V_{CC}$		

**Note)** NORM – NS: NORMAL TAPE – NORMAL SPEED

NORM – HS: NORMAL TAPE – HIGH SPEED

CrO<sub>2</sub> – NS: CrO<sub>2</sub> TAPE – NORMAL SPEED

CrO<sub>2</sub> – HS: CrO<sub>2</sub> TAPE – HIGH SPEED

METAL – NS: METAL TAPE – NORMAL SPEED

METAL – HS: METAL TAPE – HIGH SPEED

120 $\mu$ s – NS: EQ = 120 $\mu$ s – NORMAL SPEED

120 $\mu$ s – HS: EQ = 120 $\mu$ s – HIGH SPEED

70 $\mu$ s – NS: EQ = 70 $\mu$ s – NORMAL SPEED

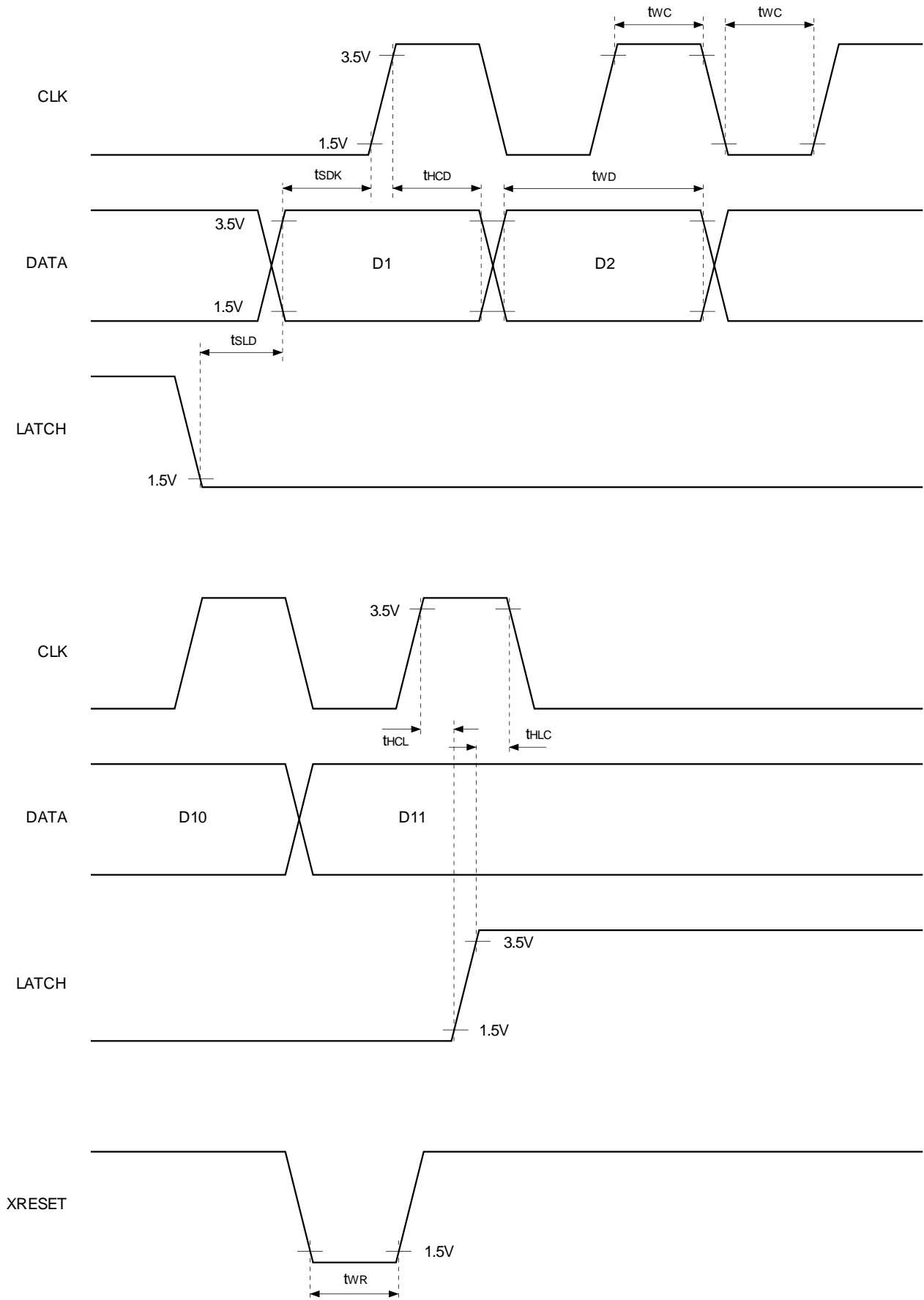
70 $\mu$ s – HS: EQ = 70 $\mu$ s – HIGH SPEED

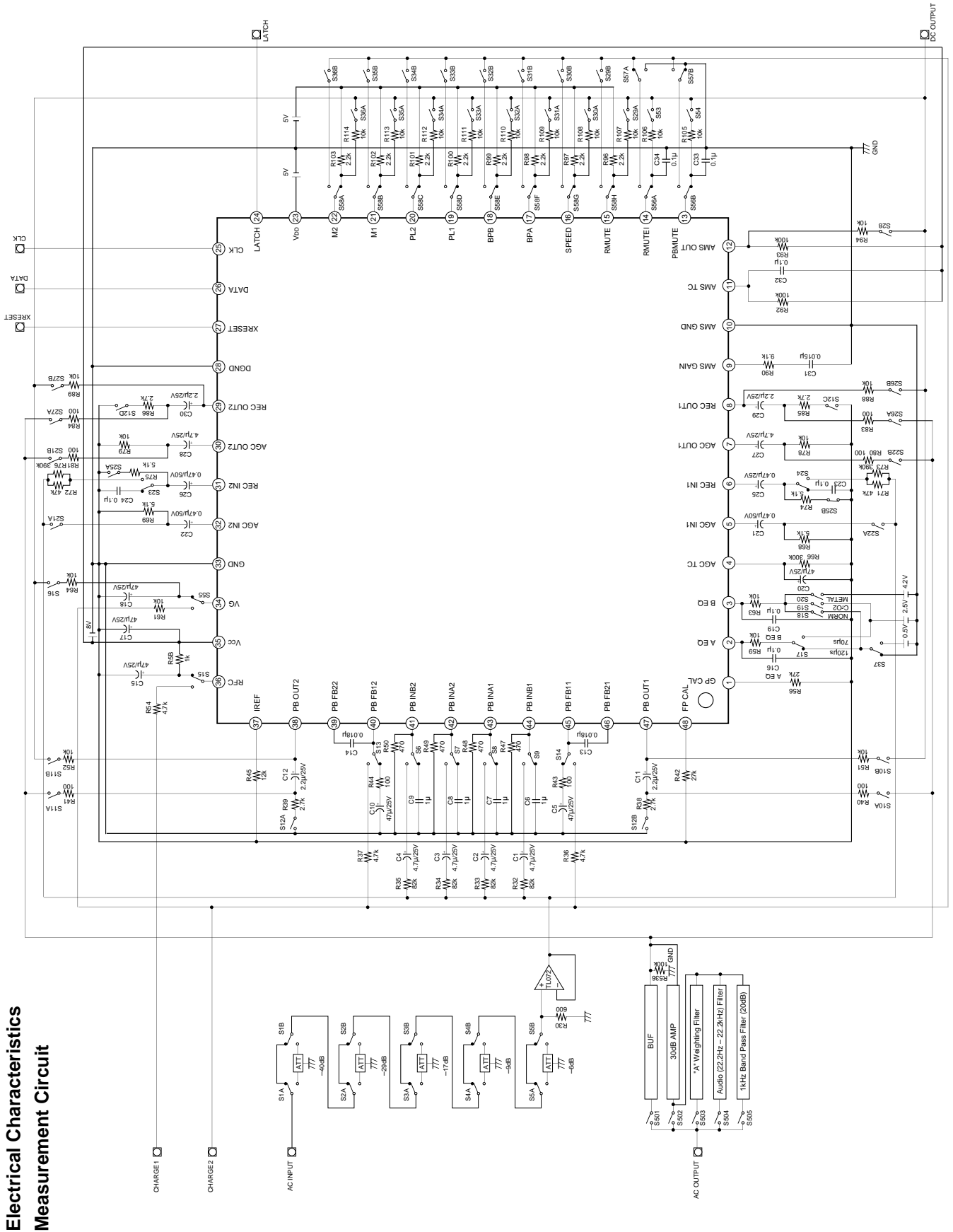
Item		Measurement conditions	Min.	Typ.	Max.	Unit
11-bit serial data interface block	Low level input voltage	$V_{IL}$ (LATCH/CLK/DATA/XRESET) (Pins 24, 25, 26, 27)	0.0	—	1.5	V
	High level input voltage	$V_{IH}$ (LATCH/CLK/DATA/XRESET) (Pins 24, 25, 26, 27)	3.5	—	$V_{DD}$	
	Low level output voltage	$V_{OL}$ , $I_{OL} = 2\text{mA}$ (max) (Pins 15, 16, 17, 18, 19, 20, 21, 22)	0.0	—	0.5	
	High level output off leak current	$I_{OZ}$ Leak current which flows to the output pin when $I_{OZ}$ output is open; applied voltage is 10V. (Pins 15 to 22)	—	—	1.0	$\mu\text{A}$
	Maximum clock frequency	(1) $f_{CK}$	500	—	—	kHz
	Minimum clock pulse width	(2) $t_{WC}$	—	—	1.0	$\mu\text{s}$
	Minimum reset pulse width	(3) $t_{WR}$	—	—	1.0	
	Minimum data setup time	(4) $t_{SDK}$ (DATA → CLK)	—	—	1.0	
	Minimum data hold time	(5) $t_{HCD}$ (CLK → DATA)	—	—	1.0	
	Minimum data pulse width	(6) $t_{WD}$	—	—	2.0	
	Minimum latch setup time	(7) $t_{SLD}$ (LATCH → DATA)	—	—	1.0	
	Minimum latch hold time	(8) $t_{HCL}$ (CLK → LATCH)	—	—	1.0	
Minimum clock hold time	(9) $t_{HLC}$ (LATCH → CLK)	—	—	1.0		

**Note)**

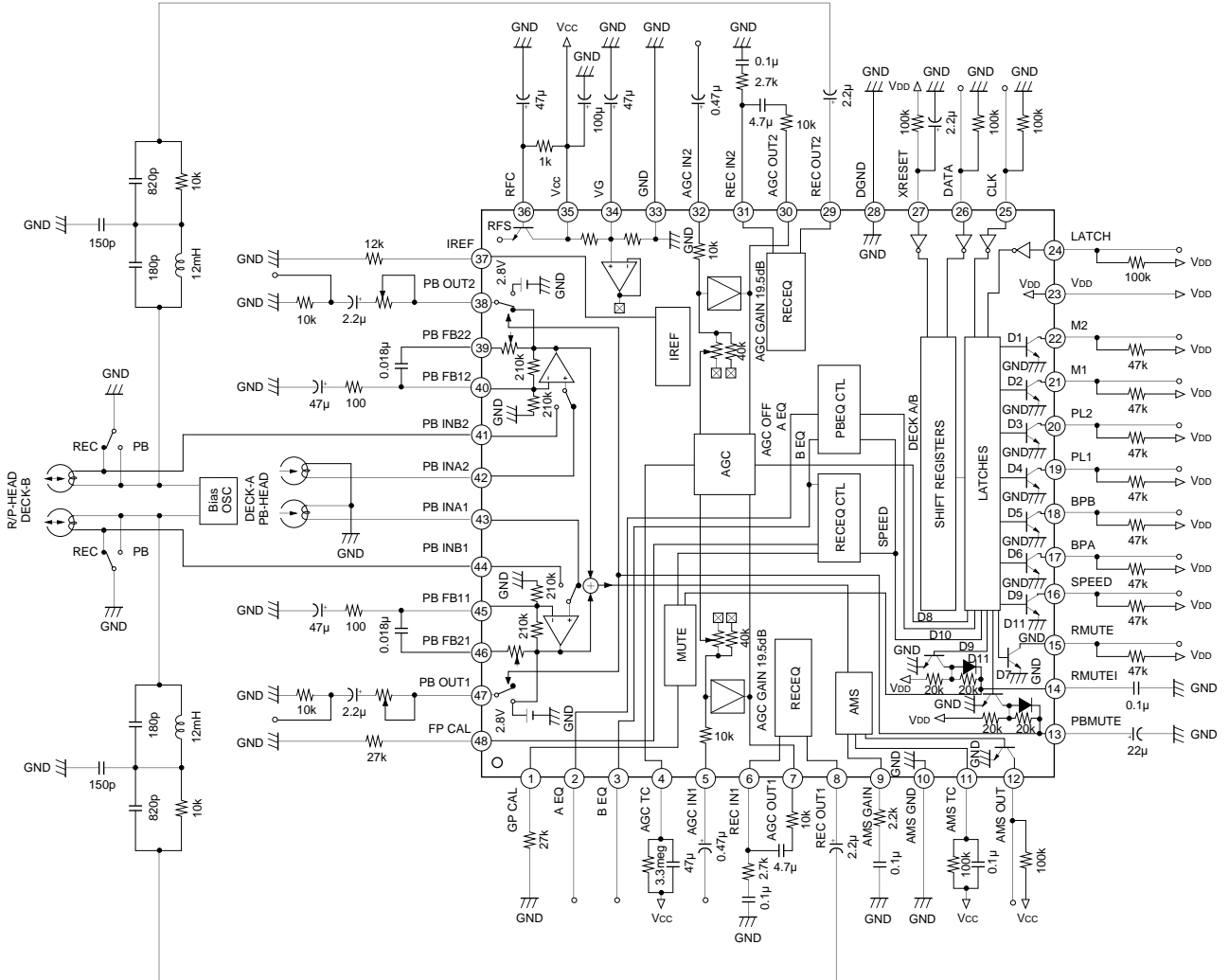
- $V_{DD}$  is CPU supply voltage of 5.0V.
- $V_{CC}$  is 10.0V for high level output off-leak current.
- The threshold levels of low level input voltage and high level input voltage depend on  $V_{DD}$ . Input level detection is done by comparison with  $V_{DD}/2$ . (Refer to “Equivalent circuit” of Pin Description.)

Timing Chart for 11-bit Serial Data Interface ( $V_{DD} = 5.0V$ )





Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

**1. System control mode**

Playback and recording equalizer

(1) Playback equalizer (120μs/70μs)

		A-EQ (Pin 2)		B-EQ (Pin 3)	
		L	H	L	M/H
DECK-AB (serial data D10 (Pin 25))	L	120μs (DECK A)	70μs (DECK A)	According to A-EQ control	
	H	According to B-EQ control		120μs (DECK B)	70μs (DECK B)

(2) Playback mute (Pin 13)

ON/OFF control is performed by 11-bit serial data interface D7 (Pin 26). A capacitor for setting the switching time constant is connected.

$$\text{Time constant} = 20\text{k}\Omega \times C$$

(3) Recording equalizer (Normal, CrO<sub>2</sub>, Metal)

B-EQ (Pin 3)	L	M	H
REC MODE	NORMAL (TYPE I)	CrO <sub>2</sub> (TYPE II)	METAL (TYPE IV)

(4) Recording mute (Pin 14)

ON/OFF control is performed by 11-bit serial data interface D11 (Pin 26). A fader function is achieved using a time constant circuit formed with the external capacitor and incorporated 20kΩ resistor.

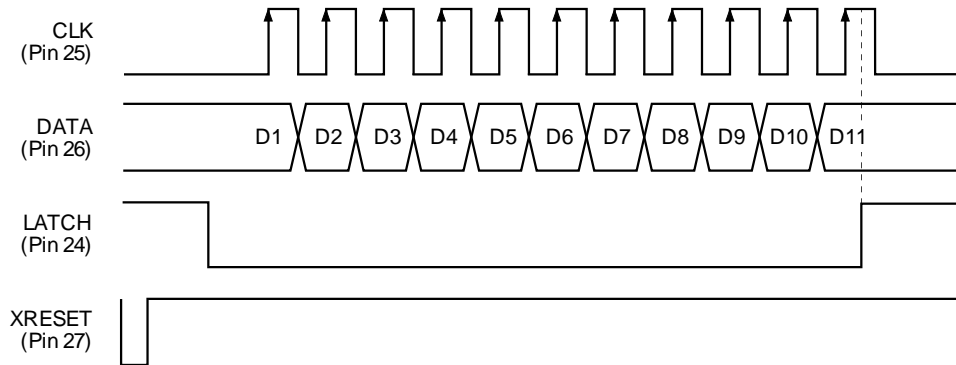
(5) FP CAL (Pin 48)

The standard resistor setting is 27kΩ, but when resistance value is larger, fo (Hz) is lower, and when resistance value is smaller, fo (Hz) is higher. (fo: high-band peak frequency)

(6) GP CAL (Pin 1)

The standard resistor setting is 27kΩ, but when resistance value is larger, high-band peak gain is larger, and when resistance value is smaller, high-band peak gain is smaller.

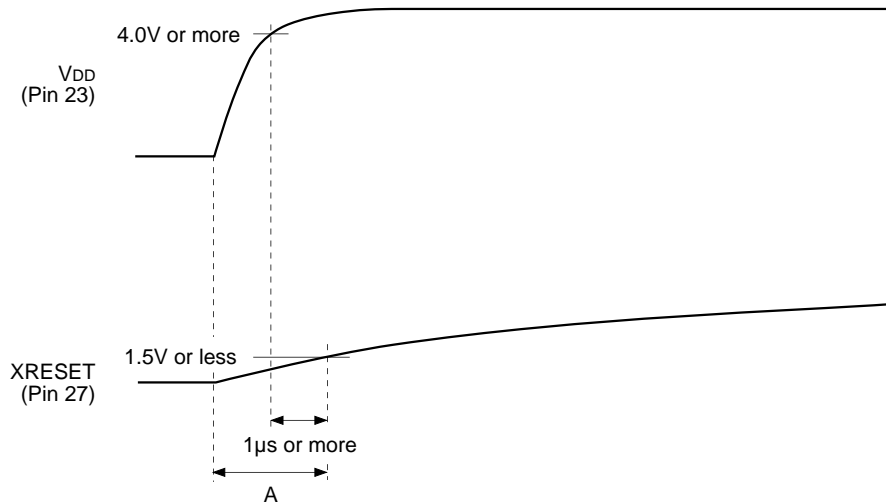
2. 11-bit serial data interface



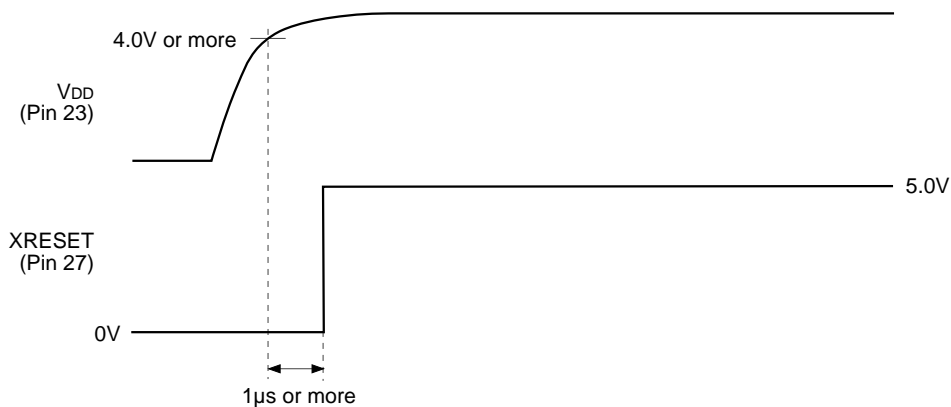
- The DATA signal is taken in at the rising edge of the CLK signal.
- The DATA signal is taken into the internal shift register when the LATCH signal is low. (Outputs (Pins 15 to 22) hold the previous value while the LATCH signal is low.)
- The internal shift register data is latched and output in parallel at the rising edge of the LATCH signal. (Internal shift register data is loaded while the LATCH signal is high.)
- The CLK signal of the 11th bit should fall after the LATCH signal rises.
- Reset is done when the XRESET pin is low. (asynchronous method)  
Outputs (Pins 15 to 22) are all high (open) during reset.

DATA (Pin 26)	Control signal	Output		
		Output pin	Input set at low	Input set at high
D1	M2	Pin 22	Low	High (OPEN)
D2	M1	Pin 21	Low	High (OPEN)
D3	PL2	Pin 20	Low	High (OPEN)
D4	PL1	Pin 19	Low	High (OPEN)
D5	BPB	Pin 18	Low	High (OPEN)
D6	BPA	Pin 17	Low	High (OPEN)
D7	PB MUTE	—	Low mute OFF	High mute ON
D8	AGC OFF	—	AGC function stops	AGC function operates
D9	SPEED	Pin 16	Low, normal speed	High (open) 1.7
D10	DECK AB	—	DECK A selected	DECK B selected
D11	REC MUTE	Pin 15	Low mute OFF	High (open) mute ON

- Make sure that  $V_{DD}$  is 4.0V or more and XRESET is 1.5V or less, and 1 $\mu$ s or more when resetting by applying CR time constant to XRESET (Pin 27) and turning power ON.



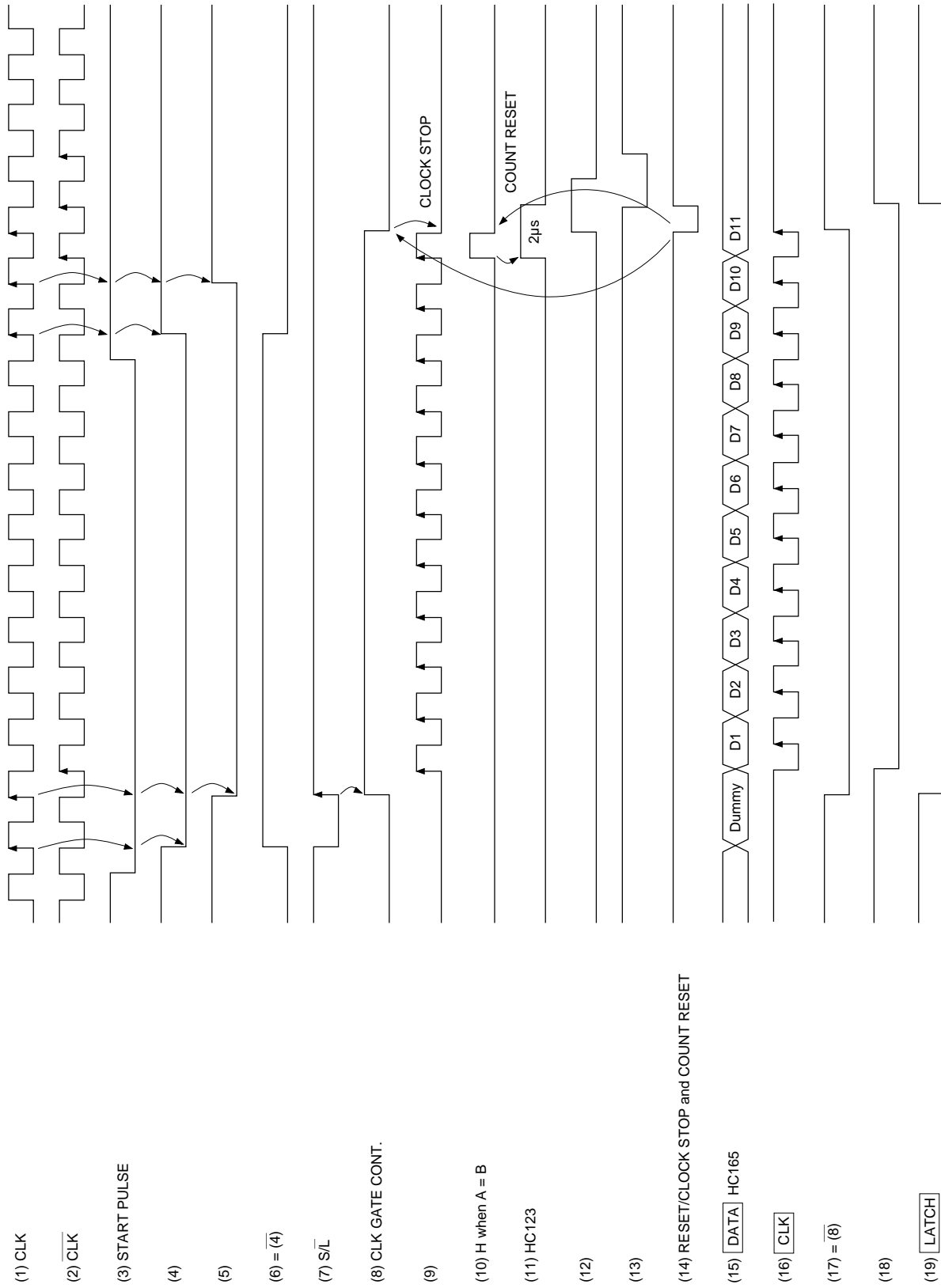
- XRESET (Pin 27) input level detection is done by comparison with  $V_{DD}/2$ . The level should be  $V_{DD}/2 > XRESET$  during the interval A.
- For resetting with CPU when power is turned ON



- Examples of AGC control during timer recording
  - (1) Resets when power is turned ON (AGC function operates).
  - (2) AGC is turned OFF after AGC inputs (Pins 5 and 32) rise. (External capacitor charge of AGC TC is discharged.)
  - (3) AGC is turned ON and timer recording begins.



Timing Chart for 11-bit Serial Data Transfer Evaluation Tool



The numbers (1) to (19) correspond to those of test pins for the 11-bit serial data transfer evaluation tool circuit.

3. AMS

(1) AMS output logic

Detection status	Signal detection	No signal detection
AMS OUT (Pin 12)	Low	High

AMS OUT (Pin 12) is an open collector output pin. When a 3.9 kΩ resistor is connected to Vcc = 8V:  
 Low: approximately 0.5V (I<sub>OL</sub> = 2mA (max.))  
 High: 8V

Fig. 1 shows the AMS block diagram.

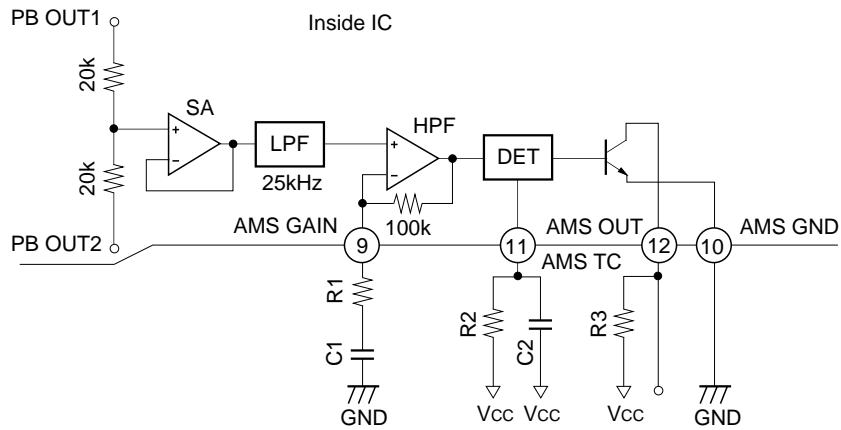


Fig. 1. AMS Block Diagram

Fig. 2 shows the frequency response of the signal output from HPF.

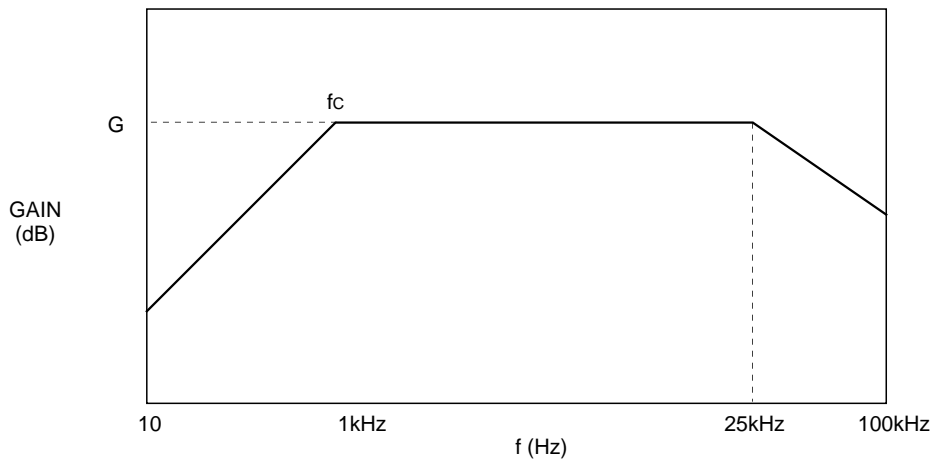


Fig. 2. Frequency Response

## (2) AMS level setting

The AMS level is set by adjusting HPF gain and cut-off frequency with the external resistor and capacitor at Pin 9.

G and  $f_c$  in Fig. 2 are obtained from the following formula.

$$G = 20\log(1 + 100k/R1) \text{ [dB]} \dots\dots\dots (1)$$

$$f_c = 1 / (2 \cdot \pi \cdot C1 \cdot R1) \text{ [Hz]}$$

Full-wave rectifier is applied for the signal at DET.

Signal detection time is set by the time constant of Pin 11 external resistor and capacitor.

DET signal detection level:

$$= -7.5\text{dBm (typ.)}$$

$$= \text{playback equalizer reference output level} + \text{AMS level} + \text{HPF gain} \dots\dots\dots (2)$$

Playback equalizer reference output level of  $-21\text{dBm}$  is  $0\text{dB}$ .

### Ex.)

To set AMS level at  $-25\text{dB}$ , determine and set the constant for Pin 9 external resistor.

(Calculate assuming  $\text{PBOUT1} = \text{PBOUT2}$ )

First, get the required HPF gain from formula (2).

$$-7.5\text{dBm} = -21\text{dBm} + (-25\text{dB}) + \text{HPFgain},$$

so HPF gain =  $38.5\text{dB}$ .

Next, get Pin 9 external resistance from formula (1).

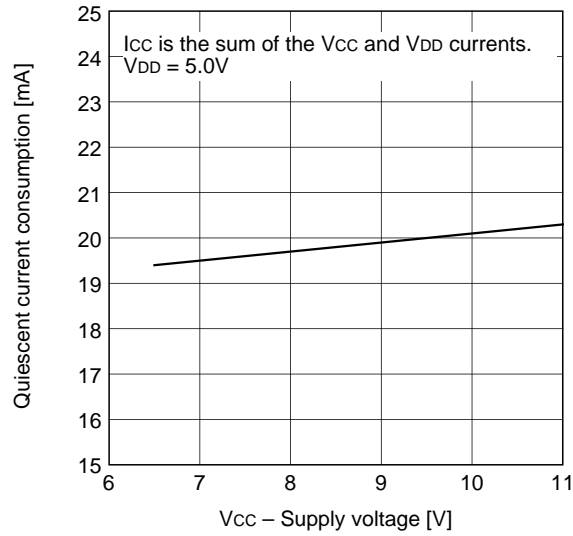
$$38.5\text{dB} = 20\log(1 + 100k / R1),$$

so  $R1 \approx 1.2\text{k}\Omega$ ,

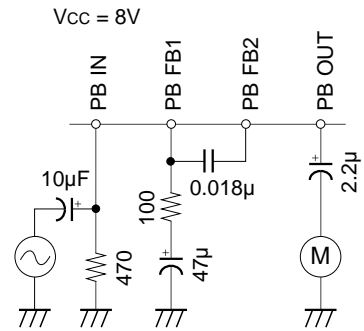
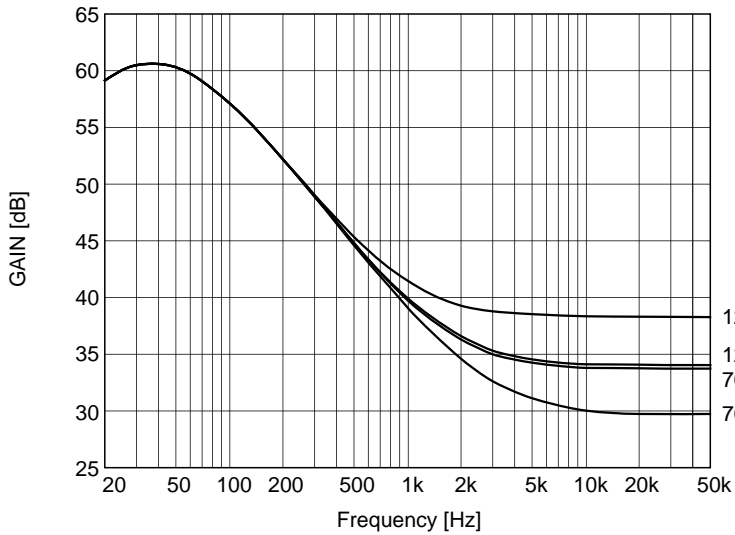
and external resistance is  $1.2\text{k}\Omega$ .

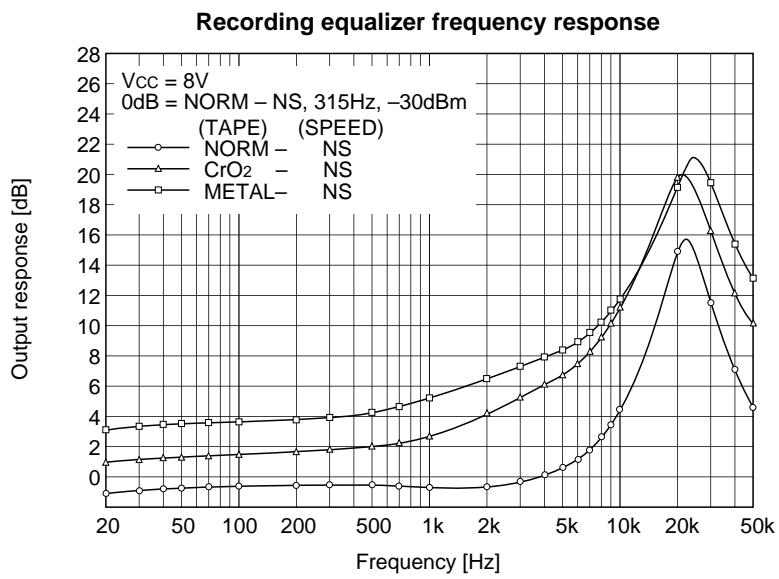
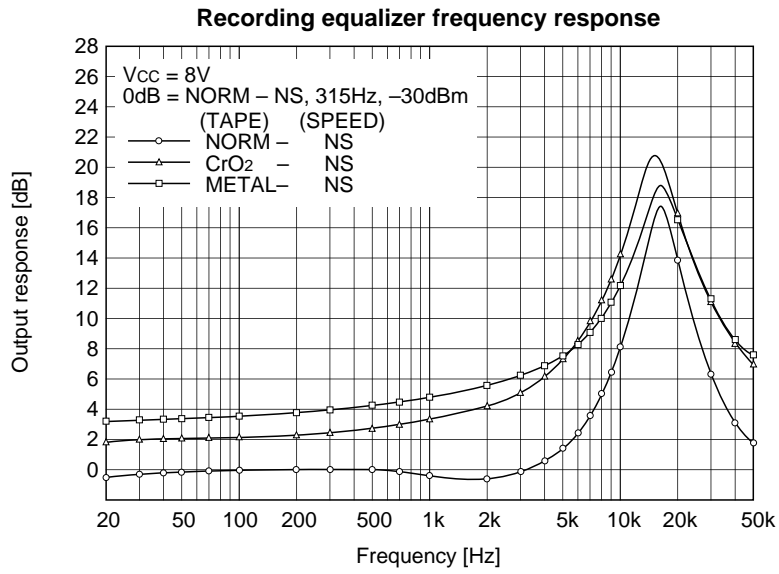
Example of Representative Characteristics

Quiescent current consumption vs. Supply voltage

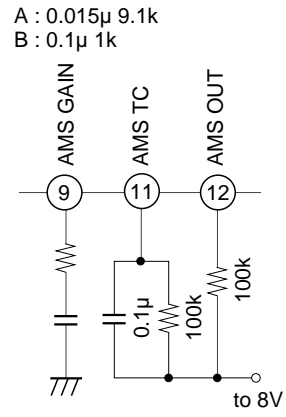
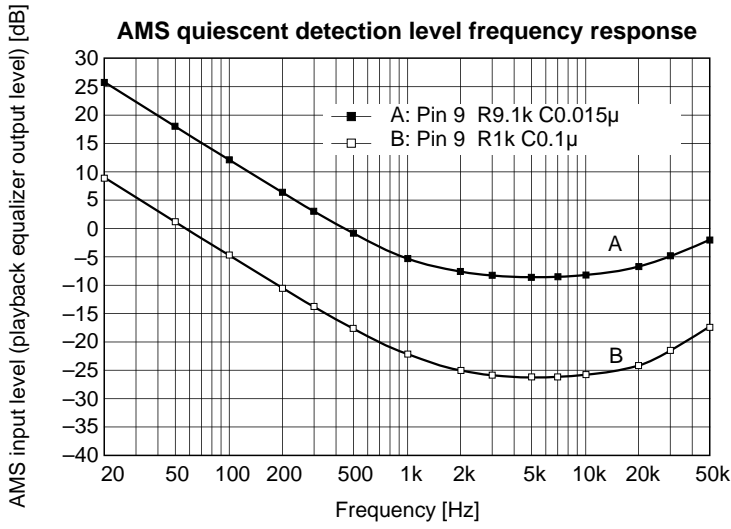


Playback equalizer frequency response

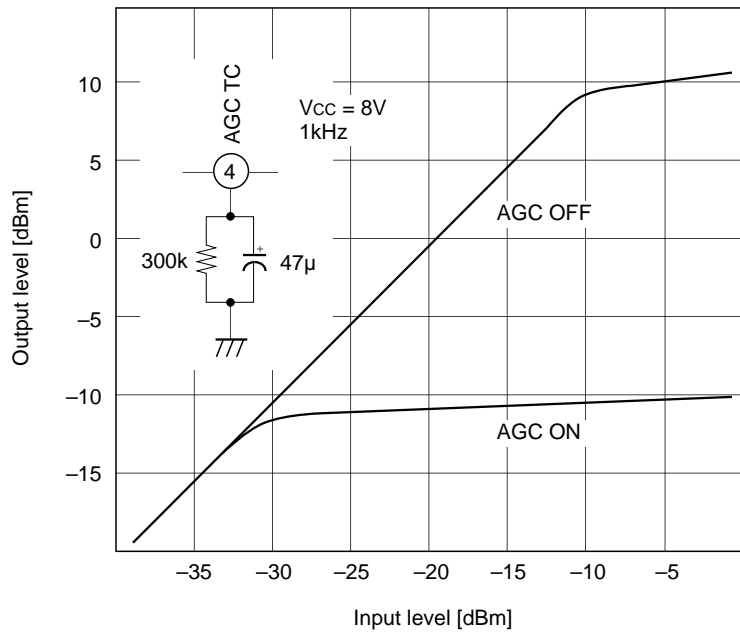




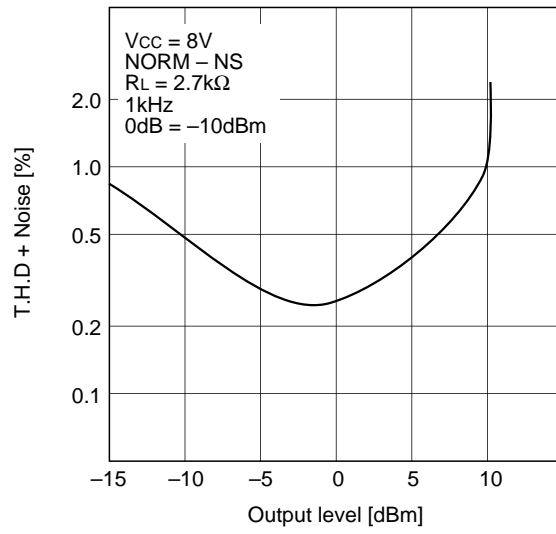
V<sub>CC</sub> = 8V  
 120μs - NS  
 AMS OUT 8V  
 0dB = -21dBm, 315Hz (playback equalizer reference output level)



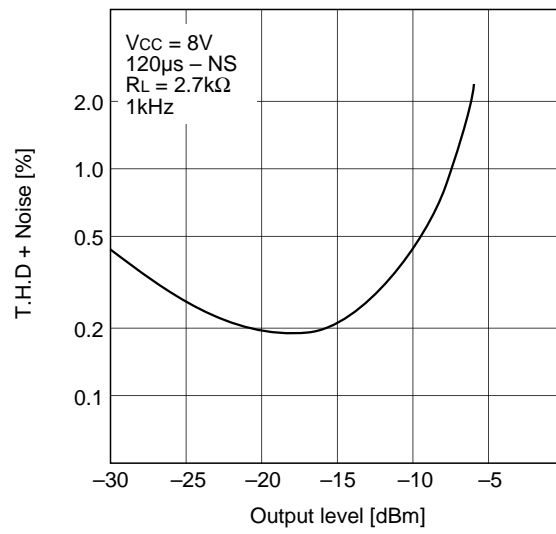
### AGC output characteristics



**Recording equalizer total harmonic distortion**

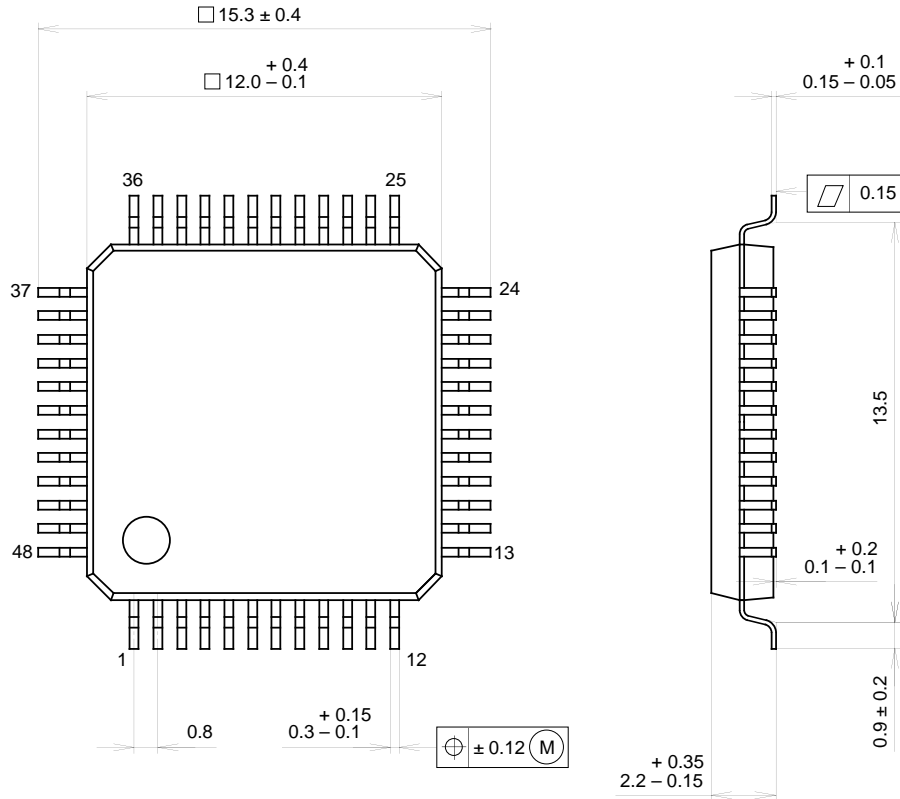


**Playback equalizer total harmonic distortion**



Package Outline Unit: mm

48PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-48P-L04
EIAJ CODE	*QFP048-P-1212-B
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.7g

NOTE : PALLADIUM PLATING  
 This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).



LittleDiode supplies new, hard to find or obsolete electronic components and semiconductors all over the world.

With over two million different components listed you are sure to find the part you need.

Feel free to visit us today at our online store:

[LittleDiode.com](http://LittleDiode.com)

Looking forward to providing you with the best possible service.