SONY

CXA1644P

Echo Effect Generator

Description

The CXA1644P is an echo effect generator IC designed for use in a karaoke set.

Features

- All the functions required for producing echo effects into a single chip.
- Delay time 100ms (typ.)
- Few external parts
- Combined with a 2-channel surround IC (CXA1673), produces full-fledged surround effects.
- Variable effect volume

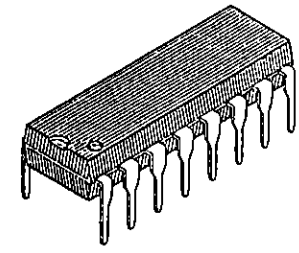
Applications

Karaoke set, TV (surround), etc.

Structure

Bi-CMOS IC

16 pin DIP (Plastic)



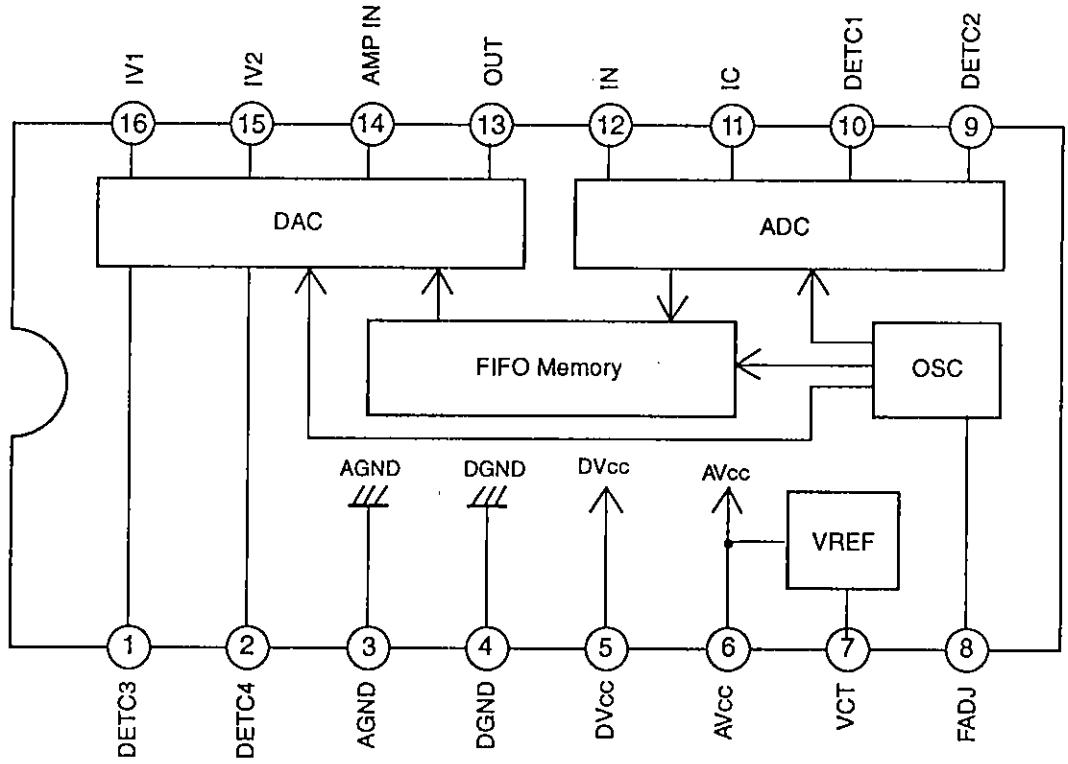
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	Vcc	7	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−65 to +150	°C
• Allowable power dissipation	PD	900	mW

Operating Conditions

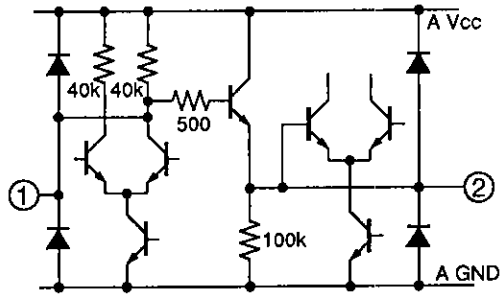
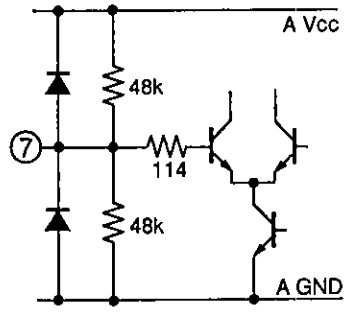
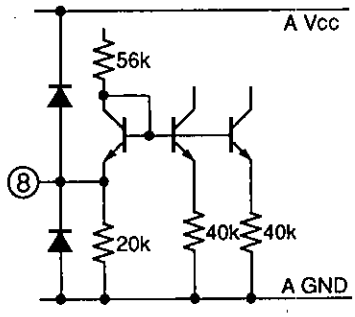
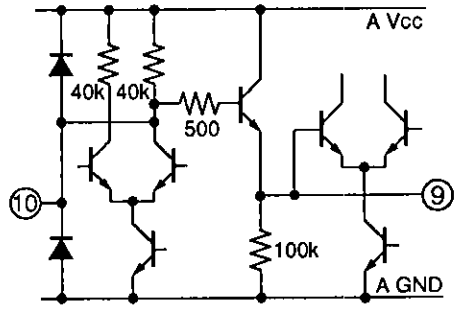
• Supply voltage	Vcc	4.0 to 6.0	V

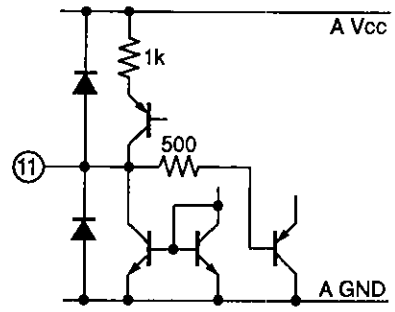
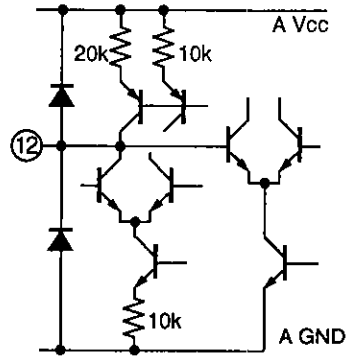
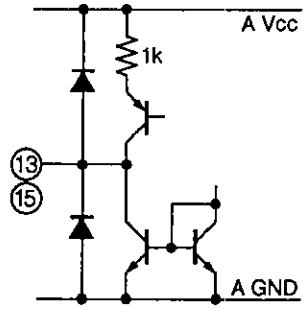
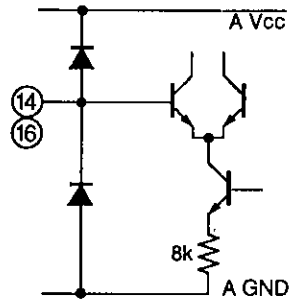
Block Diagram and Pin Configuration



E92303-TE

Pin Description

No.	Symbol	Equivalent circuit	voltage (V)	Description
1 2	DETC 3 DETC 4		4.0 3.3	Connects smoothing capacitors of level detectors for D/A converter.
3	AGND		0	GND for analog
4	DGND		0	GND for digital
5	DVcc		5.0	Vcc for digital
6	AVcc		5.0	Vcc for analog
7	VCT		2.5	Center of power supply. Connects a ripple eliminating capacitor.
8	FADJ		0.22	Adjusts the oscillation frequency of clock oscillator
9 10	DETC 2 DETC 1		3.3 4.0	Connects smoothing capacitors of level detectors for A/D converter.

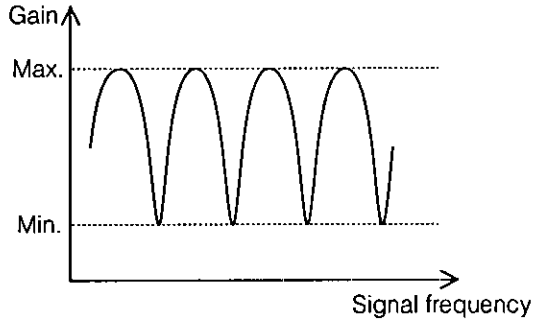
No.	Symbol	Equivalent circuit	voltage (V)	Description
11	IC		—	Pin 11...Connects the external capacitor of A/D converter. A triangular wave is output during no signal.
12	IN		2.5	Input pin of A/D converter.
13 15	OUT IV 2		2.5 2.5	Pin 13..Output pin of output amplifier. Pin 15..Output pin of D/A converter.
14 16	AMP IN IV 1		2.5 2.5	Pin 14...Input pin of output amplifier. Pin 16...Connects the external element of D/A converter.

Electrical Characteristics (Ta=25°C, Vcc=5.0V)

Test No.	Item	Symbol	Conditions	SW1	SW2	Test Point	Min.	Typ.	Max.	Unit
1	Supply current	Icc	No signal	OFF	ON	Vcc		4.8	7.3	mA
2	Gain	Ga	500Hz 250mVrms input (Note 1)	OFF	ON	A	–3	0	3	dB
3	Total harmonic distortion	THD	500Hz 250mVrms input (Note 2)	OFF	ON	A		0.3	1.5	%
4	Maximum input level	V_{IMAX}	f=500Hz THD+N=5% (Note 2)	OFF	ON	A	250	350		mVrms
5	Noise voltage	Vn	No signal IHF–A weighted	OFF	ON	A		–76	–67	dBv
6	Delay time	Td	500Hz 250mVrms input	OFF	ON	A, B	60	100	130	ms

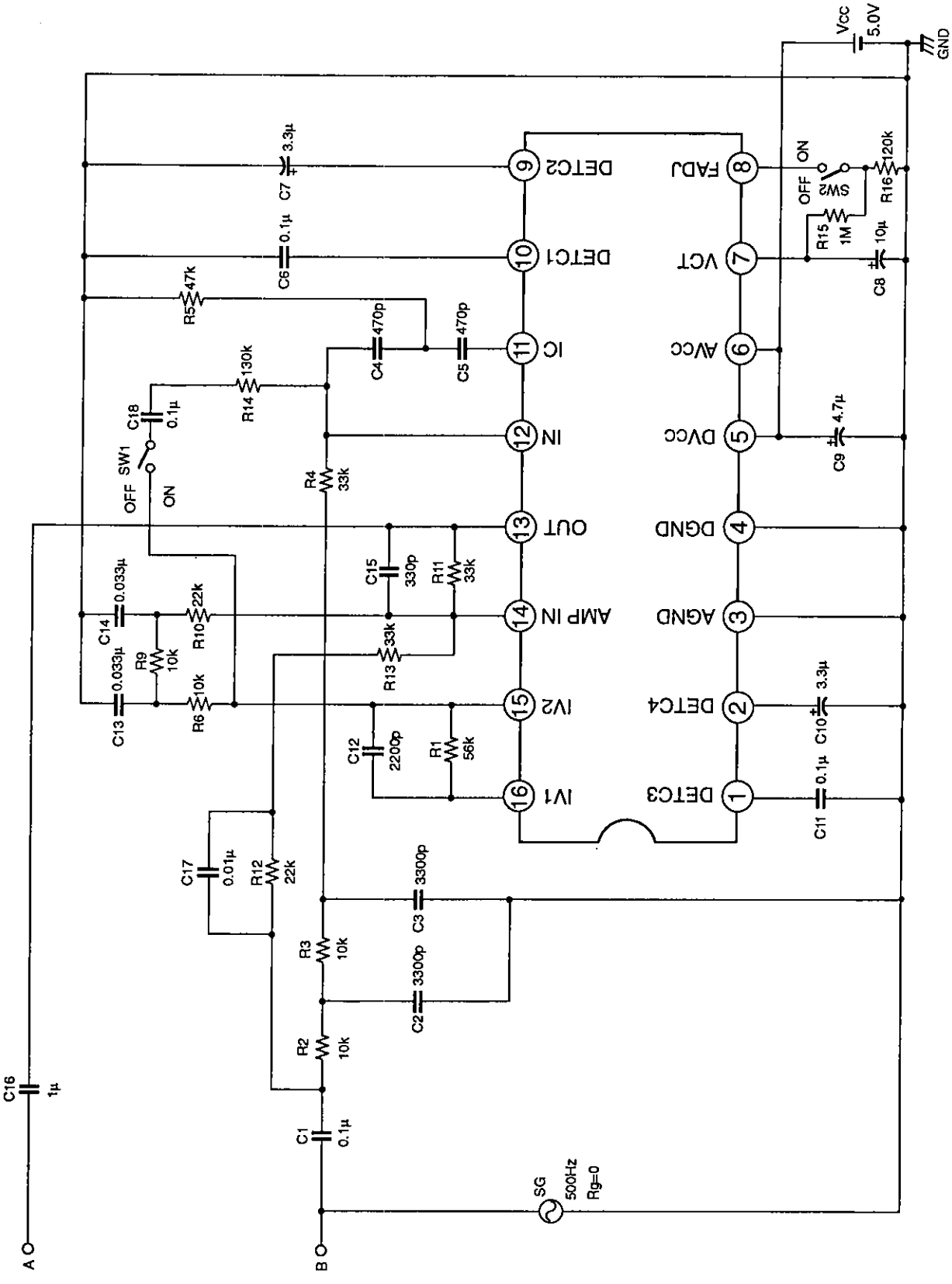
SW1 : ECHO SW
SW2 : FADJ SW

(Note 1) The frequency characteristics of gain produce ripples as shown below because of the system configuration of the CXA1644P. Here the maximum value of gain at around the signal frequency of 500Hz is defined as the gain.

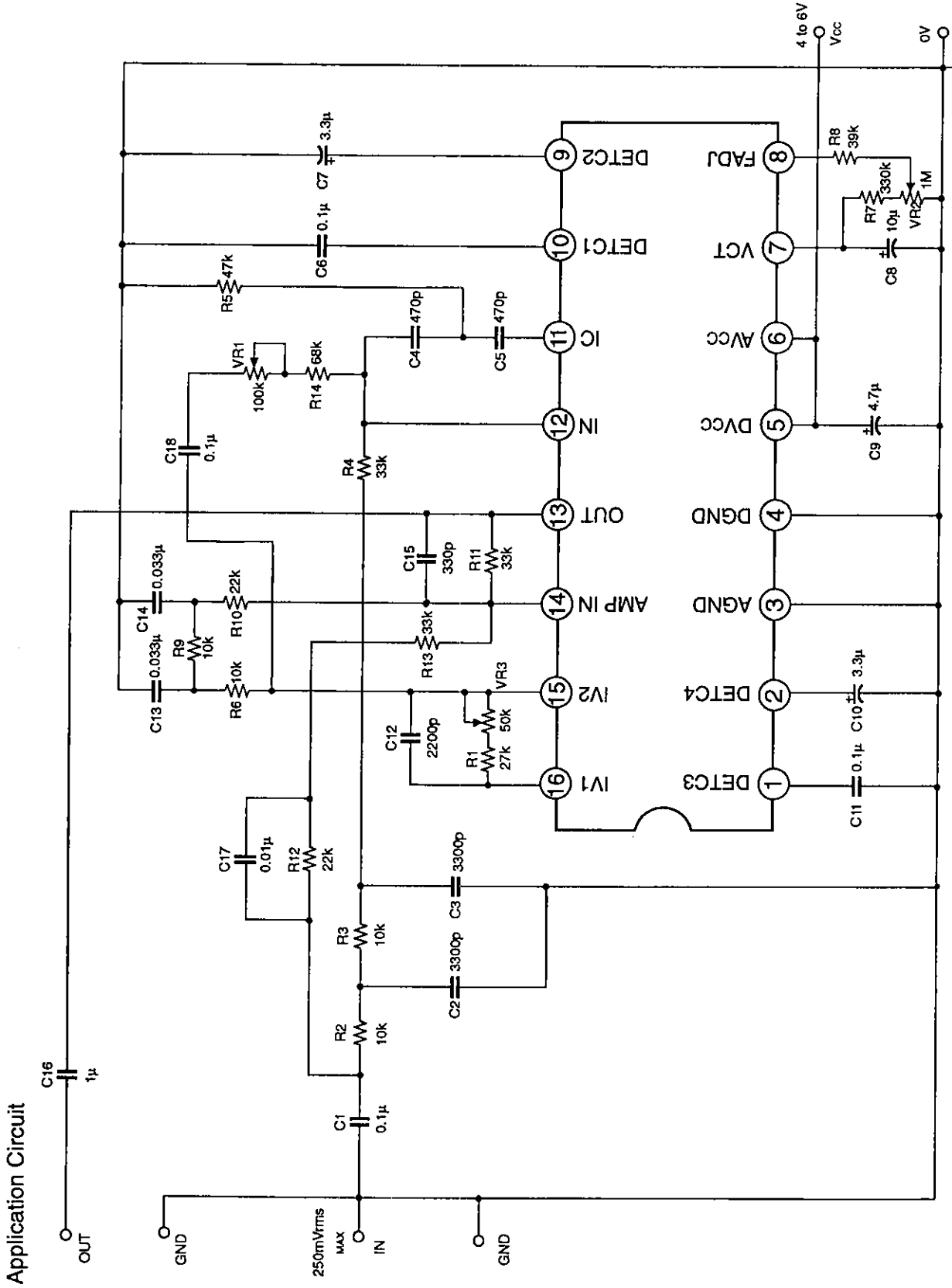


(Note 2) The signal frequency should be that the gain becomes the maximum at around the signal frequency of 500Hz.

Electrical Characteristics Measurement Circuit



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

Description of Operation

The CXA1644P is a digital echo IC using a 1-bit oversampling A/D converter.

The input signal is input to Pin 12 for A/D conversion. The input sensitivity of the A/D converter is determined by R2+R3+R4. The A/D converter extends the dynamic range by joint use of a signal level detector for adaptive control of the maximum signal level.

The output data of the A/D converter is 8192 clock delayed by FIFO memory (8 kbits). The output data of FIFO memory is converted to analog signal by the D/A converter. The D/A converter jointly uses a signal level detector of the same construction used by the A/D converter.

The output current of the D/A converter is I-V converted by the inversion amplifier between Pins 16 and 15. At the same time, the I-V converter constitutes the 1st-order LPF determined by the time constant of C12 • (R1+VR3). The VR3 is used to adjust the gain irregularities of the A/D and D/A converters. The output signal (Pin 15) of D/A converter is led to the 2nd-order LPF composed of R6, R9, R10, C13 and C14 to eliminate high frequency noise components before it is input to Pin 14. The inversion amplifier between Pins 14 and 13 is used as an adder. Non-delayed input signal is input through C17, R12 and R13 to Pin 14 for addition of the input signal with the high-frequency component emphasized by the circuit. The added signal is led through C15 and VR11 to attenuate the unwanted high-frequency component by their time constants and is output as voltage from Pin 13.

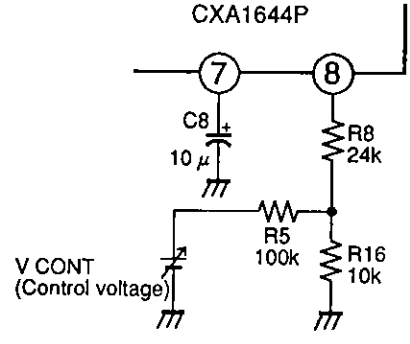
The output signal of the D/A converter is fed back through C18, VR1 and R14 to Pin 12. This feedback and the delay caused by the FIFO memory generate echo effects. The depth of the echo effects is variable by changing the resistance value of VR1.

The FIFO memory of the CXA1644P has a fixed capacity. The delay time is adjusted by changing the cycle of sampling clock. The clock cycle is adjustable by VR2.

Notes on Operation

1. Setting delay time

The delay time in the Electrical Characteristics denotes the range where the delay time varies when measured by an electrical characteristic measurement circuit. For how the delay time varies when VR2 is adjusted, refer to Graphs 1 and 2. Graph 1 shows the variation of the delay time in a standard IC, but the control characteristics vary within the range shown in Graph 2 due to IC irregularities. The delay time may be adjusted by applying control voltage from outside as shown below instead of using VR2 in the Application Circuit. Graph 3 shows the variation of the delay time caused by changing the control voltage over a range from 0 to 5 V when Vcc=5 V. When this control voltage is replaced by the output voltage of DA converter controlled by microcomputer, the delay time can be controlled by microcomputer.

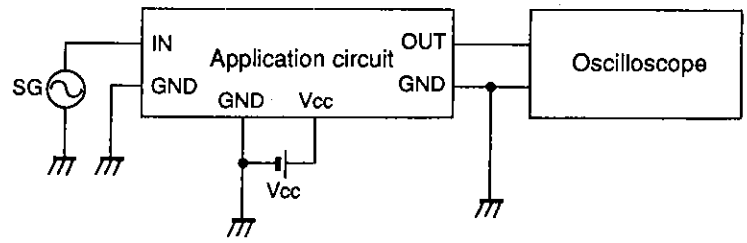


For adjusting the delay time, use the following methods.

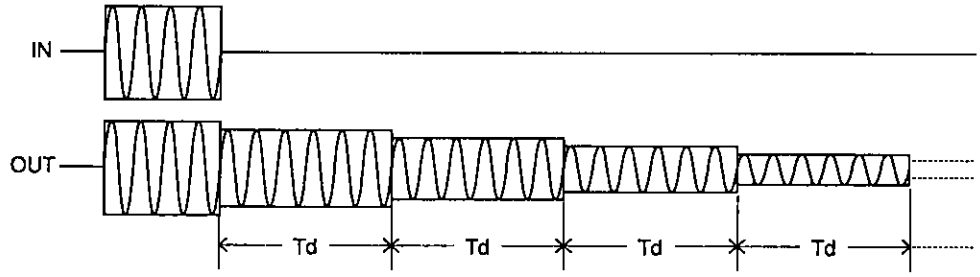
(1) Input one-shot tone burst and observe the envelope of the output signal with an oscilloscope.

(2) Observe the clock cycle with an oscilloscope and calculate the delay time on the basis of the clock cycle.

Method (1)



Make connections as shown above, and input one-shot tone burst from SG. At the time, a waveform such as shown below is output to OUT. The "Td" of the envelope is the delay time.



Method (2)

This method is used not to directly observe the output waveform but to observe the clock cycle and calculate the delay time on the basis of the value of the clock cycle.

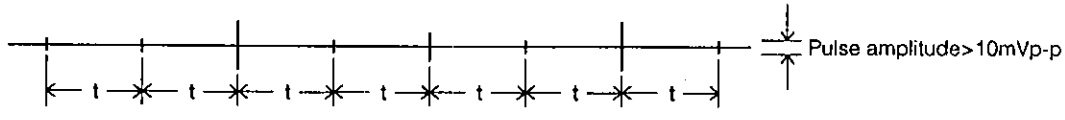
The delay time "Td" can be obtained from the clock cycle T_{CLK} as stated in the following formula.

$$Td\ [ms] = 16.3 \bullet T_{CLK}\ [\mu s] + 0.7$$

To set the delay time of 100ms for example, set the T_{CLK} to 6.09µs.

Observe the clock cycle as described below.

Pulses synchronized with the clock cycle can be observed at the input virtual ground point (Pin 16) of the I-V conversion amplifier of the D/A converter. The waveform at Pin 16 is as follows.



The pulse amplitude is not constant, but the interval t is constant. Substitute this t into the foregoing formula as T_{CLK}. Then the delay time can be obtained.

2. Input sensitivity

The input sensitivity of the CXA1644P is determined by R2+R3+R4 in the Application Circuit. The constant in the Application Circuit is set so that no clipping occurs until 250mVrms input. To change the input sensitivity, proceed as described below.

[Ex.] To set the input sensitivity at 1/2, or to set it so that no clipping occurs until 500 mVrms input,

(1) Double R2+R3+R4 as much value as Application Circuit.

R2 10kΩ -> 22kΩ
R3 10kΩ -> 22kΩ
R4 33kΩ -> 68kΩ

(2) Halve C2 and C3 shown in the Application Circuit

This is aimed at maintaining the time constant of LPF in the input section equal. In this example, since R2 and R3 have values 2.2 times, C2 and C3 are reduced to 1/2.2.

C2 3300pF -> 1500pF
C3 3300pF -> 1500pF

(3) Double R1+VR3 as much value as Application Circuit.

This is aimed at maintaining the gain from the input pin to the output pin equal. In this example, R2+R3+R4 have values approximately 2.1 times the values shown in the Application Circuit. Therefore, R1+VR3 are obtained as 2.1 times as large.

R1 27kΩ -> 56kΩ
VR3 50kΩ -> 100kΩ

(4) Halve C12 in the Application Circuit.

This is aimed at maintaining the frequency characteristic of I-V conversion amplifier of the D/A converter equal.

C12 2200pF -> 1200pF

(5) Double R14+VR1 as much value as Application Circuit.

This is aimed at maintaining each gain product of the A/D converter, D/A converter and feedback circuit equal to produce the same echo effects as in the Application Circuit.

R14 68kΩ -> 130kΩ
VR3 100kΩ -> 200kΩ (220kΩ)

3. Characteristics of C16

Determine the polarity of C16 on the basis of the DC operating point of the load (OUT pin). The DC operating point of Pin 13 is the center of Vcc (Vcc/2).

- Fig. 1 shows the polarity of C16 when the DC operating point of the OUT pin is higher than Vcc/2 of the CXA1644P.
- Fig. 2 shows the polarity of C16 when the DC operating point of the OUT pin is lower than Vcc/2 of the CXA1644P.
- When the DC operating point of the OUT pin is equal to Vcc/2 of the CXA1644P, either of Figs. 1 and 2 will do.

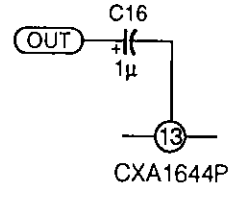


Fig.1

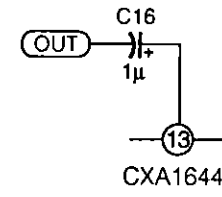
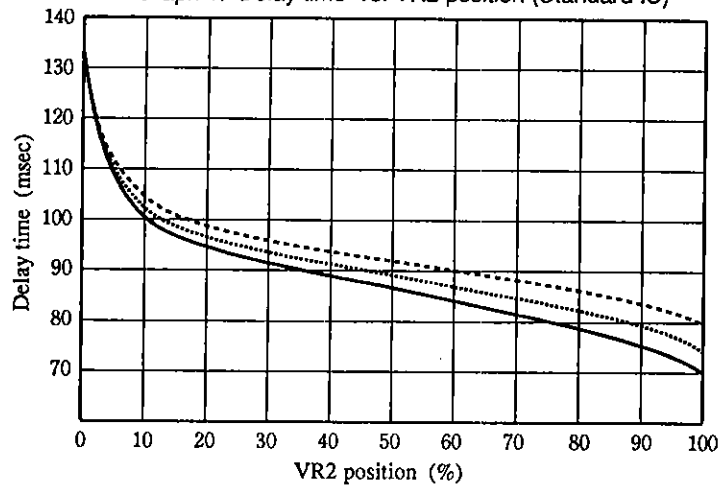
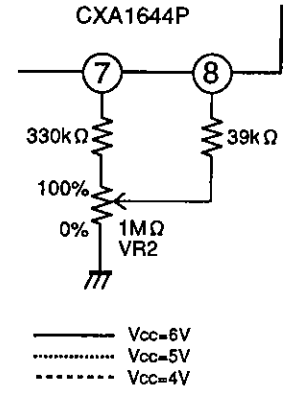


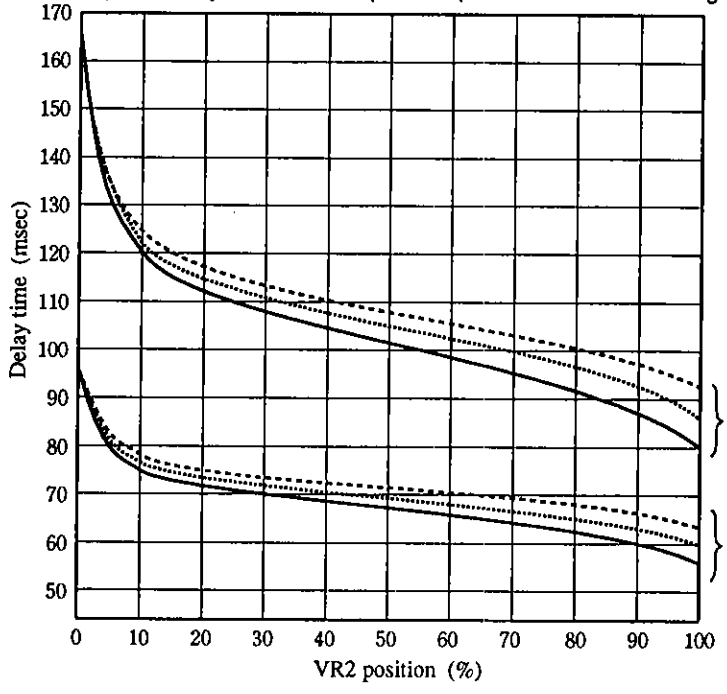
Fig.2

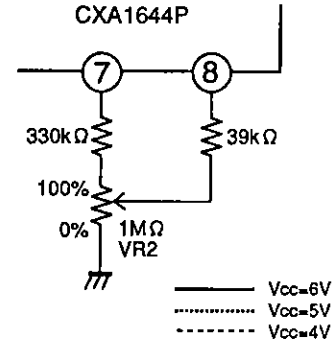
Graph 1. Delay time vs. VR2 position (Standard IC)



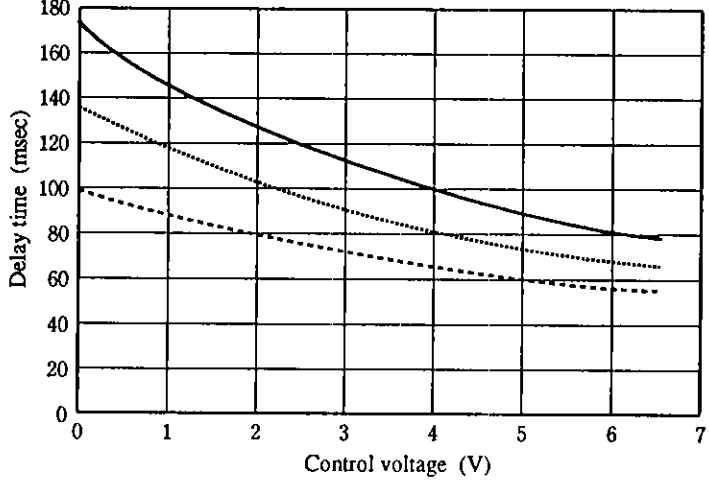


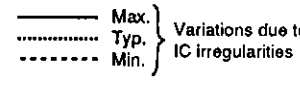
Graph 2. Delay time vs. VR2 position (Variations due to IC irregularities)





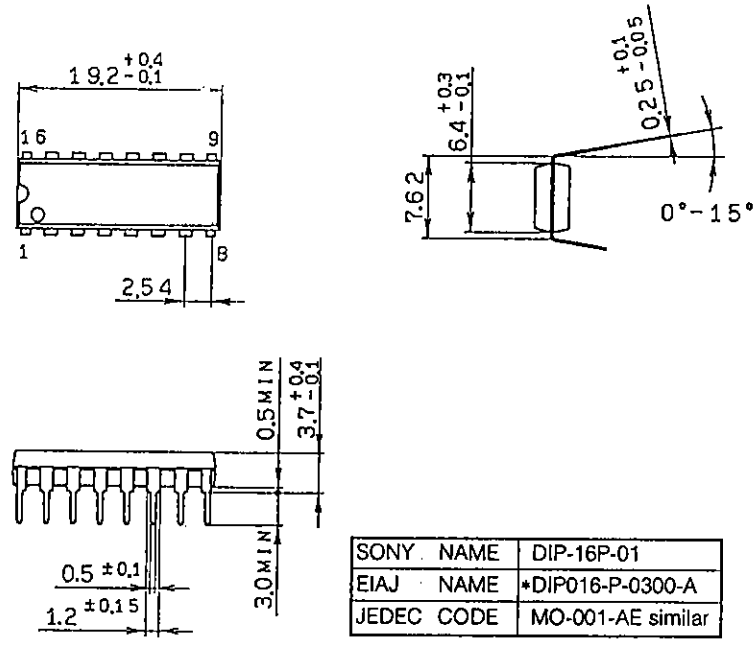
Graph 3. Delay time vs. Control voltage





Package Outline Unit : mm

16pin DIP (Plastic) 300mil 1.0g



SONY	NAME	DIP-16P-01
EIAJ	NAME	*DIP016-P-0300-A
JEDEC	CODE	MO-001-AE similar

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