

VCR Image I/O Signal Processing

**Description**

CXA1201 is an IC developed for the VIDEO, AGC, and IN/OUT processes of the VCR. A combination with CXA1200 permits consistent Y/C main signal processing with a 8 mm video.

**Features**

- Single power supply operation 5V.
- Reduced external parts by containing the AGC time constant.
- Accommodation to BUS LINE.
- Compatible to any VCR format.

**Functions**

- INPUT-Select-SW
- VIDEO-AGC AMP
- SYNC SEPARATOR
- DDS (Y singal superimpose circuit)
- JOG and PCM after-recording applicable.
- VIDEO output buffer
- 75Ω VIDEO-OUT driver
- AGC OFF 2dB Amplifier
- BUS LINE input and serial data output.
- 4.2V built-in regulator

**Structure**

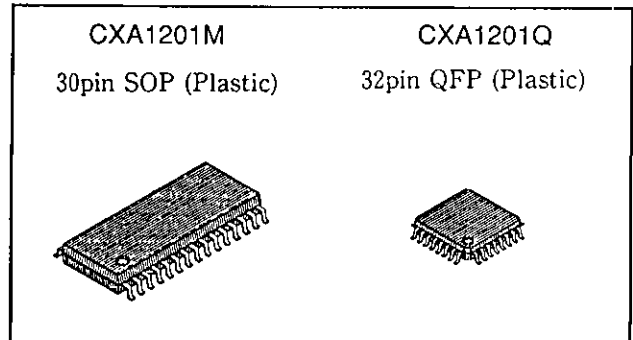
Bipolar silicon monolithic IC

**Absolute Maximum Ratings (Ta=25°C)**

• Supply voltage	V <sub>cc</sub>	7	V
• Operating temperature	T <sub>opr</sub>	-10 to +75	°C
• Storage temperature	T <sub>stg</sub>	-55 to +150	°C
• Allowable power dissipation (When mounted on the board)	P <sub>d</sub>	930	mW

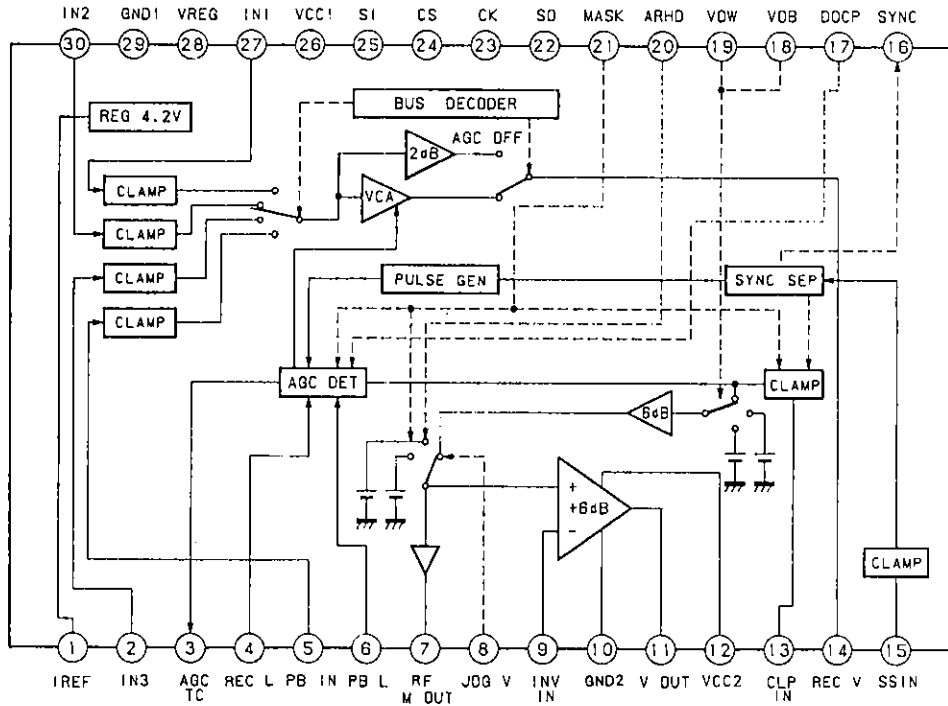
**Recommended Operating Conditions (Ta=25°C)**

• Supply voltage	V <sub>cc</sub>	5 ± 0.25	V
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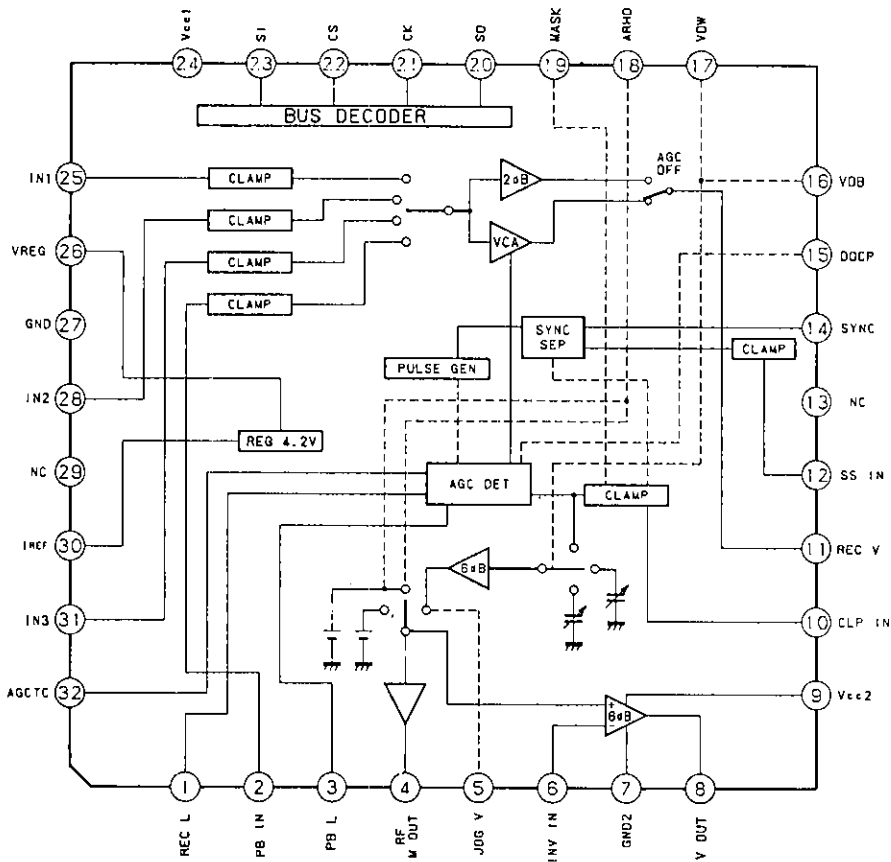


Block Diagram and Pin Configuration

CXA1201M

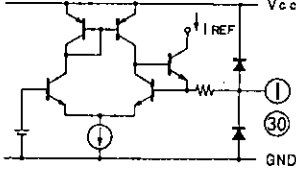
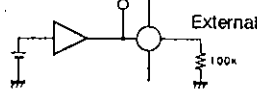
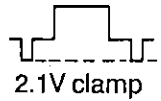
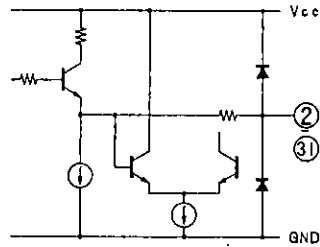
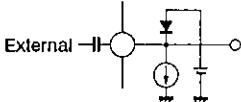
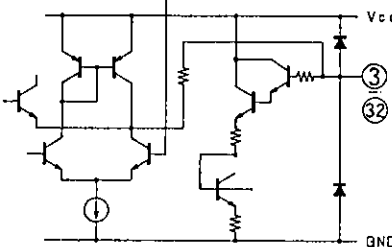
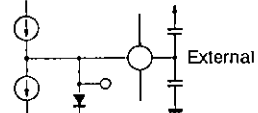
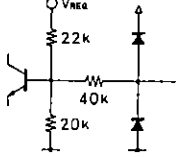
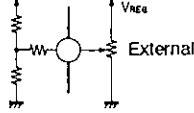
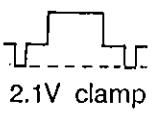
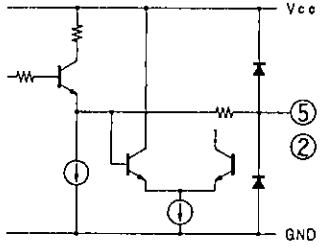
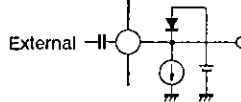
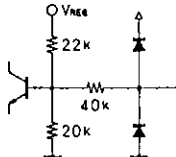
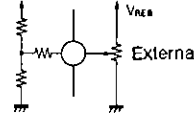


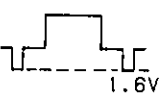
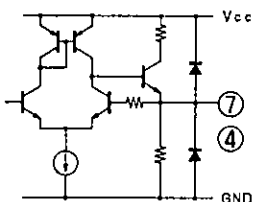
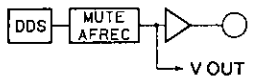
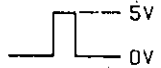
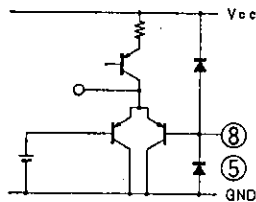
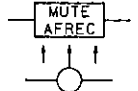
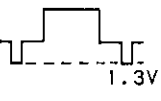
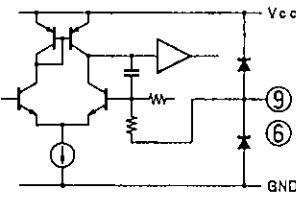
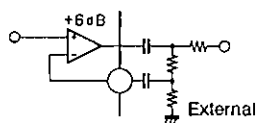

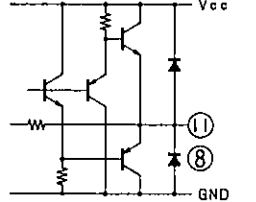
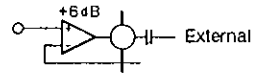
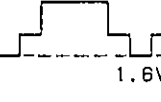
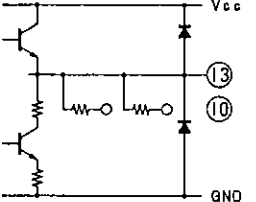
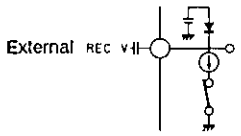
CXA1201Q



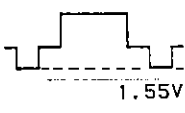
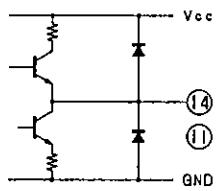
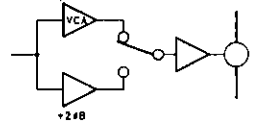
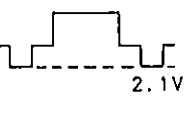
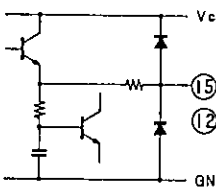
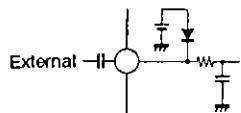
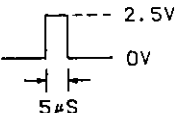
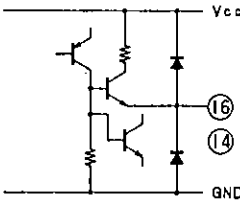
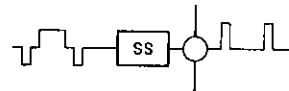
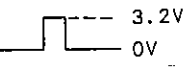
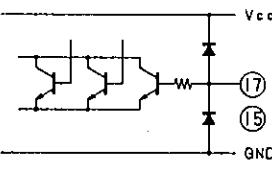
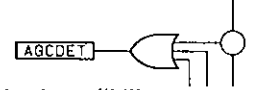
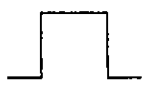
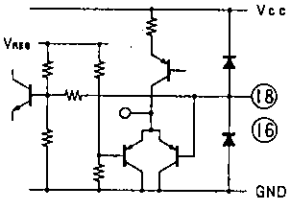
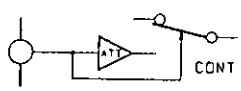
Pin Description

( ) indicates the pin number of CXA1201Q.  
 $V_{CC} = 5V, T_a = 25^\circ C$

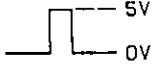
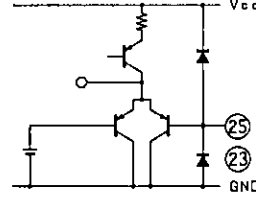
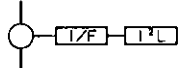

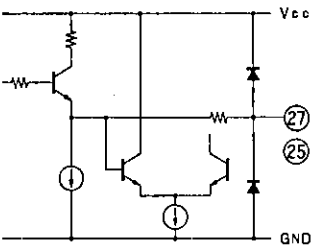
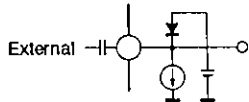
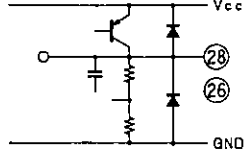

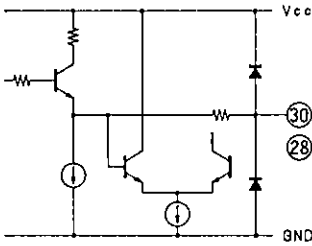
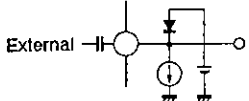
No.	Symbol	Voltage	Equivalent Circuit	Description
1 (30)	IREF	2.1V D.C.		1/2 potential of VREG. The internal reference current is made by attaching a resistor externally.
				
2 (31)	IN 3	Video signal input (0.5Vp-p) 		Video signal input pin by diode clamp.
				
3 (32)	AGC TC	Open emitter		AGC time constant pin.
				
4 (1)	REC L	2.0V center		0 dB level adjusting pin for REC.
				
5 (2)	PB IN	Video signal input (0.5Vp-p) 		Video signal input pin by diode clamp (input for PB).
				
6 (3)	PB L	2.0V center		0 dB level adjusting pin for REC (adjustment for PB).
				

No.	Symbol	Voltage	Equivalent Circuit	Description
7 (4)	RF MOUT	Video signal input (1Vp-p)* 		Output pin to RF MOD IC. 
8 (5)	JOG V	Pulse input  (V <sub>TH</sub> : 1.7V)		Pin that inputs the dummy V signal upon playback at a changed speed. 
9 (6)	INV IN	Video signal input (1Vp-p) 		Inversion input pin for V sag calibration of the VIDEO OUT 75Ω driver. 
10 (7)	GND 2	—	—	GND for the VIDEO OUT 75Ω driver.
11 (8)	V OUT	Video signal input (2Vp-p) 		Output pin of the VIDEO OUT 75Ω driver. 
12 (9)	Vcc 2	Apply 5.0V	—	Vcc for the VIDEO OUT 75Ω driver.
13 (10)	CLP IN	Video signal input (0.5Vp-p) 		The RECV output of the video signal is C-coupled, treated with synchroniza- tion clamp, then input to the IC again. 

\*Note) For the 0 dB video Input and AGC ON.  
The same applies to the following.

No.	Symbol	Voltage	Equivalent Circuit	Description
14 (11)	RECV	Video signal input (1Vp-p) 		REC VIDEO output pin. VCA or 2 dB Amp output. 
15 (12)	SS IN	Video signal input (0.5Vp-p) 		Diode clamp input pin of the SYNCSEP circuit. 
(13)	—	NC	—	—
16 (14)	SYNC	Comp Sync output 		Comp Sync output pin. 
17 (15)	DOCP	Pulse input  $(V_{TH}: 2.1V)$		AGC DET hold draw control pulse input pin.  Inhibited at "H"
18 (16)	VOB	Pulse input 		Input of the DDS background level and SW pulse. 

No.	Symbol	Voltage	Equivalent Circuit	Description
19 (17)	VOW	Pulse Input 		Input of the DDS character level and SW pulse.
20 (18)	ARHD	Pulse Input  $(V_{TH}: 2.7V)$		PCM after recording area HD pulse input pin.
21 (19)	MASK	Pulse Input  $(V_{TH}: 1.7V)$		PCM after recording mask pulse input pin.
22 (20)	SO	Pulse input 		Mode switching logic pulse output pin.
23 (21)	CK	Pulse Input 		Mode switching logic pulse input pin (clock).
24 (22)	CS	Pulse Input 		Mode switching logic pulse input pin (chip select).

No.	Symbol	Voltage	Equivalent Circuit	Description
25 (23)	SI	Pulse Input 		Mode switching logic pulse input pin (serial in). 
26 (24)	Vcc 1	Apply 5.0V	—	Vcc other than VIDEO OUT.
27 (25)	IN 1	Video signal input (0.5Vp-p)  2.1V clamp		Video signal input pin by diode clamp. 
28 (26)	VREG	4.2V		Built-in voltage regulator output pin.
29 (27)	GND 1	—	—	GND other than VIDEO OUT.
30 (28)	IN 2	Video signal input (0.5Vp-p)  2.1V clamp		Video signal input pin by diode clamp. 
(29)	—	NC	—	—

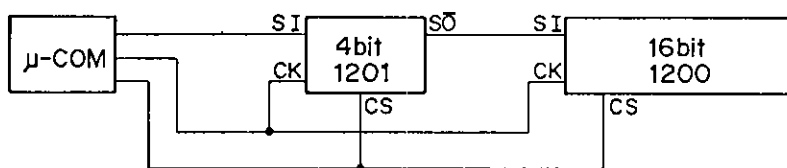
## Electrical Characteristics

(Vcc = 5V, Ta = 25°C)

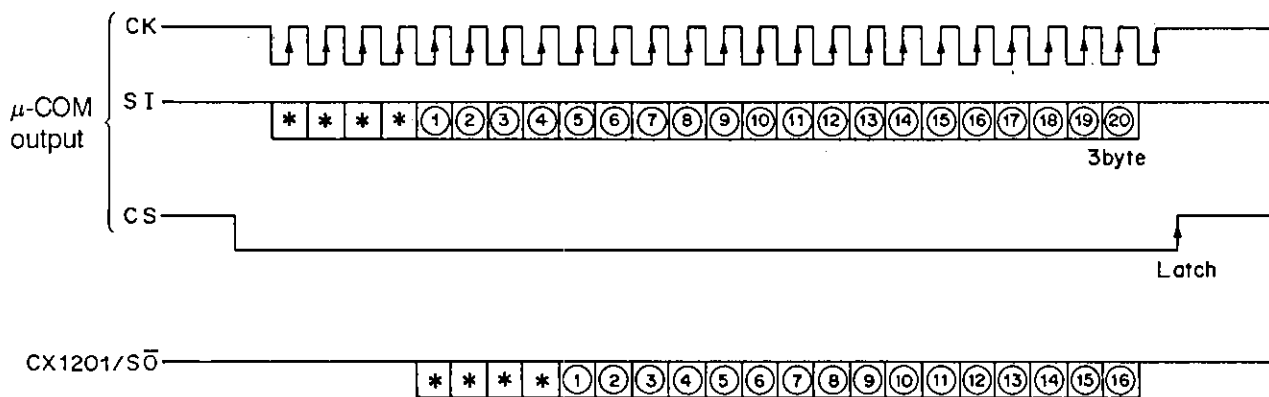
Test item	Symbol	Conditions	Test point	Min.	Typ.	Max.	Unit
Current consumption	Icc	For 0 dB Y signal input	12+26	16	23	30	mA
REMOUT frequency characteristic 5M/500K	Ro-f	A 357m Vp-p Sin wave is put on the Input SYNC 0 dB 50% white signal	7	-1.5		1.0	dB
V out frequency characteristic 5M/500K	Vo-f	A 357m Vp-p Sin wave is put on the Input SYNC 0 dB 50% white signal	11	-1.5		1.0	dB
Sync AGC Input small level	AGC-L	Input SYNC-6 dB all black signal	14		143		mVp-p
Sync AGC Input large level	AGC-H	Input SYNC+6 dB	14		143		mVp-p
Peak AGC operation	AGC-P	Input SYNC-6dB 100% white all sections	14		535		mVp-p
DDS 6 dB amplifier gain	DDS+6	Input SYNC 0 dB 100% white all sections	7	5.5		6.4	dB
Input-Vout amplifier gain	Vo+6	Input SYNC 0 dB 100% white all sections	11	11.2		12.6	dB
AGC OFF mode amplifier gain	AGC OFF	Input SYNC 0 dB 100% white all sections	14		2		dB
SYNC SEP output LO	SS-L	Input SYNC 0 dB all black	16			0.4	V
SYNC SEP output HI	SS-H	Input SYNC 0 dB all black	16	2.3			V
SYNC SEP output delay	SS-D	Input SYNC 0 dB all black	16			0.7	μs
SYNC SEP output pulse width	SS-W	Input SYNC 0 dB all black	16		5		μs
SYNC SEP operation upper limit	SS-O	Input SYNC 0 dB all black	14			+6	dB
SYNC SEP operation lower limit	SS-U	Input SYNC 0 dB all black	14	-6			dB
SI, CK, CS Input LO level	LIN-L	Input CMOS drive				1.8	V
SI, CK, CS Input HI level	LIN-H	Input CMOS drive		2.4			V
SO output LO level	SO-L	No load	22			1.8	V
SO output HI level	SO-H	No load	22	2.4			V
CK-SO delay	CK-SO	No load		150		850	ns
VREG D.C.	VREG	Load 25kΩ	28	4.04		4.32	V
IREF D.C.	V-IREF	Load 100kΩ	1	2.02		2.16	V
REMOUT SYNC DC	VRS	For SYNC 0 dB	7	1450	1600	1750	mV

Test item	Symbol	Conditions	Test point	Min.	Typ.	Max.	Unit
VOB black level	VOB-B	DC difference with NTSC VOB=2.5V	7		250		mV
VOB gray level	VOB-G	DC difference with NTSC BOB=5.0V	7		650		mV
VOW gray level	VOW-G	DC difference with NTSC VOW=2.5V	7		570		mV
VOW white level	VOW-W	DC difference with NTSC VOW=5.0V	7		970		mV
MASK ON RFM output	MASK	DC difference with NTSC MASK=4.0V	7		250		mV
MASK ON + ARHD ON RFM output	ARMD	DC difference with NTSC MASK=4.0V ARHD=4.0V	7	-60		+60	mV
JOGV ON RFM output	JOGV	DC difference with NTSC JOGV=4.0V	7	-60		+60	mV

CXA1200 and 1201 Connection Diagram

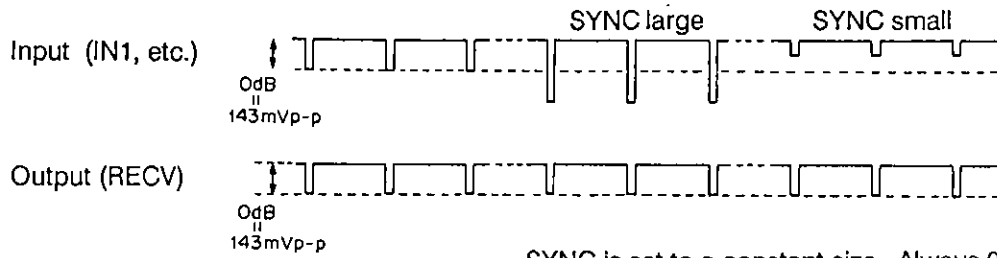


Timing Chart



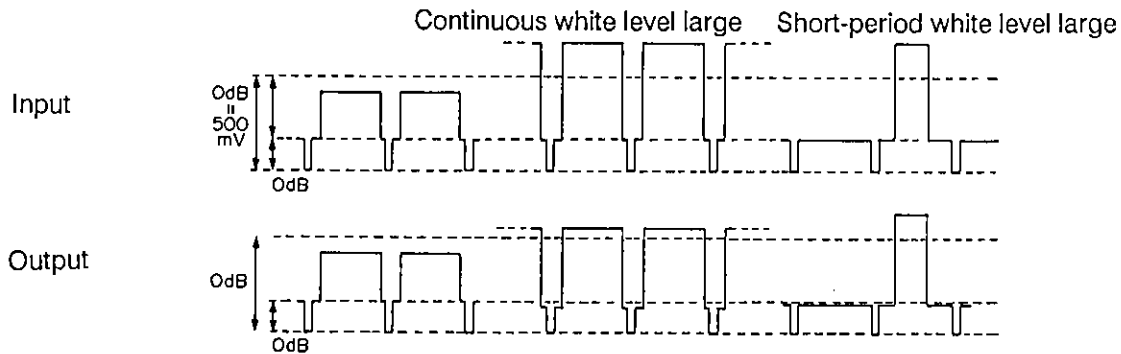
CXA1201 SYNC & PEAK AGC Operation Chart

1) SYNC AGC



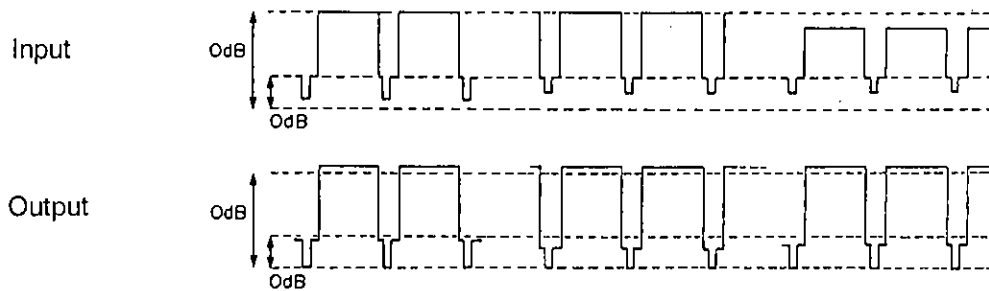
SYNC is set to a constant size. Always 0 dB within the cover range.

2) PEAK AGC



The p-p value of SYNC-white level is set to a constant or smaller value.  
The AGC operation is low if the white level large period is short.

3) SYNC & PEAK AGC

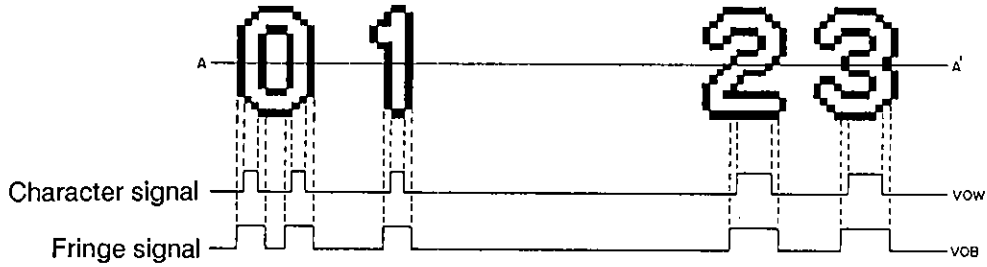


The PEAK AGC operation is higher.

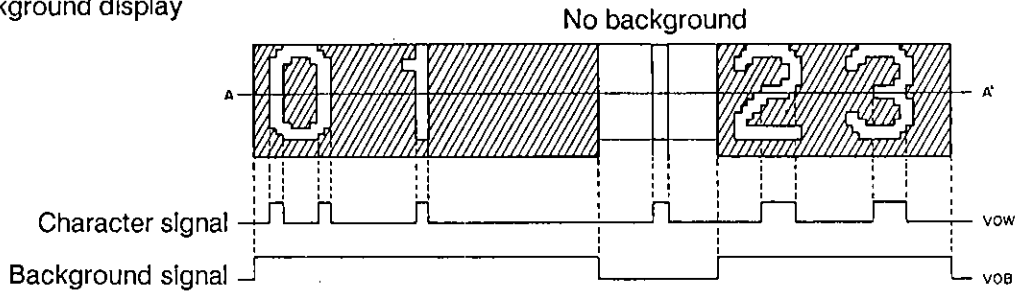
When the SYNC shrinking Y signal comes in, SYNC AGC tries to elongate.  
However, PEAK AGC works stronger and suppresses to a certain level.

Y Signal Superimpose Circuit

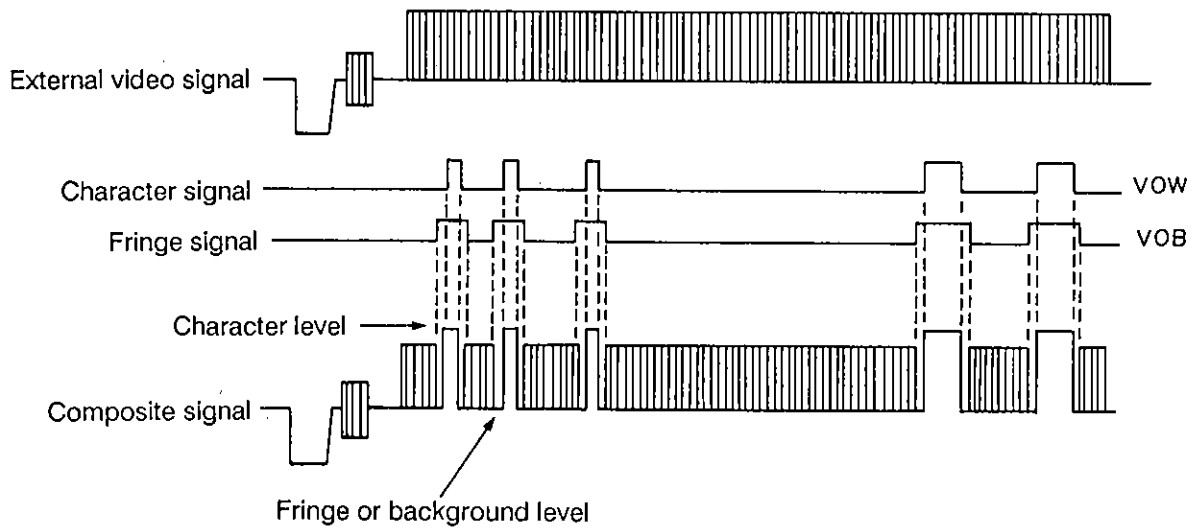
(a) Fringed display



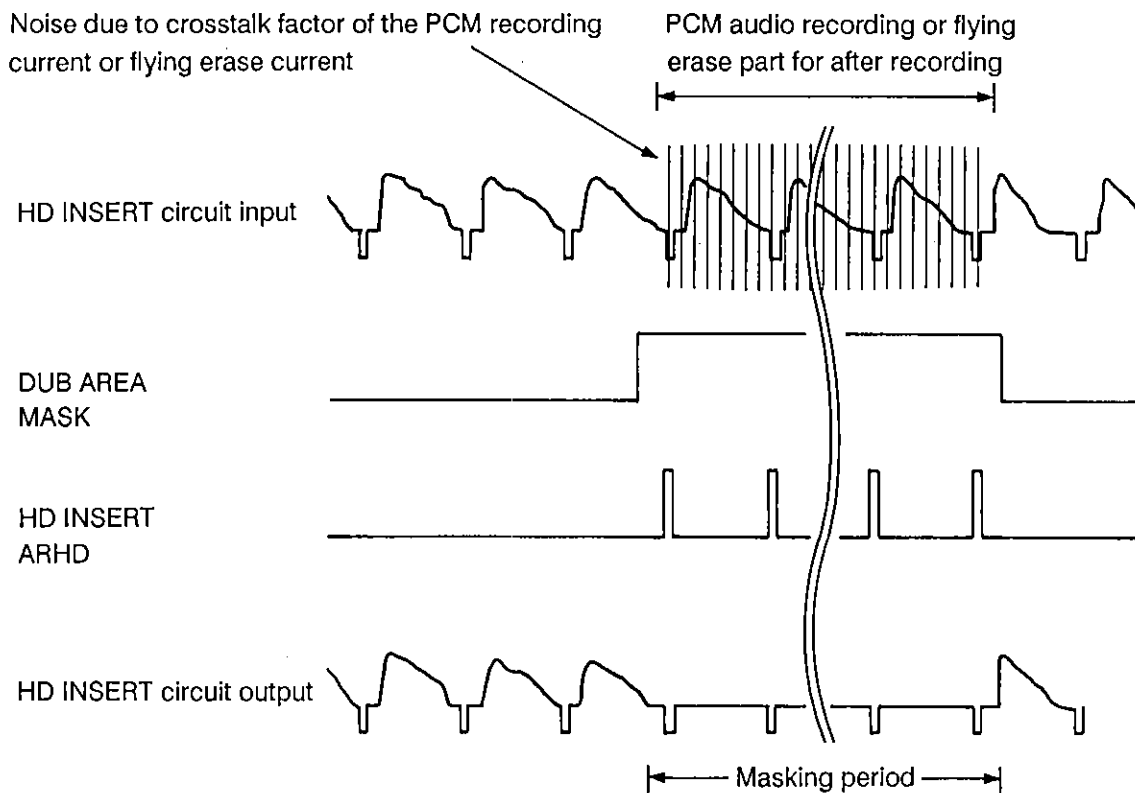
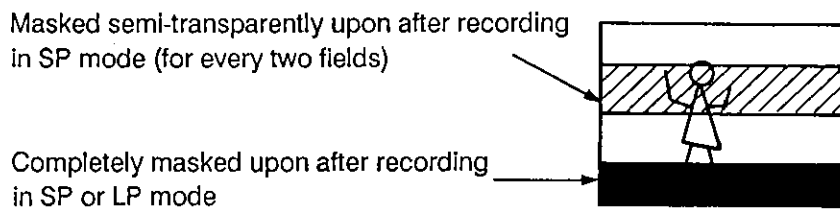
(b) Background display



Timing of the character signal, fringe signal, and background signal



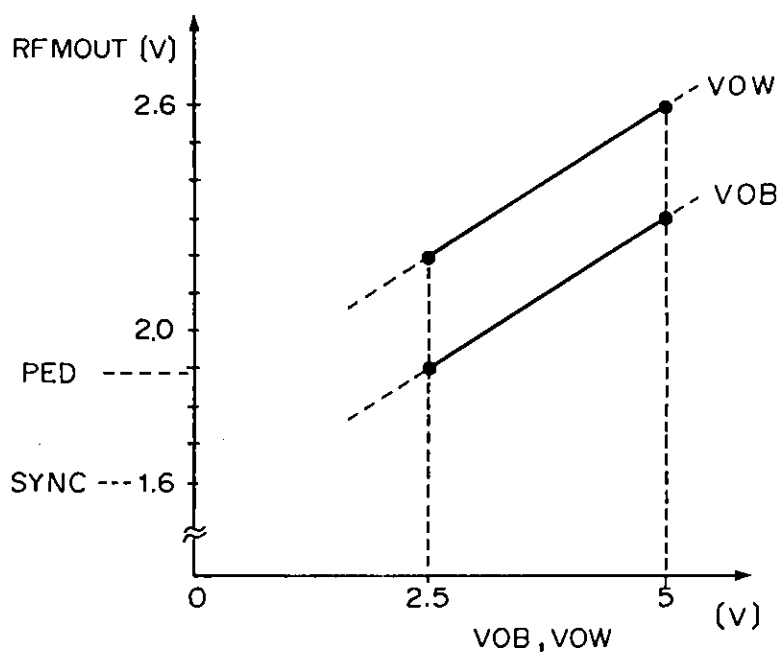
Operation for PCM after recording



CXA1201 DDS and JOG PCM Logic Chart

Input						Output	
MUTE	JOGVD	MASK	ARHD	VOB	VOW		
H	*	*	*	*	*	PED	1.9V
L	H	*	*	*	*	SYNC	1.6V
L	L	H	L	*	*	PED	1.9V
L	L	H	H	*	*	SYNC	1.6V
L	L	L	*	M	L	BLACK	1.9V
L	L	L	*	H	L	GRAY	2.3V
L	L	L	*	*	M	GRAY	2.2V
L	L	L	*	*	H	WHITE	2.6V
L	L	L	*	L	L	NORMAL	

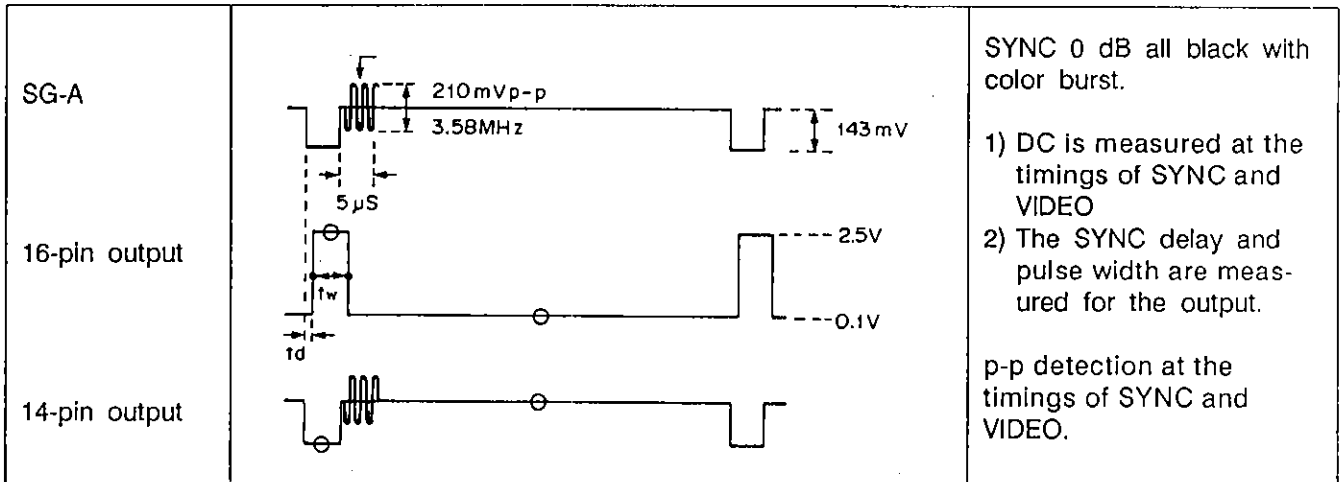
VOB and VOW I/O Chart



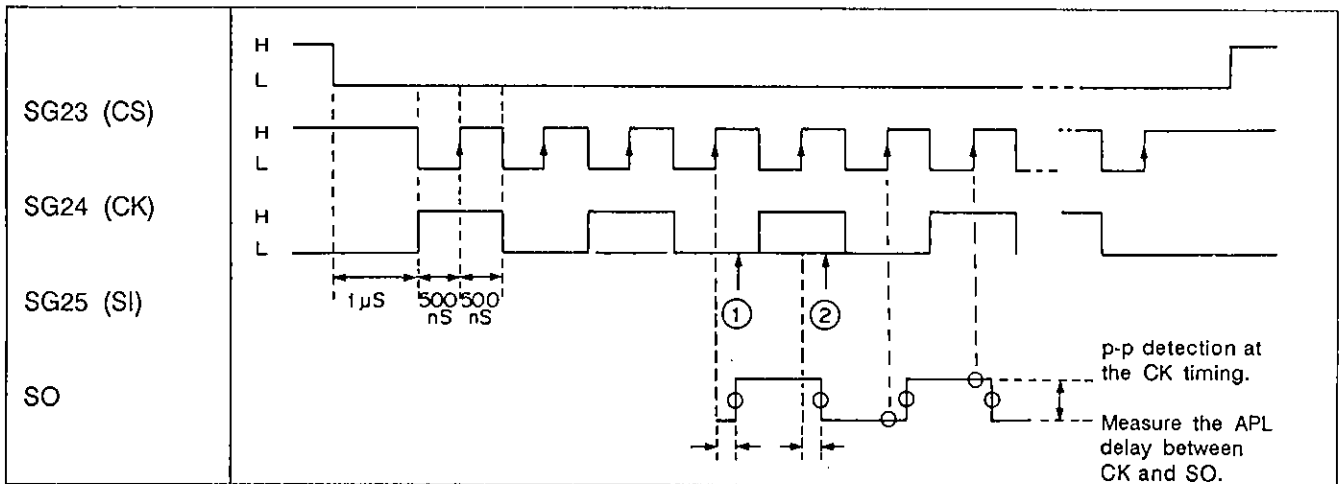
Y Signal Test Method

<p>Frequency characteristics measurement</p> <p>SG14</p>		<p>The sin wave is put on 50% white. The frequency is 500kHz and 5MHz.</p>
<p>SYNC AGL</p> <p>SG-A</p> <p>14-pin output</p>		<p>SYNC+6dB</p> <p>p-p detection at SYNC and VIDEO timings</p>
<p>Peak AGL</p> <p>SG-A</p>		<p>SYNC-6dB</p> <p>p-p detection of the 100% white all field output</p>
<p>GAIN measurement</p> <p>SG-A</p> <p>14-pin</p>		<p>NTSC standard Y signal 500mVp-p SYNC 0dB 100% white</p> <p>DC is measured at the SYNC and VIDEO timings, and the difference is specified.</p>

SYNC SEP Test Method



Serial data I/O Test Method

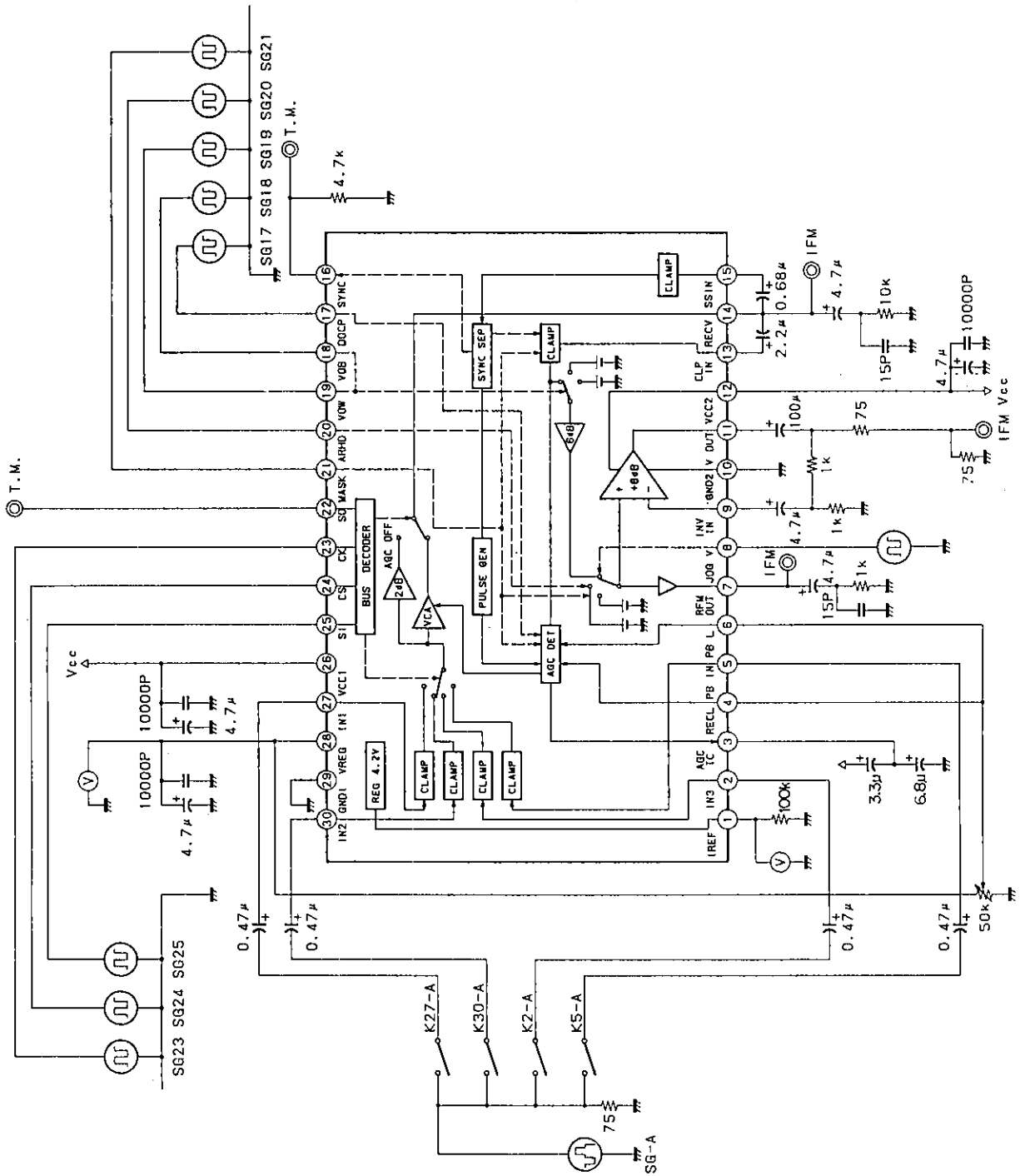


Serial Data Input Example

(H & L of CMOS are used.)

<p>SG23 SG24 SG25</p>		<p>IN1, AGC ON, MUTE OFF Each timing and cycle are same as in the serial data I/O test method.</p>
<p>SG23 SG24 SG25</p>		<p>IN2, AGC ON, MUTE OFF</p>
<p>SG23 SG24 SG25</p>		<p>IN3, AGC ON, MUTE OFF</p>
<p>SG23 SG24 SG25</p>		<p>PBIN, AGC ON, MUTE OFF</p>
<p>SG23 SG24 SG25</p>		<p>IN1, AGC ON, MUTE ON</p>
<p>SG23 SG24 SG25</p>		<p>IN1, AGC OFF, MUTE OFF</p>

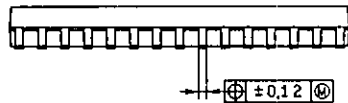
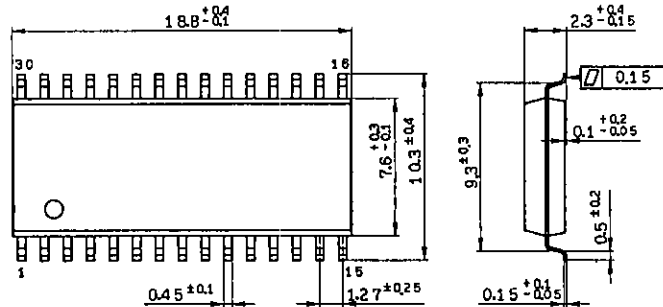
Electrical Characteristics Test Circuit (CXA1201M)



Package Outline Unit:mm

CXA1201M

30pin SOP (Plastic) 375mil 0.7g

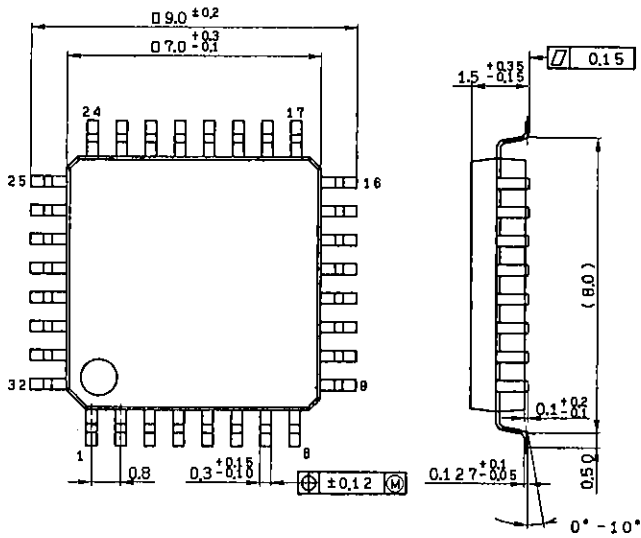


SONY NAME	SOP-30P-L01
EIAJ NAME	*SOP030-P-0375-A
JEDEC CODE	

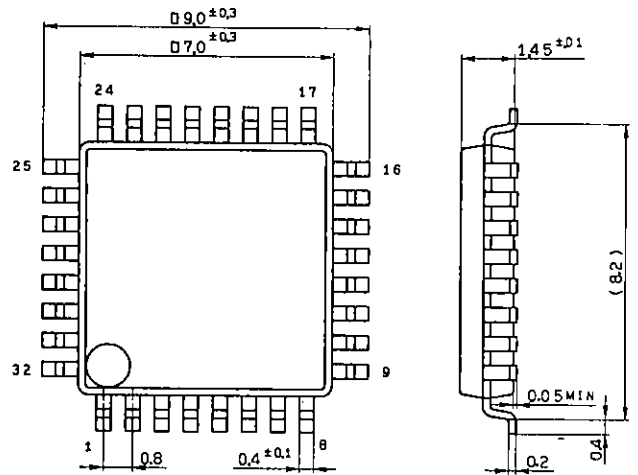
CXA1201Q

32pin QFP (Plastic) 0.2g

32pin QFP (Plastic) 0.2g



SONY NAME	QFP-32P-L01
EIAJ NAME	*QFP032-P-0707-A
JEDEC CODE	



SONY NAME	QFP-32P-L0B1
EIAJ NAME	*QFP032-P-0707-AR
JEDEC CODE	

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