

Comlinear CLC415

Quad, Wideband Monolithic Op Amp

General Description

The CLC415 is a wideband, quad, monolithic operational amplifier designed for intermediate-gain applications where power and cost per channel are of primary concern. Benefiting from Comlinear's current feedback architecture, the CLC415 offers a gain range of ± 1 to ± 10 while providing stable, oscillation-free operation without external compensation, even at unity gain.

Operating from $\pm 5V$ supplies, the CLC415 consumes only 50mW of power per channel, yet maintains a 160MHz small-signal bandwidth and a 1500V/ μs slew rate. High density applications requiring an integrated solution will enjoy the CLC415's 70dB channel isolation (input referred @ 5MHz).

With its exceptional differential gain and phase, typically 0.03% and 0.03° @ 3.58MHz, the CLC415 is designed to meet the performance and cost per channel requirements of high volume composite video applications. The CLC415's large-signal bandwidth, high slew rate and high drive capability are features well suited for RGB-video applications.

The CLC415 is a quad version of the high speed CLC406 while the CLC414 is a lower power quad version of the same. Both of these quads afford the designer lower power consumption and lower cost per channel with the additional benefit of requiring less board space per amplifier.

Constructed using an advanced, complementary bipolar process and Comlinear's proven current feedback architectures, the CLC415 is available in several versions to meet a variety of requirements.

CLC415AJP	-40°C to +85°C	14-pin plastic DIP
CLC415AJE	-40°C to +85°C	14-pin plastic SOIC
CLC415ALC	-40°C to +85°C	dice
CLC415AMC	-55°C to +125°C	dice qualified to Method 5008, MIL-STD-883, Level B
CLC415A8B	-55°C to +125°C	14-pin hermetic CERDIP, MIL-STD-883, Level B
CLC415A8D	-55°C to +125°C	14-pin sidebraced CERDIP, MIL-STD-883, Level B

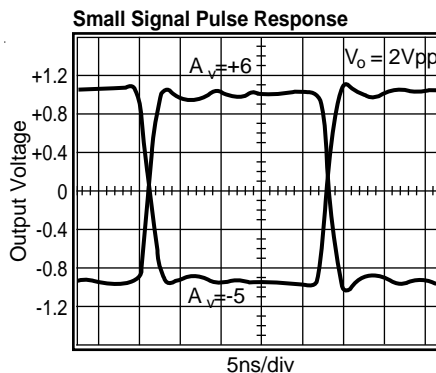
DESC SMD number: 5962-90994

Features

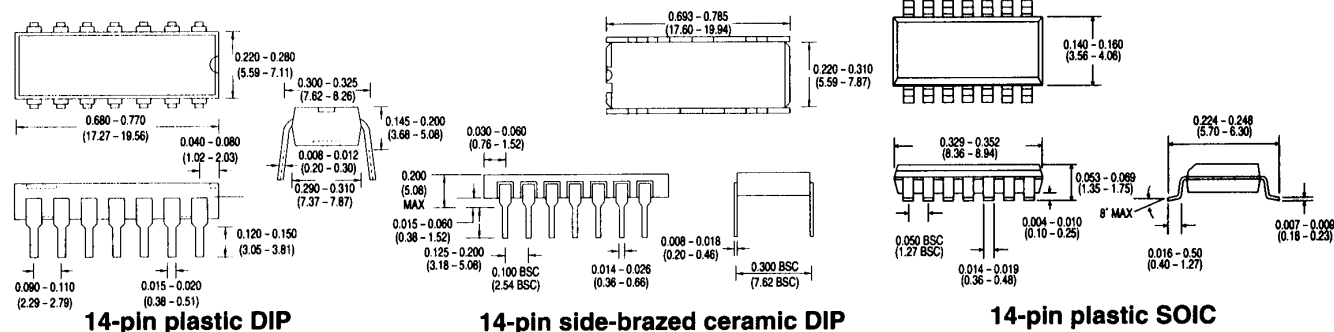
- 160MHz small signal bandwidth
- 0.05% settling in 12ns
- Low power, 160mW (40mW disabled)
- Low distortion, -60dBc at 20MHz
- Fast disable (200ns)
- Differential gain/phase: 0.01%/0.01°
- ± 1 to ± 8 closed-loop gain range

Applications

- Video switching and distribution
- Analog bus driving (with disable)
- Low power "standby" using disable
- Fast, precision A/D conversion
- D/A current-to-voltage conversion
- IF processors
- High-speed communications



Package Dimensions



CLC415 Electrical Characteristics ($A_v = +6$, $V_{cc} = \pm 5V$, $R_L = 100\Omega$, $R_f = 500\Omega$; unless specified)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS				UNITS	SYMBOL
Ambient Temperature	CLC415AJ/AI	+25°C	-40°C	+25°C	+85°C			
Ambient Temperature	CLC415A8/AL/AM	+25°C	-55°C	+25°C	+125°C			
FREQUENCY DOMAIN RESPONSE								
† -3dB bandwidth	$V_{out} < 2V_{pp}$	160	>120	>120	>90	MHz	SSBW	
	$V_{out} < 5V_{pp}$	120	>85	>90	>80	MHz	LSBW	
gain flatness ¹	$V_{out} < 2V_{pp}$							
† peaking	DC to 25MHz	0	<0.2	<0.2	<0.2	dB	GFPL	
† peaking	>25MHz	0	<0.5	<0.5	<0.5	dB	GFPH	
† rolloff	DC to 50MHz	0.2	<0.7	<0.7	<1.1	dB	GFR	
linear phase deviation	DC to 75MHz	0.5	<1.0	<1.0	<1.3	°	LPD	
differential gain ($A_v = +2$)	150Ω load, 3.58MHz	0.03	<0.08	<0.08	<0.08	%	DG1	
	4.43MHz	0.03	<0.10	<0.10	<0.10	%	DG2	
differential phase ($A_v = +2$)	150Ω load, 3.58MHz	0.03	<0.08	<0.08	<0.08	°	DP1	
	4.43MHz	0.03	<0.10	<0.10	<0.10	°	DP2	
crosstalk input referred	5MHz (all hostile)	65	<60	<60	<59	dB	XT	
input referred	5MHz (chan. to chan.)	70	<63	<63	<62	dB	CXT	
TIME DOMAIN RESPONSE								
rise and fall time	2V step	2.0	<3.0	<3.0	<4.0	ns	TRS	
	5V step	3.0	<4.0	<3.6	<4.5	ns	TRL	
settling time to 0.1%	2V step	12	<18	<18	<22	ns	TS	
overshoot	2V step	8	<12	<12	<12	%	OS	
slew rate		1500	>1200	>1200	>1000	V/μs	SR	
DISTORTION AND NOISE RESPONSE								
†2nd harmonic distortion	$2V_{pp}$, 20MHz	-44	<-38	<-38	<-34	dBc	HD2	
†3rd harmonic distortion	$2V_{pp}$, 20MHz	-54	<-46	<-46	<-42	dBc	HD3	
equivalent noise input								
non-inverting voltage	>1MHz	3.0	<3.6	<3.6	<4.0	nV/√Hz	VN	
inverting current	>1MHz	11.5	<14	<14	<16	pA/√Hz	ICN	
non-inverting current	>1MHz	2.0	<2.6	<2.6	<3.0	pA/√Hz	NCN	
total noise floor	>1MHz	-157	<-155	<-155	<-154	dBm _{1Hz}	SNF	
total integrated noise	>1MHz to 100MHz	37	<44	<44	<48	μV	INV	
STATIC, DC PERFORMANCE								
*input offset voltage		2	<9	<5	<10	mV	VIO	
average temperature coefficient		20	<50	—	<50	μV/°C	DVIO	
*input bias current	non-inverting	5	<25	<13	<13	μA	IBN	
average temperature coefficient		30	<150	—	<50	nA/°C	DIBN	
*input bias current	inverting	3	<18	<10	<15	μA	IBI	
average temperature coefficient		20	<100	—	<50	nA/°C	DIBI	
†power supply rejection ratio		55	>47	>47	>45	dB	PSRR	
common mode rejection ratio		50	>45	>45	>43	dB	CMRR	
*supply current, all channels	no load	20	<27	<26	<24	mA	ICC	
MISCELLANEOUS PERFORMANCE								
non-inverting input resistance		1300	>300	>600	>600	kΩ	RIN	
non-inverting input capacitance		1.0	<2.0	<2.0	<2.0	pF	CIN	
output impedance	DC	0.2	<0.6	<0.3	<0.2	Ω	RO	
output voltage range	$R_L = 100\Omega$	±2.6	±2.3	±2.5	±2.5	V	VO	
common mode input range		±2.2	±1.4	±2.0	±2.0	V	CMIR	
output current		70	50	50	50	mA	IO	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

V_{cc}	±7V
I_{out}	output is short circuit protected to ground, however, maximum reliability is obtained if I_{out} does not exceed... 70mA
common mode input voltage	± V_{cc}
differential input voltage	±10V
maximum junction temperature	+175°C
operating temperature range	
AJ/AI:	-40°C to +85°C
AB/AL/AM:	-55°C to +125°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C

Miscellaneous Ratings

recommended gain range: ±1 to ±10

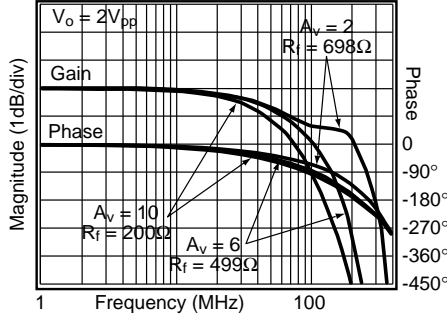
Notes:

- * AJ, AJ 100% tested at +25°C, sample at +85°C.
- † AJ Sample tested at +25°C.
- † AI 100% tested at +25°C.
- * A8 100% tested +25°C, -55°C, +125°C.
- † A8 100% tested +25°C, sample at -55°C, +125°C.
- * AL, AM 100% wafer probed at +25°C to +25°C min/max specifications.

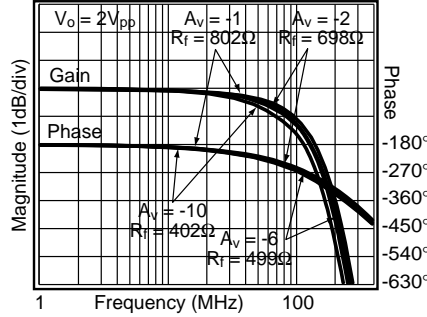
note 1: Gain flatness tests performed from 0.1 MHz

CLC415 Typical Performance Characteristics ($\tau_A = 25^\circ$, $A_V = +6$, $V_{CC} = \pm 5V$, $R_L = 100\Omega$, $R_f = 100\Omega$; unless specified)

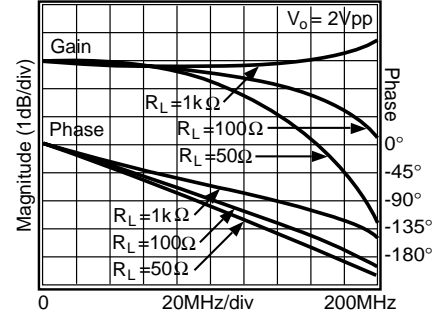
Non-Inverting Frequency Response



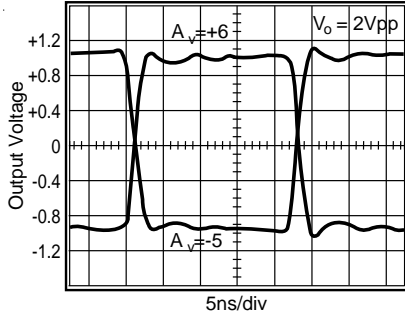
Inverting Frequency Response



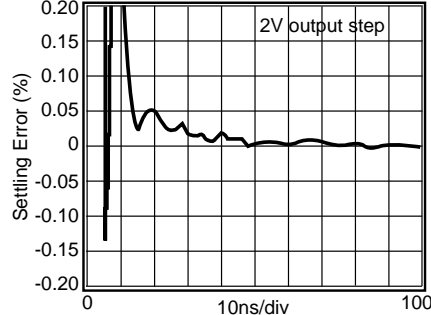
Frequency Response for Various R_L 's



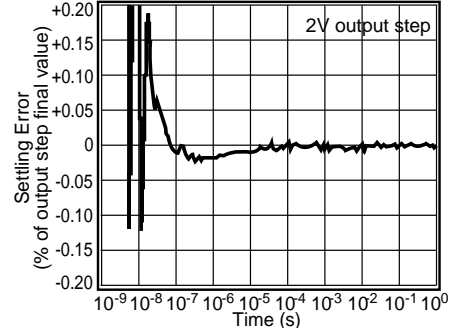
Small Signal Pulse Response



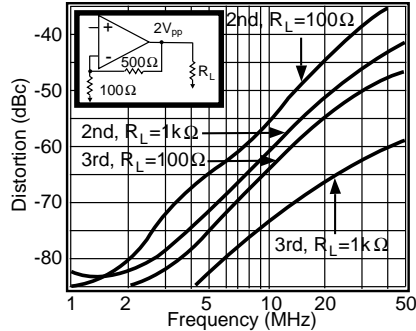
Short-Term Settling Time



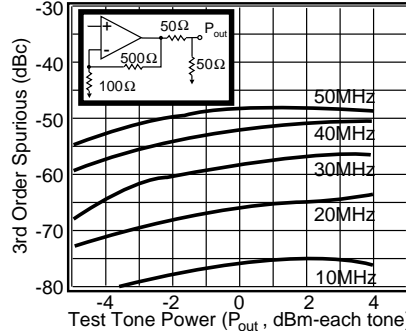
Long-Term Settling Time



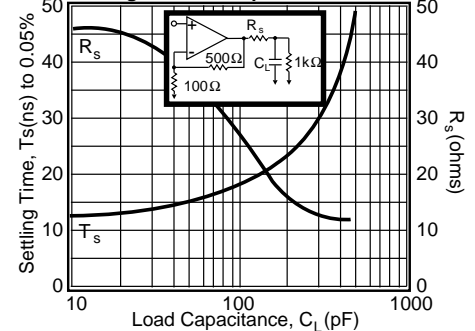
2nd and 3rd Harmonic Distortion



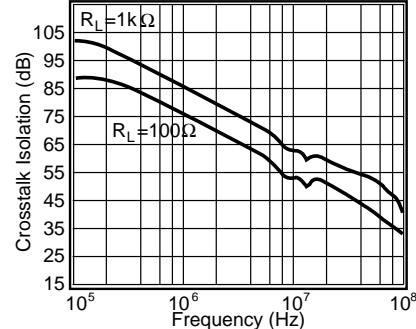
2-Tone, 3rd Order Spurious Levels



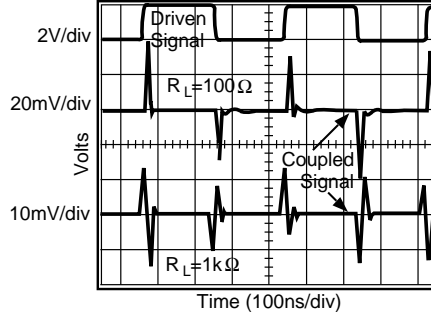
Settling Time vs. Capacitive Load



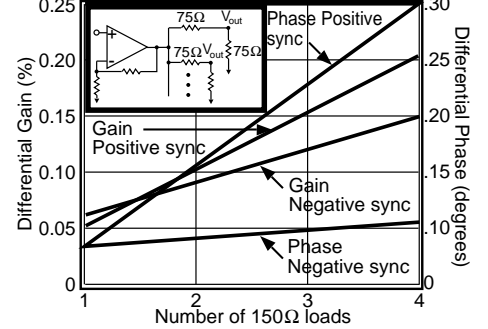
All Hostile Crosstalk Isolation



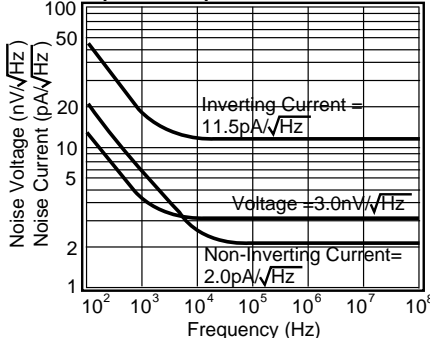
Most Susceptible Channel-Channel Pulse Coupling



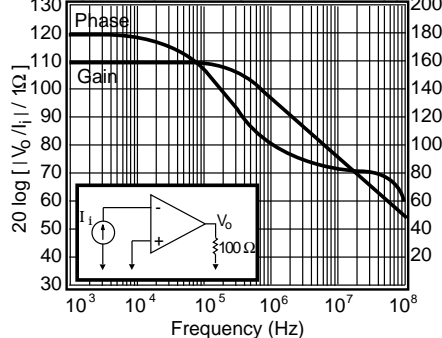
Differential Gain and Phase (4.43 MHz, $A_V = +2$)



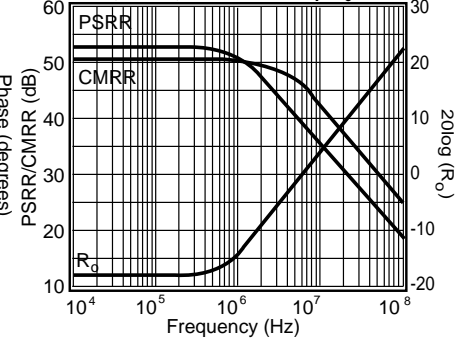
Equivalent Input Noise



Open-Loop Transimpedance Gain, Z(s)



PSRR, CMRR, and Closed Loop R_o



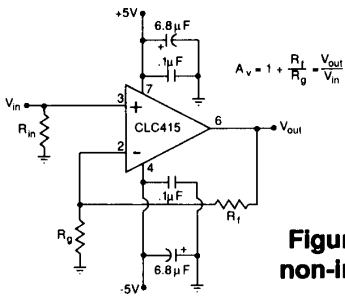
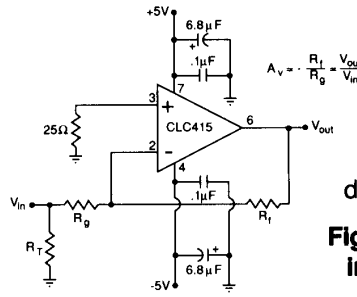


Figure 1: recommended non-inverting gain circuit



Select R_T to yield desired $R_{in} = R_T \parallel R_g$
Figure 2: recommended inverting gain circuit

Feedback Resistor

The CLC415 achieves its exceptional AC performance while requiring very low quiescent power by using the current feedback topology and an internal slew rate enhancement circuit. The loop gain and frequency response for a current feedback op amp is predominantly set by the feedback resistor value. The CLC415 is optimized for a gain of +6 to use a 500Ω feedback resistor (use a 900Ω R_f for maximally flat response at a gain of +2). Using lower values can lead to excessive ringing in the pulse response while a higher value will limit the bandwidth.

Application Note OA-13 provides a more detailed discussion of choosing a feedback resistor. The equations found in this application note are to be considered a starting point for the determination of R_f at any gain. The value of input impedance for the CLC415 is approximately 60Ω. These equations do not account for parasitic capacitance at the inverting input nor across R_f . The plot found below entitled “Recommended R_f vs. Gain” offers values of R_f which will optimize the frequency response of the CLC415 over its ±1 to ±10 gain range. Unlike voltage feedback, current feedback op amps require a non-zero R_f for unity gain followers.

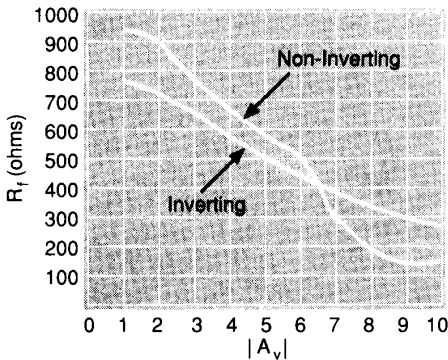


Figure 3: recommended R_f vs. gain

Unused Amplifiers

It is recommended that any unused amplifiers in the quad package be connected as unity gain followers ($R_f = 500\Omega$) with the non-inverting input tied to ground through a 50Ω resistor.

Slew Rate and Harmonic Distortion

Please see the application information for the CLC406.

Differential Gain and Phase

Differential gain and phase performance specifications are common to composite video distribution applications. These specifications refer to the change in small signal gain and phase of the color subcarrier frequency (4.43MHz for PAL composite video) as the amplifier output is swept over a range of DC voltages. Application Note OA-08 provides an additional discussion of differential gain and phase measurements.

Non-inverting Source Impedance

For best operation, the DC source impedance looking out of the non-inverting input should be less than 3kΩ but greater than 20Ω. Parasitic self oscillations may occur in the input transistors if the DC source impedance is out of

this range. This impedance also acts as the gain for the non-inverting input bias and noise currents and therefore can become troublesome for high values of DC source impedance. The inverting configuration of Figure 2 shows a 25Ω resistor to ground on the non-inverting input which insures stability but does not provide bias current cancellation. The input bias currents are unrelated for a current feedback amplifier which eliminates the need for source impedance matching to achieve bias current cancellation.

DC Accuracy and Noise

Please refer to the application information section of the CLC406 for a discussion of output offset voltage and spot noise calculation.

Crosstalk

In any multi-channel integrated circuit there is an undesirable tendency for the signal in one channel to couple with and reproduce itself in the output of another channel. This effect is referred to as crosstalk. Crosstalk is expressed as channel separation or channel isolation which indicates the magnitude of this undesirable effect. This effect is measured by driving one or more channels and observing the output of the other undriven channel(s). The CLC415 plot page offers two different graphs detailing the effect of crosstalk over frequency. One plot entitled “All-Hostile Crosstalk Isolation” graphs all-hostile, input-referred crosstalk. All-hostile crosstalk refers to the condition where three channels are driven simultaneously while observing the output of the undriven fourth channel. Input-referred implies that crosstalk is directly affected by gain and therefore a higher gain increases the crosstalk effect by a factor equal to that gain setting. The plot entitled “Most Susceptible Channel-to-Channel Pulse Coupling” describes the effect of crosstalk when one channel is driven with a 2V_{pp} pulse while the output of the most effected channel is observed.

Printed Circuit Layout

As with any high speed component, a careful attention to the board layout is necessary for optimum performance. Of particular importance is the careful control of parasitic capacitances on the output pin. As the output impedance plot shows, the closed loop output for the CLC415 eventually becomes inductive as the loop gain rolls off with increasing frequency. Direct capacitive loading on the output pin can quickly lead to peaking in the frequency response, overshoot in the pulse response, ringing or even sustained oscillations. The “Settling Time vs. Capacitive Load” plot should be used as a starting point for the selection of a series output resistor when a capacitive load must be driven. A quad amplifier will require careful attention to signal routing in order to minimize the effects of crosstalk. Signal coupling through the power supplies can be reduced with bypass capacitors placed close to the device supply pins.

Evaluation Board

Evaluation PC boards (part number 730024 for through-hole and 730031 for SOIC) for the CLC415 are available.

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