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POwer SEMiconductors Italian COrporation

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## PHASE CONTROL THYRISTOR

# AT405

Repetitive voltage up to **1200 V**  
Mean on-state current **305 A**  
Surge current **2.8 kA**

### FINAL SPECIFICATION

gen 03 - ISSUE : 05

| Symbol               | Characteristic                                   | Conditions                                   | T <sub>j</sub><br>[°C] | Value     | Unit             |
|----------------------|--|--|------------------------|-----------|------------------|
| <b>BLOCKING</b>      |  |  |                        |           |                  |
| V <sub>RRM</sub>     | Repetitive peak reverse voltage                  |  | 125                    | 1200      | V                |
| V <sub>RSM</sub>     | Non-repetitive peak reverse voltage              |  | 125                    | 1300      | V                |
| V <sub>DRM</sub>     | Repetitive peak off-state voltage                |  | 125                    | 1200      | V                |
| I <sub>RRM</sub>     | Repetitive peak reverse current                  | V=VRRM                                       | 125                    | 30        | mA               |
| I <sub>DRM</sub>     | Repetitive peak off-state current                | V=VDRM                                       | 125                    | 30        | mA               |
| <b>CONDUCTING</b>    |  |  |                        |           |                  |
| I <sub>T(AV)</sub>   | Mean on-state current                            | 180° sin, 50 Hz, Th=55°C, double side cooled |                        | 305       | A                |
| I <sub>T(AV)</sub>   | Mean on-state current                            | 180° sin, 50 Hz, Tc=85°C, double side cooled |                        | 245       | A                |
| I <sub>TSM</sub>     | Surge on-state current                           | sine wave, 10 ms                             | 125                    | 2.8       | kA               |
| I <sup>2</sup> t     | I <sup>2</sup> t                                 | without reverse voltage                      |                        | 39 x1E3   | A <sup>2</sup> s |
| V <sub>T</sub>       | On-state voltage                                 | On-state current = 600 A                     | 25                     | 1.88      | V                |
| V <sub>T(TO)</sub>   | Threshold voltage                                |  | 125                    | 1.0       | V                |
| r <sub>T</sub>       | On-state slope resistance                        |  | 125                    | 1.900     | mohm             |
| <b>SWITCHING</b>     |  |  |                        |           |                  |
| di/dt                | Critical rate of rise of on-state current, min.  | From 75% VDRM up to 300 A, gate 10V 5ohm     | 125                    | 200       | A/μs             |
| dv/dt                | Critical rate of rise of off-state voltage, min. | Linear ramp up to 70% of VDRM                | 125                    | 500       | V/μs             |
| t <sub>d</sub>       | Gate controlled delay time, typical              | VD=100V, gate source 10V, 10 ohm, tr=.5 μs   | 25                     | 0.7       | μs               |
| t <sub>q</sub>       | Circuit commutated turn-off time, typical        | dV/dt = 20 V/μs linear up to 75% VDRM        |                        | 200       | μs               |
| Q <sub>rr</sub>      | Reverse recovery charge                          | di/dt=-20 A/μs, I <sub>r</sub> = 195 A       | 125                    |           | μC               |
| I <sub>rr</sub>      | Peak reverse recovery current                    | VR= 50 V                                     |                        |           | A                |
| I <sub>H</sub>       | Holding current, typical                         | VD=5V, gate open circuit                     | 25                     | 300       | mA               |
| I <sub>L</sub>       | Latching current, typical                        | VD=5V, tp=30μs                               | 25                     | 700       | mA               |
| <b>GATE</b>          |  |  |                        |           |                  |
| V <sub>GT</sub>      | Gate trigger voltage                             | VD=5V  | 25                     | 3.5       | V                |
| I <sub>GT</sub>      | Gate trigger current                             | VD=5V  | 25                     | 200       | mA               |
| V <sub>GD</sub>      | Non-trigger gate voltage, min.                   | VD=VDRM                                      | 125                    | 0.25      | V                |
| V <sub>FGM</sub>     | Peak gate voltage (forward)                      |  |                        | 20        | V                |
| I <sub>FGM</sub>     | Peak gate current                                |  |                        | 8         | A                |
| V <sub>RGM</sub>     | Peak gate voltage (reverse)                      |  |                        | 5         | V                |
| P <sub>GM</sub>      | Peak gate power dissipation                      | Pulse width 100 μs                           |                        | 75        | W                |
| P <sub>G</sub>       | Average gate power dissipation                   |  |                        | 1         | W                |
| <b>MOUNTING</b>      |  |  |                        |           |                  |
| R <sub>th(j-h)</sub> | Thermal impedance, DC                            | Junction to heatsink, double side cooled     |                        | 95        | °C/kW            |
| R <sub>th(c-h)</sub> | Thermal impedance                                | Case to heatsink, double side cooled         |                        | 20        | °C/kW            |
| T <sub>j</sub>       | Operating junction temperature                   |  |                        | -30 / 125 | °C               |
| F                    | Mounting force                                   |  |                        | 4.9 / 5.9 | kN               |
|                      | Mass   |  |                        | 55        | g                |

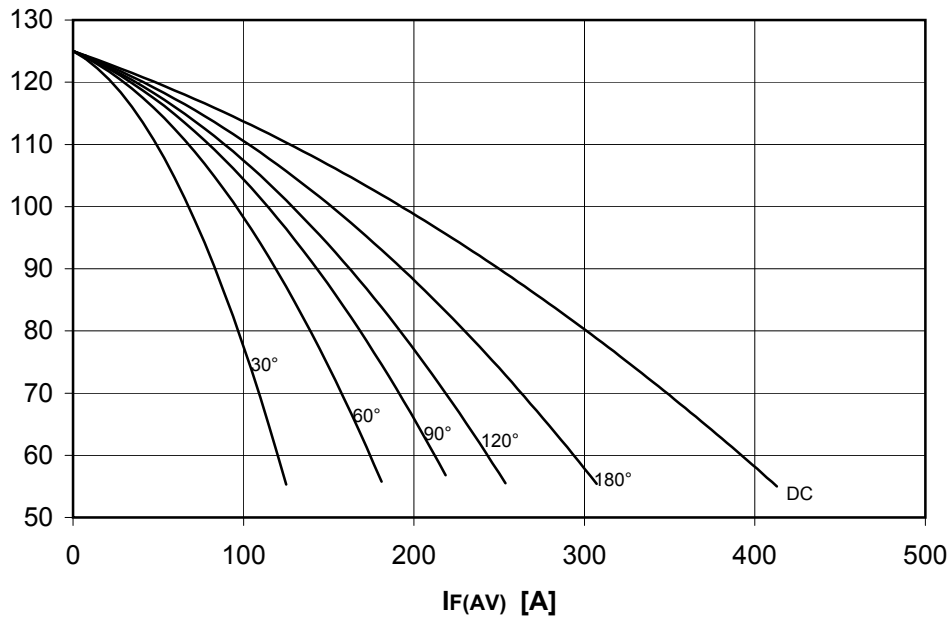
### ORDERING INFORMATION : AT405 S 12

standard specification   VDRM&VRRM/100

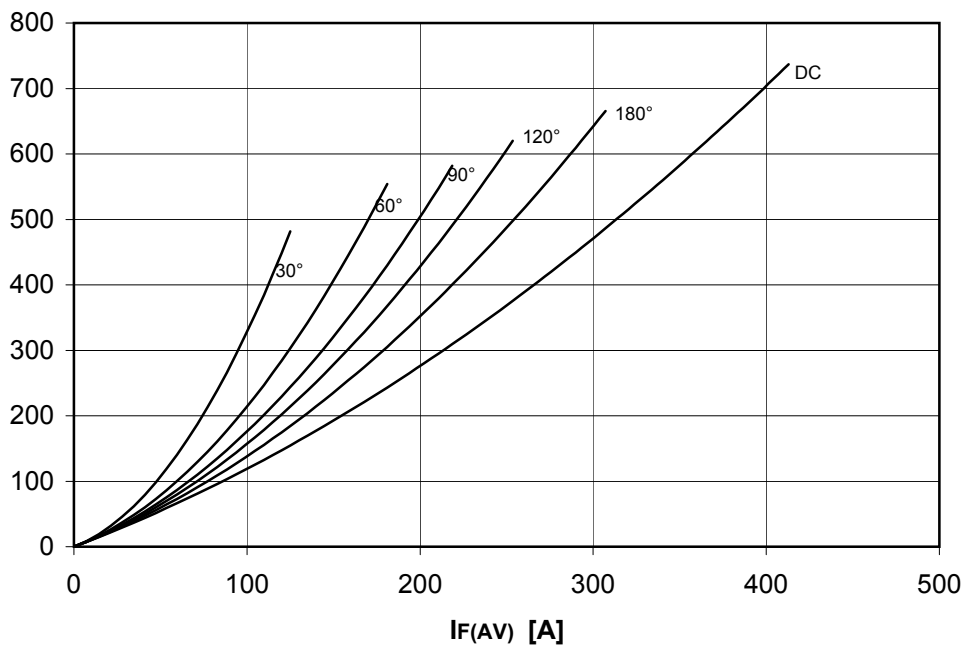
## DISSIPATION CHARACTERISTICS

SQUARE WAVE

Th [°C]



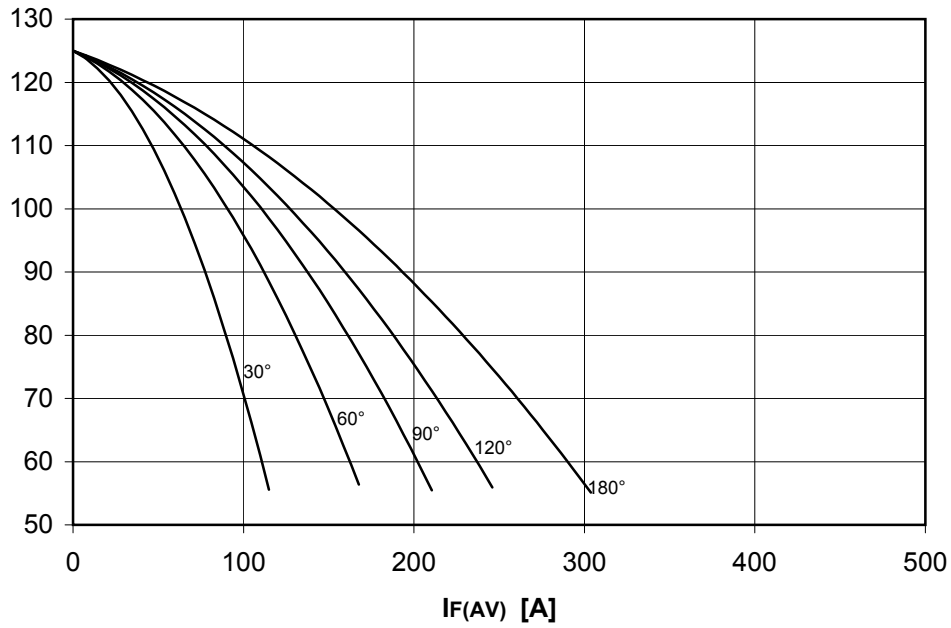
PF(AV) [W]



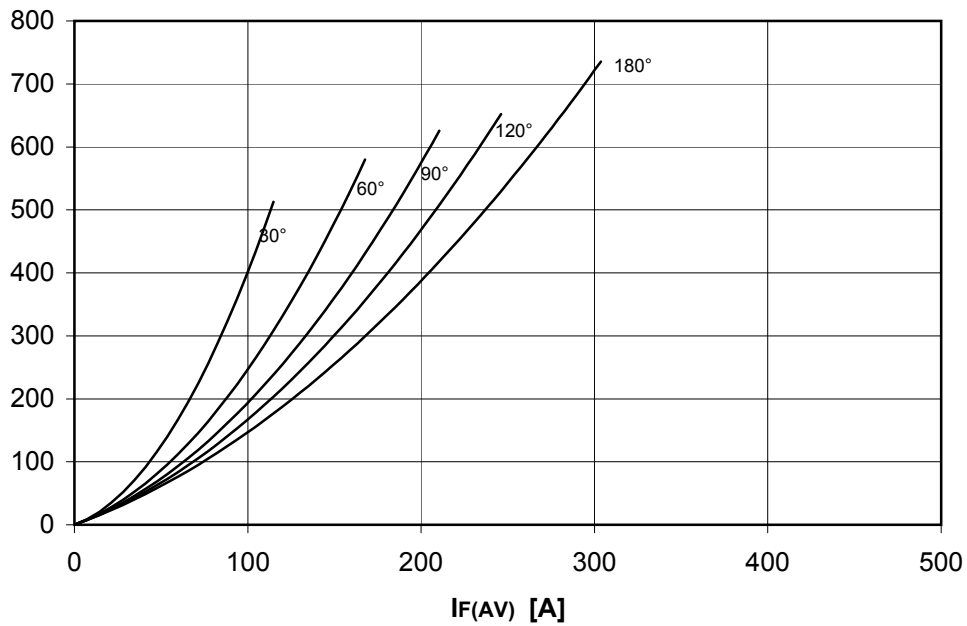
## DISSIPATION CHARACTERISTICS

SINE WAVE

Th [°C]



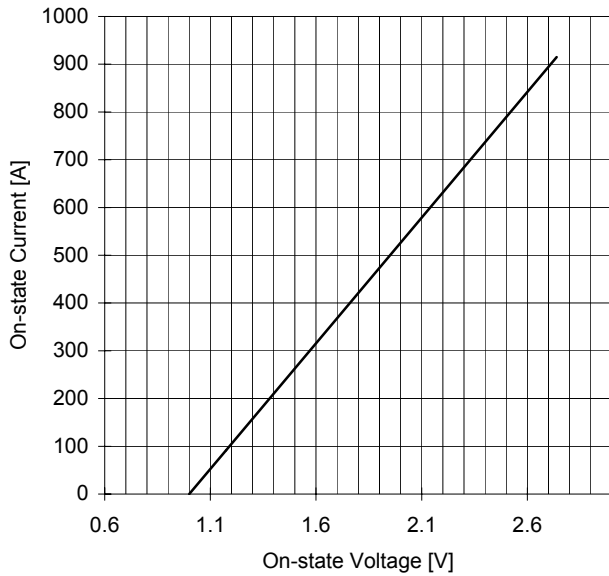
PF(AV) [W]



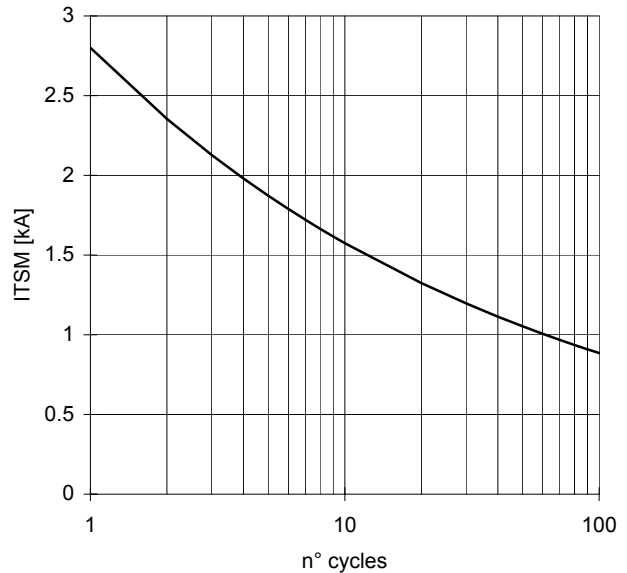
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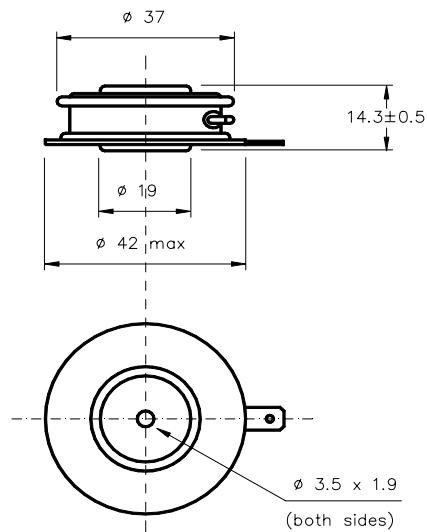
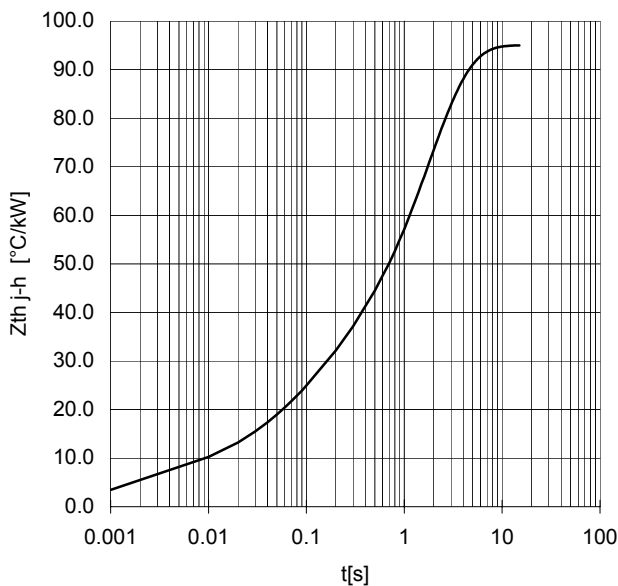
ON-STATE CHARACTERISTIC  
 $T_j = 125\text{ }^\circ\text{C}$



SURGE CHARACTERISTIC  
 $T_j = 125\text{ }^\circ\text{C}$



TRANSIENT THERMAL IMPEDANCE  
DOUBLE SIDE COOLED



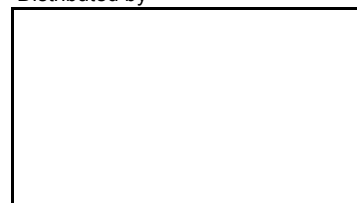
Dimensions  
in mm



Cathode terminal type DIN 46244 - A 4.8 - 0.8

Gate terminal type AMP 60598 - 1

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All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness  $< .03\text{ mm}$  and roughness  $< 2\text{ }\mu\text{m}$ .

In the interest of product improvement POSEICO S.p.A. reserves the right to change any data given in this data sheet at any time without previous notice.

If not stated otherwise the maximum value of ratings (symbols over shaded background) and characteristics is reported.



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