

# AN8104FBP

## High speed Low Power Consumption 8-Bit A/D Converter

### ■ Overview

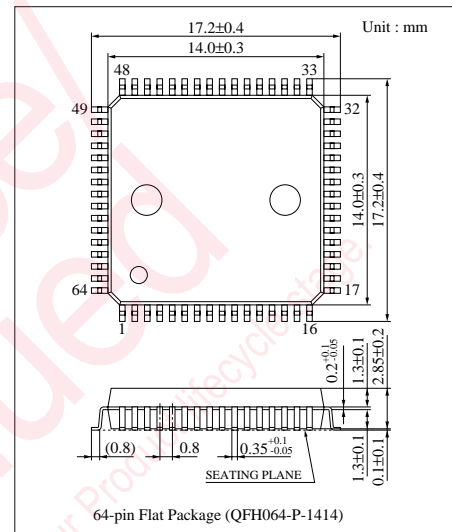
The AN8104FBP is a 8-bit A/D converter for measurement which uses the high frequency bipolar process to suppress the power consumption. It can operate with single power supply of -5.2V and maximum conversion rate of 125 MSPS, realizing the wide input band and the low error rate.

### ■ Features

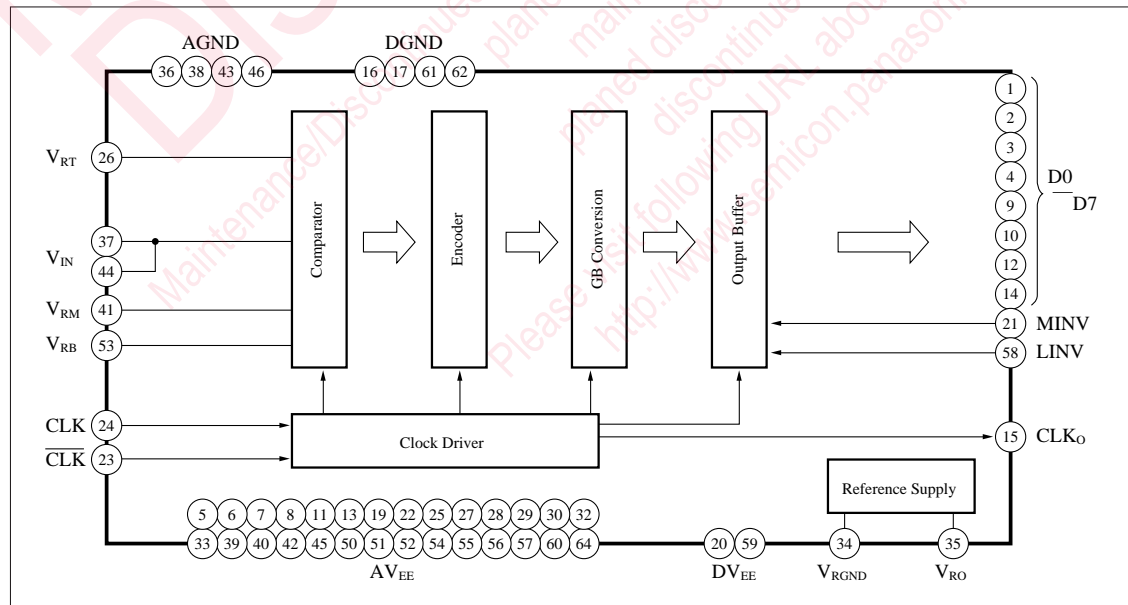
- 8-bit resolution
- High speed : maximum conversion rate of 125MSPS (min.)
- Wide input band : 250MHz, typ.(-3dB)
- Low error rate :  $10^{-12}$  tps or lower
- Low input capacitance : 15pF
- Input/Output form : ECL level

### ■ Application Field

- Measuring equipment such as digital oscilloscope
- Image processing



### ■ Block Diagram



## ■ Absolute Maximum Ratings (Ta=25°C)

| Parameter                             | Symbol  | Rating                  | Unit |
|---------------------------------------|---|-------------------------|------|
| Supply voltage                        | V <sub>EE</sub>                                     | -6.0 to +0.3            | V    |
| Analogue input voltage                | V <sub>IN</sub>                                     | V <sub>EE</sub> to +0.3 | V    |
| Digital input voltage                 | V <sub>CLK</sub> /V <sub>CLK</sub>                  | V <sub>EE</sub> to +0.3 | V    |
| Digital output current                | I <sub>CLKO</sub> /I <sub>D0</sub> —I <sub>D7</sub> | -20                     | mA   |
| Reference power supply output current | I <sub>RO</sub>                                     | 25                      | mA   |
| Reference resistive current           | I <sub>RT</sub> /I <sub>RB</sub>                    | +20/-20                 | mA   |
| Reference voltage                     | V <sub>RT</sub> /V <sub>RB</sub> /V <sub>RM</sub>   | V <sub>EE</sub> to +0.3 | V    |
| Power dissipation                     | P <sub>D</sub>                                      | 964*                    | mW   |
| Operating ambient temperature         | T <sub>opr</sub>                                    | -20 to +70              | °C   |
| Storage temperature                   | T <sub>stg</sub>                                    | -55 to +150             | °C   |

\* Ta=75°C

## ■ Recommended Operating Conditions (Ta=25°C)

| Parameter                 | Symbol                         | min             | typ  | max             | Unit |
|---------------------------|--------------------------------|-----------------|------|-----------------|------|
| Supply voltage            | V <sub>EE</sub>                | -5.4            | -5.2 | -5.0            | V    |
| Reference voltage         | V <sub>RT</sub>                | —               | 0.0  | —               | V    |
|                           | V <sub>RB</sub>                | —               | -2.0 | —               | V    |
| Analogue input voltage    | V <sub>IN</sub>                | V <sub>RB</sub> | —    | V <sub>RT</sub> | V    |
| Digital input voltage     | V <sub>IH</sub>                | -1.1            | -0.9 | —               | V    |
|                           | V <sub>IL</sub>                | —               | -1.7 | -1.5            | V    |
| Clock input pulse width * | t <sub>H</sub> /t <sub>L</sub> | —               | 2.5  | —               | ns   |

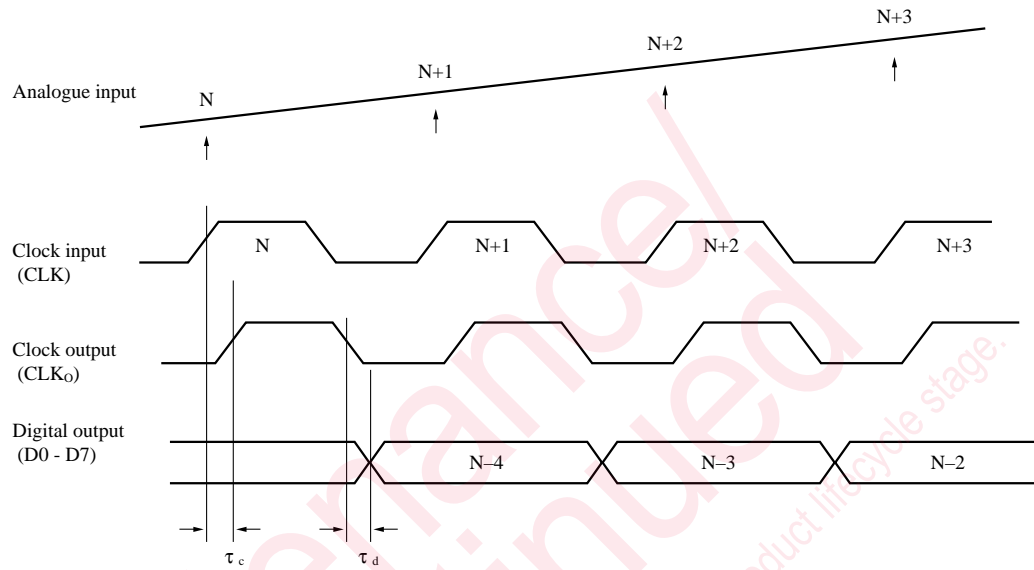
\* f<sub>CLK</sub>=200MHz

## ■ Electrical Characteristics (V<sub>EE</sub>=-5.2V, Ta=25°C)

| Parameter                             | Symbol            | Condition  | min  | typ               | max   | Unit             |
|---------------------------------------|-------------------|--|------|-------------------|-------|------------------|
| Supply current                        | I <sub>EE</sub>   |  | -300 | -125              | —     | mA               |
| Reference power supply output voltage | V <sub>RO</sub>   | I <sub>RO</sub> =10mA, V <sub>RGND</sub> =0V                         | -2.2 | -2.0              | -1.8  | V                |
| Reference supply current              | I <sub>RGND</sub> | Reference power supply output under no Load                          | —    | 0.6               | 5     | mA               |
| Reference resistive current           | I <sub>RT</sub>   | V <sub>RT</sub> =0V  | —    | 9                 | 20    | mA               |
|                                       | I <sub>RB</sub>   | V <sub>RB</sub> =2.0V  | -20  | -9                | —     | mA               |
| Input bias current                    | I <sub>IN</sub>   | V <sub>IN</sub> =1.0V  | —    | 480               | 1000  | μA               |
| Clock input current                   | I <sub>IH</sub>   | V <sub>CLK</sub> =-1.105V  | —    | 0.5               | 5     | μA               |
| Digital output voltage                | V <sub>OH</sub>   | R <sub>L</sub> =100Ω TO V <sub>T</sub> =-2.0V                        | -1.1 | -0.9              | -0.6  | V                |
|                                       | V <sub>OL</sub>   |  | -2.0 | -1.8              | -1.6  | V                |
| Linearity error                       | E <sub>L</sub>    | V <sub>RT</sub> -V <sub>RB</sub> =2.0V                               | —    | ±0.25             | ±0.65 | LSB              |
| Differential linearity error          | E <sub>D</sub>    | V <sub>RT</sub> -V <sub>RB</sub> =2.0V                               | —    | ±0.25             | ±0.65 | LSB              |
| Maximum conversion rate               | F <sub>CMAX</sub> |  | 125  | —                 | —     | MHz              |
| Input dynamic range                   |                   |  | —    | 2                 | —     | V <sub>P-P</sub> |
| Equivalent input impedance *1         | R <sub>IN</sub>   | V <sub>IN</sub> =-1V   | —    | 50                | —     | kΩ               |
| Input capacitance *1                  | C <sub>IN</sub>   | V <sub>IN</sub> =-1V   | —    | 15                | —     | pF               |
| Error rate *1                         |                   | f <sub>CLK</sub> =125MHz, f <sub>IN</sub> =40.5MHz<br>8LSB or higher | —    | 10 <sup>-12</sup> | —     | tps              |
| Quantization noise *2                 | SINAD             | f <sub>CLK</sub> =125MHz, f <sub>IN</sub> =10.000125MHz              | —    | 43                | —     | dB               |
|                                       |                   | f <sub>CLK</sub> =125MHz, f <sub>IN</sub> =100.000125MHz             | —    | 34                | —     | dB               |
| Input band *1                         | BW <sub>F</sub>   | V <sub>IN</sub> =1.4V <sub>P-P</sub> , -3dB                          | 200  | —                 | —     | MHz              |
| Clock duty *1                         | DTY               | f <sub>CLK</sub> =125MHz   | —    | 50                | —     | %                |
| Clock output delay *1                 | τ <sub>c</sub>    |  | —    | 6.5               | —     | ns               |
| Digital output delay *1               | τ <sub>d</sub>    |  | —    | 1.3               | —     | ns               |

\*1 Design reference value but not guaranteed one \*2 Total harmonics distortion included

## ■ Timing Chart



## ■ Output Code

| Step | Input signal |          |      | Digital output   |               |                  |                  |
|------|--------------|----------|------|------------------|---------------|------------------|------------------|
|      | 2.000VFS     | 7.8125mV | STEP | MINV= L, LINV= L |               | MINV= H, LINV= L | MINV= L, LINV= H |
|      |              |          |      | M<br>76543210    | L<br>76543210 | M<br>76543210    | L<br>76543210    |
| 000  | -2.000000    |          |      | 0000000          | 1000000       | 0111111          | 1111111          |
| 001  | -1.9921875   |          |      | 0000001          | 1000001       | 0111110          | 1111110          |
| .    | .            |          |      | .                | .             | .                | .                |
| .    | .            |          |      | .                | .             | .                | .                |
| .    | .            |          |      | .                | .             | .                | .                |
| 127  | -1.0078125   |          |      | 0111111          | 1111111       | 0000000          | 1000000          |
| 128  | -1.000000    |          |      | 1000000          | 0000000       | 1111111          | 1000000          |
| 129  | -0.9921875   |          |      | 1000001          | 0000001       | 1111110          | 1000001          |
| .    | .            |          |      | .                | .             | .                | .                |
| .    | .            |          |      | .                | .             | .                | .                |
| .    | .            |          |      | .                | .             | .                | .                |
| 254  | -0.0078125   |          |      | 1111110          | 0111110       | 1000001          | 1000001          |
| 255  | 0.000000     |          |      | 1111111          | 0111111       | 1000000          | 1000000          |

## ■ Pin Descriptions

| Pin No.  | Symbol                                       | Pin name  | Standard waveform          | Voltage level        | Description  |
|--|--|---|----------------------------|----------------------|--|
| 37<br>44   | $V_{IN}$                                     | Analogue input  |                            | -2 to 0V             | It is an input pin of analogue signal for A/D conversion circuit.  |
| 36, 38<br>43, 46   | AGND   | Analogue ground   |                            | 0V                   | Connect AGND and DGND with the possible lowest impedance at one point as near as possible to the chip.   |
| 5, 6, 7<br>8, 11, 13<br>19, 22, 25<br>27, 28, 29<br>30, 32, 33<br>39, 40, 42<br>45, 50, 51<br>52, 54, 55<br>56, 57, 60<br>64 | $A_{VEE}$                                    | Analogue negative power supply pin  |                            | -5.2V                | It is a power supply pin for analogue circuit block. Connect tantalum capacitor of several $\mu\text{F}$ and ceramic capacitor of $0.1\mu\text{F}$ as near as possible to this pin between this pin and DGND.  |
| 20, 59   | $D_{VEE}$                                    | Analogue negative power supply pin  |                            | -5.2V                | It is a power supply pin for digital. Connect tantalum capacitor of several $\mu\text{F}$ and ceramic capacitor of $0.1\mu\text{F}$ as near as possible to this pin between this pin and AGND or DGND.   |
| 26<br>41<br>53   | $V_{RT}$<br>$V_{RM}$<br>$V_{RB}$             | Reference voltage high level,<br>Reference voltage middle point level,<br>Reference voltage low level   |                            | 0V<br>-1.0V<br>-2.0V | It is used to set the reference voltage for comparator. Normally, $V_{RT}$ is given 0V and $V_{RB}$ is given -2V. Connect tantalum capacitor of several $\mu\text{F}$ and ceramic capacitor of $0.1\mu\text{F}$ in parallel between each pin and analogue ground. $V_{RM}$ is provided for linearity compensation which gives middle point potential between $V_{RT}$ and $V_{RB}$ . However, it is normally opened. |
| 16, 17<br>61, 62   | DGND   | Digital ground  |                            | 0V                   | Connect AGND and DGND with the possible lowest impedance at one point as near as possible to the chip.   |
| 23<br>24   | $\overline{\text{CLK}}$<br>CLK               | Clock input   | Refer to the timing chart. | ECL                  | It is a clock for sampling. For their timing, refer to the timing chart.   |
| 15   | $\text{CLK}_O$                               | Clock output  | Refer to the timing chart. | ECL                  | It is a clock output pin of ECL level.   |
| 1<br>2<br>3<br>4<br>9<br>10<br>12<br>14  | D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | Digital output (LSB),<br>Digital output,<br>Digital output,<br>Digital output,<br>Digital output,<br>Digital output,<br>Digital output,<br>Digital output (MSB) | Refer to the timing chart. | ECL                  | It is an output pin of ECL Level.  |
| 21<br>58   | MINV<br>LINV                                 | Digital output setting pin,<br>Digital output setting pin   |                            | ECL                  | Setting the MINV pin to "H" level inverts the data output, D7. Setting the LINV pin to "H" level inverts the data outputs (D0 - D6). The output is inverts synchronously with clock.   |
| 34<br>35   | $V_{RGND}$<br>$V_{RO}$                       | Ground pin for reference Power supply,<br>Reference power supply output   |                            | 0V<br>-2.0V          | It is a GND pin for reference power supply. It is an output pin for power supply for A/D reference voltage low level.  |

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