

AN8102FBP

Super High Speed Low Power Consumption 8-Bit A/D Converter

Overview

The AN8102FBP is a 8-bit A/D converter for measurement which uses the high frequency bipolar process to suppress the power consumption.

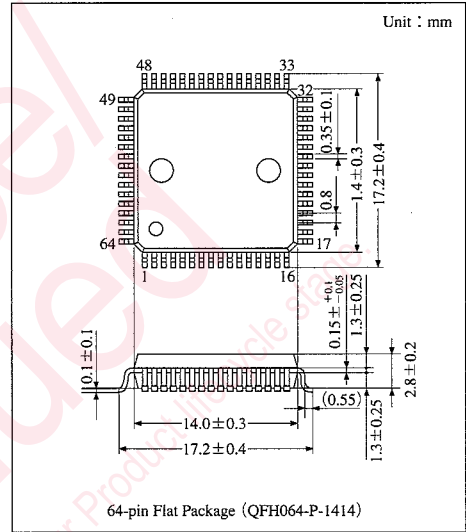
It can operate with single power supply of -5.2V and maximum conversion rate of 125MSPS, realizing the low error rate.

Features

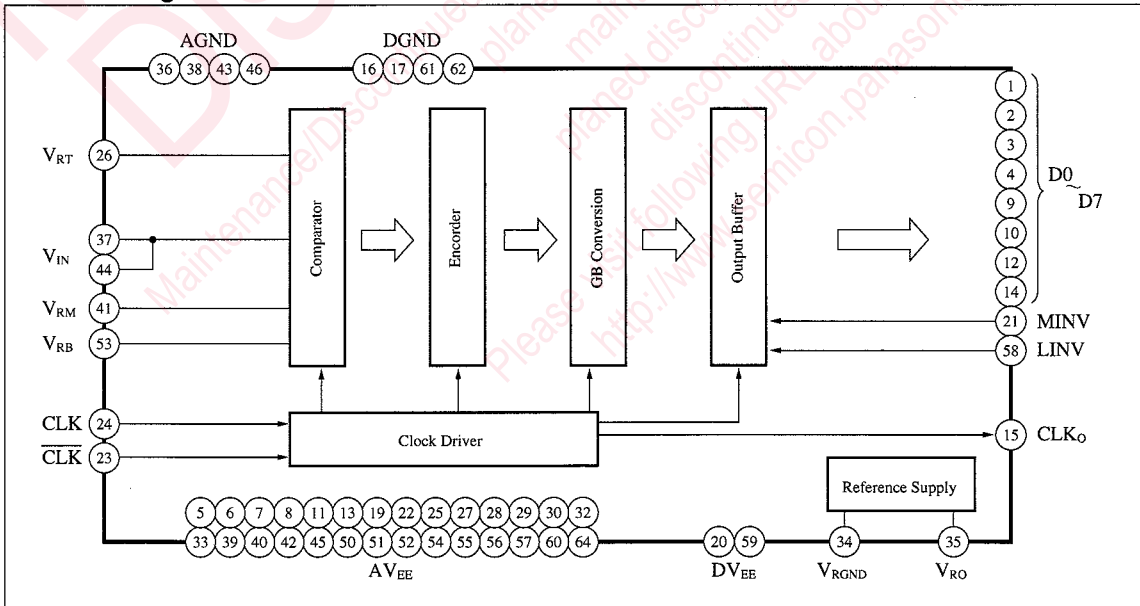
- 8-bit resolution
- Super high speed : maximum conversion rate of 125 MSPS (min.)
- Low error rate : 10^{-12} tps or lower
- Low input capacitance : 15pF
- Input/Output form : ECL level

Application Field

- Measuring equipment such as digital oscilloscope
- Image processing



Block Diagram



Absolute Maximum Rating (Ta=25°C)

Parameter	Symbol	Rating	Unit
Supply voltage	V _{EE}	-6.0 to +0.3	V
Analogue input voltage	V _{IN}	V _{EE} to +0.3	V
Digital input voltage	V _{CLK} /√V _{CLK}	V _{EE} to +0.3	V
Digital output current	I _{CLKO} /I _{D0} ~I _{D7}	-20	mA
Reference power supply output current	I _{RO}	25	mA
Reference resistive current	I _{RT} /I _{RB}	+20/-20	mA
Reference voltage	V _{RT} /V _{RB} /V _{RM}	V _{EE} to +0.3	V
Power dissipation	P _D	964*	mW
Operating ambient temperature	T _{opr}	-20 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C

* Ta=70°C

Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	min	typ	max	Unit
Supply voltage	V _{EE}	-5.4	-5.2	-5.0	V
Reference voltage	V _{RT}	—	0.0	—	V
	V _{RB}	—	-2.0	—	V
Analogue input voltage	V _{IN}	V _{RB}	—	V _{RT}	V
Digital input voltage	V _{IH}	-1.1	-0.9	—	V
	V _{IL}	—	-1.7	-1.5	V
Clock input pulse width *	t _H /t _L	—	5	—	ns

* f_{CLK} = 100MHz

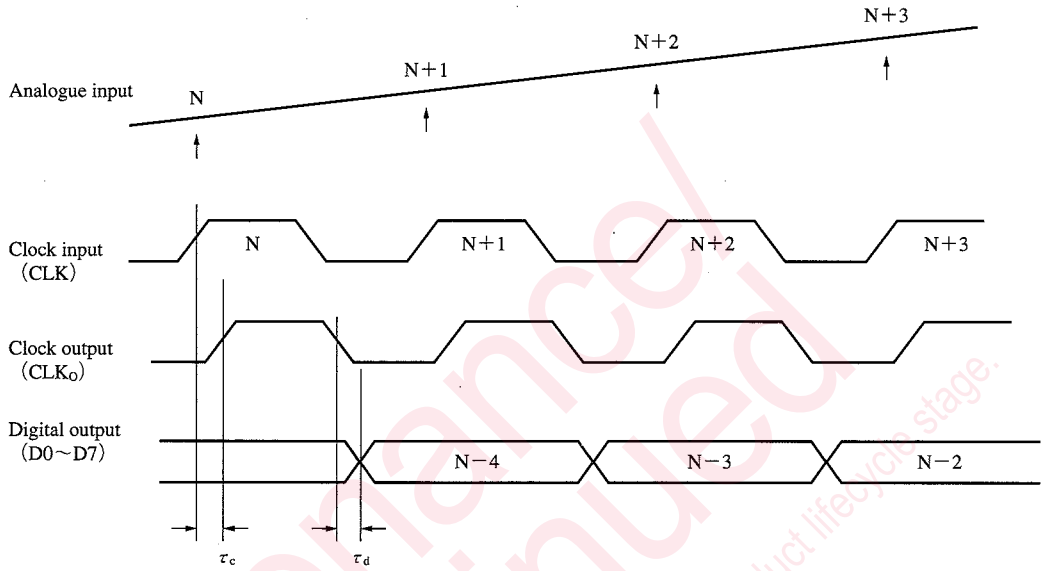
Electrical Characteristics (V_{EE} = -5.2V, Ta=25°C)

Parameter	Symbol	Condition	min	typ	max	Unit
Supply current	I _{EE}		-195	-135	-85	mA
Reference power supply output voltage	V _{RO}	I _{RO} = 10mA, V _{RGND} = 0V	-2.2	-2.0	-1.8	V
Reference supply current	I _{RGND}	Reference power supply output under no Load	0.5	2.0	5	mA
Reference resistive current	I _{RT}	V _{RT} = 0V	4	10	20	mA
	I _{RB}	V _{RB} = -2.0V	-20	-10	-4	mA
Input bias current	I _{IN}	V _{IN} = -1.0V	—	120	250	μA
Clock input current	I _{IH}	V _{CLK} = -1.105V	—	1.0	5.0	μA
Digital output voltage	V _{OH}	R _L = 100Ω TO V _T = -2.0V	-1.1	-0.9	-0.6	V
	V _{OL}		-2.0	-1.8	-1.6	V
Linearity error	E _L	V _{RT} - V _{RB} = 2.0V	—	±0.25	±0.5	LSB
Differential linearity error	E _D	V _{RT} - V _{RB} = 2.0V	—	±0.25	±0.5	LSB
Maximum conversion rate	F _{CMAX}		125	—	—	MHz
Input dynamic range			—	2	—	V _{p-p}
Equivalent input impedance *1	R _{IN}	V _{IN} = -1V	—	350	—	kΩ
Input capacitance *1	C _{IN}	V _{IN} = -1V	—	15	20	pF
Error rate *1		f _{CLK} = 125MHz, f _{IN} = 40.5MHz 8LSB or higher	—	—	10 ⁻¹²	tps
Quantization noise *2	SINAD	f _{CLK} = 125MHz, f _{IN} = 10MHz	38	43	—	dB
		f _{CLK} = 125MHz, f _{IN} = 50MHz	30	35	—	dB
Input band *1	BW _F	V _{IN} = 2V _{p-p} , -3dB	—	125	—	MHz
Clock duty *1	DTY	f _{CLK} = 125MHz	30	50	70	%
Clock output delay *1	τ _c		5	7	9	ns
Digital output delay *1	τ _d		—	1.3	—	ns

*1 Design reference value but not guaranteed one *2 Total harmonics distortion included

A/D and D/A Converters

■ Timing Chart



■ Output Code

Step	Input signal			Digital output					
	2.000VFS	7.8125mV	STEP	MINV=L, LINV=L		MINV=H, LINV=L		MINV=L, LINV=H	
				M	L	M	L	M	L
000		-2.0000000		00000000	10000000	01111111			
001		-1.9921875		00000001	10000001	01111110			
.				
.				
127		-1.0078125		01111111	11111111	00000000			
128		-1.0000000		10000000	00000000	11111111			
129		-0.9921875		10000001	00000001	11111110			
.				
.				
254		-0.0078125		11111110	01111110	10000001			
255		-0.0000000		11111111	01111111	10000000			

Pin Descriptions

Pin No.	Symbol	Pin name	Standard waveform	Voltage level	Description
37 34	V_{IN}	Analogue input		-2 to 0V	It is an input pin of analogue signal for A/D conversion circuit.
36, 38 43, 46	AGND	Analogue ground		0V	Connect AGND and DGND with the possible lowest impedance at one point as near as possible to the chip.
5, 6, 7 8, 11, 13 19, 22, 25 27, 28, 29 30, 32, 33 39, 40, 42 45, 50, 51 52, 54, 55 56, 57, 60 64	AV_{EE}	Analogue negative power supply pin		-5.2V	It is a power supply pin for analogue circuit block. Connect tantalum capacitor of several μF and ceramic capacitor of 0.1 μF as near as possible to this pin between this pin and AGND.
20, 59	DV_{EE}	Digital negative power supply pin		-5.2V	It is a power supply pin for digital circuit block. Connect tantalum capacitor of several μF and ceramic cap capacitor of 0.1 μF as near as possible to this pin between this pin and DGND.
26 41 53	V_{RT} V_{RM} V_{RB}	Reference voltage high level Reference voltage middle point level Reference voltage low level		0V -1.0V -2.0V	It is used to set the reference voltage for comparator. Normally, V_{RT} is given 0V and V_{RB} is given -2 V. Connect tantalum capacitor of several μF and ceramic capacitor of 0.1 μF in parallel between each pin and analogue ground. V_{RM} is provided for linearity compensation which gives middle point potential between V_{RT} and V_{RB} . However, it is normally opened.
16, 17 61, 62	DGND	Digital ground		0V	Connect AGND and DGND with the possible lowest impedance at one point as near as possible to the chip.
23 24	\overline{CLK} CLK	Clock input	Refer to the timing chart	ECL	It is a clock for sampling. For their timing, refer to the timing chart.
15	CLK _O	Clock output	Refer to the timing chart	ECL	It is a clock output pin of ECL level.
1 2 3 4 9 10 12 14	D0 D1 D2 D3 D4 D5 D6 D7	Digital output (LSB) Digital output Digital output Digital output Digital output Digital output Digital output Digital output (MSB)	Refer to the timing chart	ECL	It is an output pin of ECL Level.
21 58	MINV LINV	Digital output setting pin Digital output setting pin		ECL	Setting the MINV pin to "H" level inverts the data output, D7. Setting the LINV pin to "H" level inverts the data outputs (D0 ~ D6). The output is inverts synchronously with clock.
34 35	V_{RGND} V_{RO}	Ground pin for reference power supply reference power supply output		0V -2.0V	It is a GND pin for reference power supply. It is an output pin for power supply for A/D reference voltage low level.



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