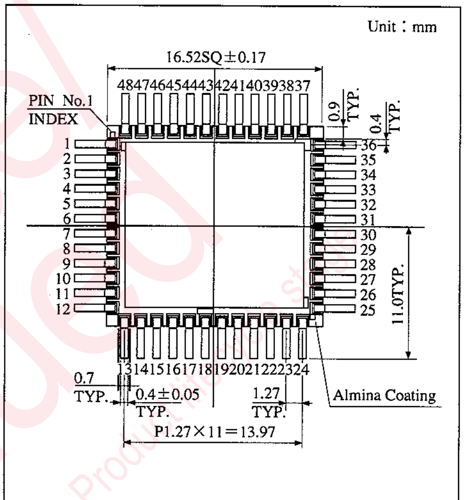
AN8100

Super High speed Low Power Consumption 6-Bit A/D Converter

■ Overview

The AN8100 is a 6-bit A/D converter for measurement which uses the high frequency bipolar process to suppress the power consumption. It can operate at the maximum conversion rate 1 GHz.

Since it incorporates the D/A converter whose input is directly connected with A/D block, it can construct the 2-step parallel type A/D converter of high resolution.



48-pin Ceramic QFP (CQFP-48)

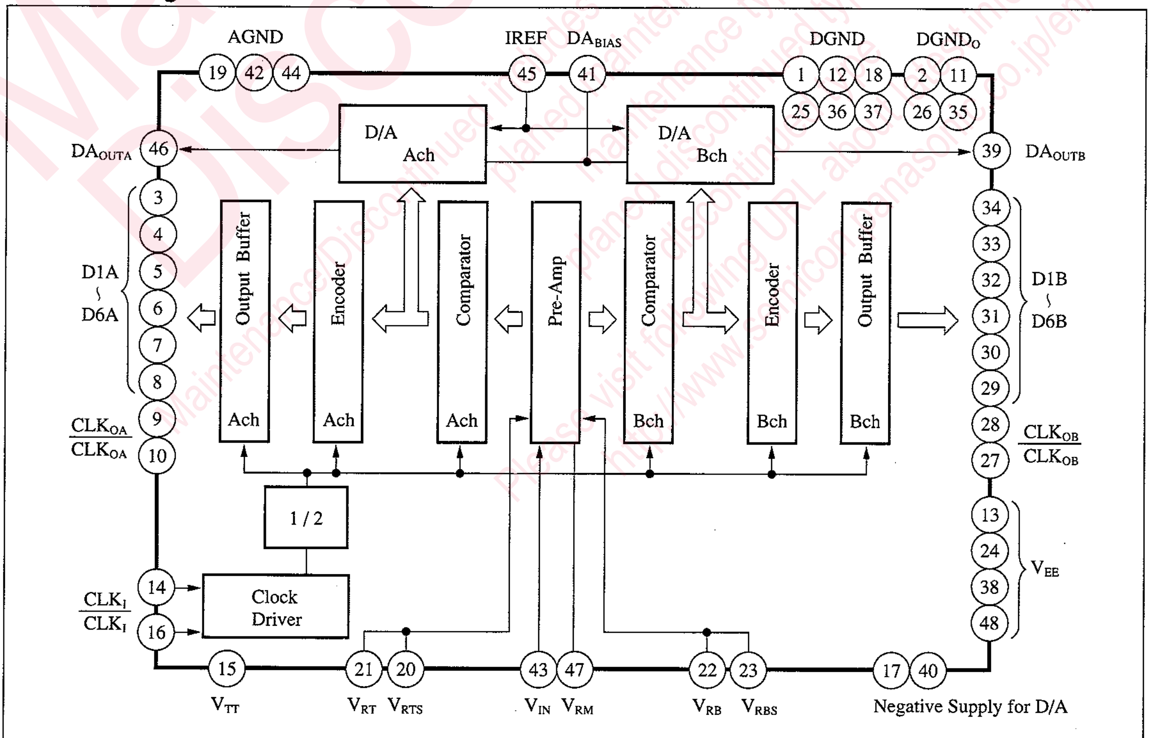
■ Features

- 6-bit resolution A/D and D/A converter
- A/D block : Maximum conversion rate ; 1 GSPS (min.)
  Low error rate ; 10^{-9} tps or lower
  Output code ; Gray code
- D/A block : Maximum conversion rate ; 1 GSPS (min.)
  Full-scale current ; 20mA

■ Application Field

- Measuring equipment such as digital oscilloscope
- Radar

■ Block Diagram



■ Absolute Maximum Rating (Ta=25℃)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{EE}/DAV_{EE}	−6.0 to +0.5	V
Supply current	I_{EE}	1000	mA
Analogue input voltage	V_{IN}/V_{IREF}/DA_{BIAS}	V_{EE} to +0.5	V
Analogue input current	I_{IN}	80	mA
Digital output voltage	V_{CLK}/$\overline{V_{CLK}}$	−4.7 to +0.5	V
Digital output current	I_{CLKO}/$\overline{I_{CLKO}}$/I_{DIA}~I_{D6B}	−40	mA
Reference input current	I_{RT}/I_{RB}	+45/−45	mA
Reference resistive voltage	V_{RB}/V_{RT}/V_{RM}	V_{EE} to +0.5	V
Aanlogue output current	I_{OUT}	30	mA
Power dissipation	P_D	5400*	mW
Operating ambient temperature	T_{opr}	−25 to +75	℃
Storage temperature	T_{stg}	−55 to +150	℃

* Under the conditions : Ta=75℃, Aluminium heat sink (16mm×16mm×16mm : four fins), air of 2m/s

■ Recommended Operating Conditions (Ta=25℃)

Parameter	Symbol	min	typ	max	Unit
Negative supply voltage	V_{EE}/DAV_{EE}	−5.46	−5.2	−4.94	V
Reference voltage	V_{RT}	—	−0.7	—	V
	V_{RB}	—	−1.7	—	V
Analogue input voltage	V_{IN}	V_{RB}	—	V_{RT}	V
Digital input voltage	V_{IH}	−1.1	−0.9		V
	V_{IL}	—	−1.7	−1.5	V
Reference voltage for D/A	DA_{BIAS}	—	−3.6	—	V
Reference resistance for D/A	R_{IREF}	—	1.0	—	kΩ
Clock input pulse width *	t_H	—	0.5	—	ns

* f_{CLK}=1GHz

■ Electrical Characteristics (V_{EE}=−5.2V, Ta=25℃)

Parameter	Symbol	Condition	min	typ	max	Unit
Supply current	I_{EE}	Supply current of A/D, D/A converter	−850	−760	—	mA
Reference current	I_{RT}	V_{RT}=−0.7V	—	10	20	mA
	I_{RB}	V_{RB}=−1.7V	−20	−10	—	mA
Analogue input resistance	R_{IN}	Between V_{IN} and AGND	46	50	54	Ω
Clock input resistance	R_{CLK}	Between CLK_{IN} and V_{TT}	46	50	54	Ω
Clock input voltage	V_{IH}		−1.1	—	−0.7	V
	V_{IL}		−1.9	—	−1.5	V
Digital output voltage	V_{OH}	R_L=50Ω TO V_{TT}=−2.0V	−1.03	—	—	V
	V_{OL}		—	—	−1.6	V
A/D Block						
Resolution	RES		—	6	—	BIT
Linearity error	E_L	V_{IN}=1V_{p-p}	—	±0.25	±0.5	LSB
Differential linearity error	E_D	V_{IN}=1V_{p-p}	—	±0.25	±0.5	LSB
Maximum conversion rate	F_{CMAX}		1.0	—	—	GHz
Analogue input non-saturation ragnge	V_{IN}		V_{EE}+2.5	—	0.3	V
Input capacitance *1	C_{IN}	V_{IN}=−1.2V	—	7.5	—	pF

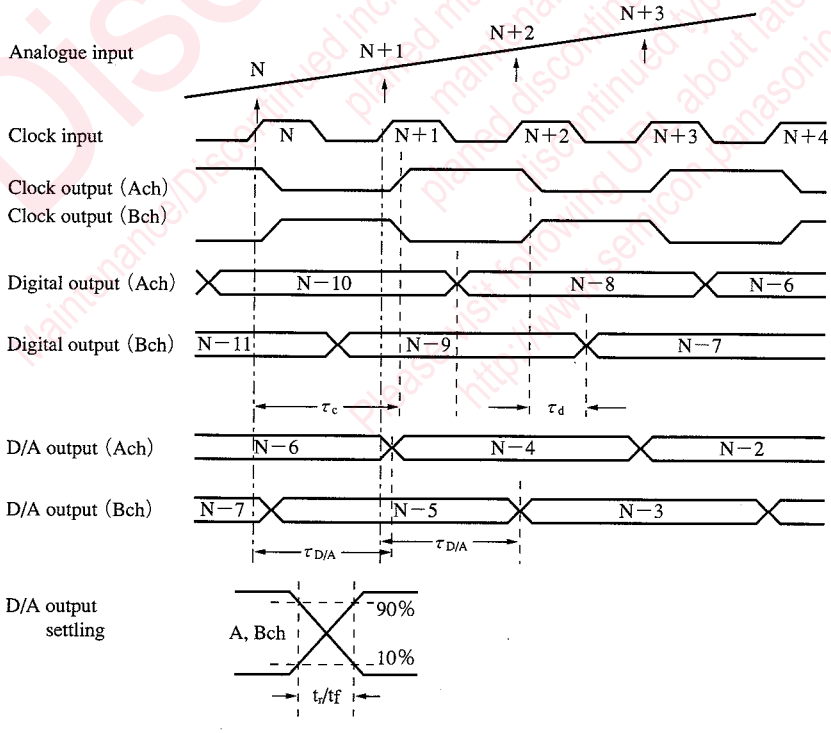
*1 Design reference value but not guaranteed one *2 Total harmonics distorsion included

■ Electrical Characteristics (cont.) (V_{EE} = −5.2V, Ta = 25℃)

Parameter	Symbol	Condition	min	typ	max	Unit
Error rate *1		f_{CLK} = 1GHz, f_{IN} = 400MHz, 80% FS input, 3 LSB or more	—	—	10^{-9}	tps
Quantization noise *2	SINAD	f_{CLK} = 1GHz, f_{IN} = 62.5MHz	32	34	—	dB
		f_{CLK} = 1GHz, f_{IN} = 400MHz *1	—	32	—	dB
Input band *1	BW_F	−3dB	—	1	—	GHz
A/D output matching *1			—	0.05	—	LSB
Missing code *1		f_{IN} = 400MHz, No missing code	—	—	—	—
Systematic jitter *1			—	10	—	ps.
Clock output delay *1	τ_c		—	1.5	—	ns
Digital output delay *1	τ_d		—	0.55	0.70	ns
D/A Block						
Resolution	RES		—	6	—	BIT
Differential linearity error	E_L	Integral Linearity Error of A/D+D/A	—	±0.5	±1.0	LSB
Differential linearity error	E_D	Differential Linearity Error	—	±0.5	±0.98	LSB
Full-scale matching	I_{FSM}	DA_{BIAS} = −3.6V, I_{OUT} = 20mA	—	±0.75	±1.0	%
Zero-scale output current	I_{ZS}	DA_{BIAS} = −3.6V	−100	−20	—	μA
Rise/Fall time *1	t_r/t_f	10 to 90% of full scale	—	2	—	ns
Analogue output delay *1	$\tau_{D/A}$		—	1.2	—	ns
Maximum conversion rate	F_{CMAX}		1.0	—	—	GHz

*1 Design reference value but not guaranteed one *2 Total harmonics distorsion included

■ Timing Chart



Output Code

Step	Input signal 1.000VFS 15.625nV STEP	A/D block Digital output (Gray code) Ach, Bch M L 654321	D/A block Analogue output Ach, Bch 50Ω load resistance (V)
00	−1.700000	000000	−0.000000
01	−1.684375	000001	−0.015625
·	·	·	·
31	−1.215625	010000	−0.484375
32	−1.200000	110000	−0.500000
33	−1.184375	110001	−0.515625
·	·	·	·
62	−0.715625	100001	−0.984375
63	−0.700000	100000	−1.000000

Pin Descriptions

Pin No.	Symbol	Pin name	Standard waveform	Voltage level	Description
43	V_{IN}	Analogue input		−0.7 ~ −1.7V	It is an input pin of analogue signal for A/D conversion circuit. 50Ω resistance is used to connect AGND and V_{IN}
19, 42 44	AGND	Analogue ground		0V	Connect AGND and DGND with the possible lowest impedance at one point as near as possible to the chip.
13, 24 38, 48	V_{EE}	Negative power supply pin		−5.2V	Connect tantalum capacitor of several μF and ceramic capcacitor of 0.1 μF as near as possible to this pin between this pin and AGND or DGND.
20 21 22 23 47	V_{TRTS} V_{RT} V_{RB} V_{RBS} V_{RM}	Sense pin Reference voltage high level Reference voltage low level Sense pin Reference voltage middle point level		−0.7V −0.7V −1.7V −1.7V −1.2V	It is used to set the reference voltage for comparator. Normally, V_{RT} is given −0.7V and V_{RB} is given −1.7V. Connect tantalum capacitor of several μF and ceramic capacitor of 0.1 μF in parallel between each pin and analogue ground. V_{RM} is provided for linearity conpemsation which gives middle point potential between V_{RT} and V_{RB}. However, it is normally opened.
1, 12 18, 25 36, 37	DGND	Digital ground		0V	Connect AGND and DGND with the possible lowest impedance at one point as near as possible to the chip.
2, 11 26, 35	$DGND_O$	Digital ground for output		0V	It is a ground pin for digital output.
14 16	$\overline{CLK_I}$ CLK_I	Clock input	Refer to the timing chart	ECL ECL	It is a clock for sampling. Each of these pins is connected with V_{TT} pin through resistor of 50Ω.
9 10 27 28	CLK_{OA} $\overline{CLK_{OA}}$ $\overline{CLK_{OB}}$ CLK_{OB}	Clock output		ECL	It is a clock output pin of ECL level.ith this signal, the digital output of A or Bch can be latched.

■ Pin Descriptions (cont.)

Pin No.	Symbol	Pin name	Standard waveform	Voltage level	Description
15	V_{TT}	Negative power supply pin for clock signal termination		−2.0V	
3	D1A	Ach. digital output (LSB)	Refer to the timing chart	ECL	It is an output pin of ECL level.
4	D2A	Ach. digital output			
5	D3A	Ach. digital output			
6	D4A	Ach. digital output			
7	D5A	Ach. digital output			
8	D6A	Ach. digital output (MSB)			
29	D6B	Bch. digital output (MSB)	Refer to the timing chart	ECL	It is an output pin of ECL level.
30	D5B	Bch. digital output			
31	D4B	Bch. digital output			
32	D3B	Bch. digital output			
33	D2B	Bch. digital output			
34	D1B	Bch. digital output (LSB)			
17, 40	DAV_{EE}	Negative power supply for D/A		−5.2V	Connect tatalum capacitor of several μF and ceramic capacitor of 0.1 μF in parallel between this pin and analogue ground. Set the voltage same as negative power supply pin V_{EE}.
46	DA_{OUTA}	Ach. analogue output pin,		0~20mA	It should be connected to AGND through load resistance of 50Ω.
39	DA_{OUTB}	Bch. analogue output pin		0~20mA	It should be connected to AGND through load resistance of 50Ω.
41	DA_{BIAS}	Reference voltage pin for D/A		−3.6V	Connect tatalum capacitor of several μF and ceramic capacitor of 0.1 μF in parallel between this pin and analogue ground.
45	I_{REF}	Reference current input pin for D/A			It should be connected to AGND through 1kΩ.

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