A Smart Regulator Design for Network Interface Cards Using the Si91860

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INTRODUCTION

The Advance Configuration and Power Interface (ACPI) specification minimizes power consumption in desktop and other PC systems and yet maintains full operation. The Instantly Available PC (IAPC) is one aspect of power saving when the entire system is not required to be on. IAPC maintains power to the critical circuitry to wake up the PC up from sleep mode at a power management event (PME) such as a phone–ring or a LAN signal. The response to a PME might be to move the entire system, or specific devices, to the fully operational power state or to a lower power state, depending upon the event and the current power state.

The Vishay Siliconix Si91860 is a power IC specifically designed to regulate power for network interface cards (NIC), PCMCIA cards, and PCI interface cards in desktop and notebook computers. The Si91860 400-mA smart regulator combines an ultra-low supply current that reduces power consumption with a highly integrated design that that requires only four external components for a complete application circuit.

PCI cards are designed to support three different voltage sources – the 5-V primary input (V_{IN}), the 5-V standby input (V_{SB}) from the legacy PCI system or motherboard, and the 3.3-V auxiliary supplies (V_{AUX}). In sleep mode, the PCI bus and its standard voltage rails are powered down, while the auxiliary 3.3-V supply remains on. The Si91860 monitors each voltage supply and selects the supply most appropriate for delivering an uninterrupted, regulated, glitch-free 3.3-V output to the PCI card chipset. The Si91860 can handle 400-mA of continuous load current from any of the available power sources, providing a 25-mA headroom over the 375 mA required by the PCI Bus Power Management Interface specification of 375 mA in enabled mode.

Si91860 Operation:

The Si91860 consists of two 5-V to 3.3-V linear regulators, a low-resistance power switch, voltage monitors for the input supplies, and control logic. Figure 1 provides the block diagram of the Si91860. Either of the two linear regulators can supply a constant 3.3-V output from the 5-V inputs. The total combined dropout across the regulator and switch is low enough to maintain the output regulation at a peak 600-mA load and minimum input voltage. Irrespective of which input is used, the 3.3-V output is well regulated with dynamic line/load regulation and output voltage immunity to any input switchovers.

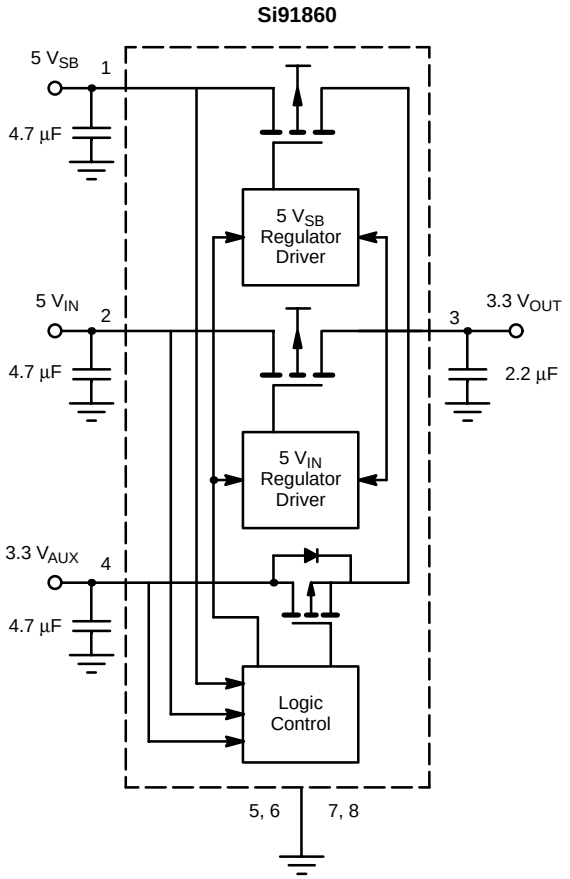

FIGURE 1. Block Diagram

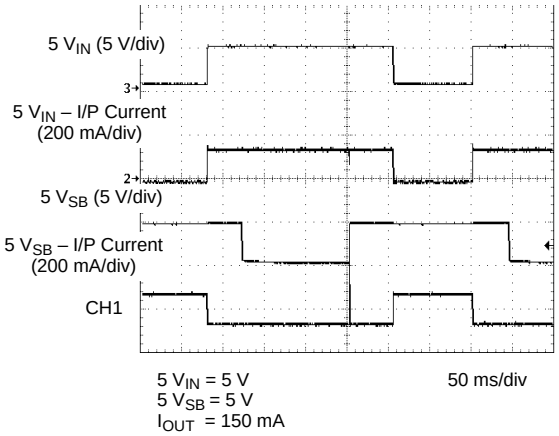

FIGURE 2. Switching Between Inputs

The voltage levels on the V_{IN} and V_{SB} are monitored and compared to a threshold voltage of 4.35 V. If the voltage on the input is above this threshold, the associated regulator may be enabled. Logic circuitry enables the V_{IN} regulator over the V_{SB} if both are present and valid. The 5-V standby regulator will be enabled provided that the voltage level is above the lockout threshold and the 5-V_{IN} input is not present. If neither of the 5-V inputs is above the lockout threshold, the 3.3-V V_{AUX} input powers the output through the bypass transistor. The waveforms in Figure 2 illustrate the priority control in switching between the V_{IN}, V_{SB}, and V_{AUX} input supplies.

Disturbances on the output resulting from the switchover from the main 5-V_{IN} input to the standby 5-V_{SB} input, and vice versa, may be caused by delays in the control circuitry and amplifiers. The Si91860 is designed to reduce their occurrence by minimizing delays during transitions. As shown in Figures 3 through 6, the output is recovered within two microseconds during the switchovers from the 5-V_{IN}, 5-V_{SB}, and 3.3-V_{AUX} inputs.

The 5-V V_{IN} and 5-V V_{SB} regulators use a p-channel power MOSFET series element that reduces the power consumption of the Si91860 by significantly reducing the ground current. MOSFETs provide higher peak drive currents than solutions using bipolar series elements, where the maximum current drawn is limited by the available base current. The 3.3-V V_{AUX} bypass switch has an on-resistance of just 0.2-Ω, and drops only 80 mV at 400-mA load. The 3.3-V V_{AUX} gate threshold voltage of the bypass transistor is 0.8 V and needs a minimum of 2 V on the auxiliary input for a 400-mA output current.

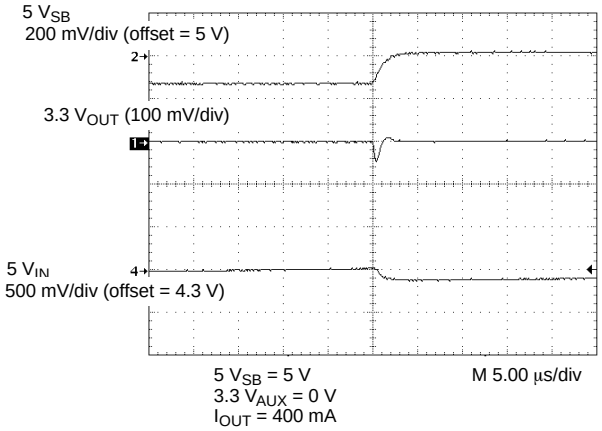

FIGURE 3. 5-V_{IN} Power Up (5 V_{SB} = 5 V)

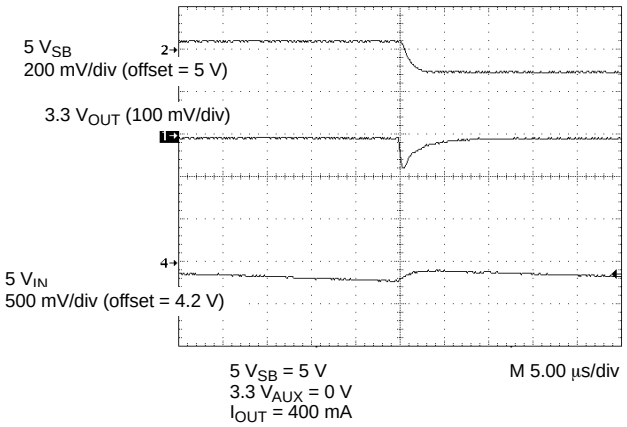

FIGURE 4. 5-V_{IN} Power Down (5 V_{SB} = 5 V)

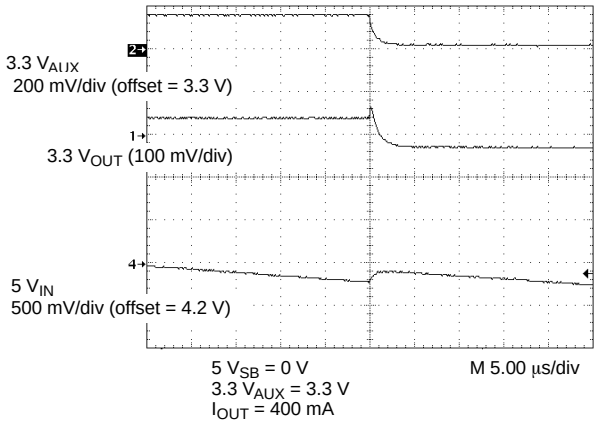

FIGURE 5. 5-V_{IN} Power Down (3.3 V_{AUX} = 3.3 V)

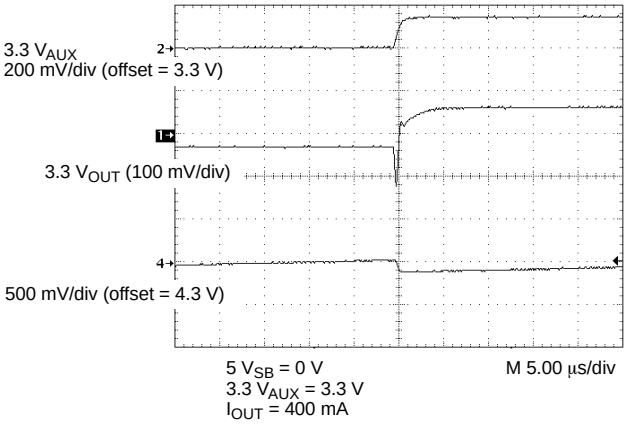

FIGURE 6. 5-V_{IN} Power Up (3.3 V_{AUX} = 3.3 V)

Input Voltage Hysteresis:

During power-up of the device, the circuit draws a high current to charge up the empty capacitor. The input inrush currents could be several times higher than the normal operating currents of the regulator. For the Si91860, the inrush current during the power-up consists of two components: a) charging of the input capacitor, and b) the output load and charging of the output capacitor. The input capacitor, charging inrush current may be neglected if it is charged with the finite rise time of the source voltage. When the rising input voltage reaches the V_{IN}-select of 4.3 V, the Si91860 turns on to charge the output capacitor while delivering the load current. The output capacitor is at this point charged with a 4.3-V differential and can produce very high current pulse for a short duration.

The large input inrush current can produce a substantial voltage glitch if the inductive impedance of the input trace is not low enough. The Si91860 is provided with a 230-mV hysterisis at the main and stand-by inputs to avoid any oscillations and system locking during start up. Refer to Figure 7 for the effect of source/trace impedance on the primary input. The Si91860 is powered up through inductive and resistive impedance values of 125 nH and 50 mΩ, respectively.

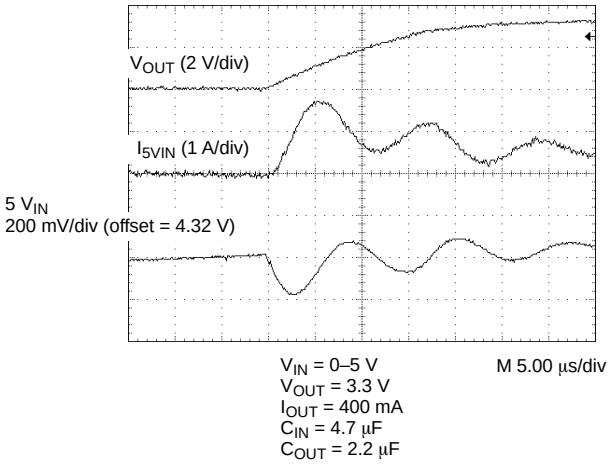

FIGURE 7. Voltage Glitch at 5 V_{IN}

Power Dissipation/Junction Temperature:

The 5-V V_{IN} and 5-V V_{SB} are rated to deliver up to a 600-mA peak current for two milliseconds. The internal logic allows the current to be drawn from one regulator at a time. The maximum load current is specified for continuous operation and for finite pulse widths. Maximum allowable junction temperature, junction-to-ambient thermal impedance at a thermal equilibrium, and the ambient temperature determine the continuous current rating at a given input-to-output differential. The input voltage, p-channel power MOSFET transconductance, and the transient thermal impedance between junction to lead are major issues for the peak current amplitude and pulse width. The maximum continuous power dissipation can be calculated using the following equation:

$$P_D = \left(5\ V_{IN} - 3.3\right) \times I_{OUT} + 5\ V_{IN} \times I_{GND}$$

The worst-case scenario in minimum continuous power dissipation would occur at 5-V V_{IN} = 5 V_{SB} = 5.5 V and I_{OUT} = 400 mA. The Si91860 does not draw any current from the 3.3-V V_{AUX} when the 5-V V_{IN} and 5-V V_{SB} are present. Refer to the Si91860 datasheet for the typical values of the 5-V V_{IN} and 5-V V_{SB} supply currents.

The maximum continuous power dissipation of the Si91860 can be calculated using the following equation:

$$P_{DMAX} = \frac{\left(T_{JMAX} - T_{AMAX}\right)}{\theta_{JA}}$$

The absolute maximum junction temperature allowed for Si91860 is 150°C, while the junction-to-ambient thermal impedance is 62.5°C/W. The junction-to-ambient thermal impedance is measured with the device mounted and all leads soldered on the 1.6-mm glass epoxy FR4 PC board with a 1-oz copper area.

Short Circuit / Over Temperature Protection:

In the event of a short circuit in the equipment powered by the 5-V V_{IN} and 5-V V_{SB}, the Si91860 limits the maximum current to prevent damage to the electronics. The peak current through the Si91860 is typically limited to 800 mA during continuous short circuit at the output. In bypass mode, the device is not current limited. It is advised to limit the source current of the 3.3-V V_{AUX} in case of short circuit in the bypass mode.

The Si91860 is designed with an over-temperature protection circuit that prevents thermal runaways in the p-channel power MOSFETs. The Si91860 will shut off and stop sourcing the current as soon as the junction temperature exceeds the over-temperature limit. If the junction temperature reaches 165°C, an internal control circuit shuts off the p-channel power MOSFET. The Si91860 will remain disabled until the chip temperature drops below 145°C, at which point it will turn on automatically. The 20°C temperature hysterisis avoids possible oscillation and minimizes the risk of damage by reducing the average power delivery during fault conditions.

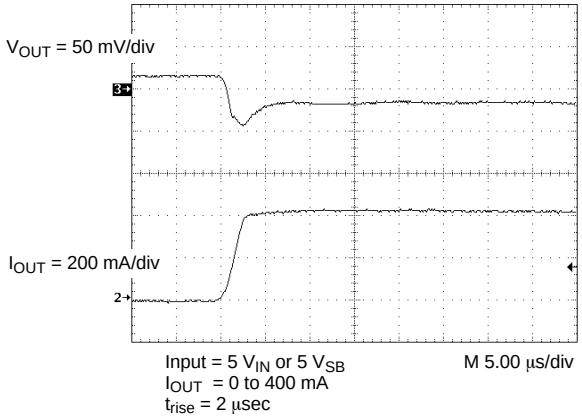

FIGURE 8. Load Transient Response-1

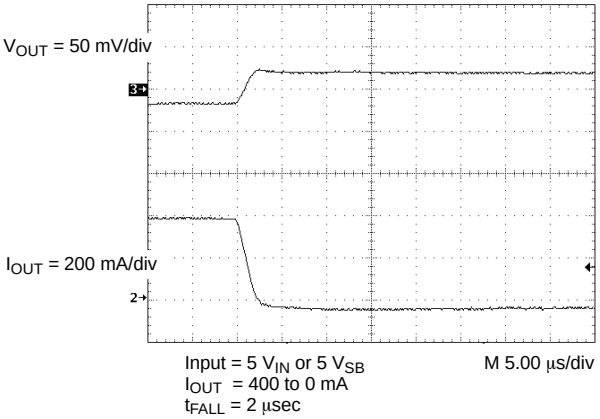

FIGURE 9. Load Transient Response-2

Loop Compensation and Load Transient Response:

For stable operation of a closed loop electronic system, such as a voltage regulator, the feedback loop needs to be compensated to keep the total phase lag encountered at less than 360°C for a signal having a total gain greater than or equal to unity. The phase lag includes the 180° phase change caused by the negative feedback.

The linear regulator closed loop has two poles. The first is a low-frequency pole (P_1) that results from the output capacitance (C_{OUT}) and the channel length modulation parameter of the p-channel MOSFET. The location of this pole changes with the output load. The second pole (P_2) is introduced by the compensation capacitor, the parasitics of the series pass element, and the error amplifier of the regulator.

The Si91860 uses an internal zero to achieve a stable feedback loop that eliminates the need to rely on the ESR value of the output capacitors. The location of the internal zero is changed to offset any effect of the load on the low-frequency pole, P_1. This internal zero also offers the freedom to use a low-ESR ceramic X5R or Y5V capacitor for lower noise. As a result of the internal compensation of the Si91860, a closed-loop bandwidth as high as 100 kHz is achieved with approximately a 60° phase margin.

High closed-loop bandwidth, along with a sufficient phase margin, results in a good dynamic load response. With a closed-loop bandwidth of 100 kHz or more, the Si91860 needs a lower output capacitor for a given dynamic load response performance. Also, the freedom to use a very low ESR ceramic capacitor further reduces the form factor for enhanced performance. The output voltage drop is the result of output capacitance, the ESR of the output capacitance, and the response time of the device for a given step load. With a 2-µs slew rate step load from zero to 400 mA, the output drops by less than 50 mV and recovers to the regulated voltage in less than 5 µs. Refer to Figures 8 and 9 for the transient load response with a 2.2-µF ceramic capacitor at the output.

$$\Delta V = \frac{I_{STEP} \times t_{RESPONSE}}{C_{OUT}} + I_{STEP} \times ESR$$

where:

I_{STEP} = Output step load (A)
ESR = ESR of Output capacitor (W)
$t_{RESPONSE}$ = Response time of the regulator (S)
$t_{RESPONSE}$ depends on the unity gain bandwidth and the phase margin of the closed loop.

Input Capacitor Selection:

The input capacitor selection is dominated by the source impedance, the resistive and inductive impedance of the trace, the rising edge hysterisis, the output capacitance, and the maximum load. The input bypass capacitor, located close to the Si91860, supports short glitches of about one microsecond. A 4.7-µF to 10-µF ceramic capacitor with Y5V dielectric is recommended for a small, low-cost solution. An X5R dielectric is recommended for better temperature characteristics. Minimizing the source trace inductance reduces the capacitance requirement.

PCB Layout:

The component placement around the Si91860 should be done carefully to achieve good dynamic line and load response. The input and output capacitors should be kept close to the Si91860. The rise in junction temperature depends on how efficiently the heat is carried away from the junction to the ambient. The junction-to-lead thermal impedance is a characteristic of the package and is fixed. By increasing the size of the copper area on the PCB, lead-to-ambient thermal impedance can be reduced. Increase the ground trace area to reduce the junction-to-ambient thermal impedance.

Although the Si91860 is provided with the input hysterisis, the system can break into oscillations if the input impedance is not low enough. The input trace inductance and resistance should be kept low to achieve overall input impedance of the source at the input of the Si91860. Wide traces from source to the primary, standby, and auxiliary inputs are recommended, with a large ground plane for the ground connection.

For a turn-on rise time (Δt) and the input inrush current (ΔI), the maximum trace/source inductance and resistance that could be tolerated can be estimated using the following equation:

$$V_{GLITCH} = (L_{TRACE(max)} \times \frac{\Delta I}{\Delta t} + R \times \Delta I)$$

L = Trace Inductance (H)

R = Source plus trace resistance (Ω)

The expected V_{GLITCH} should be less than the rising edge hysterisis of the 5-V V_{IN} and 5-V V_{SB}.

Refer to Figure 7 for an example of the observed glitch at the input terminal with a 0.05-Ω source plus trace resistance and a125-nH trace inductance. (5-inches long trace would have approximately 125-nH inductance.)

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