Designing A Low-Noise Low-Dropout Regulator with the Si9183

Nitin Kalje

INTRODUCTION

Vishay's Si9183DT is a high-performance CMOS LDO that offers one of the lowest dropout voltages in the industry in a space-saving 150-mA SOT23-5 package. Low Dropout Regulators (LDO) provide a regulated output power in battery-operated portable systems. The low dropout characteristic extends the lower operating voltage limit of the power source, thus prolonging the battery life. In addition, the low insertion loss and high ripple rejection ratio of LDOs help to reduce system noise.

Cell phones, PDAs, and other battery-powered portable devices, require a well designed power management architecture. Selecting the right components for power-management circuitry prolongs battery life by efficiently processing the power and routing any reserved power to higher functions and/or standby time. The Si9183DT's LDO characteristics are superior as determined by its low dropout voltage, ground current, peak output current capability, power dissipation noise and ripple rejection specifications. The regulator is suitable for portable and noise-sensitive appliances such as cellular phones, and, due to its low dropout voltage, is ideal as a post-regulator for switch mode power converters.

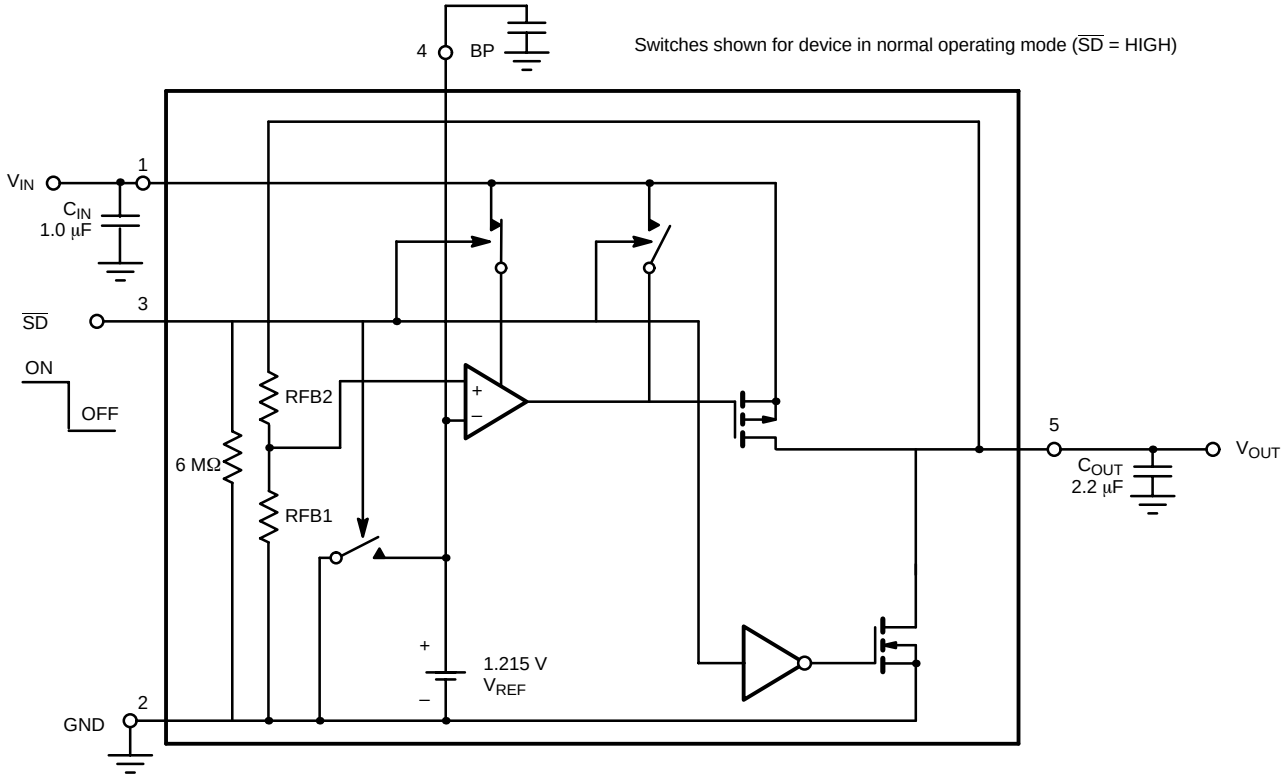


FIGURE 1. 150-mA CMOS LDO Regulator (Fixed Output)

SI9183 OPERATION

Choosing the right series pass element for the regulator is key to achieving low dropout voltages and high efficiency. LDO regulators are functionally no different than variable resistance series elements, where the voltage drop across the pass element is equal to the input-to-output voltage differential. The variable resistor can either be a bipolar transistor, controlled by the base current, or a CMOS transistor, which is controlled by the gate voltage. The series pass element operates in two different regions depending upon the input voltage. If the input voltage is higher than the output voltage, the p-channel power MOSFET operates in the saturation region and acts as a controlled current source . This drain current is a function of the transconductance of the power MOSFET $G_m = \frac{dI_D}{dV}$.

When the input voltage decreases to (V_{OUT} + ($R_{ON} \times I_{OUT}$)), the voltage regulator cannot maintain a regulated output. If the input voltage falls below this voltage, the p-channel power MOSFET enters a linear region. In this linear region, the gate voltage changes with input voltage, and is not a function of the output or control voltage. All the circuits in the Si9183DT are designed to operate with input voltages as low as 2 V and output voltages down to 1.5 V.

The maximum gate-to-source voltage (V_{GS}) is the same as the input voltage at any load or input-to-output differential. The gate-to-source voltage should be high enough to operate the p-channel MOSFET in the saturation region. The available drain current is proportional to the square of the difference between the applied and threshold gate voltage. The Si9183DT gate threshold is 0.8 V and needs a minimum V_{GS} of 1.8 V to produce a 300-mA peak current, which can be drawn for 2 ms. The package is designed to handle the power dissipated during the peak current pulse period. A low junction-to-lead thermal resistance enhances the power-handling capability of the Si9183DT.

LOOP COMPENSATION

The basic objective of closed-loop compensation is to increase the stability of the feedback loop. This is achieved by keeping the total phase lag encountered to less than 360° for a signal having a total gain of greater than or equal to unity. The phase lag includes the 180° phase change caused by the negative feedback. High closed-loop bandwidth with a solid phase margin reduces the response time and improves the dynamic line and load characteristic.

The closed loop has two poles for the Si9183. A low frequency pole, P_O, is a result of output capacitance C_{OUT} and the channel length modulation parameter of the P-Channel MOSFET. The location of this pole changes with the output load. The second pole is introduced by the compensation capacitor, parasitics of the series pass element, and the error amplifier of the regulator. The error amplifier output impedance and the gate capacitance of the power MOSFET determine the location of the second pole.

The Si9183DT uses an internal zero to achieve a stable feedback loop that eliminates the need to rely on the ESR value of output capacitors for a zero. The location of the internal zero is changed to offset any effect of the load on the low frequency pole P_O. This internal zero offers the freedom to use a low-ESR ceramic X5R or Y5V capacitor for lower output noise. By means of the internal compensation of the Si9183DT, a closed-loop bandwidth as high as 100 kHz can be achieved easily with a phase margin no lower than 60°. See Figure 2.

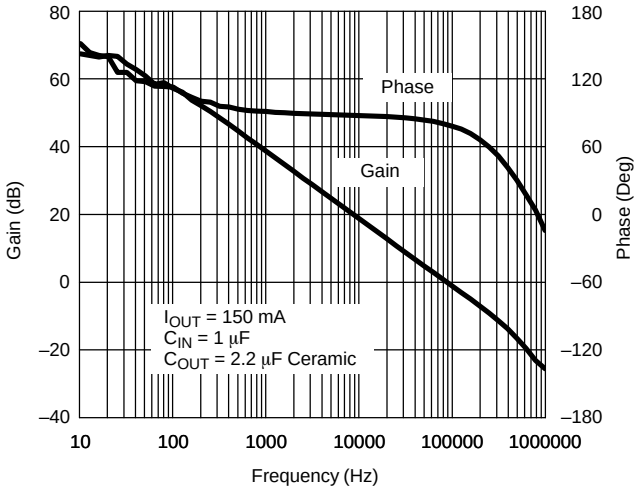


FIGURE 2. Closed Loop Bandwidth

INPUT/OUTPUT CAPACITOR SELECTION

The circuit stability and output voltage during line and load step changes dominate the selection criteria of input and output capacitors. An input bypass capacitor is required in applications involving long inductive traces between the source and LDO. For shorter traces and lower source impedance applications, a 1-µF ceramic capacitor is recommended. A higher step load at the output demands higher capacitance and a lower ESR value at the output. A 2.2-µF to 10-µF ceramic capacitor with a Y5V dielectric is recommended and an X5R dielectric is recommended for better temperature characteristics. The Si9183DT requires only a small output capacitor because of a high closed-loop bandwidth of 100 kHz or more. The unity gain cross-over frequency is lower at the higher output capacitance, as the low frequency pole P_O appears lower on the frequency scale.

The peak deviation to load transient is given by:

$$\Delta V = \frac{I_{STEP} \times t_{RESPONSE}}{C_{OUT}} + I_{STEP} \times ESR \quad (1)$$

where:

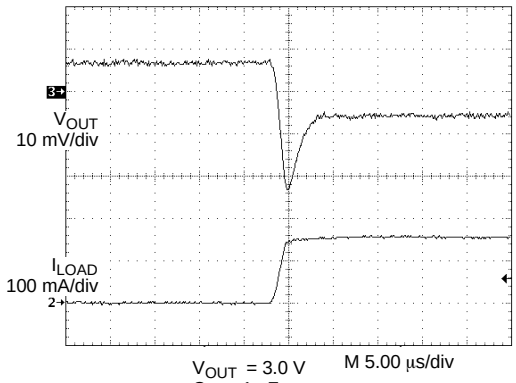
I_{STEP} = Output step load (A)
ESR = ESR of Output capacitor (Ω)
$t_{RESPONSE}$ = Response time of the regulator (s)
$t_{RESPONSE}$ depends on the unity gain bandwidth and the phase margin of the closed loop.

With a 2.2-μF ceramic capacitor at the output, the maximum deviation observed in the output voltage is 25 mV, with less than a 3-μs recovery time (refer to Figures 3 and 4). The recovery time of the output from overshoot during the load removal depends on the amount of overshoot, the output capacitor, and the load current.

SHUTDOWN

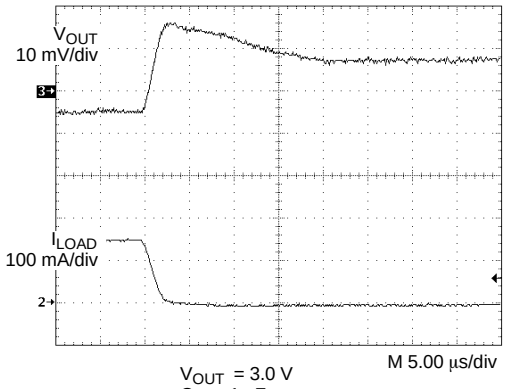
The Si9183DT is provided with an ON/$\overline{OFF}$ control pin (named $\overline{SD}$), which opens and closes the internal power MOSFET switch and controls the total current drawn by the entire circuit. The current in shutdown mode is less than 1 μA, reducing the drain on the battery in standby mode and increasing standby time. While a low at $\overline{SD}$ pin opens the switch, a high at the $\overline{SD}$ pin enables the regulator operation. This allows the Si9183DT to be used as a high-current, simple-disconnect switch that produces a regulated output. It is recommended that the user connect the SD pin to the input V_{IN} when not in use.

The output terminal is pulled low internally to quickly discharge the output capacitor when $\overline{SD}$ is pulled low. The internal pull down is approximately 150 Ω and requires 2 ms to discharge the 2.2-μF output capacitor. Refer to Figures 5 and 6 for turn-on and turn-off of waveforms.



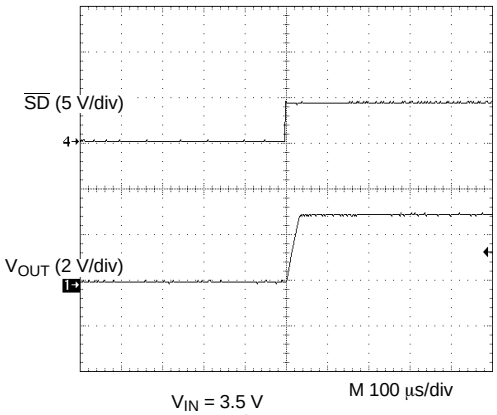
V_{OUT} = 3.0 V
C_{IN} = 1 μF
C_{OUT} = 2.2 μF
I_{LOAD} = 1 to 150 mA
t_{rise} = 2 μsec
V_{IN} = 4.0 V

FIGURE 3. Load Transient Response — 1



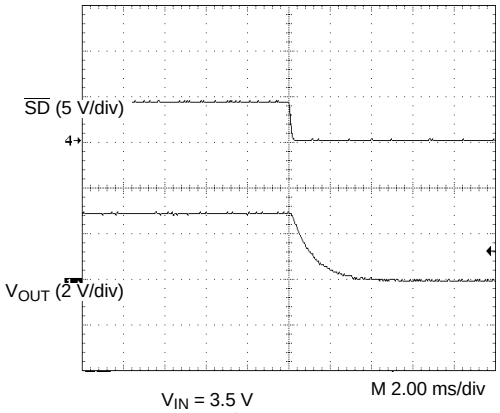
V_{OUT} = 3.0 V
C_{IN} = 1 μF
C_{OUT} = 2.2 μF
I_{LOAD} = 150 to 1 mA
t_{fall} = 2 μsec
V_{IN} = 4.0 V

FIGURE 4. Load Transient Response — 2



V_{IN} = 3.5 V
V_{OUT} = 2.5 V
I_{OUT} = 0 mA
C_{IN} = 1 μF
C_{OUT} = 2.2 μF

FIGURE 5. Si9183DT — Turn-on Through $\overline{SD}$



V_{IN} = 3.5 V
V_{OUT} = 2.5 V
I_{OUT} = 0 mA
C_{IN} = 1 μF
C_{OUT} = 2.2 μF

FIGURE 6. Si9183DT — Turn-off Through $\overline{SD}$

ADJUSTABLE/LOW NOISE FIXED OUTPUT VOLTAGE VERSIONS

The Si9183DT is available in two versions. Version A has a fixed output and the provision for bypassing the bandgap reference for lower noise. The fixed output options are 1.5 V, 1.8 V, 2.0 V, 2.5 V, 2.8 V, 3.0 V, 3.3 V, 3.6 V, and 5.0 V. In Version B, the non-inverting input of the error amplifier is connected to the FB pin to provide an adjustable output. The lower resistor R2 of the sensing network should be in the 25-kΩ to 150-kΩ range for low power consumption while maintaining adequate noise immunity. (refer to Figures 7 and 8). Calculate the high-side resistor using the equation:

$$R1 = \frac{(V_{OUT} - 1.215)}{1.215} R2 \qquad (2)$$

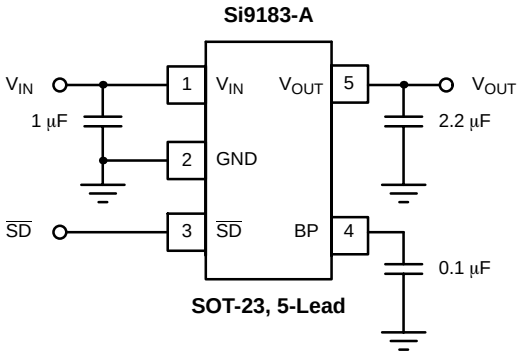


FIGURE 7. Version A with Low Output Noise

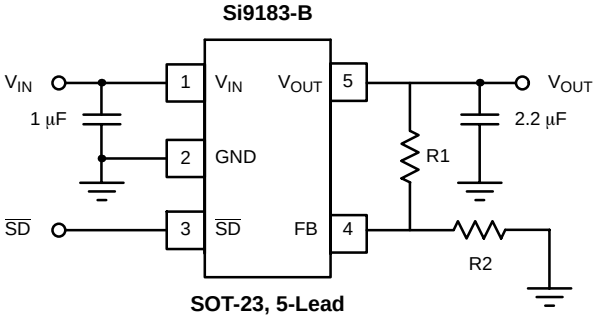


FIGURE 8. Version B with Adjustable Output

POWER DISSIPATION

The Si9183DT is rated to deliver up to a 300-mA peak current for 2 ms. This maximum load current is specified for continuous operation and for finite pulse widths. Maximum allowable junction temperature, junction-to-ambient thermal impedance at a thermal equilibrium, and the ambient temperature all determine the continuous current rating at a given input-to-output differential. The input voltage, p-channel power MOSFET transconductance, and the transient thermal impedance between the junction and lead are major issues for the peak current amplitude and the pulse width. The maximum power dissipation allows for a safe junction temperature and is calculated using the following equation:

$$P_D = (V_{IN} - V_{OUT}) I_{OUT} + V_{IN} \times I_{GND}$$

$$\text{Efficiency} = \frac{V_{OUT} \times I_{OUT}}{V_{IN}(I_{OUT} + I_{GND})} \qquad (3)$$

$$P_{DMAX} = \frac{(150 - T_A)}{\theta_{JA}}$$

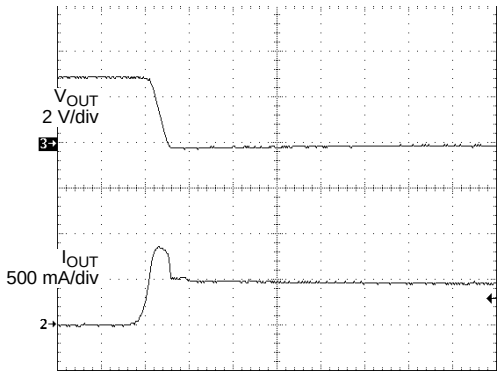
where:

θ_{JA} = 180°C/W (All leads soldered to PC board on 1-oz copper)

PROTECTION CIRCUITRY

Short Circuit

In the event of a short circuit in the load powered by an LDO, the Si9183DT limits the maximum current to prevent damage to the electronics. The peak current through the Si9183DT is typically limited to 400 mA during a continuous short circuit at the output. Refer to Figure 9. The current overshoot at the short circuit is an output capacitor discharge. The Si9183 uses low capacitor, limiting the total energy discharge in the electronics.



$V_{IN} = V_{OUT} + 1$
$C_{OUT} = 2.2\ \mu F$
$C_{IN} = 1\ \mu F$

FIGURE 9. Output Short Circuit Current

Over-Temperature

The Si9183DT is designed with an over-temperature protection circuit to prevent thermal runaway in the p-channel power MOSFET. If the temperature reaches 165°C, an internal control circuit shuts off the p-channel power MOSFET. The LDO will be disabled until the chip temperature drops below 145°C, and will re-engage automatically. The 20°C temperature difference avoids possible oscillation and reduces the average power delivery during fault conditions to reduce the risk of damage. Refer to Figure 10.

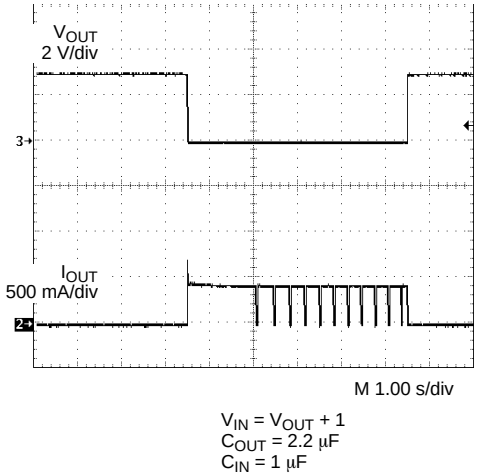


FIGURE 10. Output Short Circuit Protection

PCB Layout

The component placement around the LDO should be done carefully to achieve good dynamic line and load response. The input and noise capacitor should be kept close to the LDO. The rise in junction temperature depends on how efficiently the heat is carried away from junction-to-ambient. The junction-to-lead thermal impedance is a characteristic of the package and is fixed. The thermal impedance between lead-to-ambient can be reduced by increasing the copper area on PCB. Increase the input, output and ground trace area to reduce the junction-to-ambient thermal impedance.

littlediode
COMPONENTS FOR ALL

Littlediode supplies new, hard to find or obsolete electronic components and semiconductors all over the world.

With over two million different components listed you are sure to find the part you need.

Feel free to visit us today at our online store:

LittleDiode.com

Looking forward to providing you with the best possible service.