Designing A High-Frequency, Higher-Power Buck/Boost Converter for Multi-Cell Input Configurations Using Si9168

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INTRODUCTION

The Si9168 is a high-frequency synchronous dc-to-dc controller designed for higher-power buck or boost conversion applications in end products running off 2-cell Lithium Ion or 6-cell NiCd or NiMH battery packs. Like the lower-power Si9167, the Si9168 is capable of operating at up to 2 MHz while offering the flexibility to choose the optimum drivers for higher current handling. Its high-frequency operation, strong totem pole drivers, selectable PWM/PSM operation modes, integrated under-voltage lockout, and soft-start features make the Si9168 suitable for 1-A to 10-A conversion applications. A synchronization feature allows designers to use multiple Si9168s for a complete power management system, where size and cost are a prime importance. The Si9168 is designed to promote efficient use of battery energy and to allow the use of smaller form factors, thanks to better heat dissipation and thereby lower operating junction temperature of power management components.

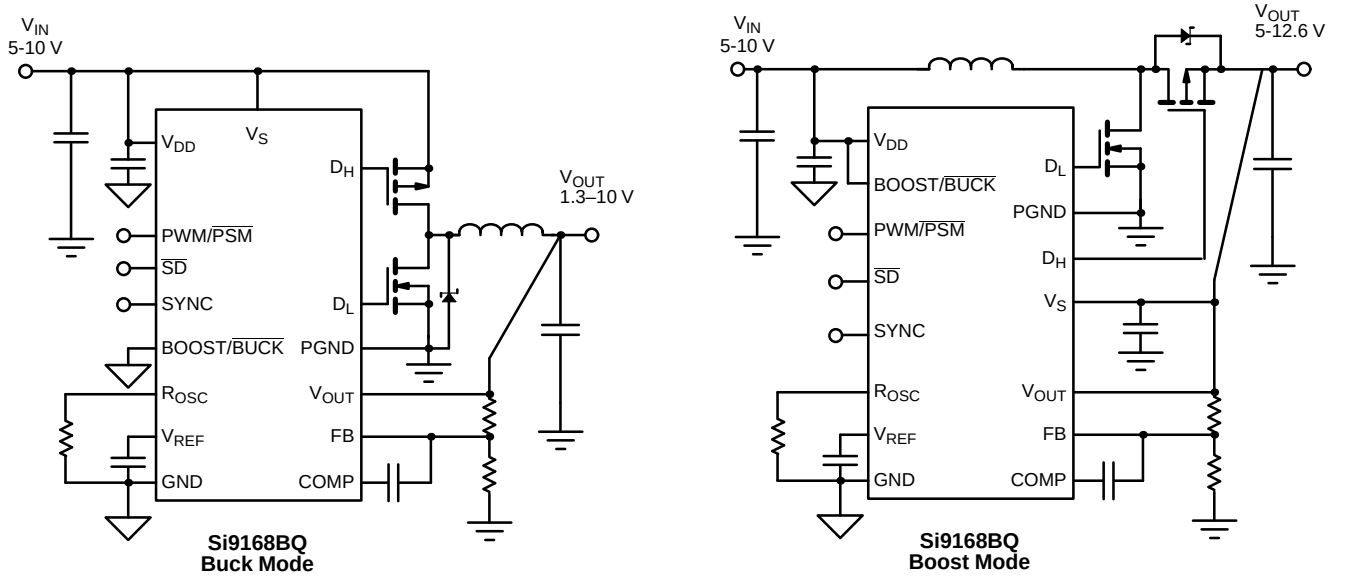
DESIGN GUIDELINES

The features and functions of the Si9168 are described in detail in the product data sheet. The following section provides design guidelines for the creation of buck and boost dc-to-dc converters using the Si9168.

Oscillator Frequency—Choosing R_{OSC}

The oscillator function is implemented with an RS flip-flop, an inverter, an internal capacitor, a temperature-compensated current source, and an external resistor. The oscillator ramp is generated by charging the internal capacitor with a constant current source. This current is mirrored from the current in R_{OSC}. The capacitor is charged from 0.5 V to a 1-V threshold, where it is discharged at a faster rate and the flip-flop is reset for the next cycle. The lower the value of Rosc, the higher the charging current and the higher the oscillator frequency. The oscillator is guaranteed to operate within ±20% with a 1% R_{OSC} for the 200-kHz to 2-MHz frequency range. Refer to Figure 2 to set the oscillator frequency.

APPLICATION SCHEMATIC



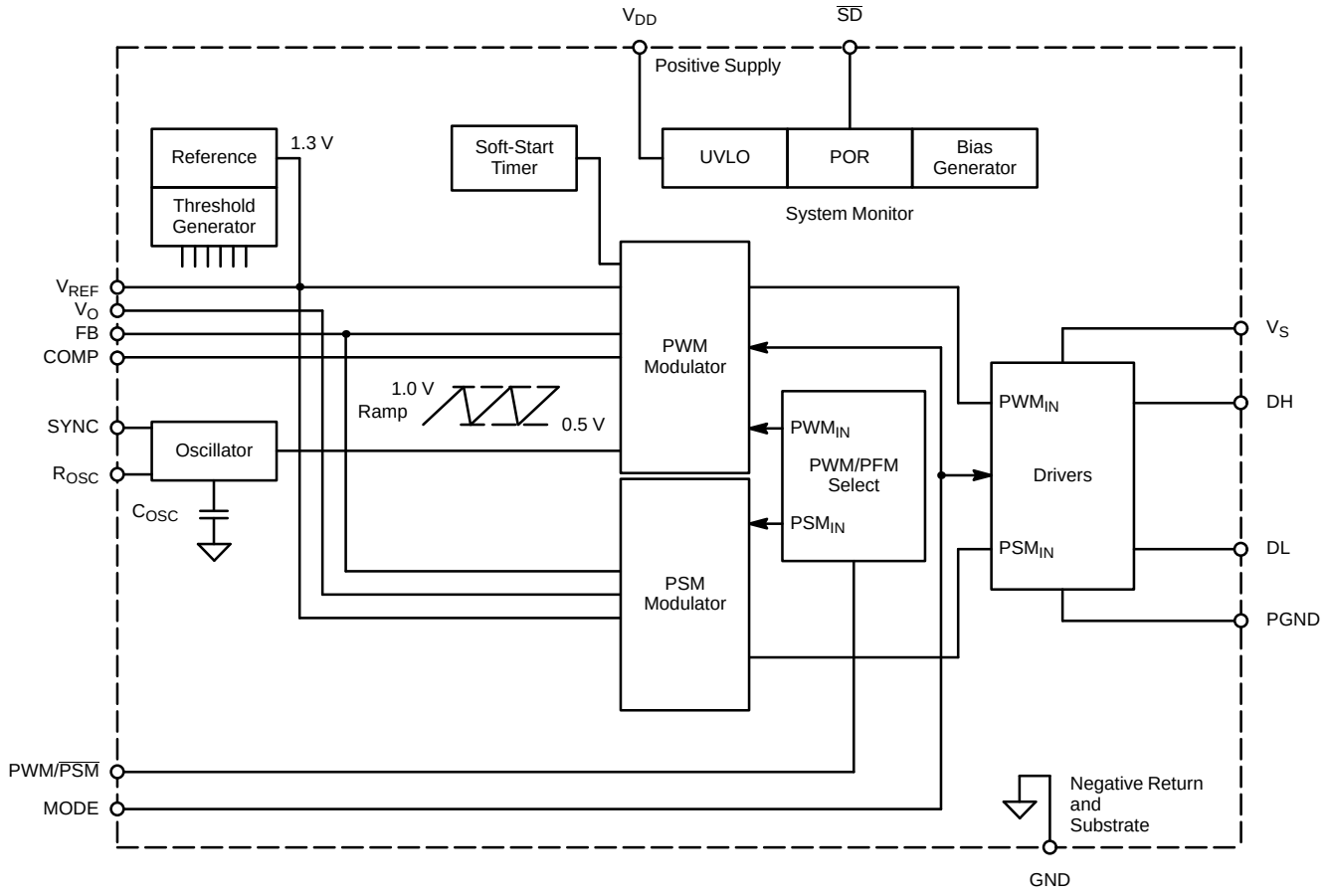


FIGURE 1.

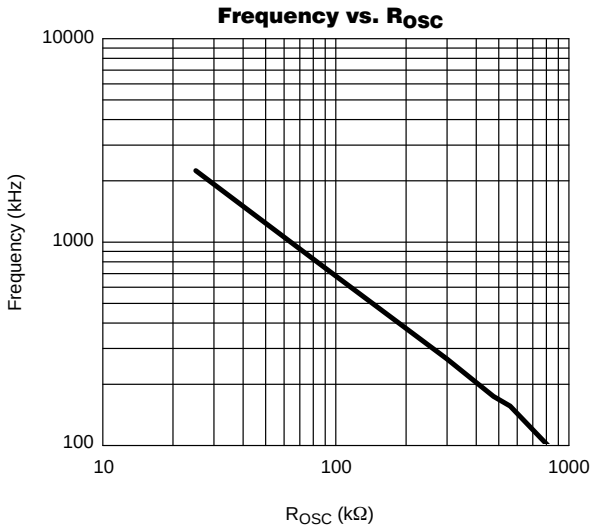


FIGURE 2. Frequency Setting

Synchronization

The internal single-shot circuit resets the flip-flop at the low-going edge of the external synchronization pulse. The external clock driving the synchronization pin does not get loaded because of the low input capacitance seen at the synchronous pin. At every cycle, the low-going external clock pulse would end the positive ramp and start the next cycle. Obviously, the external clock frequency needs to be at least 20% higher than the internal oscillator frequency for reliable synchronization. In addition, the minimum low pulse width must be 50 nS, while the fall time should not exceed 50 nS (refer to Figure 3). Figure 4 shows the synchronization achieved with the external clock running at 1.2 times the internal oscillator frequency.

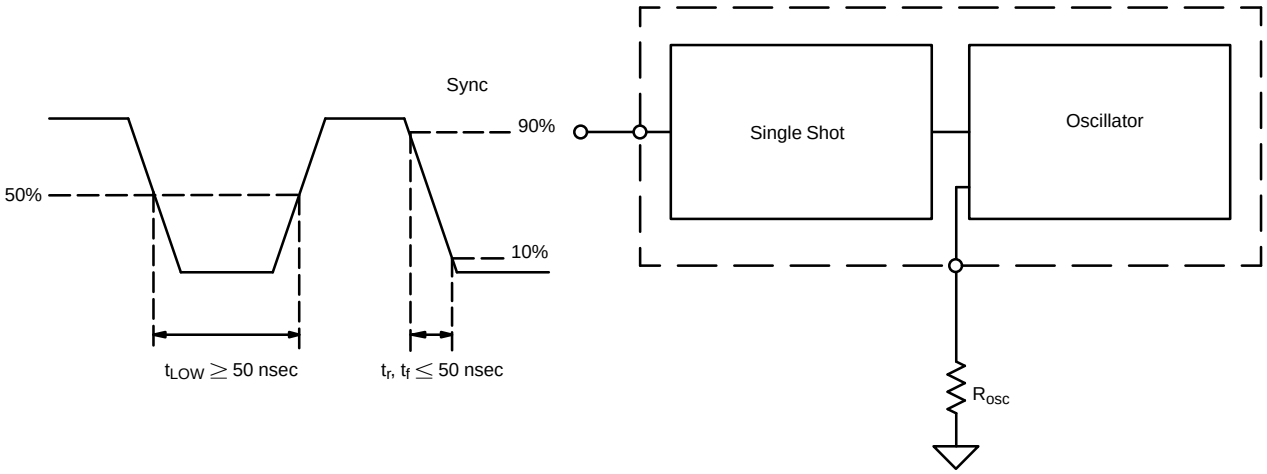
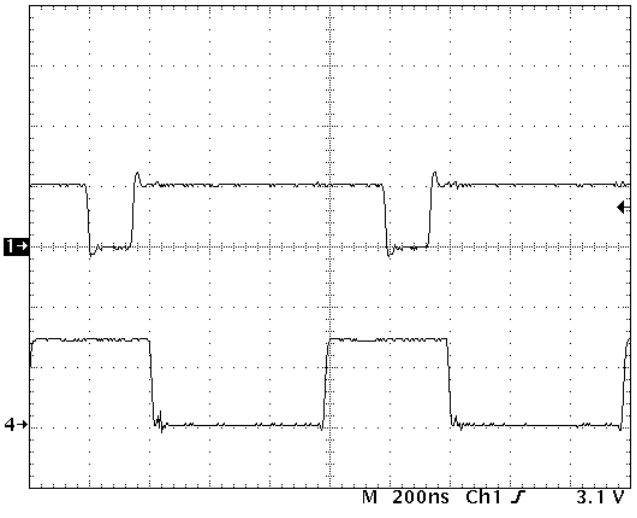


FIGURE 3. Synch Pulse Width



Ch1 – External Clock (5 V/div)
Ch4 – Drive Output (5 V/div)
F_{OSC} (Internal) – 825 kHz
F_{CLOCK} (External) – 1 MHz

FIGURE 4. Synchronization

Duty Cycle

In PWM mode, the controller operates at a fixed frequency determined by R_{OSC}. The duty cycle in buck or boost mode is a function of the difference in the input and output voltage levels, with the maximum duty ratio at a minimum input line.

At 2 MHz, the duty cycle in buck mode increases gradually up to a typical level of 80% before jumping instantaneously to 100%. At this time, the upper switch is continuously in the on state and the converter functions as a low dropout regulator. The difference between the input and output voltages is equal to the resistive drop in the upper MOSFET switch, the inductor, and the printed circuit board (pcb) traces. Since the fixed break-before-make (BBM) time causes this sudden jump, the maximum duty cycle the converter can attain before going into LDO mode will increase at lower switching frequencies.

In boost mode, the same phenomenon is observed when the duty cycle needs to be reduced down to 0%. The decrease will be gradual from 75% to 5% and abrupt from 5% to 0%. The maximum duty cycle in boost mode is limited in order to provide a fixed off-state time for an inductor to discharge before the next cycle. Obviously, the maximum achievable duty cycle is inversely proportional to the switching frequency of the converter. Refer to Figure 5 and Figure 6 for typical maximum duty cycles at selected operating frequencies.

Before selecting the operating frequency, ensure that the maximum duty cycle required at the minimum input and maximum output voltages and loads is less than or equal to the maximum provided by the Si9168. Refer equations 1 and 2 to calculate the maximum operating duty cycle at the rated load.

$$D_{MAX-BUCK} = \frac{V_{OUT\_MAX} + V_{ESR} + V_{TRACE}}{V_{IN\_MIN} - r_{DS\_p} \times I_{OUT}} \quad (1)$$

$$D_{MAX-BOOST} = \frac{V_{OUT\_MAX} + V_{ESR} + V_{TRACE} + r_{DS\_p} \times I_{IN} - V_{IN\_MIN}}{V_{OUT\_MAX} + I_{IN}\left(r_{DS\_p} - r_{DS\_n}\right)} \quad (2)$$

Where,

V_{ESR},V_{TRACE} = dc voltage drop across inductor ESR, PCB traces (V)

r_{DS_p}, r_{DS_n} = on-resistance of p- or n- channel MOSFET at an operating junction temperature (Ω)

V_{IN_MIN}, V_{OUT_MAX} = extreme minimum input and maximum output voltage (V)

I_{IN}, I_{OUT} = input supply and output load currents (A)

MOSFET Selection

Synchronous rectification is used to achieve the best possible efficiency at moderate to high load currents. A moderate to high load can be defined as the value at which the total voltage drop across the synch switch is less than the forward voltage drop of the Schottky rectifier, which otherwise is used in asynchronous dc-dc converter. At lower loads, the switching losses of the synchronous switch can outweigh the dc losses. Under such circumstances, the Si9168 operates in pulse skipping mode, where it shuts off the synchronous switch driver and allows the parallel Schottky diode to conduct. Selection criteria for the power MOSFET include on-resistance ($r_{DS(on)}$), total gate charge(Q_g), rise/fall time (t_r/t_f) and gate threshold ($V_{GS(th)}$).

MOSFET on-resistance is inversely proportional to the number of cells or the channel width, while the gate capacitance increases with the channel width. The product of the gate charge and on-resistance is thus a figure of merit, with a lower number signifying better performance. Vishay offers a wide range of PWM-optimized MOSFETs using Trench technology to provide the lowest product of on-resistance times gate charge. Lower gate charge is needed to reduce CV^2 as well as cross conduction losses by reducing the rise and fall times for a given peak gate current drive. This is critical especially when operating at a higher input voltages. It is also recommended to use a high gate threshold (4.5-V) MOSFET to reduce the CV^2 losses further. One good approach to selecting the appropriate level of on-resistance is to calculate the dc and total switching power losses at a load level where the converter will be operating most of the time and then choose a MOSFET with dc losses equal to or less than 40% of the total dc and switching losses combined. Refer to equations 3 through 10 to estimate the MOSFET dc (P_{dc}) and switching (P_{sw}) power losses in buck and boost converters at a nominal line and load.

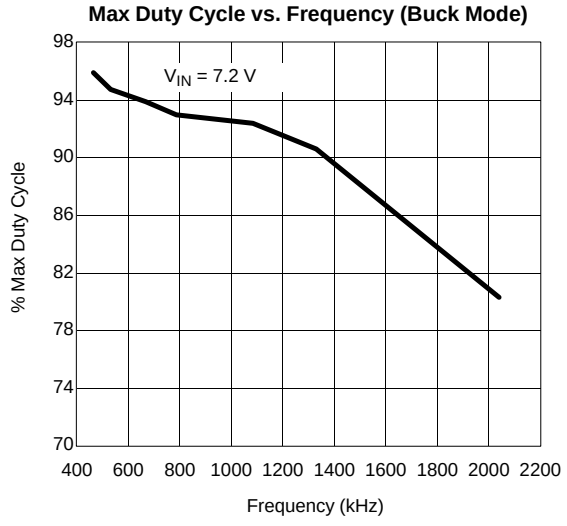


FIGURE 5.

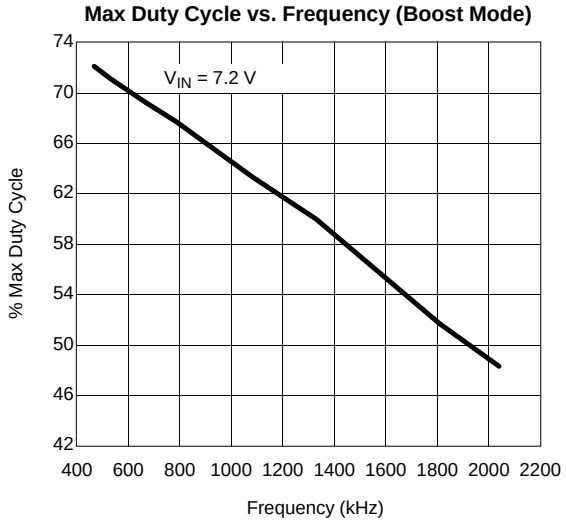


FIGURE 6.

Buck Converter

$$P_{sw-n} = Q_{gn} \times V_{in} \times F_{sw} \quad (3)$$

$$P_{dc-n} = 1.4 \times I_{rms-n} \times r_{DS(on)\_n} \quad (4)$$

$$P_{sw-P} = Q_{gp} \times V_{in} \times F_{sw} + \frac{V_{in} \times I_{pk} \times (t_r + t_f)\ f_{sw}}{2} \quad (5)$$

$$P_{dc-p} = 1.4 \times I_{rms-p} \times r_{DS(on)\_p} \quad (6)$$

Boost Converter

$$P_{sw-n} = Q_{gn} \times V_o \times f_{sw} + \frac{V_o \times I_{in} \times (t_r + t_f)}{2} \quad (7)$$

$$P_{dc-n} = 1.4 \times I_{rms-n} \times r_{DS(on)\_n} \quad (8)$$

$$P_{sw-P} = Q_{gp} \times V_{in} \times f_{sw} \quad (9)$$

$$P_{dc-p} = 1.4 \times I_{rms-p} \times r_{DS(on)\_p} \quad (10)$$

Where,

$r_{DS(on)\_p}$, $r_{DS(on)\_n}$ = on-resistance of the p- or n-channel MOSFET at 25°C junction temperature (Ω)

Q_{gn}, Q_{gp} = specified total gate charge for n-, p-channel switches at V_{IN} (C)

t_r, t_f = rise/fall time of respective switches (sec)

I_{rms-n}, I_{rms-p} = RMS currents in n-/p-channel switches (A) (see Appendix)

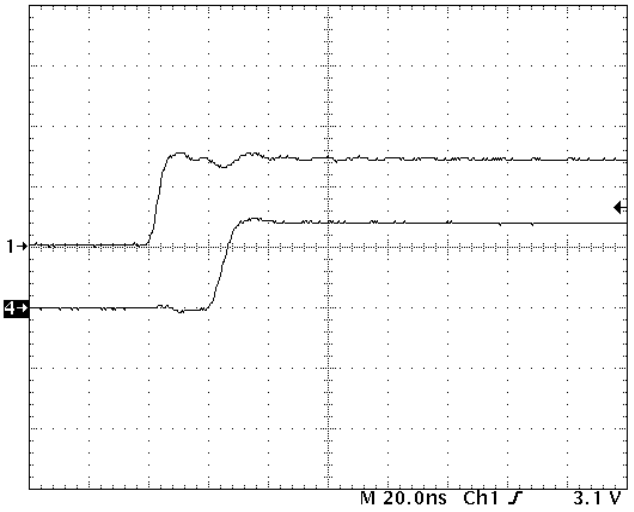
Once the dc and switching losses are determined, make sure that the MOSFET package can handle the power dissipation without the junction temperature going above 125°C in worst-case line/load and ambient temperature conditions.

Diode Selection

In PSM operation, the synchronous switch (n-channel in buck configurations and p-channel in boost configurations) is switched off to reduce switching losses. The circuit works as a non-synchronous buck or boost converter, where the diode freewheels during the off cycle. The operating frequency in PSM is kept relatively low to reduce switching losses, which means that dc losses can become significant if the parasitic body diode is used as a free wheeling diode. The use of a low forward drop Schottky diode is thus recommended to achieve good efficiency results in PSM operation.

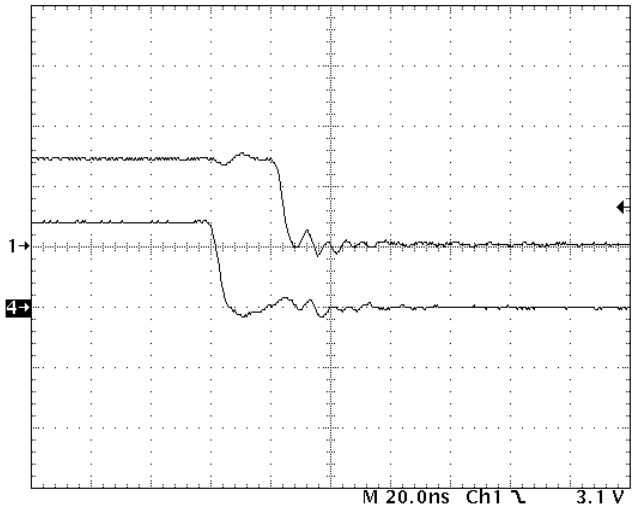
The other reason the parasitic body diode cannot be used as a freewheeling diode is its dynamic behavior, the effect of which becomes more significant during high frequency PWM operation. Break before make is internally set at about 40 nS, to avoid any possible shoot-through during the transition time. The MOSFET internal body diode, being a silicon p-n junction diode, can experience a significant reverse recovery minority carrier charge if used to conduct in the forward direction during the BBM period. The result is almost the same as shoot-through without BBM and the losses are proportional to the operating frequency. At the operating frequencies above 1 MHz, these could reduce efficiency significantly.

The Schottky should be chosen such that at a maximum peak inductor current, the forward drop is less than the forward breakdown of internal body diode. Figure 7 and 8 shows the practical waveforms explaining the BBM.



Ch1 – D_H (p-channel Drive Output) (5 V/div)
Ch4 – D_L (n-channel Drive Output) (5 V/div)

FIGURE 7. Break Before Make (N-channel turn on)



Ch1 – D_H (p-channel Drive Output) (5 V/div)
Ch4 – D_L (n-channel Drive Output) (5 V/div)

FIGURE 8. Break Before Make (P-channel turn on)

Inductor and Capacitor

Proper inductor and capacitor values should be chosen to achieve the specified input/output ripple, for a selected operating frequency. For a converter, operating at near one-megahertz switching frequency, the low ESR ceramic capacitors with values as low as 10 μF are good enough to achieve 10-mV_{p-p} ripple/noise at the output. The inductor value determines the ripple current(ΔI) in the inductor and output capacitor, for given input/output voltages and switching frequency. The total peak-to-peak output ripple is contributed by the ΔV_{ESR}, caused by the ESR of the ouptut capacitor and the ΔV_C, caused by the loss of charges from the output capacitor. Equal contribution of ripple voltage from the ESR and capacitance can be assumed for high frequency converters using the low ESR ceramic capacitors.

Buck

Refer to equation 11 in appendix to calculate the inductance value for a $\Delta I = 0.2\ I_{OUT}$. The capacitor value and ESR for output capacitor are estimated using the following equation:

$$ESR = \frac{\Delta V_{ESR}}{\Delta I}$$

$$C_{OUT} = \frac{1}{\Delta V_C} \times \frac{1}{2} \times \left[\frac{1}{2F_{sw}} \times \frac{\Delta I}{2}\right].$$

$$\text{Output Ripple } \Delta V_{p-p} = \Delta V_{ESR} + \Delta V_C.$$

Boost

Refer to Application Note AN715 to determine the required inductance for a continuous conduction mode boost conversion.

$$L_{MIN} = \frac{V_{IN}^2 \times D \times \eta}{2 \times F_{sw} \times V_{OUT} \times I_{OUT\_MIN}}$$

In a boost converter, entire load current is supplied by the output capacitor when the main switch is ON. Obviously, the output capacitance required to support the load is quite high, especially at a higher duty cycle. Moreover, the output capacitor ESR needs to be low enough for minimum voltage drop across it, while supporting the load. Use the following equation to calculate the output capacitor, for a specified ripple performance.

$$ESR = \frac{\Delta V_{ESR}}{\Delta I}$$

$$C_{OUT} = \frac{I_{OUT} \times D_{MAX}}{\Delta V_C \times F_{sw}}.$$

$$\text{Output Ripple } \Delta V_{p-p} = \Delta V_{ESR} + \Delta V_C.$$

Where,

L_{MIN} = inductance required to remain in continuous conduction mode operation (H)

D_{MAX} = maximum duty cycle at minimum V_{IN}

η = converter efficiency

I_{OUT_MIN} = minimum output current for continuous conduction mode (A)

APPENDIX

Use the following equations to calculate dc, peak, and rms values of currents in the n- and p-channel switches in buck or boost converter designs.

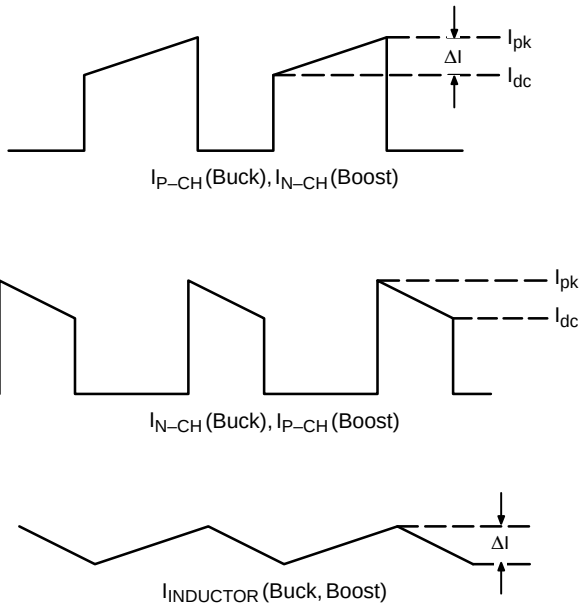


FIGURE 9. Current Waveform (Buck, Boost)

Buck Converter

$$\Delta I = \frac{(V_{in} - V_O) \times D}{L \times f_{sw}}$$

$$D = \frac{1.05\ V_O}{V_{in}} \qquad (2)$$

$$I_{dc} = I_o - \frac{\Delta I}{2}$$

$$I_{pk} = I_o + \frac{\Delta I}{2}$$

$$I_{rms-p} = \sqrt{\left(I^2_{dc} + I^2_{pk} + I_{dc} \times I_{pk}\right) \frac{D}{3}} \qquad (3)$$

$$I_{rms-n} = \sqrt{\left(I^2_{dc} + I^2_{pk} + I_{dc} \times I_{pk}\right) \frac{I - D}{3}}$$

Boost Converter

$$\Delta I = \frac{V_{in} \times D}{f_{sw} \times L} \qquad (4)$$

$$D = \frac{1.1\ (V_o - V_{in})}{V_o}$$

$$I_{dc} = I_{in} - \frac{\Delta I}{2}$$

$$I_{pk} = I_{in} - \frac{\Delta I}{2}$$

$$I_{rms\_p} = \sqrt{\left(I^2_{dc} + I^2_{pk} + I_{dc} \times I_{pk}\right) \frac{1-D}{3}}$$

$$I_{rms\_n} = \sqrt{\left(I^2_{dc} + I^2_{pk} + I_{dc} \times I_{pk}\right) \frac{D}{3}}$$

Where,

ΔI = Peak-to-Peak ripple current (A)
D = Converter Duty Cycle
I_{dc}, I_{pk} = Refer to Figure 9
I_L = Inductor Current (A)
I_{rms-P}, I_{rms-n} = RMS current thru P, N-channel switch (A)
f_{sw} = Converter switching frequency (Hz)

ADDITIONAL WAVEFORMS AND PERFORMANCE DATA

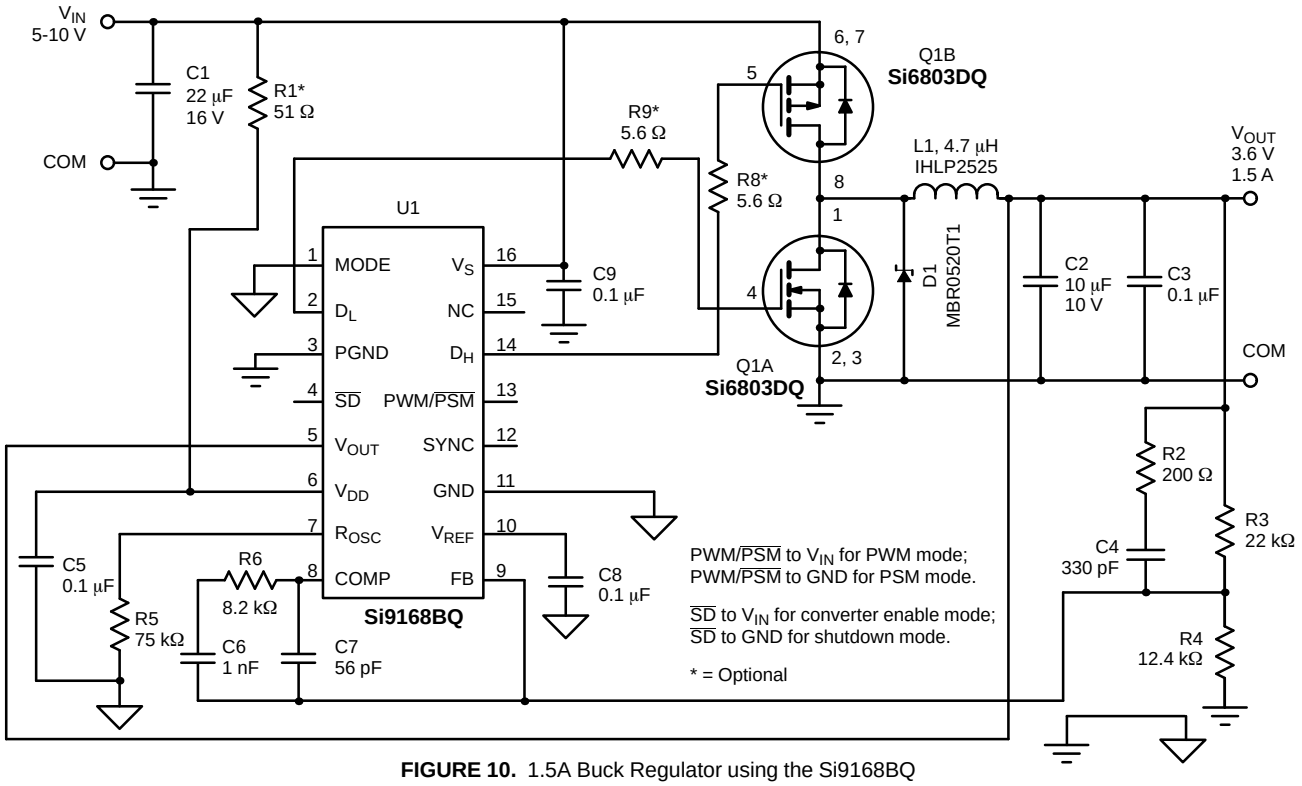


FIGURE 10. 1.5A Buck Regulator using the Si9168BQ

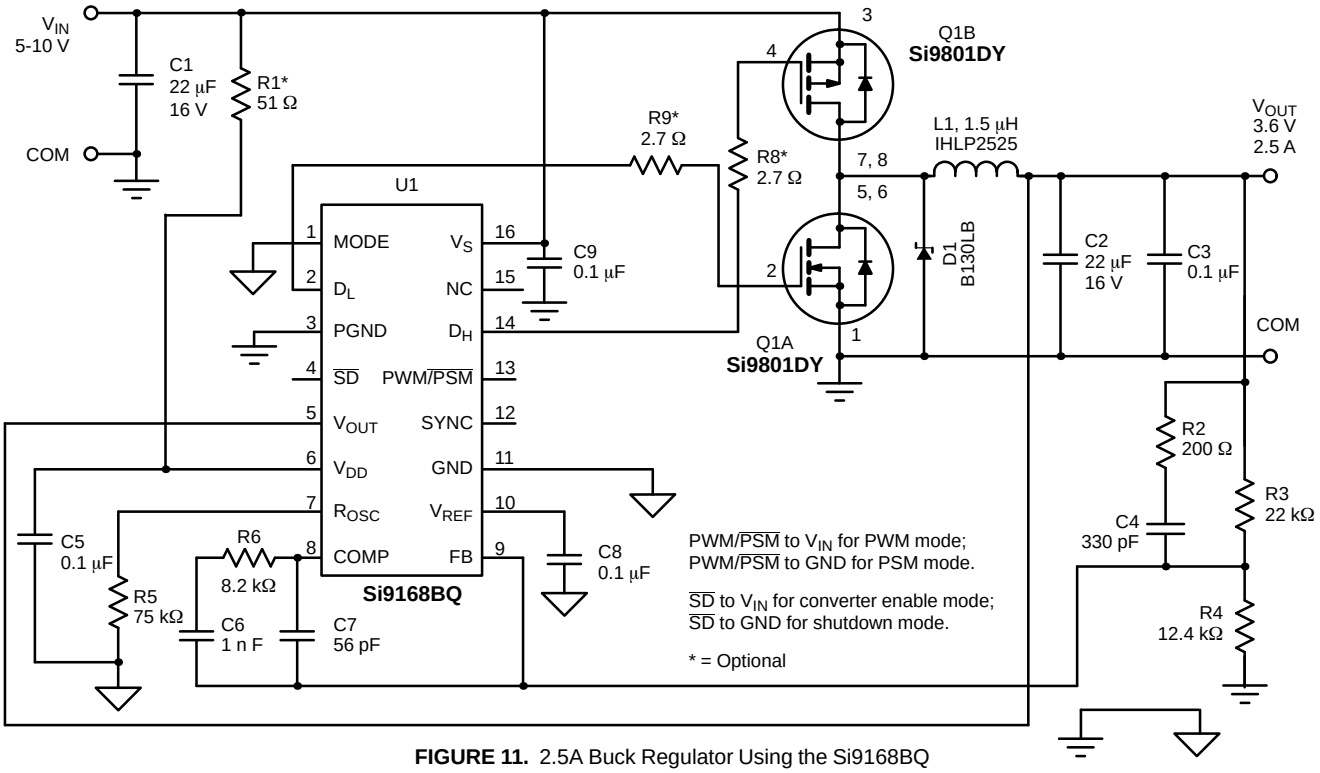


FIGURE 11. 2.5A Buck Regulator Using the Si9168BQ

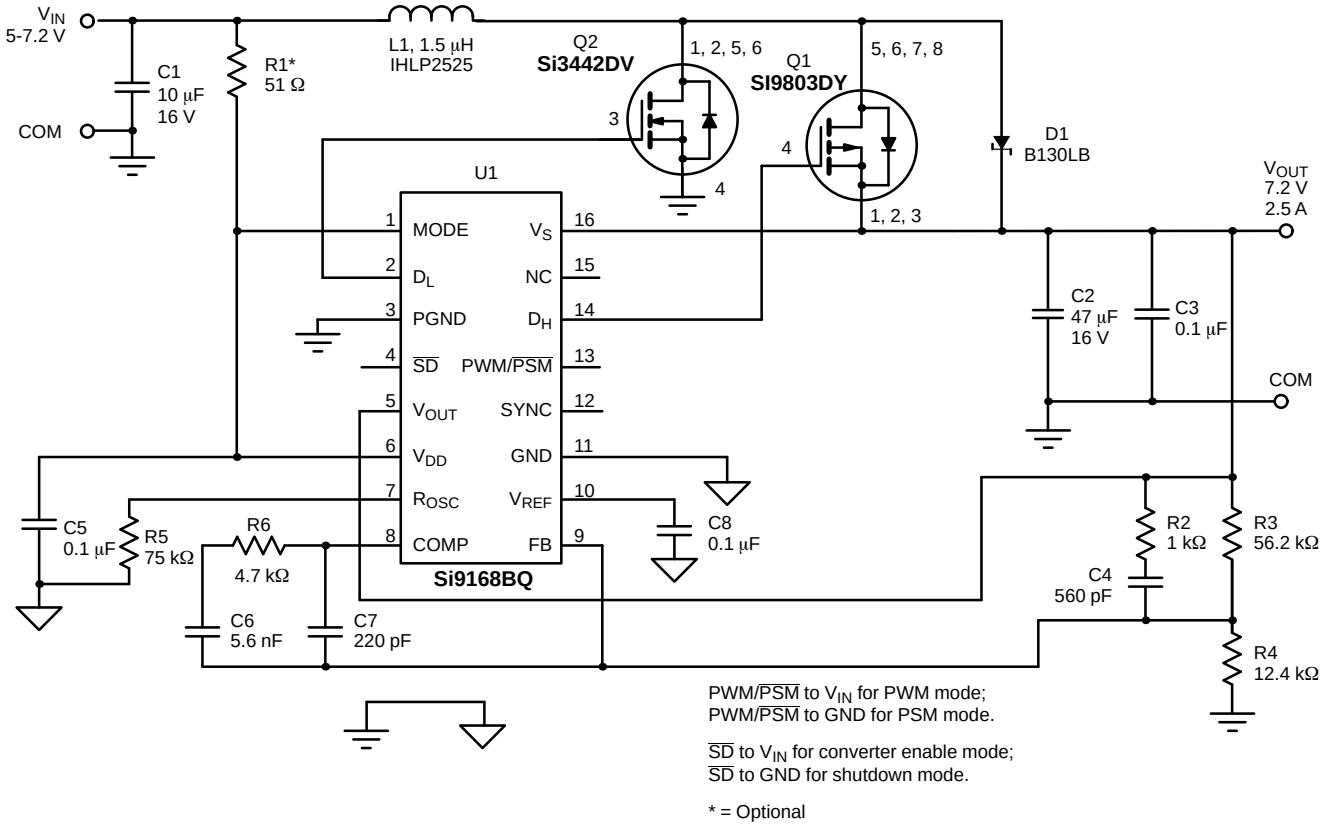


FIGURE 12. 7.2-V_O/2.5-A Boost Regulator Application

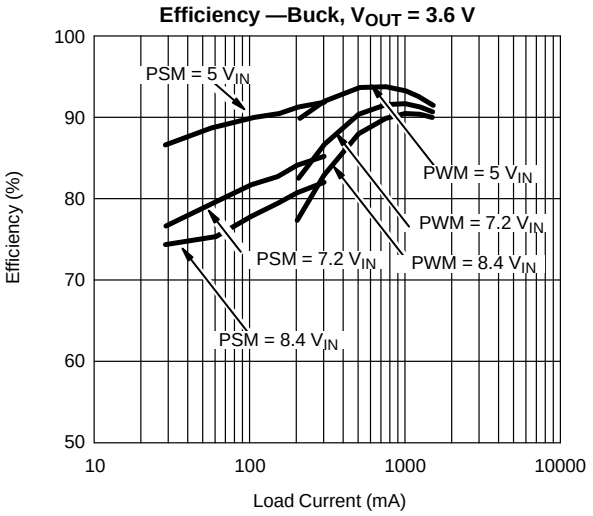


FIGURE 13. Efficiency—1.5-A Buck Converter

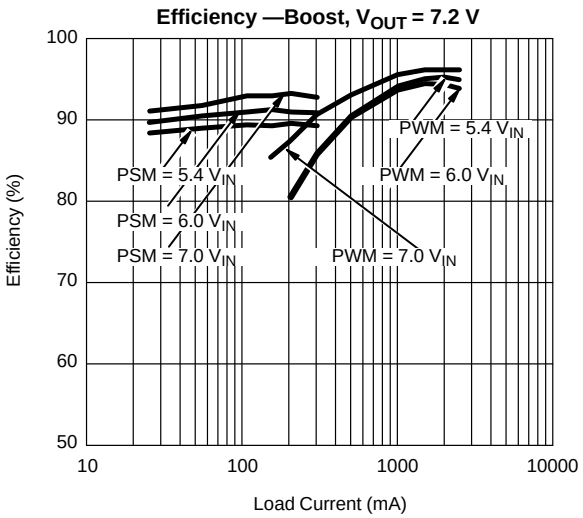
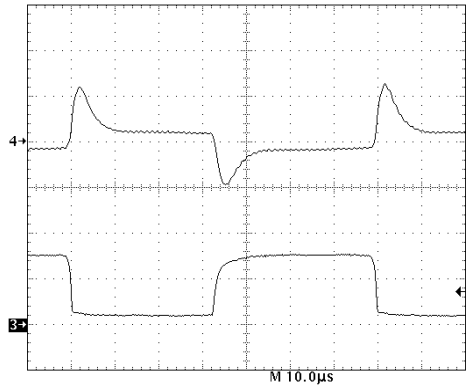
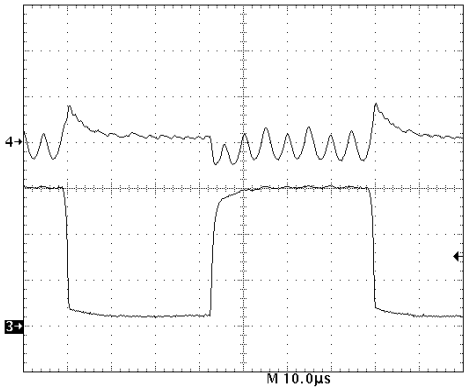


FIGURE 14. Efficiency—Boost Converter



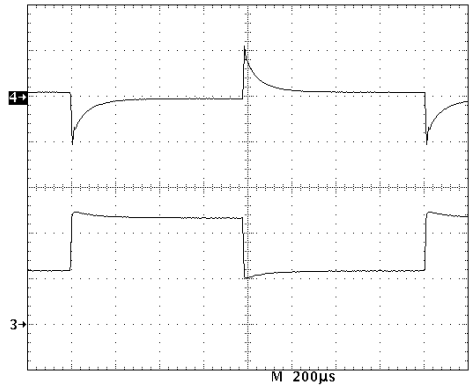
V_{IN} = 7.2 V, V_O = 3.6 V
Slew Rate – 1A/µsec
Ch 3 – Load (1A/div)
Ch4 – Output (200 mV/div)

FIGURE 15. Dynamic Load Response Buck Converter – PWM



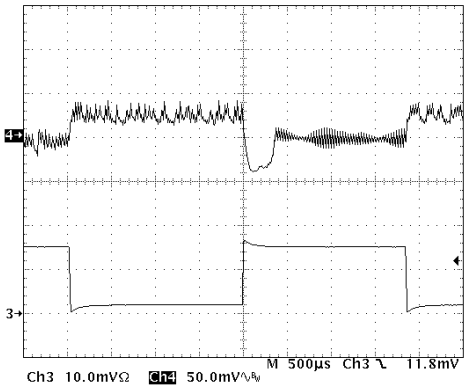
V_{IN} = 7.2 V, V_O = 3.6 V
Slew Rate – 1A/µsec
Ch 3 – Load (100 mA/div)
Ch4 – Output (100 mV/div)

FIGURE 16. Dynamic Load Response Buck Converter – PSM



V_{IN} = 5.4 V, V_{OUT} = 7.2 V
Slew Rate – 1A/µsec
Ch 3 – Load (1A/div)
Ch4 – Output (200 mV/div)

FIGURE 17. Dynamic Load Response Boost Converter – PWM



V_{IN} = 5.4 V, V_{OUT} = 7.2 V
Slew Rate – 1A/µsec
Ch 3 – Load (200 mA/div)
Ch4 – Output (50 mV/div)

FIGURE 18. Dynamic Load Response Boost Converter – PSM

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