Design A High Performance Buck or Boost Converter With Si9165

by Kin Shum

INTRODUCTION

The Si9165 is a controller IC designed for dc-to-dc conversion applications with 2.7-V to 6-V input voltage. Its high operating frequency, high efficiency, high level of integration, and low noise make Si9165 the best solution yet for cellular phone power conversion. The Si9165 can be easily configured as a synchronous buck or a boost converter with internal MOSFETs operating at switching frequencies as high as 2 MHz, which enables smaller and lighter designs. Its current capability is 600 mA with a 3.3-V or higher input voltage. High efficiency can be preserved at light load by running the converter in Pulse Skipping Modulation (PSM) mode.

Key functions of the Si9165 controller are discussed in the “Description” section of the datasheet. In this application note, additional information is provided, including design guidelines for both buck and boost configurations. Some test results are also presented. Note that the tips provided apply only to designing with the Si9165 controller. Please review Siliconix application notes AN715 and AN710 for more general design guidelines.

IC DESCRIPTION

The Si9165 is a BiCMOS controller for dc-to-dc conversion applications. Packaged in a TSSOP-20, it contains both active components required for the converter and requires minimum external components. A functional block diagram of the IC internal structure is shown in Figure 1.

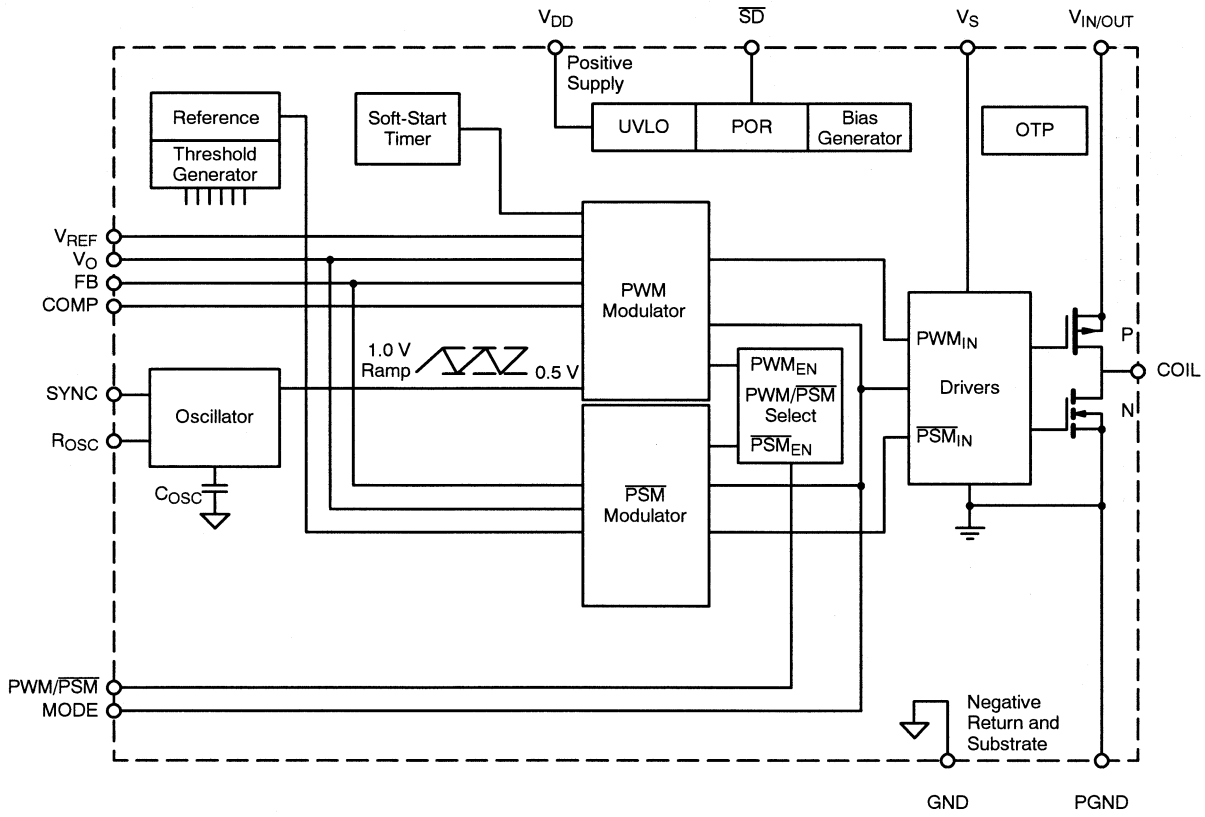

FIGURE 1.

Start-Up/UVLO

The internal under voltage lock out (UVLO) circuit keeps most of the IC function blocks off until the supply voltage (V_{DD}) increases above 2.4 V. A 100-mV hysteresis is built into the UVLO point, so the controller will be functional until V_{DD} drops below 2.3 V. This helps to eliminate the IC from bouncing between ON and OFF stages. After the IC is turned ON, it takes about 4 ms for the POR to be ready, the error amp output to charge up, and the output voltage to start ramping up. The output voltage will need an additional 3 to 4 ms to reach regulation, depending on load condition.

By-Pass Mode

When using the Si9165, the output voltage regulation point can be set within the input voltage range, regardless of whether a buck or boost configuration is being used. For instance, for an input range of 2.7 V to 4.2 V, the output voltage could be set to 3.3 V.

For a boost converter, when the input is higher than 3.3 V, the duty cycle of the switch stays at 0%, and the output voltage follows the input voltage by a voltage drop consisting of inductor resistance and MOSFET (in PWM mode) or diode (in PSM mode) drop. When the input decreases and approaches 3.3 V, the output drops to the regulation point, and the main switch starts to switch at a minimum duty cycle to keep the output regulated at 3.3 V. This duty cycle increases as the input voltage decreases. In some instances, noise can be generated during the transition because there is a minimum controllable duty cycle for any PWM controller. The frequency and amplitude of this transition noise vary depending on the compensation network. The wider the loop bandwidth (BW), the higher the switching frequency and the lower the output ripple.

For a buck converter, when input voltage is higher than 3.3 V, it is stepped down to 3.3 V at the output. As the input decreases and approaches 3.3 V, the switching duty cycle increases to the maximum duty cycle, jumping to 100% and making the high-side switch work like a saturated linear regulator. The output voltage will simply follow the input voltage by the saturation voltage until the input drops below the UVLO voltage or until another user-defined control signal disables the converter. The same noise considerations as for a boost converter apply in this case.

Buck/Boost Configuration

The Si9165 can be easily configured to function as a step-down (buck) or a step-up (boost) converter. Figures 2 and 3 show the typical application circuit for buck and boost converters, respectively. The list in Table 1 shows the key IC connection differences in the two topologies.

TABLE 1. Buck-Boost Pin Connection Comparison

Name of Pin	Buck	Boost
V_{IN}/V_{OUT}	Input	Output
MODE	Low	High
V_S	Input	Output

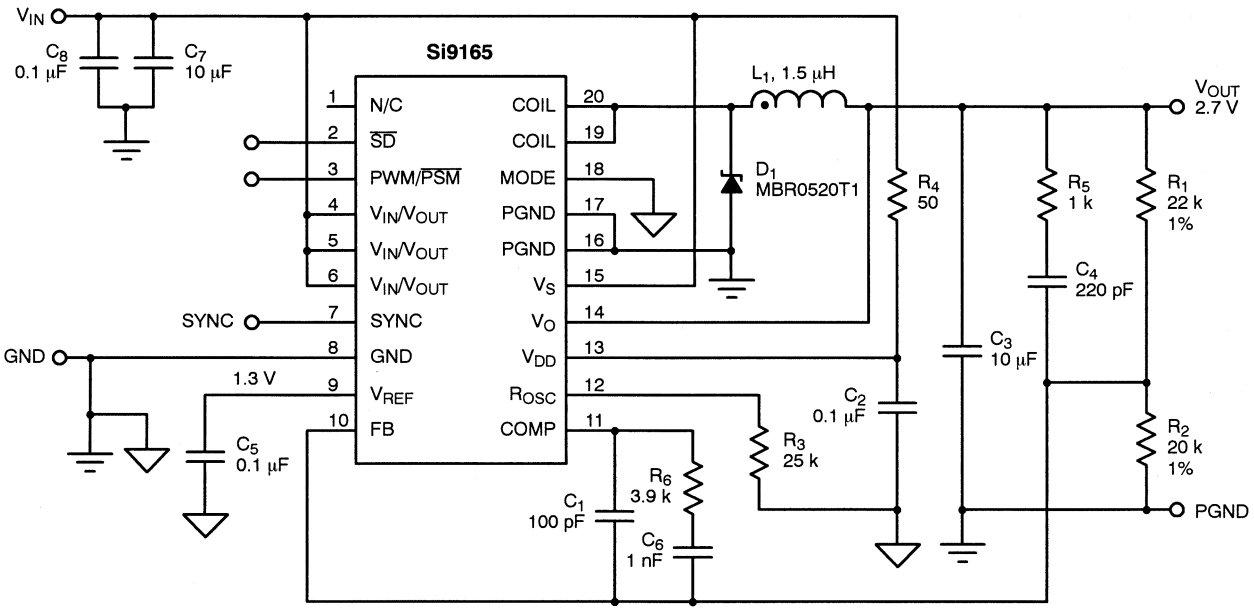

FIGURE 2. Typical Application Circuit-Buck

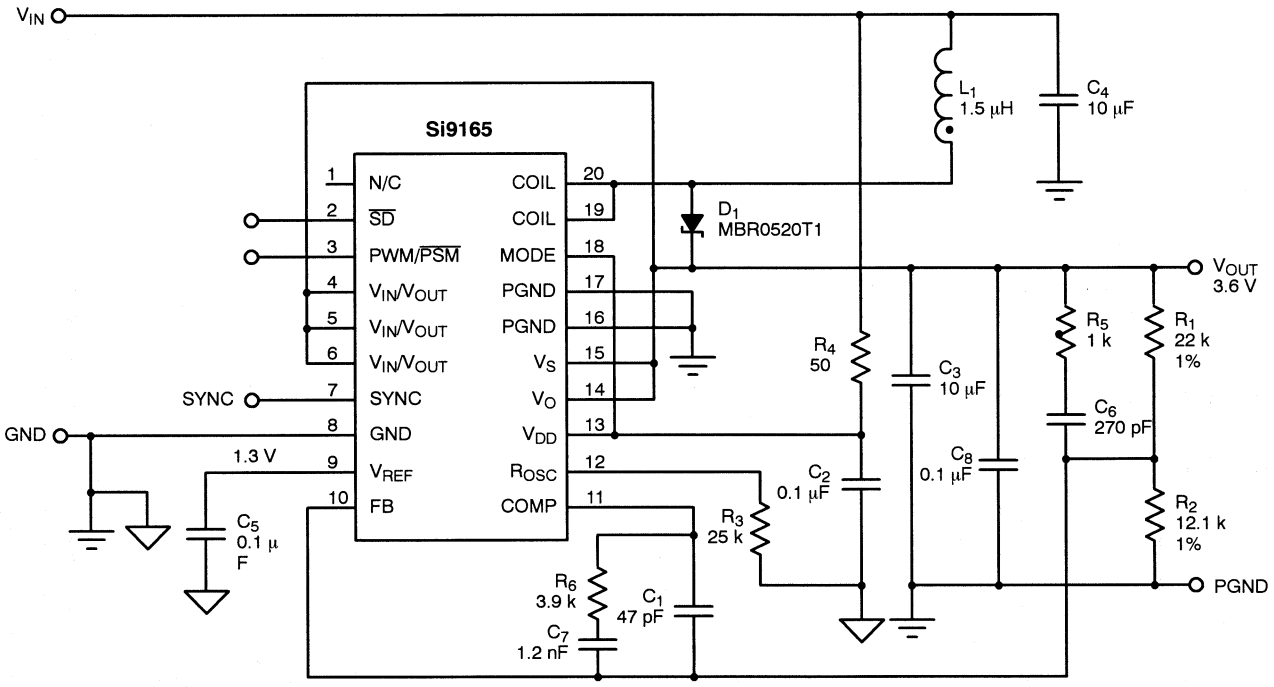

FIGURE 3. Typical Application Circuit—Boost

DESIGN GUIDELINES

Following are some design guidelines for buck and boost converters. The Si9165 combines a high level of integration while allowing the designer a considerable measure of flexibility. Key components required for a complete converter design are an inductor, input/output capacitors, and a compensation network.

Inductor Selection

An inductor is the energy storage component in a converter. Choosing an inductor means specifying its size, structure, material, inductance, saturation level, dc-resistance (DCR), and core loss. Fortunately, there are many inductor vendors that offer wide selections with ample specifications and test data, such as Vishay-Dale, Coilcraft, Coiltronics, and Sumida. The following are some key parameters that users should focus on.

In PWM mode, inductance has a direct impact on the ripple current. The peak-to-peak inductor ripple current can be calculated as

$$\text{For Buck, } I_{p-p} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}LF} \quad (1)$$

$$\text{For Boost, } I_{p-p} = \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{V_{OUT}LF} \quad (2)$$

where f = switching frequency.

Higher inductance means lower ripple current, lower rms current, lower voltage ripple on both input and output, and higher efficiency, unless the resistive loss of the inductor dominates the overall conduction loss. However, higher inductance also means a bigger inductor size and a slower response to transients. In PSM mode, inductance affects inductor peak current, and consequently impacts the load capability and switching frequency. For fixed line and load conditions, higher inductance results in a lower peak current for each pulse, a lower load capability, and a higher switching frequency.

The saturation level is another important parameter in choosing inductors. Note that the saturation levels specified in datasheets are maximum currents. For a dc-to-dc converter operating in PWM mode, it is the maximum peak inductor current that is relevant, and which can be calculated using these equations:

$$\text{For Buck, } I_{pk} = I_{OUT} + \frac{I_{p-p}}{2} \quad (3)$$

$$\text{For Boost, } I_{pk} = \frac{V_{OUT}I_{OUT}}{\eta V_{IN}} + \frac{I_{p-p}}{2} \quad (4)$$

where η = converter efficiency.

This peak current varies with inductance tolerance and other errors, and the rated saturation level varies over temperature. So a sufficient design margin is required when choosing current ratings.

A high-frequency core material, such as ferrite, should be chosen, since at 2 MHz, the core loss could lead to serious efficiency penalties. The DCR should be kept as low as possible to reduce conduction losses.

As one may have noticed, the switching frequency needs to be determined at the beginning of the design process. A high switching frequency allows the use of a smaller L/C power stage filter without any sacrifice to current/voltage ripple and conduction losses. In addition, a fast switching cycle helps speed up transient response times. However, one drawback of the high switching frequency is high gate charge and crossover switching losses, which in turn impair converter efficiency. Since the Si9165 features internal MOSFETs with low gate charge, the efficiency penalty is minimal, even at a 2-MHz switching frequency.

With a switching frequency (Fsw) capability as high as 2 MHz, the Si9165 allows use of small surface-mount inductors which are essential for compact cellular phone designs. The recommended inductance at a 2-MHz Fsw is 1.5 µH, which offers a good balance between size, ripple current, and efficiency. When a lower switching frequency is chosen, higher inductance is required to match the efficiency and ripple performance at 2 MHz. For instance, a 3-µH inductor is preferred for a 1-MHz switching frequency. In PSM mode, however, the operation is affected by inductance value but not the switching frequency.

Input/Output Capacitor Selection

Low ESR (Effective Series Resistance) capacitors are required on both the input and output to minimize voltage ripple. The ESR of the output capacitor also changes the loop stability, and it will be discussed later. At a 2-MHz Fsw, a 10-µF surface-mount ceramic capacitor is recommended at the output of the Si9165. A 10-µF ceramic or 22-µF low-ESR tantalum capacitor is recommended as the input filtering capacitor. Of course, the voltage rating on capacitor must not be neglected.

Diode Selection

To maximize converter efficiency, the use of an external Schottky diode is strongly recommended over utilizing the internal body diode of the MOSFET, which will typically have a higher forward voltage drop by comparison. The Schottky diode must be connected across the synchronous rectifying switch. In PWM mode, it carries the inductor current flow during BBM time; in PSM mode, this diode conducts all the time during inductor discharge since the rectifier switch is turned off during PSM. A low forward drop diode is preferable for its efficiency advantages and fast recovery times, which help reduce high-frequency noise.

Compensation Network

Voltage mode control is used in the Si9165 for both buck and boost converter configurations. Output voltage is sensed and fed back (pin 10, FB) to be compared with a reference voltage. The difference is amplified by the internal error amplifier. Then the output of the error amp (pin 11, COMP) is compared with a fixed ramp signal (see Figure 1), and the comparator output is a controlled pulse width used to drive the switches. As the switching duty cycle varies, the output voltage is regulated. This single control loop needs to be compensated so that the converter meets following specifications:

- Control loop stability margin
- Overshoot/undershoot at the output voltage induced by load and line transients
- Settling time for overshoot/undershoot

The peak overshoot/undershoot voltage is determined by closed-loop output impedance (Z_O). The higher the output impedance, the higher the peak. Although heavily dependent on output capacitance and inductance, Z_O is also closely related to closed loop gain. With fixed power stage components, a control loop with high bandwidth (BW) has low Z_O. Improving the compensation network is more cost-effective than increasing the size of the output capacitor and inductor. Fast settling times also rely on good loop design with high BW. Adding capacitance at the output of the power supply can reduce the peak deviation, but it can also produce several unintended results, including low BW, long settling times, reduced phase margin, and even system instability.

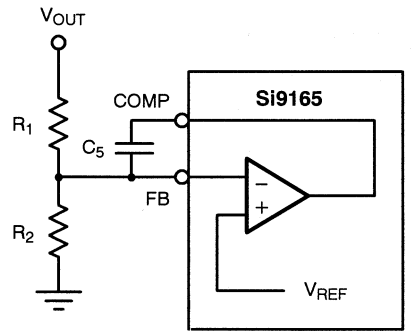

FIGURE 4. Type I Compensation Network

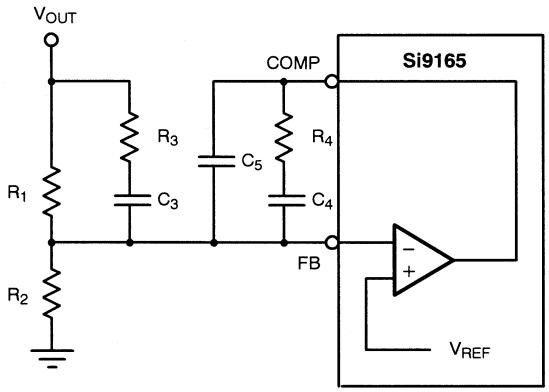

FIGURE 5. Type III Compensation Network

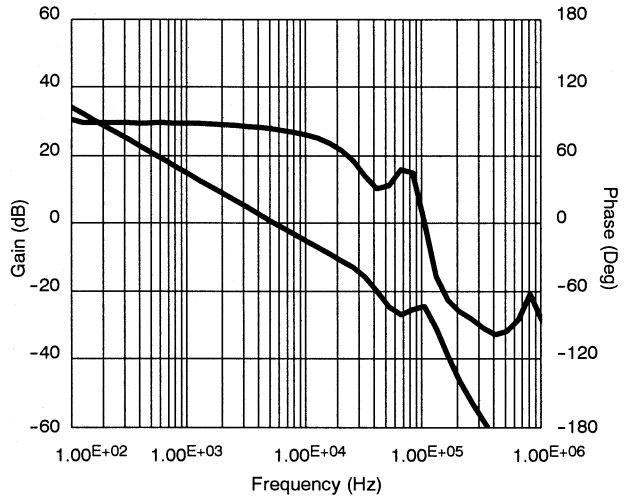

FIGURE 6. Buck Converter Loop Gain with Type I Compensation

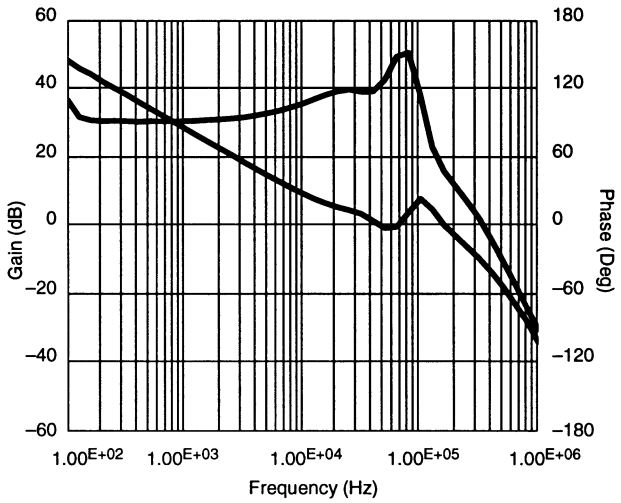

FIGURE 7. Buck Converter Loop Gain with Type III Compensation

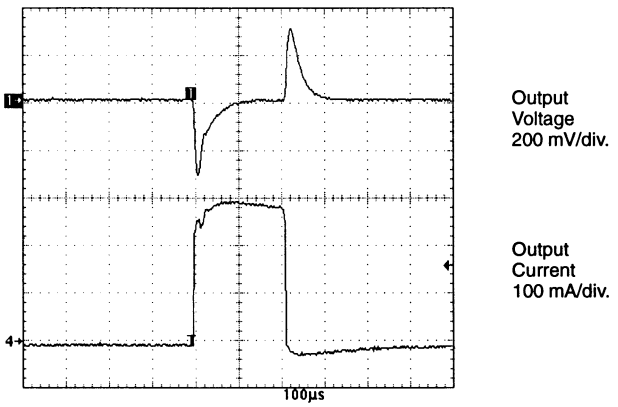

FIGURE 8. Buck Load Transient w/Type I Compensation
V_{IN} = 3.61 V, V_{OUT} = 2.676 V, 300 mA Load Transient

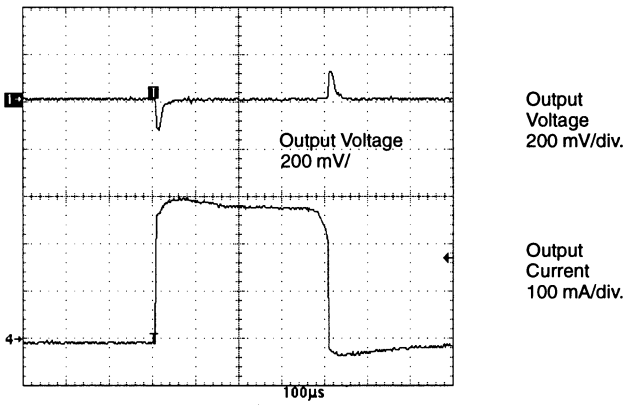

FIGURE 9. Buck Load Transient w/Type III Compensation
V_{IN} = 3.6 V, V_{OUT} = 2.64 V, 300 mA Load Transient

For voltage mode control, a simple Type I or II compensation network can easily stabilize the loop but at a cost of lower BW, which has to be at least one decade below the L-C corner frequency to preserve a good stability margin. However, Type III compensation, a more complicated design, enables higher BW even above the L-C double-pole. A buck converter is used as an example here to illustrate the difference between Type I (Figure 6) and Type III (Figure 7) compensation. With the switching frequency set to 2 MHz, a 1.5-µH to 10-µF L-C pair is used for the power stage, producing a double pole at 40 kHz. The loop gain Bode plots are measured for both types under the same conditions: V_{IN} = 3.6 V, V_{OUT} = 2.7 V, load = 300 mA. (See Figures 8 and 9). The BW is considerably higher with Type III compensation. The resulting transient waveforms for the two loops (Figures 10 and 11) show a notable improvement in both over/undershoot magnitude and recovery time with Type III compensation.

The values shown in Figure 7 work well for the Si9165 buck converter with a 3.6-V input, so long as the switching frequency is above 500 kHz, which is the range Si9165 is optimized for. Since the converter power stage gain varies with input voltage, the compensation circuit needs to be adjusted accordingly to maintain a stability margin. The circuitry in Figure 7 offers fast response with a sufficient stability margin for input voltages below 3.6 V. If the input voltage is above 3.6 V, the power stage gain, also part of the loop gain, elevates to a level that will endanger both the phase margin and gain margin of the control loop. Fortunately for buck converters, a simple change on the input lead capacitor C_3 can help compensate for this. The value can be adjusted by the simple equation shown below:

$$C_3 = \frac{3.6V \cdot 270pF}{V_{IN}} \quad (5)$$

For boost converters, the power stage behavior is more complicated. Like buck converters, the low-frequency gain varies according to the input/output condition. In addition, there are two other factors of the boost power stage gain that can be affected. The L-C double pole is a function of input/output condition as shown in (6):

$$f_{double-pole} = \frac{V_{IN}}{2\pi V_{OUT}\sqrt{LC}} \quad (6)$$

As this double pole shifts to lower frequencies, the phase delay also comes in at a lower frequency, making it difficult to cross over with the same BW. Another troublesome feature of boost power stages are their right-half-plane (RHP) zero, which can create difficulties for power supply designers. This RHP zero also varies with operating conditions as shown in (7).

$$f_{RHP-zero} = \frac{V_{IN}^2}{2\pi V_{OUT} I_{OUT} L} \quad (7)$$

When high boost ratios and heavy loads are required, this zero can move to low frequency. The negative effect of this is that it results in gain boost with an extra phase delay that will introduce instability into the loop gain. Designers must also bear in mind the variation of dc/low frequency gain of a boost converter as described in (8).

$$G_{DC} = \frac{V_{OUT}^2}{V_{IN}} \quad (8)$$

All these factors can change the loop response as line and load conditions change. Hence, when good transient response is required and a Type III network is used, the component values need to be altered to compensate for these changes. There are many was to accomplish this. Here is one approach that lowers the entire loop gain to preserve a stability margin. The feedback R_4-C_4 in series in Figure 7 can be modified as

$$C_4 = k \cdot 1200pF \quad (9)$$

$$\text{and } R_4 = \frac{3900}{k}\Omega \quad (10)$$

$$\text{where } k = \frac{V_{OUT}^2}{4.32 \cdot V_{IN}} \quad (11)$$

C_4 is used to adjust the gain at dc and low frequency, while R_4 is also adjusted so that the zero created by C_4-R_4 stays at the same frequency. The phase margin will diminish as load current increases indefinitely, since the RHP zero will close in to the crossover frequency. The design given in Figure 7 and its adjustment in (9), (10), and (11) are good for 600-mA loads, which is the maximum the Si9165 is designed for.

The divider resistor pair, R_1 and R_2 in Figures 2 and 3, determine the output regulation point. Since R_1 is part of the compensation network, it is recommended to adjust R_2 to change the regulation voltage without affecting the loop gain. With fixed R_1, R_2 can be easily calculated by (12) for the desired output voltage setting.

$$R_2 = \frac{R_1}{\frac{V_{OUT}}{V_{REF}} - 1} \quad (12)$$

The typical value for V_{REF} is 1.3 V.

Layout Issues

One of the very few drawbacks of switching power supplies is the noise level induced by their high-frequency switching performance. Parasitic inductance and junction capacitance become significant noise sources when a converter is switching at megahertz frequencies. However, noise levels can be minimized by properly laying out the components. Here are some tips for laying out buck and boost converters with the Si9165 controller.

- Minimize power traces. Since most power traces, in both buck and boost converters, carry pulsating current, energy stored in trace inductance during the pulse will be released when the pulse current stops, causing high frequency ringing with junction capacitor of the MOSFETs/diode or even the input/output capacitor. Fortunately for Si9165 users, the MOSFETs are integrated into the IC, allowing shortest trace between them. Designers will still need to keep external power traces as short as possible, including the trace from input/output capacitor to the switch, inductor to switch, inductor to input/output capacitor, and, of course, the ground trace.
- The decoupling capacitor V_{DD} has to be as close as possible to the pin to reduce the noise on this power source for the internal logic circuit.
- The V_S pin has to be close to input or output capacitor for buck or boost converters, respectively, to provide enough gate drive current without sacrificing much driving voltage. If this creates an impossible layout situation, designers may want to consider adding a 1-µF ceramic capacitor at the V_S pin, depending on the noise level.
- A high-frequency capacitor, normally a 0.1-µF ceramic capacitor, is recommended across the sources of two MOSFETs-right at the pins if possible-to reduce high-frequency noise. The impedance of these capacitors is lower at high frequencies compared with higher-value capacitors.
- To keep the gate signal clean, they have to be placed away from the inductor, since the alternating magnetic field is the primary noise source in a switching converter.

See Si9165 buck and boost converter layout as examples.

Other Issues

Sometimes higher input capacitance values are required when ultra-high-speed, large-scale load transients occur at a 2.7-V or lower input voltages. If the voltage level at V_{DD} drops below 2.3 V, the UVLO circuit will instantaneously shut off the IC and collapse the output. Best results can be achieved when a higher-value R-C filter is used on V_{DD} pin in conjunction with higher input capacitance.

The PSM feature is designed to increase efficiency under light load conditions and extend battery life. It does not offer an efficiency advantage over PWM mode when the load exceeds 100 mA and a 1.5-µH inductor is used. (Efficiency data are given in the “Experimental Results” section.) However, with a maximum of 1.5-µH inductance, the Si9165 PSM mode guarantees output regulation up to a 150-mA load for both buck and boost converters under any input/output condition.

EXPERIMENTAL RESULTS

The Si9165 controller has been fully tested in both buck and boost modes on demo boards. Some test results are summarized here. For the waveforms shown, the channel lineup from top to bottom is:

- Channel 2 - V_{OUT} voltage ripple
- Channel 4 - inductor current, 200 mA/div.
- Channel 1 - coil pin voltage, 2 V/div.

PWM Operation

- Buck mode V_{IN} = 3.6 V, V_{OUT} = 2.7 V, load = 300 mA

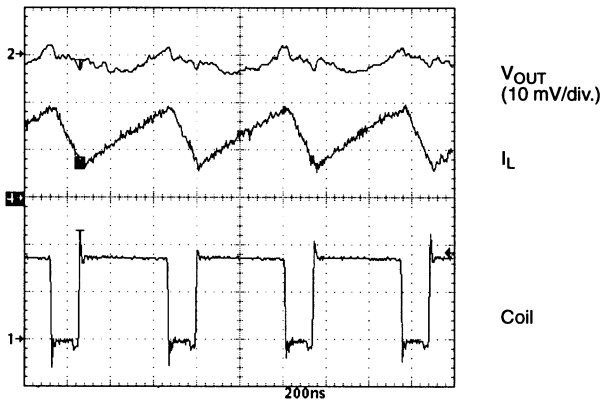

FIGURE 10. Buck PWM Waveforms

- Boost mode V_{IN} = 3.3 V, V_{OUT} = 3.7 V, load = 300 mA

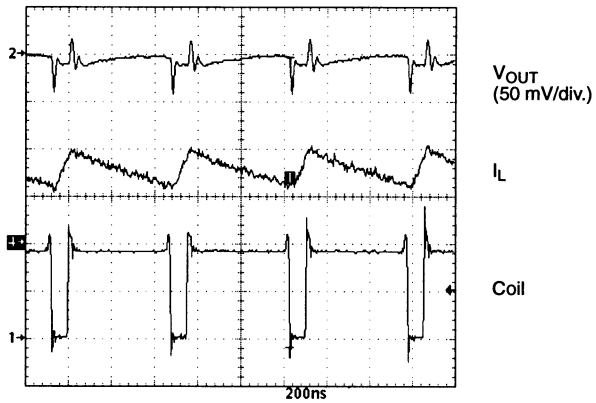

FIGURE 11. Boost PWM Waveform

PSM Operation

- Buck mode V_{IN} = 3.6 V, V_{OUT} = 2.7 V, load = 50 mA

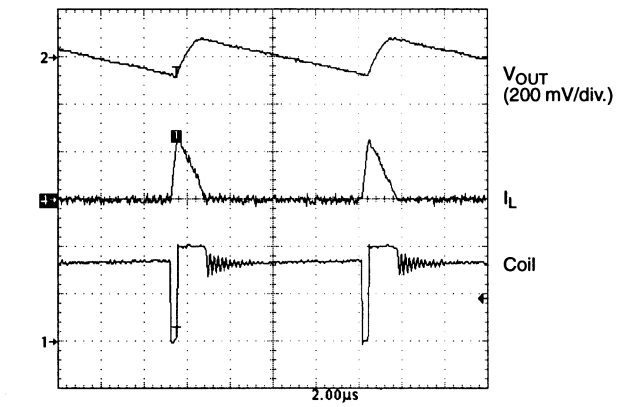

FIGURE 12. Buck $\overline{\text{PSM}}$ Waveform

- Boost mode V_{IN} = 3.3 V, V_{OUT} = 3.7 V, load = 50 mA

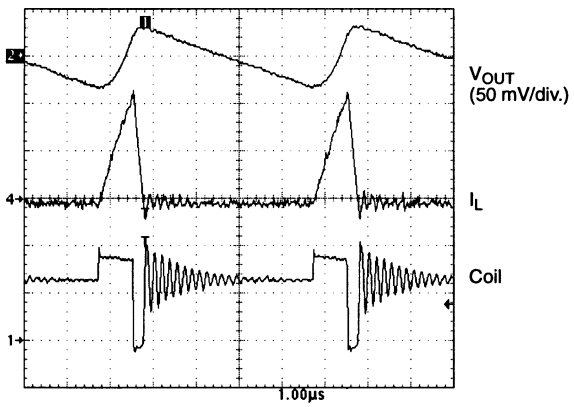

FIGURE 13. Boost $\overline{\text{PSM}}$ Waveform

Efficiency

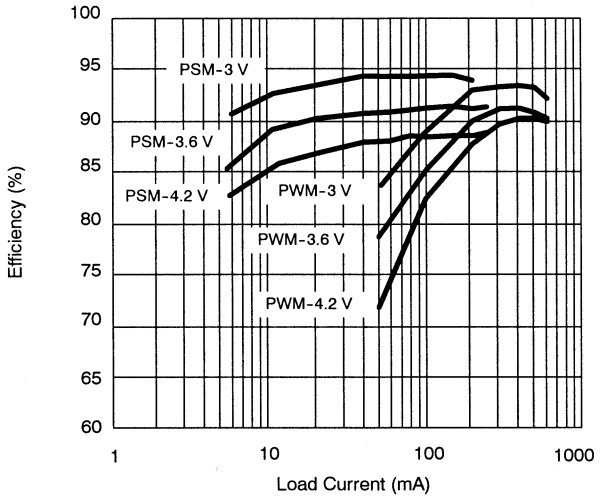

FIGURE 14. Buck Mode Efficiency w/V_{OUT} = 2.7 V

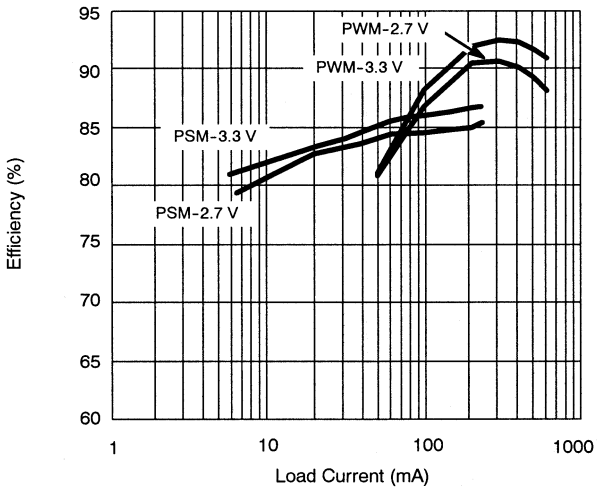

FIGURE 15. Boost Mode Efficiency w/V_{OUT} = 3.6 V

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