

AN6857N

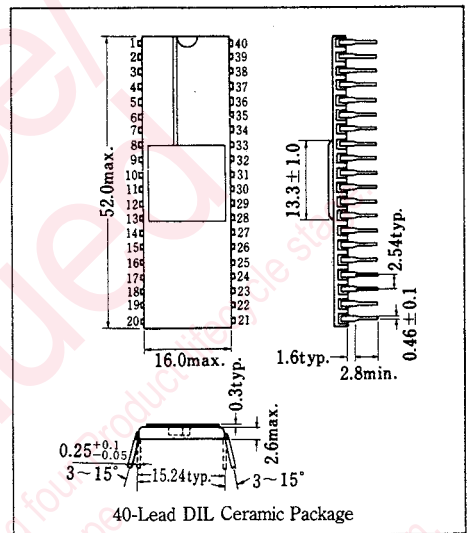
High Speed 8-bit AD Converter

■ Outline

The AN6857N is an A/D-converting parallel 8-bit monolithic bipolar IC with a high speed and low power consumption. It is suitable for A/D conversion of video band signals.

■ Features

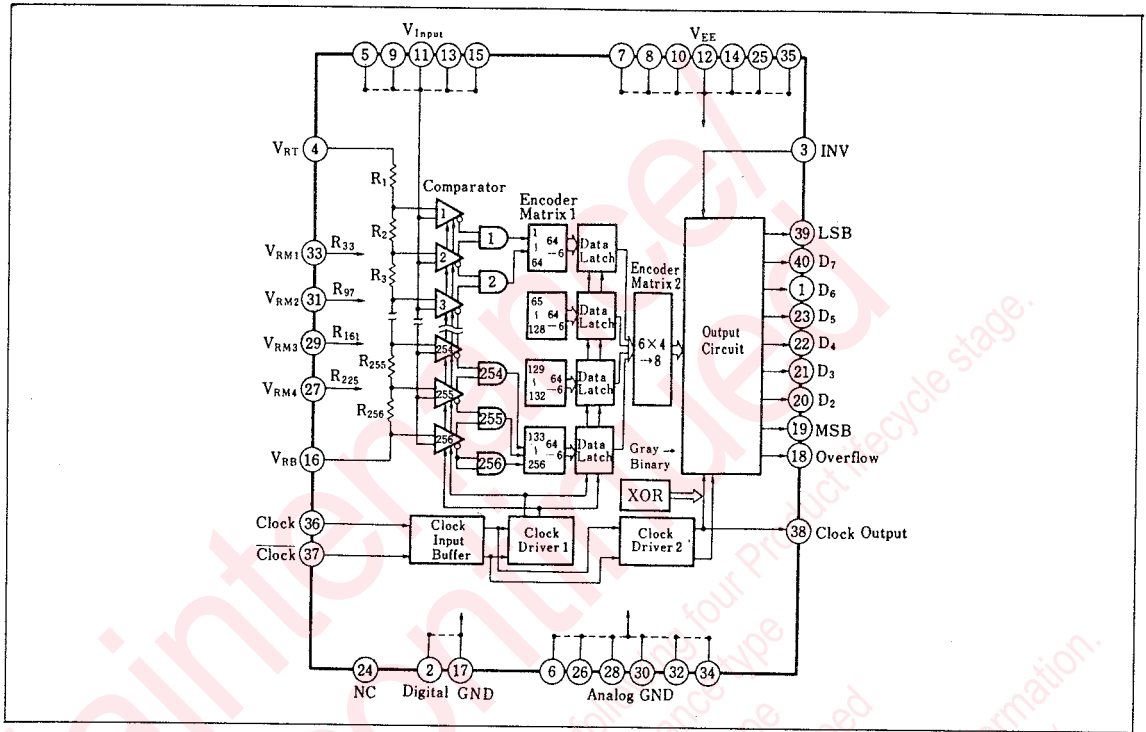
- 8-bit resolution (with overflow)
- High speed : maximum conversion speed 35 MSPS
- Sample & hold circuits not necessary
- Input dynamic range : $2V_{P-P}$
- Low power dissipation : 780mW typ.
- Digital inputs and outputs ECL compatible
- 8-bit parallel output (pure binary)



■ Quick Reference Data ($V_{EE} = -5.2V$, $T_a = 0 \sim 70^\circ C$)

Item	Symbol	Condition	Value	Unit
Resolution	RES		8	bit
Input dynamic range	$V_{in(max)}$		2	V
Linearity error	LE	$V_i = 2V_{P-P}$	$\pm \frac{1}{2}$	LSB
Max. conversion speed	$f_{MSPS(max)}$		35	MSPS
Quantization noise	S/N	$f_s = 14.32 \text{ MHz}, f_{IN} = 1 \text{ MHz}$	48	dB
		$f_s = 14.32 \text{ MHz}, f_{IN} = 4 \text{ MHz}$	40	dB
Differential gain	DG	IRE Standard 15kHz Sawtooth, 40% subcarrier	1	%
Differential phase	DP	$f_s = 14.32 \text{ MHz non-lock}$	0.5	deg

■ Block Diagram



■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	6th bit	21	3rd bit
2	Digital GND	22	4th bit
3	Output Inversion	23	5th bit
4	Ref. High Level	24	NC
5	Analog Input	25	VEE
6	Analog GND	26	Analog GND
7	VEE	27	Linearity Control
8	VEE	28	Analog GND
9	Analog Input	29	Linearity Control
10	VEE	30	Analog GND
11	Analog Input	31	Linearity Control
12	VEE	32	Analog GND
13	Analog Input	33	Linearity Control
14	VEE	34	Analog GND
15	Analog Input	35	VEE
16	Ref. Low Level	36	Clock Input (Positive)
17	Digital GND	37	Clock Input (Negative)
18	Over Flow	38	Clock Output
19	1st bit (MSB)	39	8th bit (LSB)
20	2nd bit	40	7th bit

■ Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Supply voltage	V _{EE}	-7 ~ +0.5	V
Analog input voltage	V _{ia}	V _{EE} ~ +0.5	V
Digital input voltage	V _{id}	V _{EE} ~ +0.5	V
Reference voltage	V _{REF}	V _{EE} ~ +0.5	V
Power consumption	P _D	1.2	W
Operating ambient temperature	T _{opr}	0 ~ +70	°C
Storage temperature	T _{stg}	-50 ~ +150	°C

■ Recommended Operating Conditions

Item	Symbol	min.	typ.	max.	Unit
Supply voltage	V _{EE}	-5.4	-5.2	-5.0	V
Reference voltage	V _{RT}	-0.1	0	+0.1	V
	V _{RB}	-2.1	-2.0	-1.9	V
Analog input voltage	V _i	-2.1		+0.1	V
Digital input voltage	V _{φH}	-1.105			V
	V _{φL}			-1.475	V
Digital output current	I _{OH}	-1	-2	-5	mA
Clock input pulse width (CLOCK IN)	τ _H	10			ns
	τ _L	20			ns

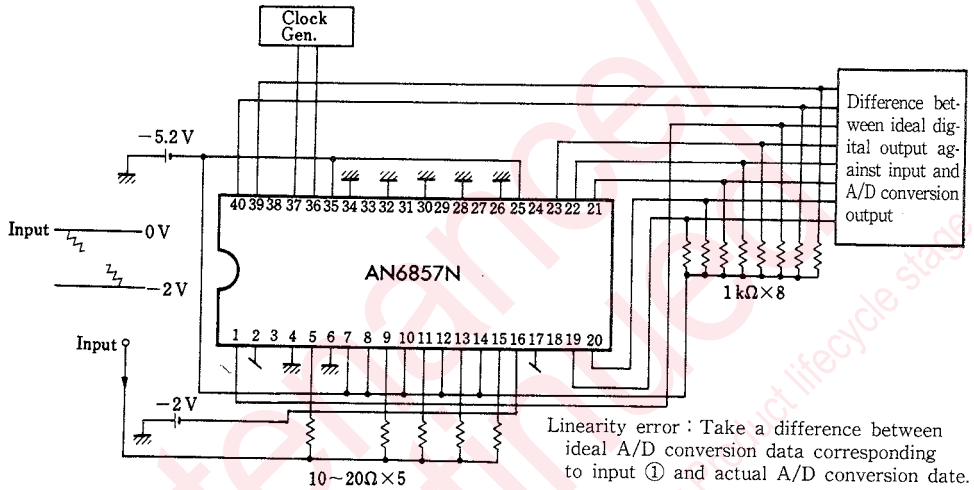
* INV terminal also acceptable even when V_{IH}=0V, V_{IL}=Open

■ Electrical Characteristics (V_{EE}=-5.2V, Ta=25°C)

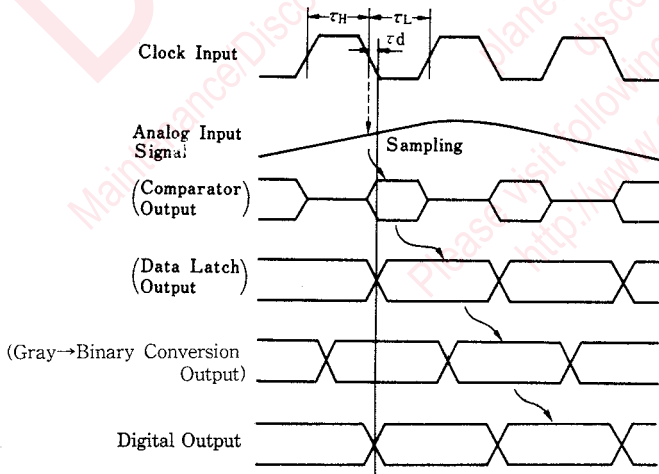
Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Supply current	I _{EE}		V _{EE} =-5.2V	-200	-150		mA
Reference resistance current	I _{RT}		V _{RT} =0V, V _{RB} =-2V		+25	+40	mA
	I _{RB}			-40	-25		mA
Equivalent input resistance	R _i *1		V _{EE} =-5.2V	10			kΩ
Input capacitance	C _i *1		Total of analog input end		100	150	pF
Input bias current	I _{Bias} *1		V _{EE} =-5.2V		125	250	μA
Clock input current	I _{φH}		I ₃₆ when V ₃₆ =-5.2V, I ₃₆ when V ₃₆ =0V			+0.6	mA
	I _{φL}		I ₃₇ when V ₃₇ =-5.2V, I ₃₇ when V ₃₇ =0V	-0.01			mA
Digital output voltage	V _{OH}		V _{EE} =-5.2V, I _{OH} =-2mA,	-0.96			V
	V _{OL}		I _{OL} =-2mA			-1.65	V
Digital output delay time	τ _d				10	15	ns
Linearity error	LE	1				± 1/2	LSB

*1 Design specification

Test Circuit 1 (LE)



■ Sampling Diagram

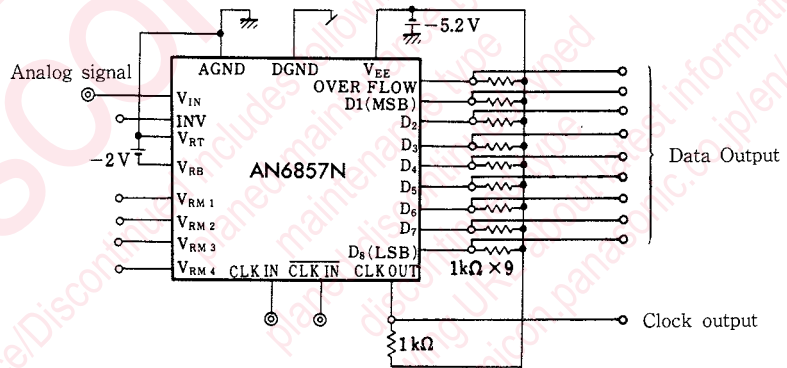


Note) Those in parentheses have no external terminal, because they are internal signals.

■ Output Cord Table

Comparator No.	Comparator Threshold Voltage		Digital Output																								
	Input 2.0000 VFS 7.8125 mV _{STEP}	Input 2.0480 VFS 8.0000 mV _{STEP}	INV. Terminal "L" Over M Flow 1 2 3 4 5 6 7 8							INV. Terminal "H" Over M Flow 1 2 3 4 5 6 7 8																	
001	-0.00781V	-0.0080V	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
002	-0.01562	-0.0160	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
127	-0.99218	-1.0160	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0
128	-1.00000	-1.0240	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0
129	-1.00781	-1.0320	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
255	-1.99218	-2.0400	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
256	-2.00000	-2.0480	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

■ External Connection Diagram



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