

AN6356N

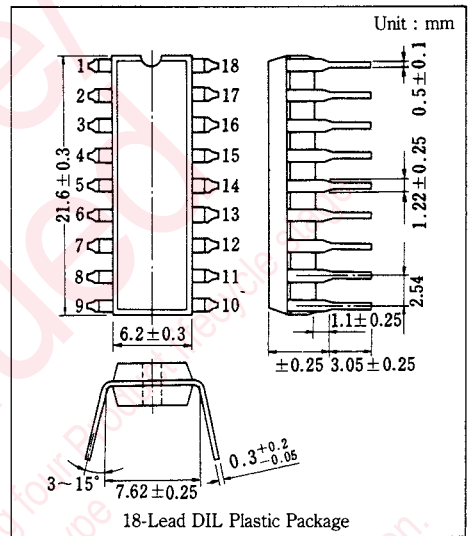
VTR Cylinder Interface Circuit

■ Outline

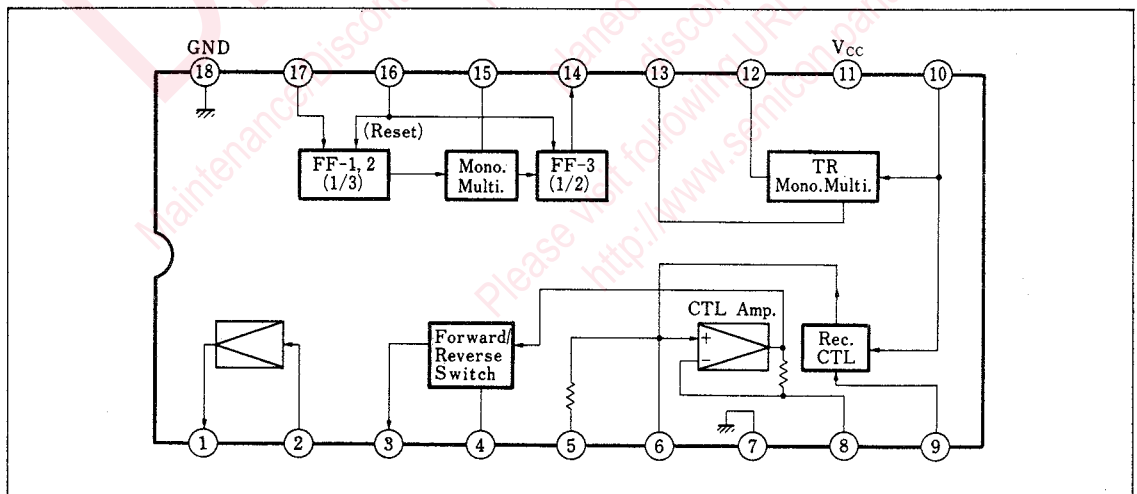
The AN6356N is an integrated circuit designed for VTR's cylinder interface.

■ Features

- The functions consist of:
 - PG monostable multivibrator
 - Tracking monostable multivibrator
 - CTL amplifier
- Supply voltage : 5V



■ Block Diagram



■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	P.B. CTL Output	10	1/2 V _{ss} Input
2	P.B. CTL Clamp Input	11	V _{cc}
3	P.B. CTL Amp. Output	12	Tracking Mono. Multi. Out.
4	Forward Reverse Select	13	Tracking Mono. Multi. Cont.
5	1/2 V _{cc}	14	Head Switch Output
6	CTL Signal	15	PG Control
7	GND	16	Cylinder PG Input
8	CTL Amp. Feedback	17	Cylinder PG Input
9	Rec./P.B. Select	18	GND

■ Absolute Maximum Ratings (T_a=25°C)

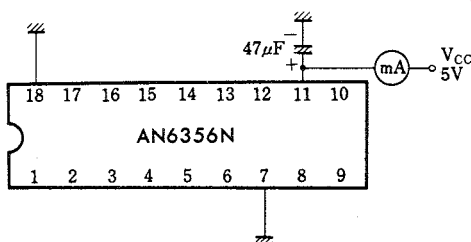
Item	Symbol	Rating	Unit
Supply voltage	V _{cc}	6.0	V
Power dissipation (T _a =70°C)	P _d	100	mW
Operating ambient temperature	T _{opr}	-20~+70	°C
Storage temperature	T _{stg}	-40~+150	°C

■ Electrical Characteristics (V_{cc}=5V, T_a=25°C)

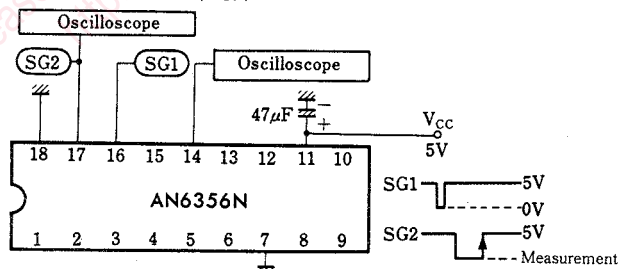
Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Circuit current	I ₁₁	1	Without load	7.0		14	mA
CY. PG. FG. input sensitivity	S _{17,16}	2,3				1.5	V
PG MM delay time	T ₁₅	4	C=0.056μF, R=20kΩ	690		860	μs
H/SW output High	V _{OH14}	5	Without load	4.6			V
H/SW output Low	V _{OL14}	5	Without load			0.4	V
1/2 V _{ss} input sensitivity	S ₁₀	6				1.5	V
Rec. start select sensitivity	S ₉	7		3.0			V
For./Rev. select sensitivity	S ₄	8		3.0			V
Rec. CTL output High	V _{OH6}	9	Without load	4.0			V
Rec. CTL output Low	V _{OL6}	9	Without load			0.4	V
PB CTL amp. gain (For.)	G _(Forward)	10		60		72	dB
PB CTL amp. gain (Rev.)	G _(Reverse)	10		59		72	dB
Tracking mono. multi. delay amount	T ₁₃	11	C=0.27μF, R=100kΩ	18		22	ms
PB CTL wave shaping input sensitivity	S ₂	12		300			mV

Note) Operating supply voltage range V_{cc(oper)}=4.5~5.5V

Test Circuit 1 (I₁₁)

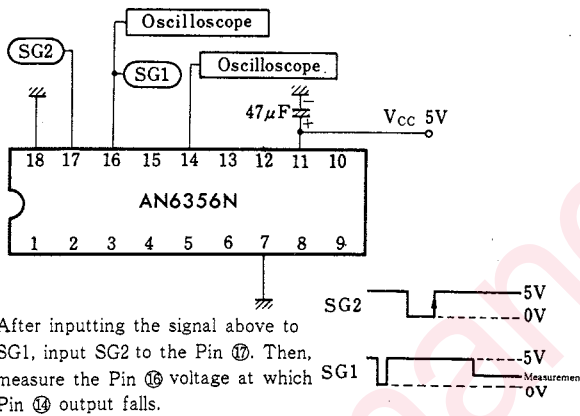


Test Circuit 2 (S₁₇)

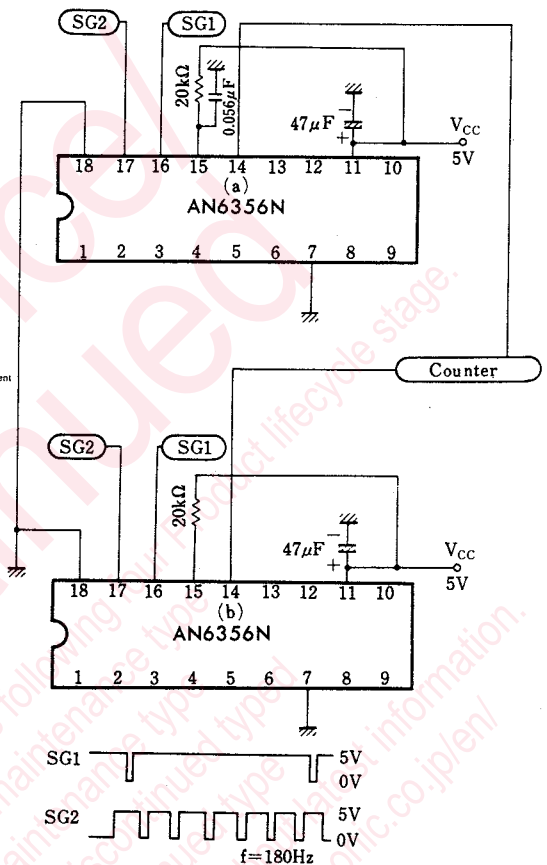


Measure the Pin ⑰ voltage at which Pin ⑭ output rises after IC internal FF reset (applying pulses to the Pin ⑯ in the circuit above).

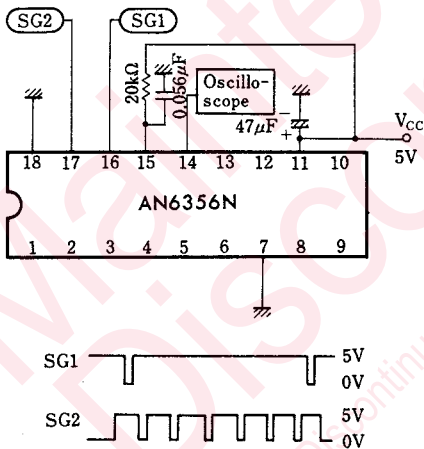
Test Circuit 3 (S₁₆)



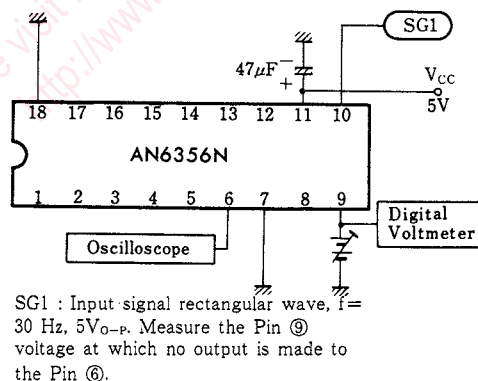
Test Circuit 4 (T₁₅)



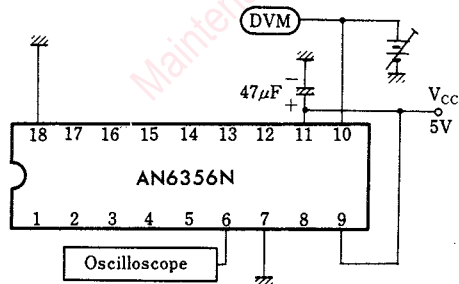
Test Circuit 5 (V_{OH14}, V_{CL14})



Test Circuit 7 (S₉)

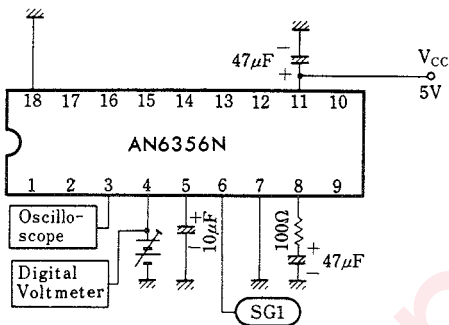


Test Circuit 6 (S₁₀)



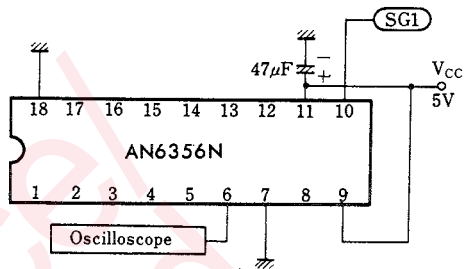
Measure the Pin ⑩ voltage at which Pin ⑥ output changes after IC internal R-S FF setting (applying pulses to the Pin ⑩ in the circuit above).

Test Circuit 8 (S₄)



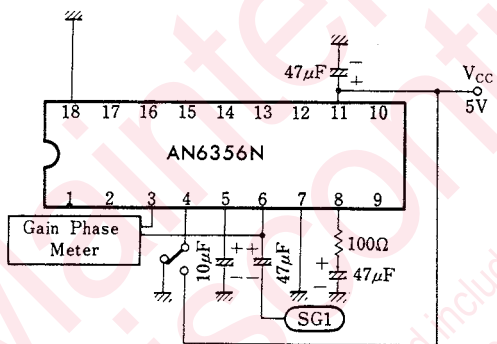
SG1 : Input signal sine wave, $f=1\text{kHz}$, $0.2\text{mV}_{\text{P-P}}$

Test Circuit 9 (V_{OH6}, V_{OL6})



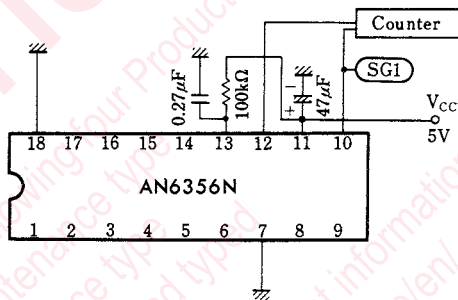
SG1 : Input signal rectangular wave, $f=30\text{Hz}$, $5\text{V}_{\text{O-P}}$

Test Circuit 10 (G_(Forward), G_(Reverse))



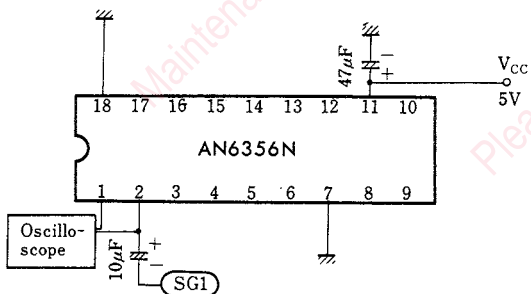
SG1 : Input signal sine wave, $f=1\text{kHz}$, $0.2\text{mV}_{\text{P-P}}$
 G_{F3} for Pin ④ GND, G_{R3} for Pin ④ V_{cc}

Test Circuit 11 (T₁₃)



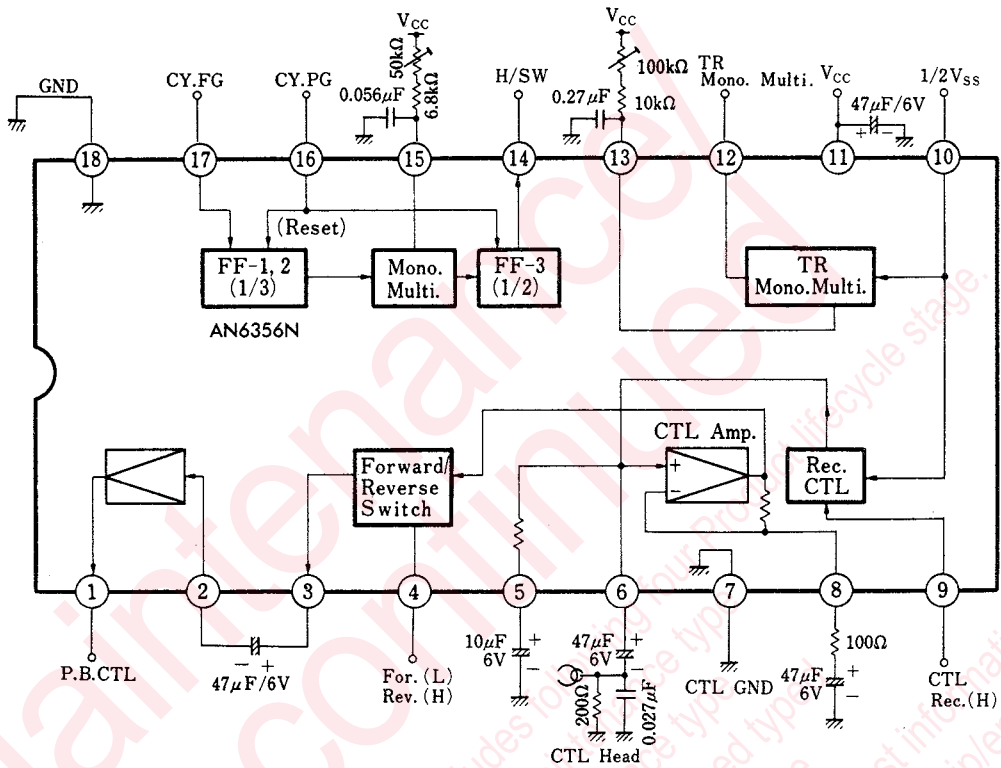
·SG1 : Input signal rectangular wave, $f=30\text{Hz}$, $5\text{V}_{\text{O-P}}$
 ·T₁₃ is a time rise of SG1 to a fall of Pin ⑬ output.

Test Circuit 12 (S₂)



·SG1 : Input signal, rectangular wave, $f=30\text{Hz}$
 ·SG1 $V_{\text{H}}-V_{\text{L}}=S_2$ when an SG1 signal level is changed and a signal is at the Pin ①.

■ Application Circuit



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