

AN6227FHN

Single chip, transmission and reception IC for PDC

■ Overview

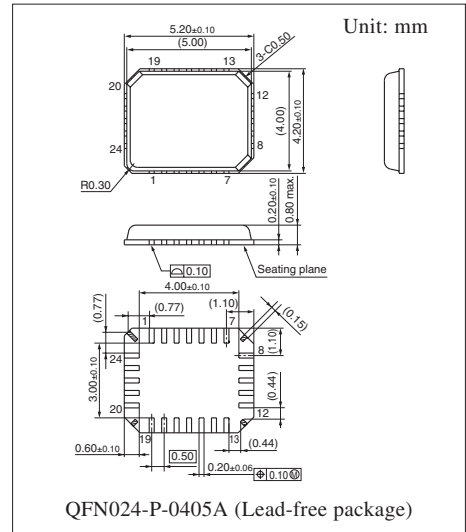
The AN6227FHN is a transmission and reception IC incorporating reception sleep function for a 1.5 GHz cellular telephone.

■ Features

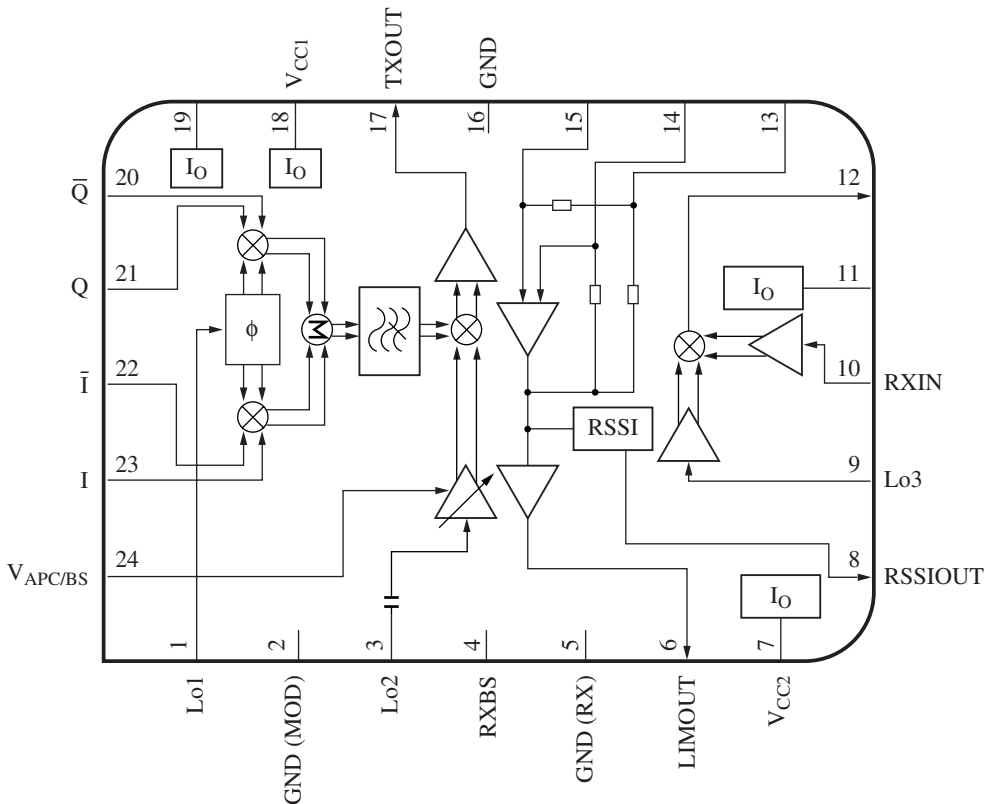
- Reception sleep function built-in
- Ultra mini-type 4 mm × 5 mm leadless package
- Current consumption: At reception: 25 mA
At transmission: 3.2 mA

■ Applications

- Cellular telephone (1.5 GHz PDC)



■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	TXLO1	TX local 1 input	13	LMDEC1	Limiter decouple 1
2	GNDMOD	TX modulator GND	14	LMDEC2	Limiter decouple 2
3	TXLO2	TX local 2	15	LMIN	Limiter input
4	RXBS	RXBS	16	GNDOUT	TX output GND
5	GNDRX	RX GND	17	TXOUT	TX output
6	LMOUT	Limiter output	18	VCCOUT	TX output V _{CC}
7	VCCLIM	V _{CC} limiter	19	VCCMOD	TX modulator V _{CC}
8	RSOUT	RSSI output	20	\bar{Q} -IN	\bar{Q} input
9	RXLOIN	RX local input	21	Q-IN	Q input
10	RXMXIN	RX mixer input	22	\bar{I} -IN	\bar{I} input
11	VCCMIX	Mixer V _{CC}	23	I-IN	I input
12	MXOUT	Mixer output	24	APC/BS	APC/BS

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V _{CC}	4.2	V
Supply current	I _{CC}	60	mA
Power dissipation *2	P _D	125	mW
Operating ambient temperature *1	T _{opr}	-30 to +80	°C
Storage temperature *1	T _{stg}	-55 to +125	°C

Note) *1: Except for the operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.

*2: P_D is the value at T_a = 80°C without a heatsink. Use this device within the range of allowable power dissipation referring to

"■ Technical Data • P_D — T_a curves of QFN024-P-0405".

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V _{CC}	2.6 to 4.0	V

■ Electrical Characteristics at T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Current consumption (transmission) *1	I _{CCTX}	Lo1 = 178 MHz, -25 dBm Lo2 = 1 619 MHz, -18 dBm V _{APC} = 2.3 V	—	25	33	mA
Sleep current *1	I _{SLTX}	No signal, V _{APC/BS} ≤ 0.3 V	—	0	10	μA

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output level 1 * ¹	P _{O1}	Lo1 = 178 MHz, -25 dBm Lo2 = 1 607 MHz, -18 dBm V _{APC} = 2.3 V	-16	-13	—	dBm
Output level 2 * ¹	P _{O2}	Lo1 = 178 MHz, -25 dBm Lo2 = 1 631 MHz, -18 dBm V _{APC} = 2.3 V	-16	-13	—	dBm
Minimum output level * ¹	P _{min}	Lo1 = 178 MHz, -25 dBm Lo2 = 1 619 MHz, -18 dBm V _{APC} = 1.0 V	—	-50	-40	dBm
Current consumption (reception) * ²	I _{CCR_X}	No signal	—	3.2	4.5	mA
Reception sleep current * ²	I _{RXSLP}	No signal, RXBS ≤ 0.3 V	—	—	10	μA
Mixer conversion gain * ²	G _{MX}	V _{MI} = 60 dBμ, SW1 = b (refer to "■ Application Circuit Example"), Excludes the filter loss of -7 dB	20	23	26	dB
Mixer maximum output amplitude * ²	V _{MX}	V _{MI} = 105 dBμ, SW1 = b (refer to "■ Application Circuit Example"), Excludes the filter loss of -7 dB	100	106	—	dBμ
Limiter voltage gain * ²	G _{LM}	V _{LI} = 15 dBμ	80	85	90	dB
Limiter maximum output amplitude * ²	V _{LM}	V _{LI} = 80 dBμ, 450 kHz component	0.90	1.25	1.60	V[p-p]
RSSI output voltage 1 * ²	V _{S(1)}	V _{LI} = 0 dBμ	0	0.23	0.6	V
RSSI output voltage 2 * ²	V _{S(2)}	V _{LI} = 115 dBμ	2.31	2.6	2.91	V
RSSI reference output slope * ³	D _S	V _S (V _{IS}) = V _{S(1)} + 0.12 V D _S = V _S (V _{IS} + 75 dBμ) - V(V _{IS})	1.39	1.8	2.19	V
RSSI output slope variation 1 * ³	ΔD _{S(1)}	ΔD _{S(1)} = 5 { V _S (V _{IS} + 15 dBμ) - V _S (V _{IS}) } / D _S	0.75	1	1.25	—
RSSI output slope variation 2 * ³	ΔD _{S(2)}	ΔD _{S(2)} = 5 { V _S (V _{IS} + 30 dBμ) - V _S (V _{IS} + 15 dBμ) } / D _S	0.75	1	1.25	—
RSSI output slope variation 3 * ³	ΔD _{S(3)}	ΔD _{S(3)} = 5 { V _S (V _{IS} + 45 dBμ) - V _S (V _{IS} + 30 dBμ) } / D _S	0.75	1	1.25	—
RSSI output slope variation 4 * ³	ΔD _{S(4)}	ΔD _{S(4)} = 5 { V _S (V _{IS} + 60 dBμ) - V _S (V _{IS} + 45 dBμ) } / D _S	0.75	1	1.25	—
RSSI output slope variation 5 * ³	ΔD _{S(5)}	ΔD _{S(5)} = 5 { V _S (V _{IS} + 75 dBμ) - V _S (V _{IS} + 60 dBμ) } / D _S	0.75	1	1.25	—

Note) *1: V_{CC1} = 3.0 V, IQ signal amplitude: 0.18 V[p-p] (both phases), DC bias: 1.6 V, (π/4 QPSK-modulated [0000] continuous wave input.

Output frequency of P_{O1}: 1429.0025 MHz, output frequency of P_{O2}: 1453.0025 Hz, output frequency of P_{min}: 1441.0025 MHz.
Output level is measured with a spectrum analyzer.

Setting of a spectrum analyzer: SPAN = 20 kHz, RBW = 300 Hz, VBW = 30 Hz, ST = 5 s

(When inputting π/4 QPSK-modulated [0000] continuous wave as IQ signal, the frequency for P_{O1}, P_{O2} and P_{min} becomes Lo frequency plus IQ signal frequency, which leads to the above value.)

Lo input level is a setting value of signal source (output impedance 50 Ω) described in the "■ Application Circuit Example".

■ Electrical Characteristics at $T_a = 25^\circ\text{C}$ (continued)

Note) (continued)

*2: Unless otherwise specified: $V_{CC2} = 3.0\text{ V}$, $R_{XBS} = 2.5\text{ V}$ to 3.0 V , $SW1 = a$ (Refer to " Application Circuit Example").

$V_{LO3} = 90\text{ dB}\mu$; $f = 129.55\text{ MHz}$, V_{MI} : $f = 130\text{ MHz}$, V_{LI} : $f = 450\text{ kHz}$

(Input level of pin 15 is excluded the loss of the matching circuit and filter.)

V_{MX} and V_{LM} are measured in high impedance.

Lo input level is a setting value of signal source (output impedance $50\ \Omega$) described in the "■ Application Circuit Example".

*3: V_{IS} is the input level V_{LI} at which the RSSI output voltage becomes $V_{S(1)} + 0.12\text{ V}$.

• Design reference data

Unless otherwise specified, $V_{CC1} = 3.0\text{ V}$.

Lo input level is a setting value of signal source (output impedance $50\ \Omega$) described in the "■ Application Circuit Example".

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Carrier leak suppression *1 (fLo2-fLo1)	CL	Lo1 = 178 MHz, -25 dBm Lo2 = 1619 MHz, -18dBm $V_{APC} = 2.3\text{ V}$	—	-35	-25	dBc
Image leak suppression *1	IL	Lo1 = 178 MHz, -25 dBm Lo2 = 1619 MHz, -18 dBm $V_{APC} = 2.3\text{ V}$	—	-35	-30	dBc
Proximity spurious suppression *1	DU	Lo1 = 178 MHz, -25 dBm Lo2 = 1619 MHz, -18 dBm $V_{APC} = 2.3\text{ V}$	—	-70	-65	dBc
Base band distortion suppression *1	BD	Lo1 = 178 MHz, -25 dBm Lo2 = 1619 MHz, -18 dBm $V_{APC} = 2.3\text{ V}$	—	-40	-30	dBc
Adjacent channel leak power suppression (30 kHz detuning) *2	BL1	Lo1 = 178 MHz, -25 dBm Lo2 = 1619 MHz, -18 dBm $V_{APC} = 2.3\text{ V}$	—	-45	-38	dBc
Adjacent channel leak power suppression (50 kHz detuning) *2	BL2	Lo1 = 178 MHz, -25 dBm Lo2 = 1619 MHz, -18 dBm $V_{APC} = 2.3\text{ V}$	—	-70	-60	dBc
Adjacent channel leak power suppression (100 kHz detuning) *2	BL3	Lo1 = 178 MHz, -25 dBm Lo2 = 1619 MHz, -18 dBm $V_{APC} = 2.3\text{ V}$	—	—	-65	dBc
APC variable width *1	L_{APC}	Lo1 = 178 MHz, -25 dBm Lo2 = 1619 MHz, -18 dBm $V_{APC} = 1.0\text{ V}$ to 2.3 V	30	37	45	dB
APC output level control sensitivity *1	S_{APC}	Lo1 = 178 MHz, -25 dBm Lo2 = 1619 MHz, -18 dBm $V_{APC} = 1.0\text{ V}/1.6\text{ V}$	37	46	55	dB/V
In-band output level deviation *1	ΔP	Lo1 = 178 MHz, -25 dBm Lo2 = 1607 MHz to 1631 MHz, -18 dBm, $V_{APC} = 2.3\text{ V}$	-1.5	—	+1.5	dB

■ Electrical Characteristics at $T_a = 25^\circ\text{C}$ (continued)

• Design reference data (continued)

Unless otherwise specified, $V_{CC1} = 3.0\text{ V}$.

Lo input level is a setting value of signal source (output impedance $50\ \Omega$) described in the "■ Application Circuit Example".

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Modulation precision *3	EVM	Lo1 = 178 MHz, -25 dBm Lo2 = 1 619 MHz, -18 dBm $V_{APC} = 2.3\text{ V}$	—	2.0	3.5	%[rms]

Note) *1: IQ signal amplitude: 0.18 V[p-p] (both phases), DC bias: 1.6 V, $\pi/4$ QPSK-modulated [0000] continuous wave input.

Measure the suppression amount for output with a spectrum analyzer.

Setting of a spectrum analyzer: SPAN = 20 kHz, RBW = 300 Hz, VBW = 30 Hz, ST = 5 s

*2: IQ signal amplitude: 0.18 V[p-p] (both phases), DC bias: 1.6 V, $\pi/4$ QPSK-modulated [PN9] continuous wave input.

To be measured by a spectrum analyzer. (By using a leak power measurement function for an adjacent channel.)

Setting of a spectrum analyzer: SPAN = 250 kHz, RBW = 1 kHz, VBW = 1 kHz, ST = 2 s

*3: IQ signal amplitude: 0.18 V[p-p] (both phases), DC bias: 1.6 V, $\pi/4$ QPSK-modulated [PN9] continuous wave input.

The output level be measured by a spectrum analyzer. (By using a modulation precision measurement function.)

■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description	I/O
1		TXLO1: Input pin of quadrature modulator.	I
2		GNDMOD: GND pin of phase shifter and modulator. Make impedance low by widening the GND pattern.	—
3		TXLO2: Local input pin for up mixer.	I
4		RXBS: On/off control pin for reception block.	I

RXBS (V)	Reception block
0 to 0.3	Off
2.5 to 3	On

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
5		GNDRX: GND pin of reception system. Make impedance low by widening the GND pattern.	—
6		LMOUT: Output pin of limiter amplifier.	O
7		VCCLIM: V _{CC} pin for IF limiter amplifier RSSI.	—
8		RSOUT: RSSI output pin. DC potential corresponding to input signal level of limiter amplifier is outputted.	O
9		RXLOIN: Local input pin for reception down mixer.	I
10		RXMXIN: Input pin to 1st. IF amplifier. Input impedance is 2 kΩ.	I
11		VCCMIX: V _{CC} pin for reception down mixer.	—
12		MXOUT: Reception down-mixer output pin.	O

■ Terminal Equivalent Circuits (continued)

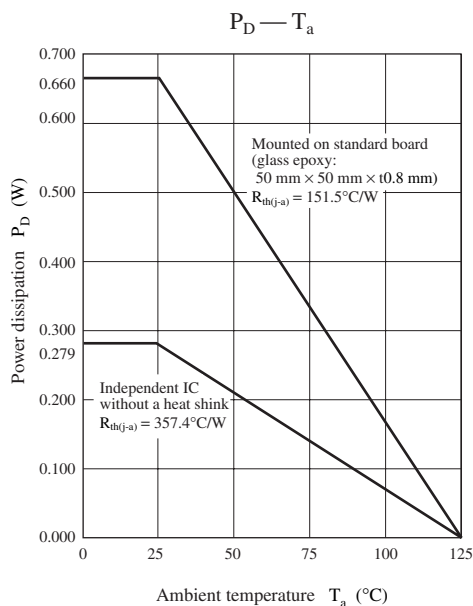
Pin No.	Equivalent circuit	Description	I/O			
13, 14		Pin 13: LMDEC1; Pin 14: LMDEC2: De-coupling pin for feedback of limiter amplifier. Connect an external capacitor to GND.	—			
15		LMIN: Limiter amplifier input pin. Input impedance is 2 kΩ.	I			
16		GNDOUT: GND pin for transmission up-mixer and RF output amplifier.	—			
17		TXOUT: RF output pin from output amplifier circuit.	O			
18		VCCOUT: V _{CC} pin for transmission up-mixer and RF output amplifier.	—			
19		VCCMOD: V _{CC} pin for phase shifter and quadrature modulator.	—			
20		\overline{Q} -IN: Q signal input pin. Relation between DC bias and amplitude is as follows:	I			
21		Q-IN: Q signal input pin. Relation between DC bias and amplitude is as follows:	I			
		<table border="1"> <thead> <tr> <th>DC bias (V)</th> <th>Amplitude (V[p-p])</th> </tr> </thead> <tbody> <tr> <td>1.6</td> <td>0.18</td> </tr> </tbody> </table> Input impedance is 100 kΩ or more.	DC bias (V)	Amplitude (V[p-p])	1.6	0.18
DC bias (V)	Amplitude (V[p-p])					
1.6	0.18					

Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O						
22		<p>\bar{I}-IN: \bar{I} signal input pin. Relation between DC bias and amplitude is as follows:</p> <table border="1"> <thead> <tr> <th>DC bias (V)</th> <th>Amplitude (V[p-p])</th> </tr> </thead> <tbody> <tr> <td>1.6</td> <td>0.18</td> </tr> </tbody> </table> <p>Input impedance is 100 kΩ or more.</p>	DC bias (V)	Amplitude (V[p-p])	1.6	0.18	I		
DC bias (V)	Amplitude (V[p-p])								
1.6	0.18								
23		<p>I-IN: I signal input pin. Relation between DC bias and amplitude is as follows:</p> <table border="1"> <thead> <tr> <th>DC bias (V)</th> <th>Amplitude (V[p-p])</th> </tr> </thead> <tbody> <tr> <td>1.6</td> <td>0.18</td> </tr> </tbody> </table> <p>Input impedance is 100 kΩ or more.</p>	DC bias (V)	Amplitude (V[p-p])	1.6	0.18	I		
DC bias (V)	Amplitude (V[p-p])								
1.6	0.18								
24		<p>APC/BC: Pin for use both as battery saving of transmission block and as power control of transmitting RF output. Control with the following conditions:</p> <table border="1"> <thead> <tr> <th>V_{APC} (V)</th> <th>Mode</th> </tr> </thead> <tbody> <tr> <td>0 to 0.3</td> <td>Off</td> </tr> <tr> <td>1.0 to V_{CC}</td> <td>On (APC control)</td> </tr> </tbody> </table> <p>Input impedance is 5 kΩ or more.</p>	V_{APC} (V)	Mode	0 to 0.3	Off	1.0 to V_{CC}	On (APC control)	I
V_{APC} (V)	Mode								
0 to 0.3	Off								
1.0 to V_{CC}	On (APC control)								

Technical Data

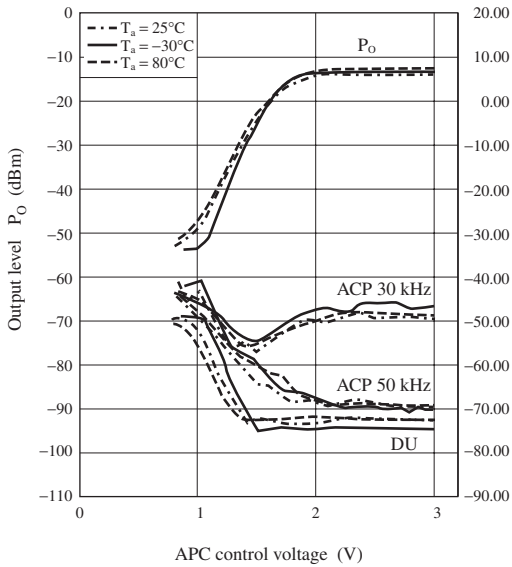
1. $P_D - T_a$ curves of QFN024-P-0405A



■ Technical Data (continued)

2. Main characteristics

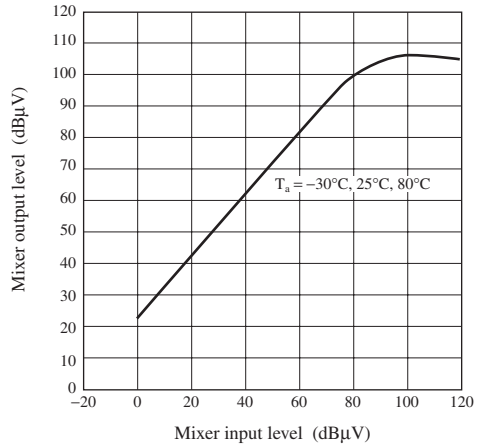
APC control voltage characteristics



$V_{CC} = 3.0\text{ V}$, $T_a = -30^\circ\text{C}$, 25°C , 80°C ,
 $BS = V_{APC} = V_{AR}$
 Lo1: 178 MHz, -25 dBm
 Lo2: 1619 MHz, -18 dBm
 I, Q: 0.18 V[p-p] (both phases) 1.6 V_{DC},
 $\pi/4$, [0000] or using PN9 stages
 continuous wave.

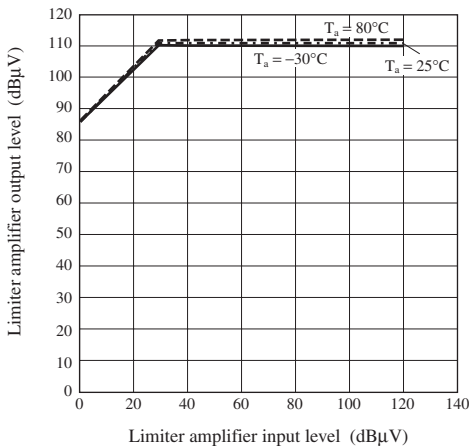
Adjacent channel leak power suppression
 amount: ACP 30 kHz, ACP 50 kHz (dBc)
 Proximity spurious suppression amount:
 DU (dBc)

Mixer characteristic



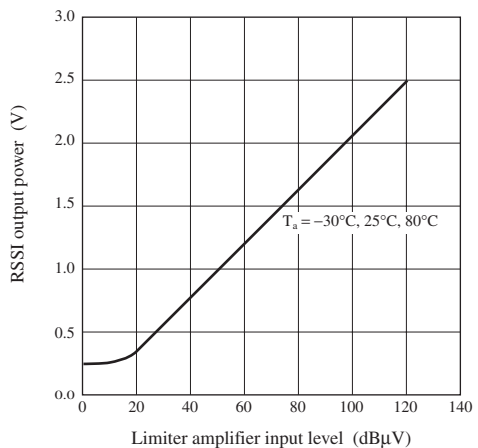
$V_{CC} = 3.0\text{ V}$, $T_a = -30^\circ\text{C}$, 25°C , 80°C
 Mixer in: 130 MHz
 Mixer out: 450 kHz
 Lo3 in: 129.55 MHz, 90 dBμV

Limiter amplifier characteristics



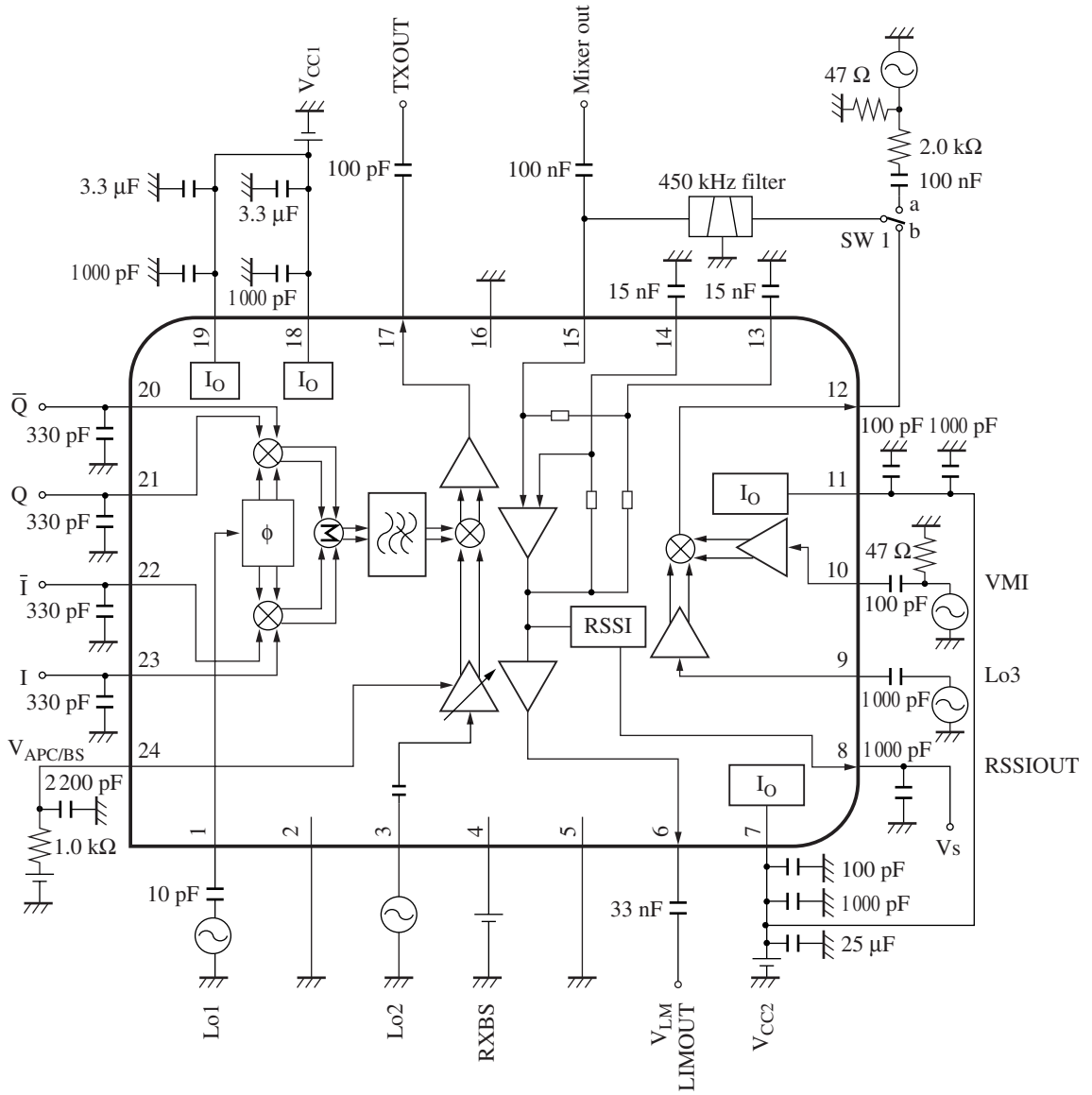
$V_{CC} = 3.0\text{ V}$, $T_a = -30^\circ\text{C}$, 25°C , 80°C ,
 $BS = 2.5\text{ V}$
 Limiter in: 450 MHz, Limiter out: 450 kHz

RSSI characteristic



$V_{CC} = 3.0\text{ V}$, $T_a = -30^\circ\text{C}$, 25°C , 80°C ,
 $BS = 2.5\text{ V}$
 Limiter in: 450 MHz, Limiter out: 450 kHz

■ Application Circuit Example



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